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PME SIO-1
Manual

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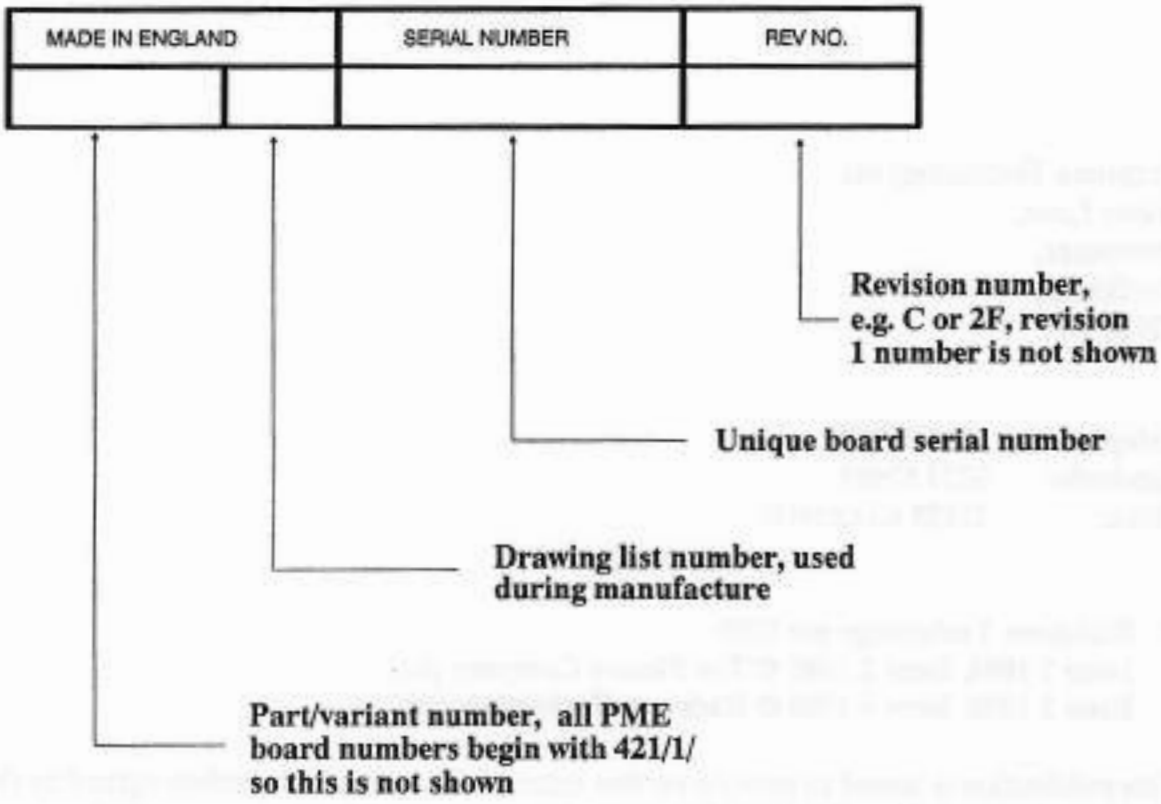
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March 1990

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Chapter 1 - Introduction

Overview

The PME SIO-1 provides six independent high performance serial I/O channels for VMEbus systems.

Each channel is implemented using a Multi-Protocol Communications Controller (MPCC) 68561, which is able to handle the following software selectable protocols:

IBM Bi-Sync communications in ASCII or EBCDIC format.

Character Orientated Protocols (COP)
BSC, DDCMP, X3.28, X.21, ISO/IS1745, ECMA16, etc.

Synchronous Bit-Orientated Protocols (BOP)
SDLC, HDLC/ADCCP, X.25, etc.

Asynchronous or Isochronous mode.

The Bit-rate for each channel is software programmable from 110 to 38400 bps.

The I/O signal assignment to the six flat cable connectors is individually configurable, via on-board wire wrap links for each channel. To interface with data communications equipment, both RS 232 and RS 422 compatible transmitters and receivers are installed.

Each I/O channel may be used in either interrupt or non-interrupt (polled) mode. For efficient handling, each MPCC contains three software programmable interrupt vectors.

A front-panel mounted RUN/LOCAL switch is provided to isolate the SIO-1 board from the VME bus. The status condition of the board is indicated by LEDs on the front panel.

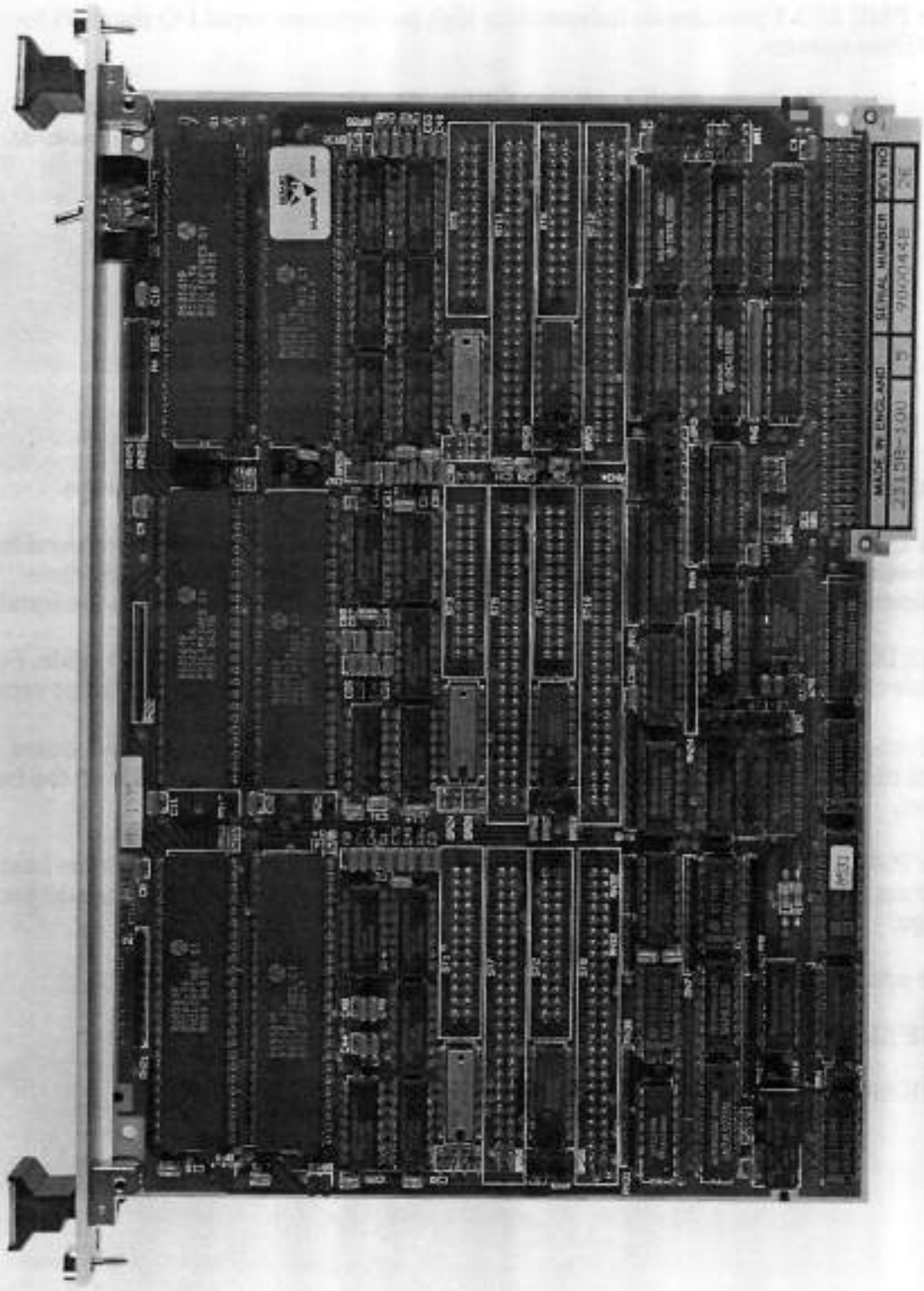
The PME SIO-1 board occupies an address area of 512 bytes (200 hex) with the base address link selectable in 512 byte increments within the 16 Mbyte VMEbus address range.

The address modifier lines are decoded in parallel to the address signals.

PME SIO-1 Variants

PME SIO-1	Serial I/O Channel	421/1/23158/100

Figure 1. PME SIO-1 Board



PME SIO-1 Features

- 6 serial I/O channels
- Multi-Protocol Communications Controller (68561) for each channel
- Asynchronous/synchronous receiver/transmitter functions
- Full/half duplex, auto-echo and local loop-back modes
- Protocols
  IBM binary synchronous communications in ASCII or EBCDIC format
  Character Orientated Protocols (COP): BSC, DDCMP, X3.28, X.21, ISO IS1745, ECMA16, etc.
  Synchronous Bit-Orientated Protocols (BOP): SDLC, HDLC/ADCCP, X.25, etc.
  Asynchronous or isochronous mode
- Modem handshake interface
- Error Control Register (ECR) control field CRC enable/disable
- Selectable CRC polynomials - CRC-16, CCITT V.41, VRC/LRC
- Selectable Parity generation/checking - enable, odd, even, or disable
- 22 directly addressable registers for flexible option selection, complete status reporting and data transfer
- Eight character receiver and transmitter buffer register
- Three separate, programmable and maskable interrupt vector registers for receiver, transmitter buffer register
- Software programmable baud rate from 110 to 38400 b.p.s.
- 16-bit data bus
- Freely configurable I/O interface signal assignment through wire wrap areas with:

5 Drivers	RS 232C compatible	)
6 Receivers	RS 232C compatible	) For each channel
2 Drivers	RS 422 compatible	)
2 Receivers	RS 422 compatible	)

- Freely selectable access address of the 6 MPCCs
- Address modifier decoding
- RUN/LOCAL mode indicated by 2 LEDs

RS 232C Interface

The PME SIO-1 is connected to serial devices via standard RS 232C interfaces with each channel capable of being configured as DTE or DCE.

Transfer characteristics are set independently by each MPCC. These include: character length, stop bit setting, parity detection, line break detection/generation and false start bit detection.

Each channel can be configured to operate from 110 bits/sec. to 38.4 k bits/sec.

Each of the six channels is terminated at a 26-pin male connector which can be connected, via flat cables, to a separate (optional) front panel. This front panel (PME SIO-1FP) takes up two standard VME slot positions and consists of the flat cable assemblies required to connect to the SIO-1 board and six 25-way "D" type connectors for interface to external serial devices.

RS 422 Interface

As an option to the use of the RS 232 interface, the board is equipped with RS 422 drivers for the data and handshake interface lines. All the data processing and handling features available for RS 232 are common to the use of RS 422.

Optional Front Panel PME SIO-1FP

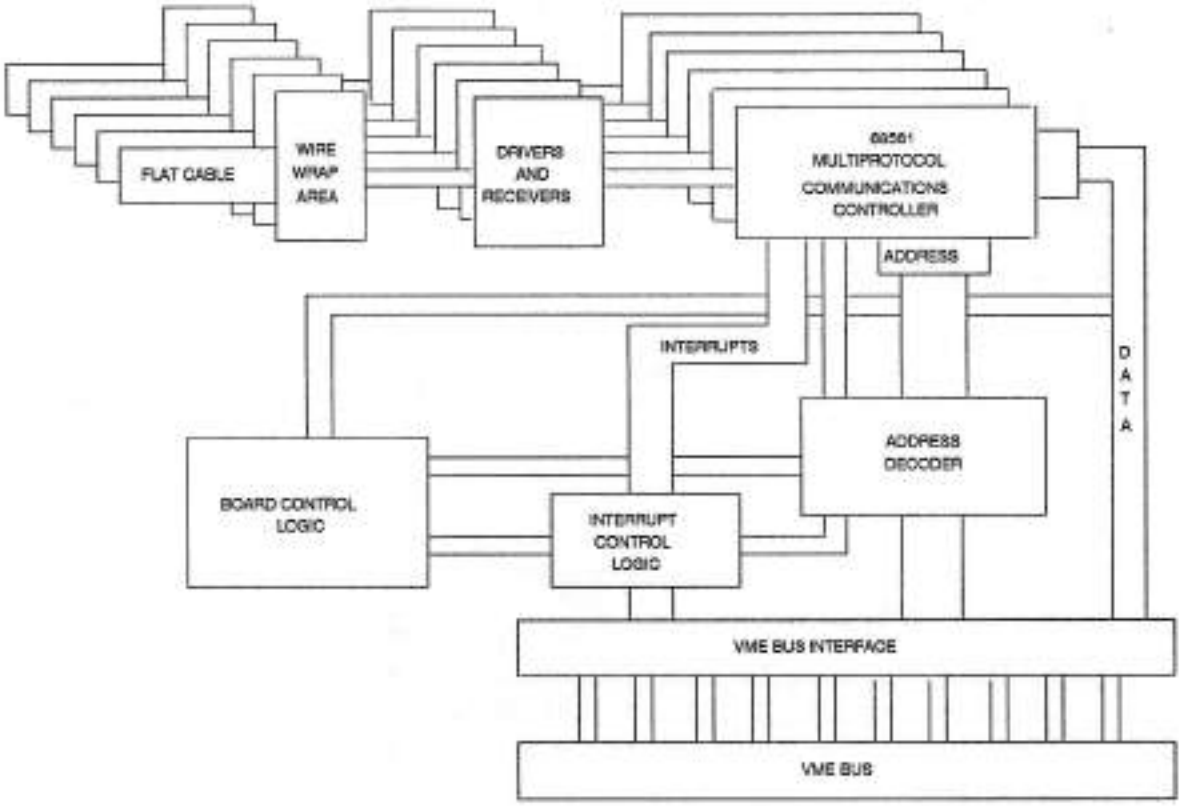
The optional front panel is recommended in the case where the peripherals are external to the system containing the SIO-1 board. Where such devices are internal to the system, they may be connected, via flat ribbon cables, direct to the board.

Where the devices are external to the system, as for a modem connected device, flat cable connectors are used to lead out to the six "D" type connectors on the optional front panel. This panel takes up two standard VME slots and is a passive device.

RUN/LOCAL Switch

The RUN/LOCAL switch is used to isolate the board from the bus during failures or maintenance. The mode is indicated by two LEDs on the front panel.

Figure 2. PME SIO-1 Block Diagram



Functional Overview

VMEbus Interface

The PME SIO-1 is a VME, A24: D16 board with optional Address Modifier (AM) decoding.

To the Host processor the PME SIO-1 appears as 512 bytes of RAM mapped into the 16 Mbyte VMEbus memory range. This provides a 64 byte address space for each of the six MPCC devices plus a reserved space of 128 bytes.

PME SIO-1 is a bus slave; it cannot initiate VMEbus cycles and is re-initialised by the VMEbus SYSRESET* signal.

User Interface

The PME SIO-1 has six communication channels, each consisting of a Multi-Protocol Communications Controller (M68561) plus associated RS 232C and RS 422 discrete logic. Each MPCC on the board works asynchronously from the system bus and responds to the controlling CPU in accordance with the selectable address and address modifier code.

Peripheral Interface Drivers and Receivers

The six communication channels of the SIO-1 are interfaced to peripherals using either RS 232C or RS 422 logic drivers and receivers.

RS 232C Interface

The RS 232C interface consists of standard driver/receiver chips (5 drivers, 6 receivers). Channels can be individually configured as Data Circuit terminating Equipment (DCE) or Data Terminal Equipment (DTE) using either a 9-wire or 3-wire connection.

RS 422 Interface

The RS 422 interface provides an alternative form of hardware interface in areas where large amounts of "noise" are likely to interfere with the data transfer. The RS 422 interface is a Balanced Digital Interface (BDI) allowing transfer rates of up to 10 Mbits/sec at short distances (10 Metres) and 100 kbits/sec at 1.2 Km, (note: these are approximate values). The RS 422 Interface on the SIO-1 consists of 2 driver and 2 receiver devices (Differential Comparators).

Multi-Protocol Communications Controller

Each of the six channels of the SIO-1 is assigned an individual MPCC and each MPCC is able to use all the listed protocols and to communicate with its 8/16 bit data bus and can be accessed via the VME bus. The internal 8 character receiver/transmitter buffer register (FIFO) reduces software handling using three separate maskable interrupt vector registers (transmitter, receiver, or handshake interface).

All the MPCCs on the board work asynchronous to the bus and respond to the controlling CPU via a jumper selectable access address and address modifier code.

Wire-Wrap Area

The wire-wrap area on the SIO-1 board is used to create a user defined set of connections between the MPCC and the transition pins. This allows the user to define specifically which MPCC signal is connected to which transition pin.

Operational Overview

The Host processor accesses the MPCCs asynchronously via the VME bus, sending control and data in either 8 or 16-bit wide format. Data and command/status information is moved between the system bus and each MPCC under control of three separate, maskable auto-vectored interrupts.

The normal sequence of events is for the host to select the MPCC/device, program the various internal MPCC registers and start sending data characters. The MPCC has an eight character FIFO buffer to hold data for transmitting or receiving and uses the interrupt structure to request/deny data from the host and to signal completion of transmission and reception.

This ability of the MPCCs to buffer up to eight received and transmitted characters optimises bus throughput and allows the host CPU more time to service the data.

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Chapter 2 - Specification

Board Specification

Interface	6 independent serial I/O channels RS232 or RS422 compatible (freely selectable)
Devices	6 Multi-Protocol Communications Controllers (68451)
Protocols	IBM BSC:ASCII EBCDIC COP:BSC, DDCMP, X3.28, X.21, ISO IS1745 BOP:SD2C, HDLC/ADCCP, X.25 Asynchronous and isochronous modes Full/half duplex, auto-echo and local loop-back modes Software programmable baud rate (110 - 38400 Baud)
Interrupts	Freely selectable interrupt request in common for the 6 I/O channels 18 different auto-interrupt vectors are programmable (3 per channel)
Bus	VME bus compatible (A24:D16) Freely selectable board base address (512 byte steps) Address modifier decoding
Timing	The normal READ/WRITE access time from the VMEbus to one of the MPCCs is: 205ns (typical), 280ns (maximum)
Power Requirements	+5V, 1.6 A (typical) 1.8 A (maximum) +12V, 300 mA (typical) 600 mA (maximum) -12V, 300 mA (typical) 600 mA (maximum)

Operating Environment

The PME SIO-1 will operate under the following conditions:

Temperature Range:	0°C to + 55°C
Cooling Requirement:	A linear airflow of not less than 500ft/min. across each card is recommended
Relative Humidity:	Up to 95% without condensation
Thermal Shock:	±5°C per minute
Altitude:	-300 to +3000 metres (-1,000 to +10,000 ft approx)
Vibration:	5 - 100Hz at 2g acceleration
Mechanical Shock:	20g for 6 milliseconds (half sine) when mounted in a suitable racking system

Storage Environment

The PME SIO-1 may be transported or stored without damage within the following limitations:

Temperature Range:	-55°C to +85°C
Relative Humidity:	Up to 95% without condensation
Thermal Shock:	±10°C per minute.
Altitude:	-300 to +16000 metres (-1,000 to +50,000 ft approx)
Vibration:	0 - 500Hz. at 2g acceleration
Mechanical Shock:	20g for 6 milliseconds (half sine)

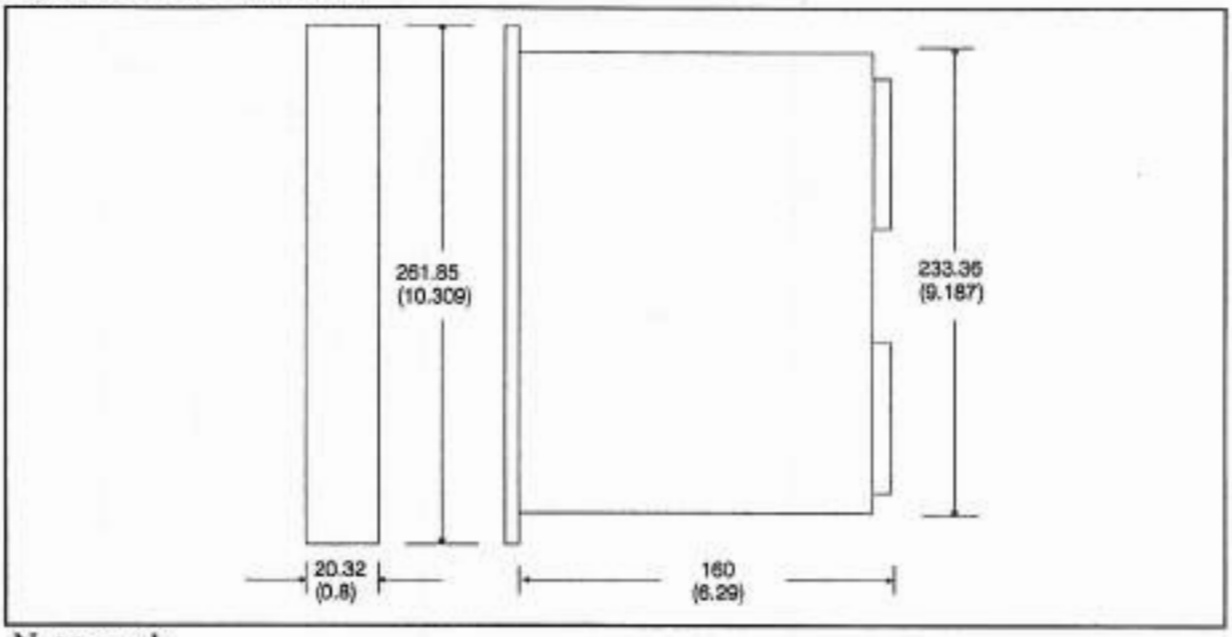
Mean Time Between Failures (MTBF)
The calculated mean time between failures for the PME SIO-1 is 67,500 hours. The failure rates used in this calculation have been derived from the British Telecom Reliability Handbook HRD4 with MIL-HDBK-217D and in-house data.

Mechanical Specification

Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3 inches)	
Weight	0.38 Kg	0.837 lb

PME SIO-1 is constructed on an 8-layer double Eurocard.

Figure 3. Board Dimensions



Not to scale.

Note: PME SIO-1 conforms to the VMEbus Specification (IEEE Std 1014) board size. Dimensions are in millimetres with inches in brackets for reference only.

Figure 4. Front Panels

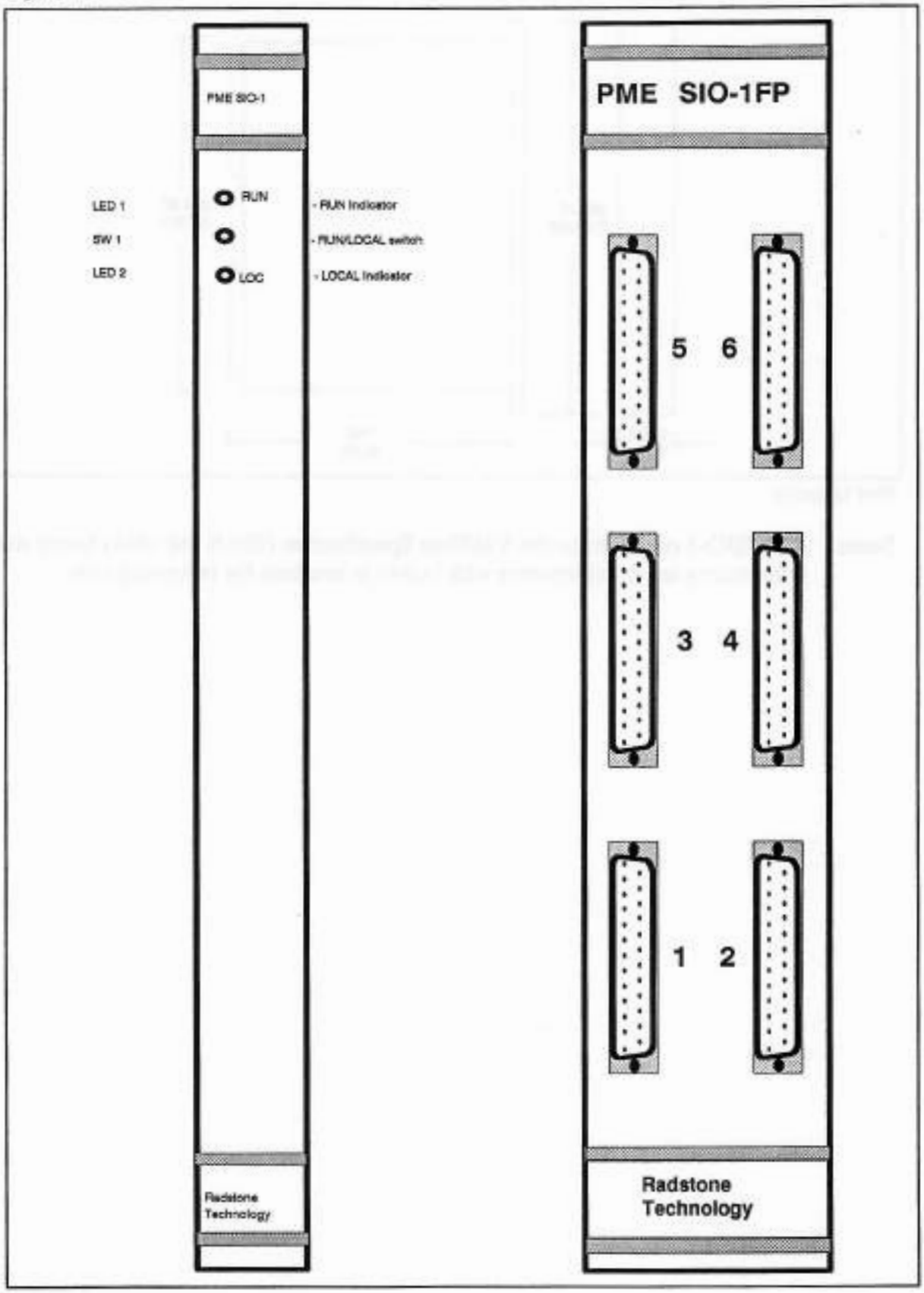
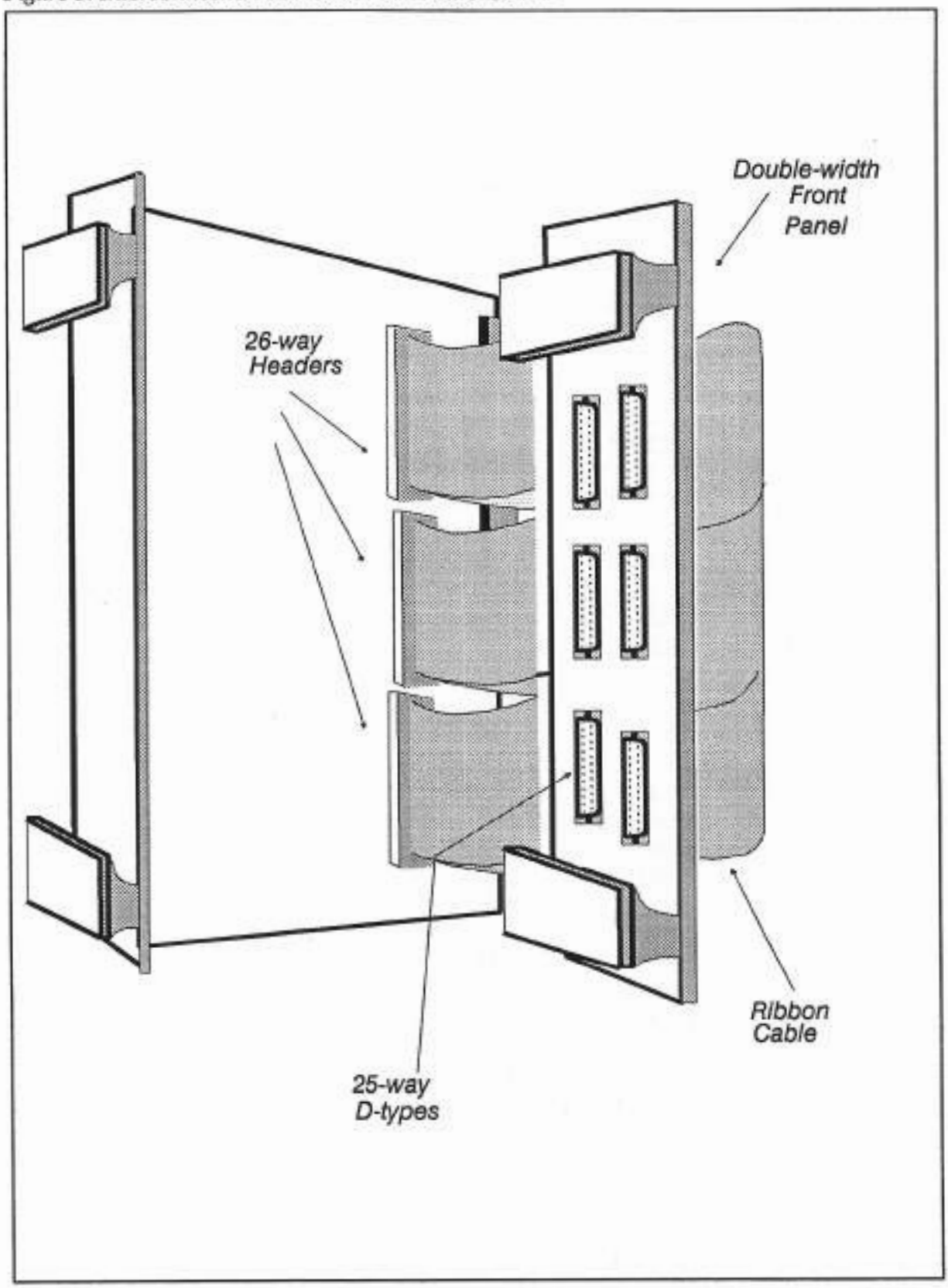


Figure 5. Interconnection between SIO-1 and SIO-1FP



Connector Pin Assignment

Connnector P1			
Pin	Row A	Row B	Row C
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BG1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5VSTDBY	+12V
32	+5V	+5V	+5V

Chapter 3 - Functional Description

Accessing the PME SIO-1

For the internal board select signal to be active, the following conditions are necessary:

i) A valid address on the VMEbus which lies within the selected address range.

ii) The comparison of the address modifier signals is correct.

iii) The board is in RUN mode.

Each MPCC uses the address signals A1 to A4 for internal register selection. The address signal A5 and the Data Strobe signal DS1* are used as a special case to allow the 8 and 16 bit mode of the MPCC, (refer to the MPCC data sheet for further details). Address signals A6, A7 and A8 are used to select one of the six MPCCs.

Data Transfer Mode

The following data transfer modes are allowed:

READ -	An 8 or 16 bit data word is transferred from one of the MPCCs to the current bus master
WRITE -	An 8 or 16 bit data word is transferred from the current bus master to one of the MPCCs

All transfers are controlled by the WRITE*, DS* and DS1* (upper and lower data strobe) signals. The board responds asynchronously to the bus master with a DTACK* (Data Transfer Acknowlege) signal. The DTACK* signal informs the bus master of a successful completion of a data transfer.

Base Address Selection

The base address of the PME SIO-1 is set up using link blocks BR1 and BR2. It may be on any 512-byte boundary within the VMEbus address range. The six MPCCs each occupy 64 bytes within the 512 bytes. The remaining 128 bytes will select the SIO-1 but not access a device. See Table 1 for memory map. Chapter 4 gives details on configuring the base address.

Table 1. PME SIO-1 Memory Map

Offset from base address (Hex)

+00	MPCC1
+40	MPCC2
+80	MPCC3
+C0	MPCC4
+100	MPCC5
+140	MPCC6
+180	Reserved
+1C0	Reserved

Address Modifier Decoding

In addition to the address signals the PME SIO-1 also receives and decodes the VME bus address modifier signals, as defined in the VME bus specification.

In the Short Supervisory I/O access mode (AM code $2D) (where $ indicates a hexadecimal number) or in the Short Non-privileged I/O access mode (AM code $29), the address signals A16 to A23 have to be disabled (set low), because they are not valid for these address modifiers.

The address modifier is set up using link block BR3. Any address modifier may be set up, including Don't Care states. Chapter 4 gives details on configuring the address modifiers.

Multi-Protocol Communications Controller (MPCC)

Each MPCC has 22 directly addressable registers. Protocols and the data transfer rate are initialized by writing to the control registers.

The MPPCs may be accessed in word or byte mode. On power-up or after a SYSRESET*, all devices will be set for byte-mode access. Chapter 4 gives details on how to configure a device for word accesses. Note that the memory map will change if word mode is selected. Table 2 gives the memory map for a device.

Table 2. MPCC Register Displacements

Byte Mode of Addressing				Word Mode of Addressing		
Addr (Hex)	Register Byte	Adr Hex	Register Byte	Addr (Hex)	Register Pair Higher Byte	Lower Byte
1	RSR	21	RCR	20	RCR	RSR
3	RDR	23		22	RDR --------	RDR
5	RIVNR	25	RIER	24	RIER	RIVNR
7		27		26		
9	TSR	29	TCR	28	TCR	TSR
B	TDR	2B		2A	TDR ---------	TDR
D	TIVNR	2D	TIER	2C	TIER	TIVNR
F		2F		2E		
11	SISR	31	SICR	30	SICR	SISR
13		33		32		
15	SIVNR	35	SIER	34	SIER	SIVNR
17		37		36		
19	PSR1	39	PSR2	38	PSR2	PSR1
1B	AR1	3B	AR2	3A	AR2	AR1
1D	BRDR1	3D	BRDR2	3C	BRDR2	BRDR1
1F	CCR	3F	ECR	3E	ECR	CCR

For easy, transparent software handling, each MPCC contains three different interrupt vector number registers which may be programmed at the user's discretion.

A common interrupt request signal is wired out of the MPCC to one of the seven VME bus interrupt request lines. This allows full asynchronous use of all the MPCCs on the board.

The three software selectable internal interrupt sources of each MPCC are:

a) the receiver interrupt

b) the transmitter interrupt

c) the modem handshake interface interrupt

Each of the three internal interrupt sources may generate an interrupt request to the VME bus if the interrupt is enabled in the interrupt mask.

MPCC Interrupt Handling

The MPCC has three interrupt vector registers:

i. Receiver Interrupt Vector Number Register (RIVNR)
ii. Transmitter Interrupt Vector Number Register (TIVNR)
iii. Serial Interrupt Vector Number Register (SIVNR)

These three interrupt vector registers have a priority within the MPCC in the order listed above.

This means that if a pending interrupt request has been generated simultaneously by both the Transmit and Receive sides of the MPCC, the host CPU will service the Receiver interrupt first then Transmitter and finally the Serial.

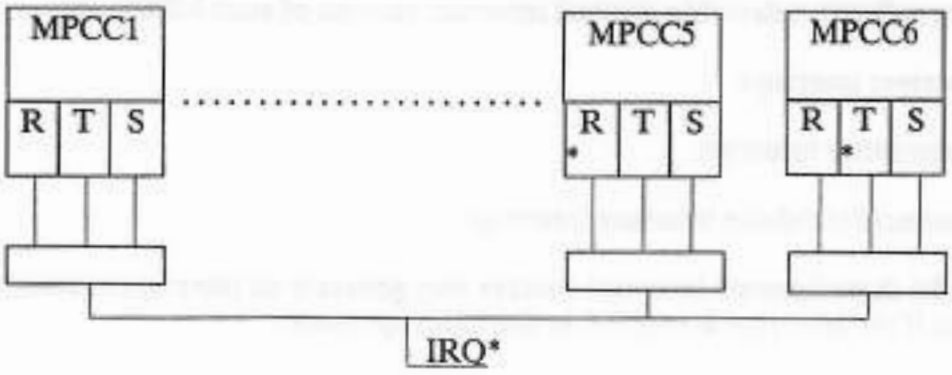
If an interrupt generating status occurs in the MPCC and the corresponding interrupt enable bit is set, the MPCC asserts its IRQ* output.

The interrupt generating status bits are allocated to the appropriate vector register. For example; If the active interrupt is Receive, the MPCC asserts the IRQ* output and then on receipt of an IACKIN* from the host processor, asserts DTACK* and places the Receive Interrupt Vector on the D0-D7 data bus.

This has the advantage that the interrupt handling program has only to read one status register to decide on the origin of the interrupt. The IRQ* line will stay asserted until the cause of the last interrupt is removed or disabled.

In parallel with the internal interrupt priority structure, each MPCC is assigned a priority in the overall board interrupt structure. This priority between MPCC devices will be recognised over any Receive/Transmit/Serial priority existing. The MPCC priority is such that MPCC 6 has the highest priority and MPCC 1 the lowest.

As an example, consider the following case of two MPCCs, both with pending interrupts, one a Receive (MPCC 5), the other a Transmit (MPCC 6):



Although the internal priority of MPCC 5 is of a higher level than that of MPCC 6, the host processor is able to recognise (by decode logic) that it must finish servicing the highest priority MPCC (MPCC 6) before MPCC 5.

The IRQ* signal must be assigned a standard VME priority level and this is performed by inserting one of seven VME IRQ* links in Field BR5. Field BR4 must also be programmed with a binary value representing the interrupt level set in BR5. It is this binary value that the interrupt logic will use to compare against the incoming interrupt level code when the CPU responds to the IRQ*.

Chapter 4 describes how to set up the interrupt level.

Run/Local Switch

This toggle switch on the front panel sets the board to LOCAL mode when the switch is up, switching is actually performed at the end of the pending cycle. The red LED lights when this mode is selected.

In LOCAL mode the IRQ output to the VME bus is forced inactive. If an IRQ output is active when the board is switched to LOCAL, a bus error may occur when this interrupt is serviced as no acknowledge signal wil be recognised by the board while in LOCAL mode. The IACKIN* signal still produces an IACKOUT* to support the interrupt daisy chain.

No write or read operations can be performed on the board while in local mode.

When switched to RUN mode, the green LED lights and normal operation takes place.

Serial Interface

The SIO-1 contains both RS 232C and RS 422A drivers and receivers. Each channel is independantly configurable to either standard. Chapter 4 describes how this is done.

RS 232C

The RS 232 portion of the SIO-1 interface conforms to EIA Standard RS 232C which covers the three areas of a communications interface; functional, electrical and mechanical. RS 232C is a North American standard but the SIO-1 also conforms to the European equivalents of RS 232C, these being, CCITT V.24 (functional), CCITT V.28 (electrical) and ISO 2110 (mechanical).

The functional part of RS 232C defines 25 interface signals and, while CCITT V.24 supports all these 25, it also includes several additional signals required for the national variations encountered in the various European telephone switching systems. Many of the 25 signals in the basic RS 232C Specification are defined for specialist functions such as Rate Selection and Secondary Channel control and the SIO-1 uses only 10 of the 25 lines. Table 3 identifies the circuit designations for both standards.

The electrical characteristics are determined by the voltages used by the interface line drivers and receivers. Nominally, the two voltages used to represent the two states of binary one and zero are +12 volts and -12 volts respectively. The SIO-1 uses standard DS1488 drivers and DS1489A receivers which conform to RS 232C and CCITT V.28.

The mechanical side of both standards defines maximum cable lengths and Plug/Connector pin-outs. The recommended maximum length of cable to be used for DTE-to-DTE or DTE-to-DCE is 50 feet or 15 meters. In practise, these distances can be extended but with possible increases in error rates. The cable should be terminated at both ends via a 25-pin D-type connector and Table 3 includes the designated pin-outs for the 9 signals used on the SIO-1. For modem use, the cable should always be in a 1:1 configuration i.e. Pin 1 to Pin 1, Pin 2 to Pin 2, etc.

Table 3. RS 232C Interface Circuit Designations

Signal name	Circuit Designation		D-Type Pin
	RS 232C	CCITT V.24	
Signal Gnd.	AB	102	7
Transmit Data	BA	103	2
Receive Data	BB	104	3
Request To Send	CA	105	4
Clear To Send	CB	106	5
Data Set Ready	CC	107	6
Data Terminal Ready	CD	108.2	20
Carrier Detect	CF	109	8
Transmit Clock	DB	114	15
Receive Clock	DD	115	17

RS 422A

The RS 422 portion of the SIO-1 interface conforms to EIA standard RS 422A. The SIO-1 also conforms to CCITT recommendations V.11 and X.27. Note that the RS 422A standard only covers the electrical specification of the interface.

RS 422A Interface circuit designations

Transmit Data
Receive Data
Request To Send
Clear To Send

Chapter 4 - Configuration

Introduction

The PME SIO-1 contains a number of link and wire-wrap areas that allow the board to be configured to individual system requirements. Soldering to the pins in these areas is not advised as damage may result, giving unreliable link or wire-wrap connections in the future. Soldering may also invalidate any warranty on the product.

User-Selectable Functions

The following functions are user-selectable by means of links or wire-wraps:

Addressing	Start address Address modifier
Interrupts	Interrupt level
Serial Interfaces	Synchronous/asynchronous operation RS 232C/RS 422A drivers and receivers Connector configuration

Delivery Configuration

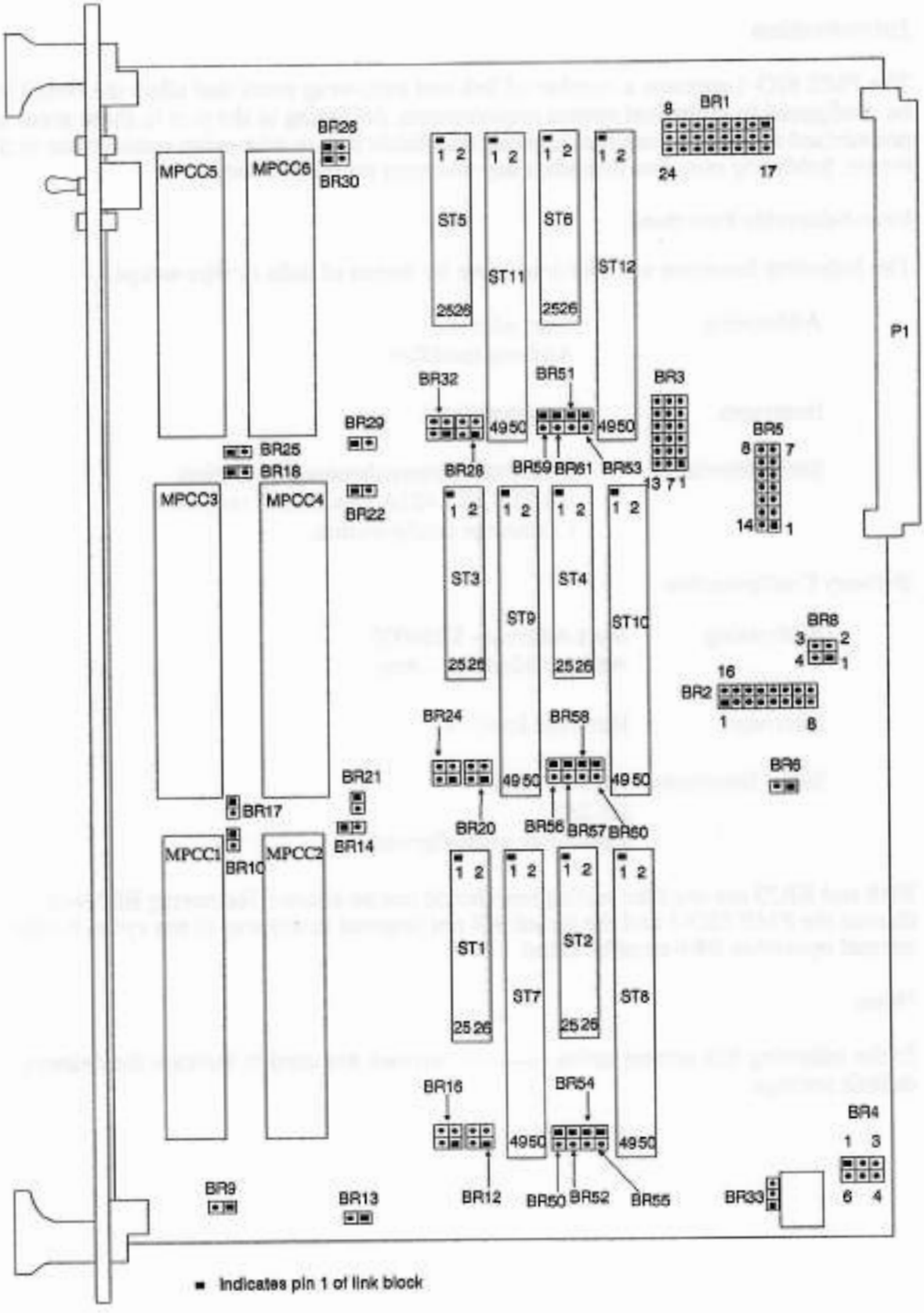
Addressing	Start Address - $B00000 Address Modifier - Any
Interrupts	Interrupt level - 4
Serial Interfaces	Asynchronous RS 232 Connector unconfigured

BR8 and BR33 are used for testing and should not be altered. Removing BR6 will disable the PME SIO-1 and the board will not respond in any way to any cycle, but for normal operation BR6 must be fitted.

Note:

In the following link setting tables, ←——→ arrows are used to indicate the delivery default settings.

Figure 6. PME SIO-1 Link Locations



Default Settings of Links (As supplied)

Jumper Area	Links fitted
BR1	2-10, 5-13, 6-14, 7-15, 8-16
BR2	1-16, 2-15, 3-14, 4-13, 5-12, 6-11, 7-10
BR3	7-13, 8-14, 9-15, 10-16, 11-17, 12-18,
BR4	1-6, 2-5
BR5	4-11
BR6	1-2
BR8	2-3
BR9	1-2
BR10	
BR12	
BR13	1-2
BR14	
BR16	
BR17	1-2
BR18	
BR20	
BR21	1-2
BR22	
BR24	
BR25	1-2
BR26	
BR28	
BR29	1-2
BR30	
BR32	
BR33	1-3
BR50	1-2
BR51	1-2
BR52	1-2
BR53	1-2
BR54	1-2
BR55	1-2
BR57	1-2
BR58	1-2
BR59	1-2
BR60	1-2
BR61	1-2

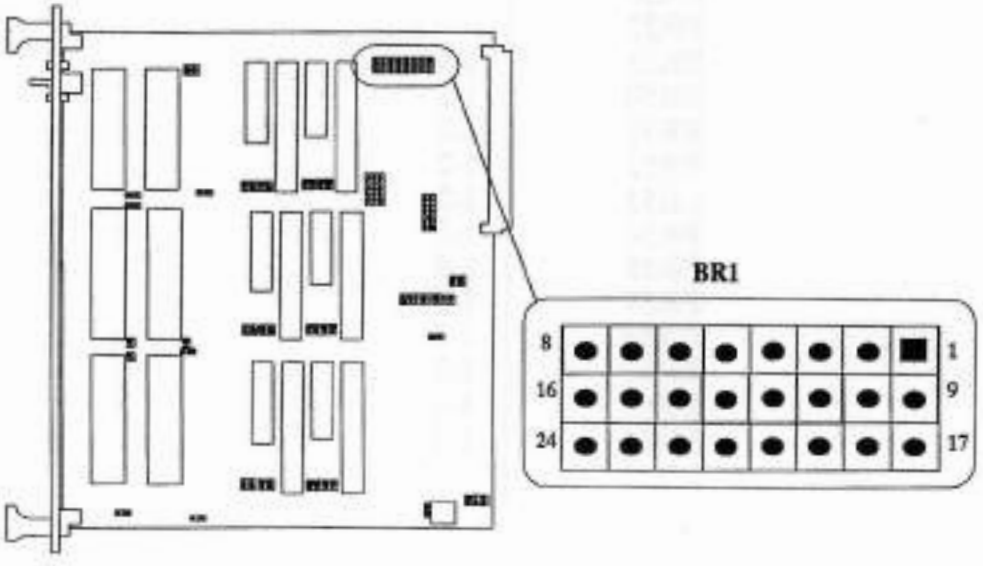
VME bus Addressing

The short address and the address modifiers of the PME SIO-1 are set up by means of three blocks of links.

BR1 selects addresses A23 through A16
BR2 selects addresses A15 through A9
BR3 selects AM codes AM0 through AM5

BR1 allows selection of high, low or don't care states on address lines A23 to A15. To decode as a Low, link between the first and second pin, to decode as don't care, link between the second and third pin, to decode as High, leave all pins open.

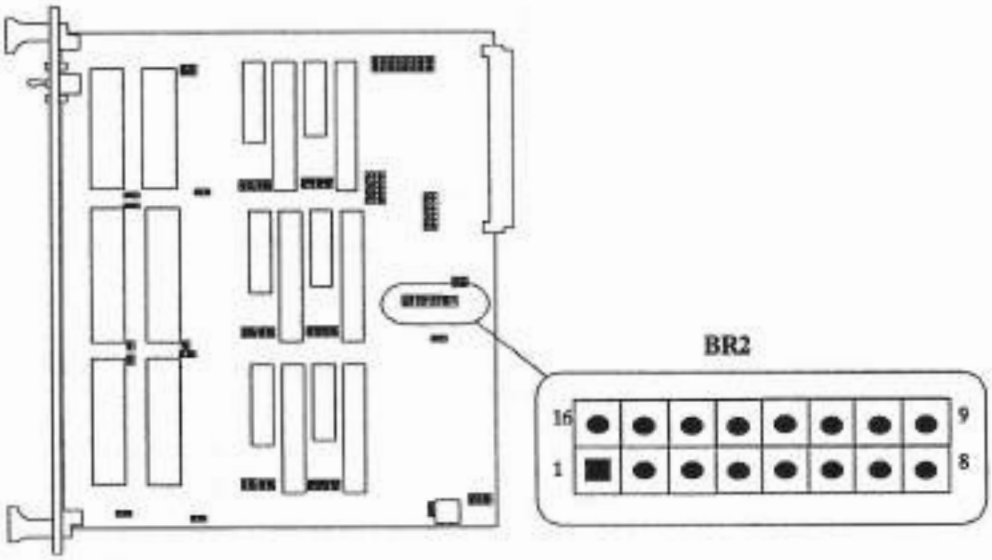
VME bus Address	BR1 Pins
A23	1 9 17
A22	2 ←→10 18
A21	3 11 19
A20	4 12 20
A19	5 ←→13 21
A18	6 ←→14 22
A17	7 ←→15 23
A16	8 ←→16 24



BR2 allows selection of high or low states on address lines A15 through A9. To decode as a High, leave the pins open.

VME bus Address	BR2 Pins
A15	1 ⟷ 16
A14	2 ⟷ 15
A13	3 ⟷ 14
A12	4 ⟷ 13
A11	5 ⟷ 12
A10	6 ⟷ 11
A9	7 ⟷ 10
Not Used	8 9

Note. It is important to leave BR2 8-9 open for correct address response.

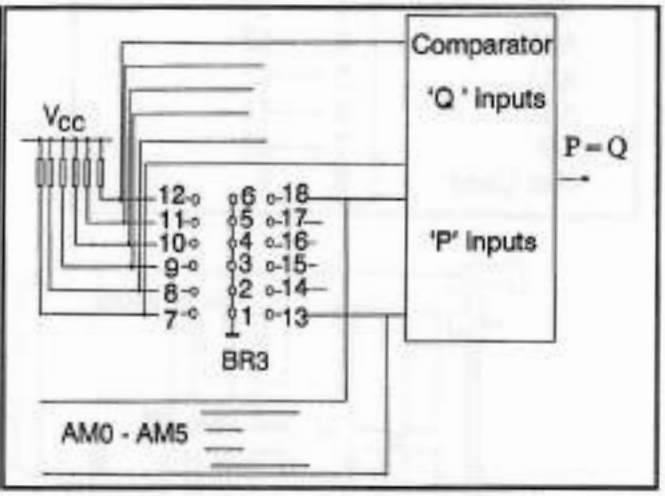


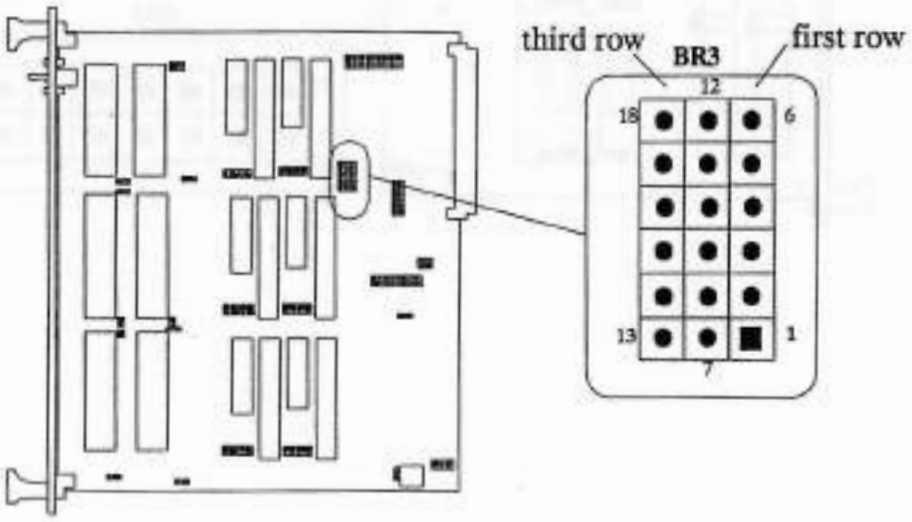
BR3 allows selection of High, Low, or don't care states on the address modifier lines. To decode as a Low, link between the first row and second row pin, to decode as a High, leave link pin open. Linking the second and third rows will link the 'P' inputs to the 'Q' inputs on the comparator chip (LS688). The corresponding 'P' and 'Q' inputs must therefore be identical, giving a 'don't care' condition.

Note that if AM codes 2D or 29 (short addressing) are selected, addresses A23 through A16 must be set up as don't cares using BR1.

Address Modifier	BR3 Pins	
AM5	18 ←→12	6
AM4	17 ←→11	5
AM3	16 ←→10	4
AM2	15 ←→9	3
AM1	14 ←→8	2
AM0	13 ←→7	1

Circuit detail





Interrupt Level

The interrupt level is set up using two sets of links, BR4 and BR5.

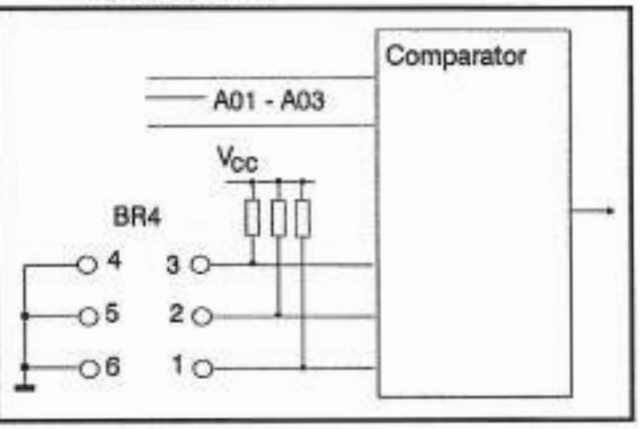
The interrupt acknowledge address is set up on BR4 for comparison with address lines A01 - A03. The interrupt level IRQ1 - IRQ7 is assigned by BR5. The values set on BR4 and BR5 should be the same, in order that the interrupt acknowledge address and selected interrupt level correspond.

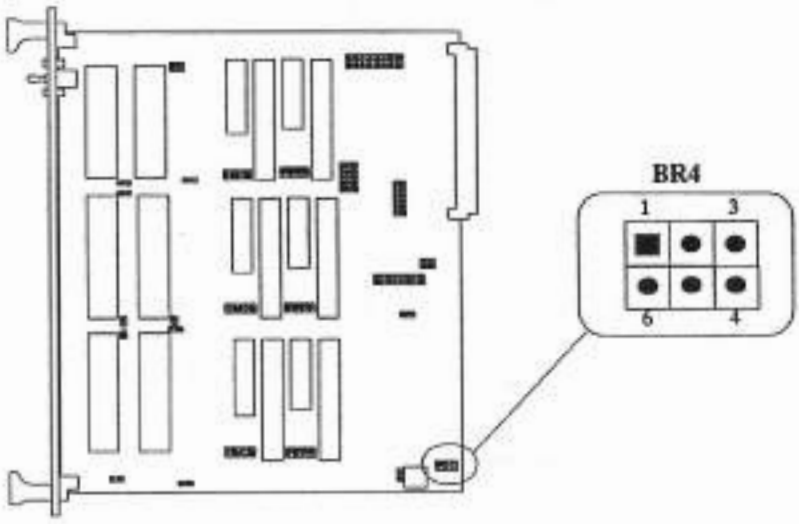
Pins 8 to 14 of BR5 are common and a single interrupt level only is allowed; BR5 should have only one link fitted.

For BR4 to decode as a Low, link the pins. To decode as a High, leave the pins open.

Circuit detail

VME bus Address	BR4 Pins
A01	1 ⟷ 6
A02	2 ⟷ 5
A03	3 4

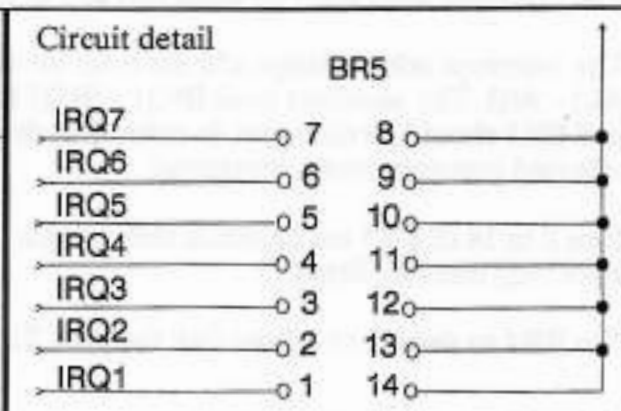


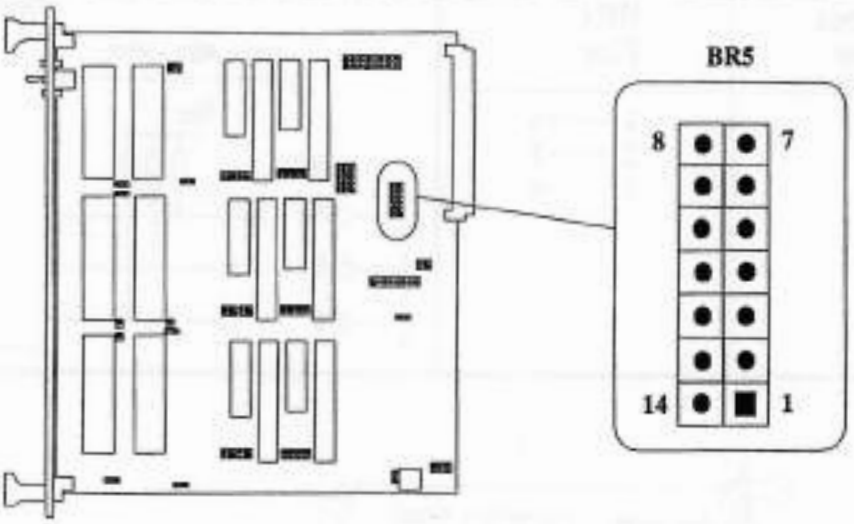


BR5 links out the interrupt line to one of the VME bus IRQ* lines. One link must be fitted. This must be the line of the same value as the interrupt address.

VME bus IRQ*	BR5 Pins	
IRQ7*	7	8
IRQ6*	6	9
IRQ5*	5	10
IRQ4*	4	11
IRQ3*	3	12
IRQ2*	2	13
IRQ1*	1	14

Circuit detail

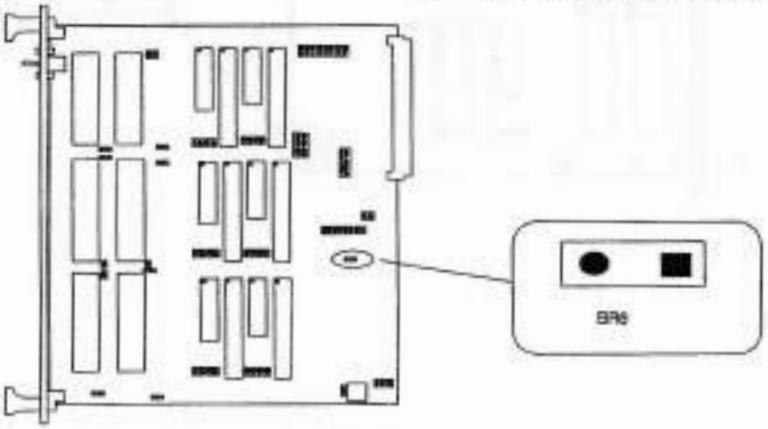




Board Disable Link BR6

The board can be disabled by removing link BR6; in this condition the board will not respond in any way to any cycle.

For normal operation BR6 must be fitted. The location of BR6 is shown below.



Serial Interfaces

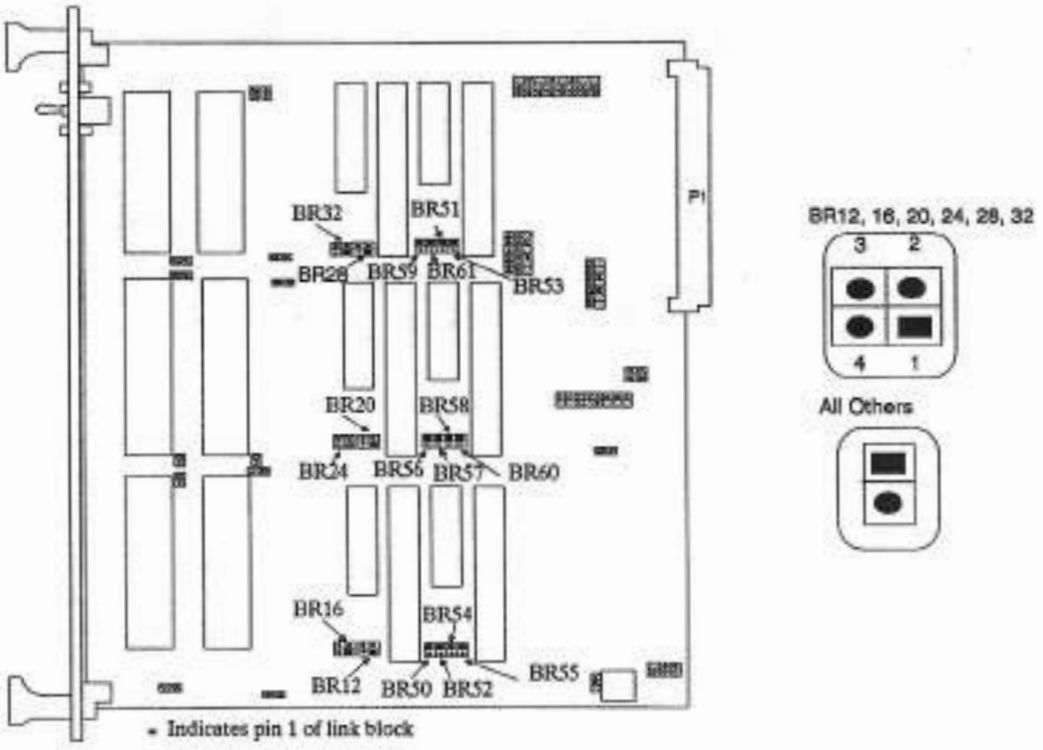
The following features are link selectable on each of the serial channels.

RS 232/RS 422
TxC Input/Output
DSR Input/Output

To Select RS 232

Two links per channel connect received data and Clear To Send to the MPCC for RS232. These must be fitted for RS232. One link block per channel is used to connect the same signals for RS422. These must be left open for RS232. See Table below.

Channel	Links fitted		Links open
1	BR50	BR52	BR12
2	BR54	BR55	BR16
3	BR56	BR57	BR20
4	BR58	BR60	BR24
5	BR59	BR61	BR28
6	BR51	BR53	BR32

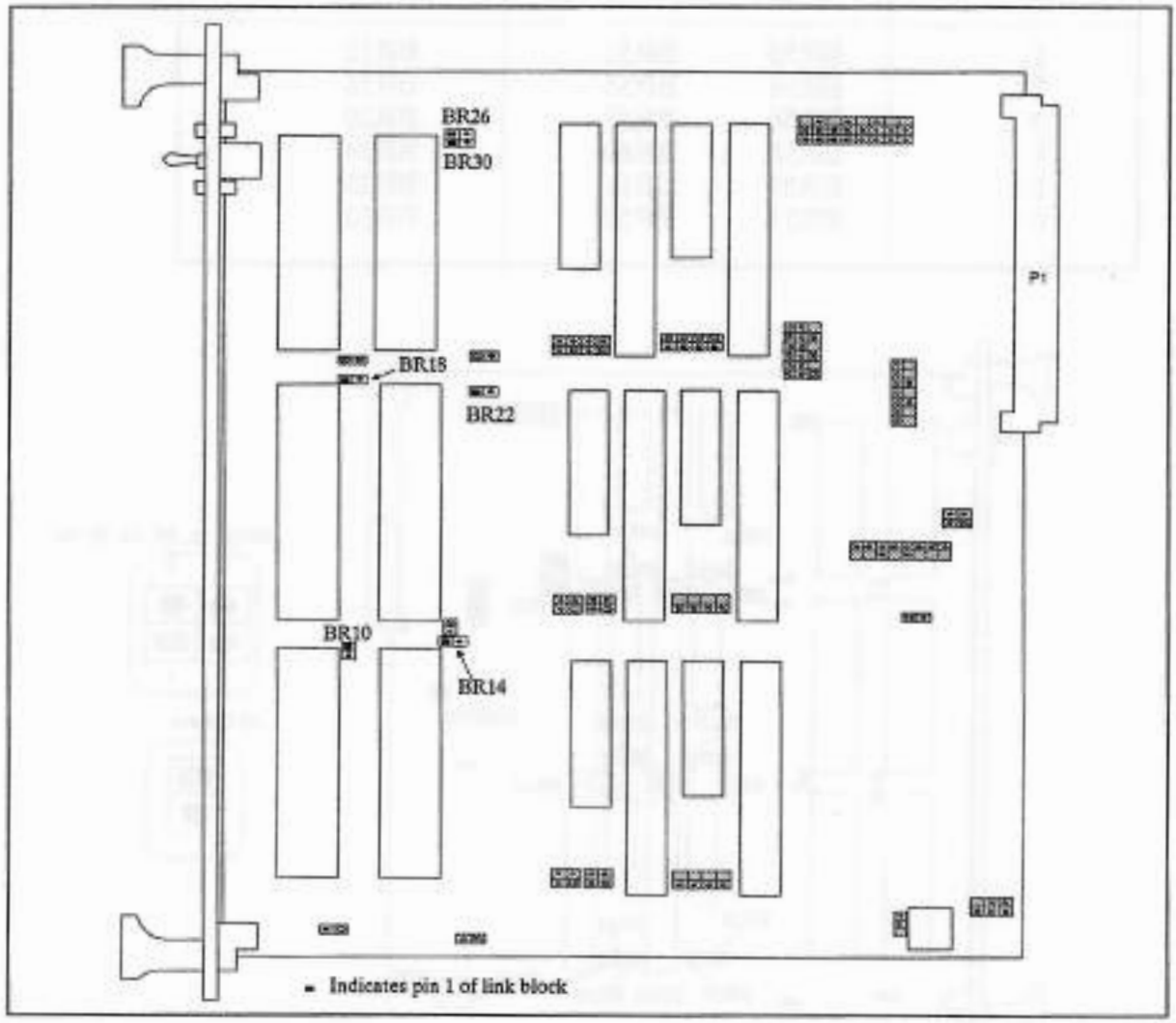


TxC

TxC may be an input or output. This is programmed in the relevant MPCC. If used as an input, the following links must be fitted. If used as an output, they must be open. This signal uses RS 232 levels only.

Channel	Link
1	BR10
2	BR14
3	BR18
4	BR22
5	BR26
6	BR30

Default is all links OUT

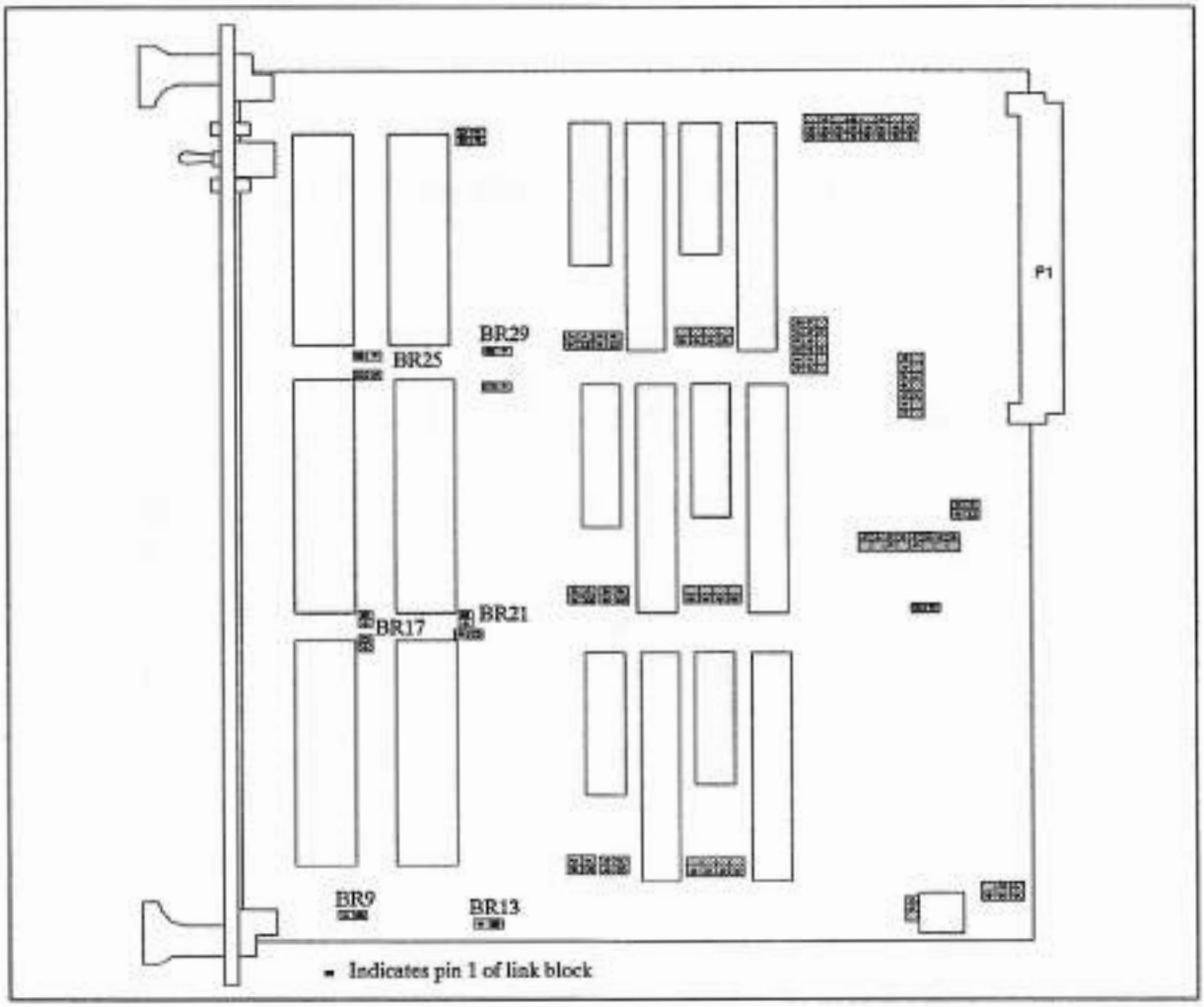


DSR

DSR may be an input or output. If used as an input the following links must be fitted. If used as an output they must be open. This signal uses RS 232 levels only.

Channel	Link
1	BR9
2	BR13
3	BR17
4	BR21
5	BR25
6	BR29

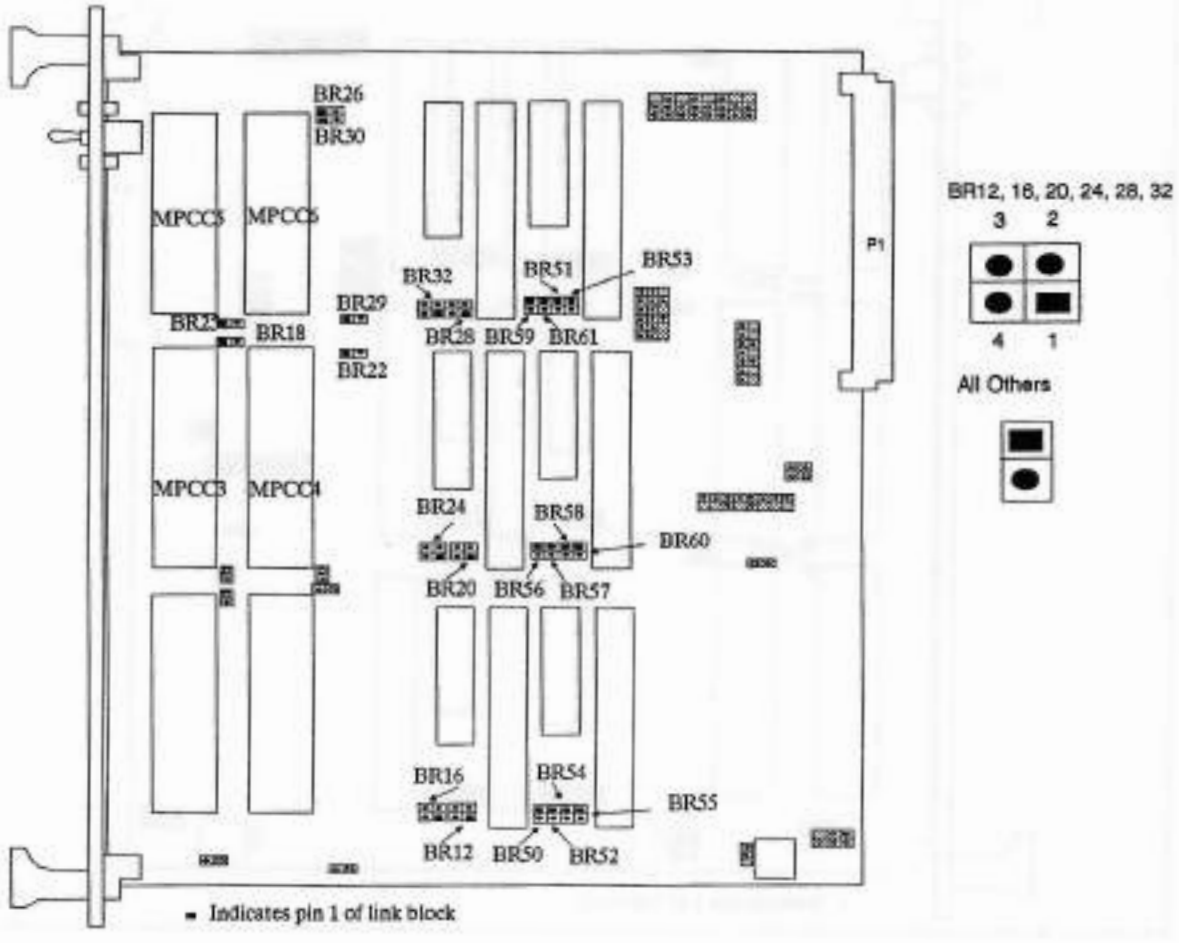
Default is all links IN



To Select RS 422

Two links per channel connect received data and Clear To Send to the MPCC for RS232. These links must be left open for RS 422. One link block per channel is used to connect the same signals for RS 422. These must be fitted for RS 422. See Table below.

Channel	Links fitted	Links open
1	BR12 1-4, BR12 2-3, ST7 31-46	BR50, BR52
2	BR16 1-4, BR16 2-3, ST8 31-46	BR54, BR55
3	BR20 1-4, BR20 2-3, ST9 31-46	BR56, BR57
4	BR24 1-4, BR24 2-3, ST10 31-46	BR58, BR60
5	BR28 1-4, BR28 2-3, ST11 31-46	BR59, BR61
6	BR32 1-4, BR32 2-3, ST12 31-46	BR51, BR53



Connector Configuration

To allow complete flexibility each channel has a wire wrap area and a transition connector.

Channel	Wire Wrap Area	Transition Connector
1	ST7	ST1
2	ST8	ST2
3	ST9	ST3
4	ST10	ST4
5	ST11	ST5
6	ST12	ST6

As each channel is identical the following description applies to all channels:

The transition connector, or flat cable connector, pin numbers correspond one to one to a twenty-five way D-type connector when using flat cable.

The wire-wrap areas allow the user to configure the connection as required. Table 4 gives the wire-wrap area pin definitions.

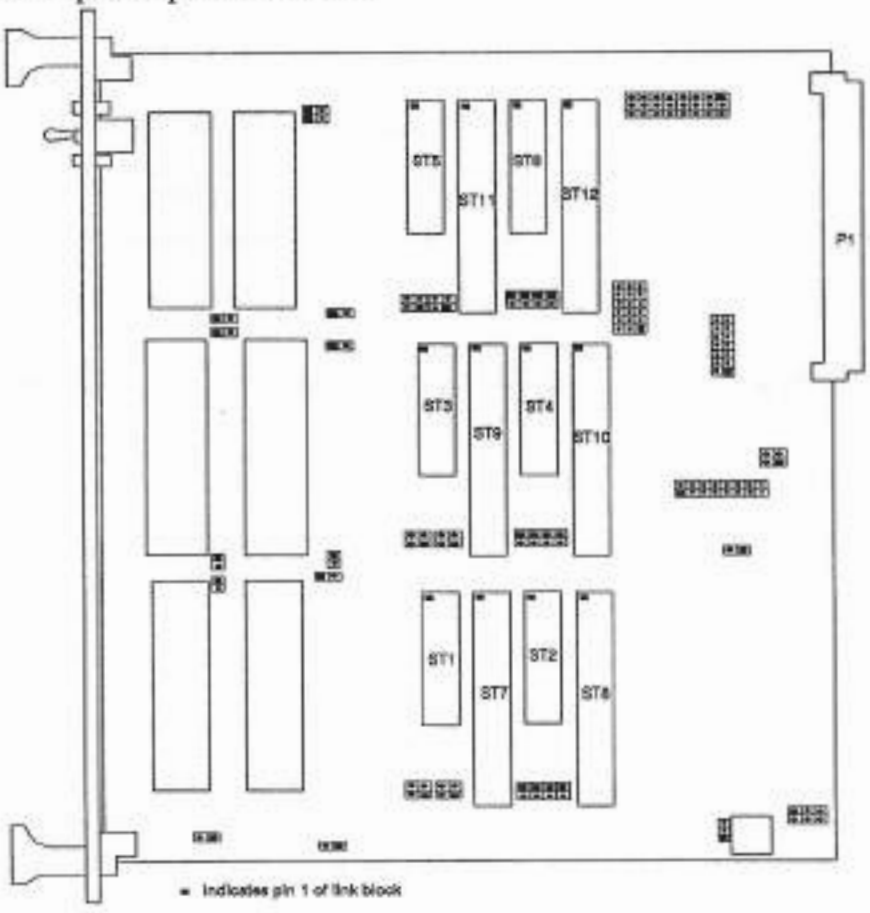


Table 4. Wire-wrap Area Pin Definitions

Wire Wrap Pin	Signal	Wire Wrap Pin	Signal	I/O
1	TC 14	26	RS 232 RTS	O
2	TC 1	27	RS 232 DTR	O
3	TC 15	28	RS 232 DSR	O
4	TC 2	29	RS 232 DSR	I
5	TC 16	30	RS 232 CTS	I
6	TC 3	31	RS 232 DCD	I
7	TC 17	32	RS 232 TxD	O
8	TC 4	33	RS 232 TxC	O
9	TC 18	34	RS 232 TxC	I
10	TC 5	35	RS 232 RxD	O
11	TC 19	36	RS 232 RxC	O
12	TC 6	37	RS 422 TxD +	O
13	TC 20	38	RS 422 TxD-	O
14	TC 7	39	RS 422 RTS +	O
15	TC 21	40	RS 422 RTS-	O
16	TC 8	41	RS 422 CTS +	I
17	TC 22	42	RS 422 CTS-	I
18	TC 9	43	RS 422 RxD +	I
19	TC 23	44	RS 422 RxD-	I
20	TC 10	45	-12V	
21	TC 24	46	+ 12V	
22	TC 11	47	-12V	
23	TC 25	48	+ 12V	
24	TC 12	49	GND	
25	TC 13	50	GND	

TC = Transition Connector

Some examples of configuring the connectors are given in the following pages:

Interface Configurations

Both 9-Wire and 3-Wire operations are covered. 3-Wire operation would normally only be used in a very simple Master/Slave configuration such a connecting a VDU to a processor, consisting as it does of only the Transmit and Receive interface lines plus a signal ground reference with no handshake controls. Synchronous communication cannot be supported by 3-Wire operation.

Full handshake facilities are provided by 9-Wire operation, either through a modem or a direct connect link and supports Synchronous communication.

The main area for possible configuration changes is the choice to operate the link via modems or as a direct connect system, a brief description of the requirements of both types of link is included here.

Modem Connection (DTE)

If the SIO board is to be linked via modems, the interface must be configured as a DTE (Data Terminal Equipment) which assumes that the signals going to/coming from the SIO-1 will be driven by some form of MODulator/DEModulator (MODEM) which will perform the necessary conversion from a digital signal to an analogue signal (and vice versa) suitable for transmission over a telephone network. DTE devices are normally said to function as a source or sink for data.

The modems and other such signal conversion devices associated with the telephone network are given the collective name of DCE (Data Circuit-termination Equipment) and do not normally source or sink data.

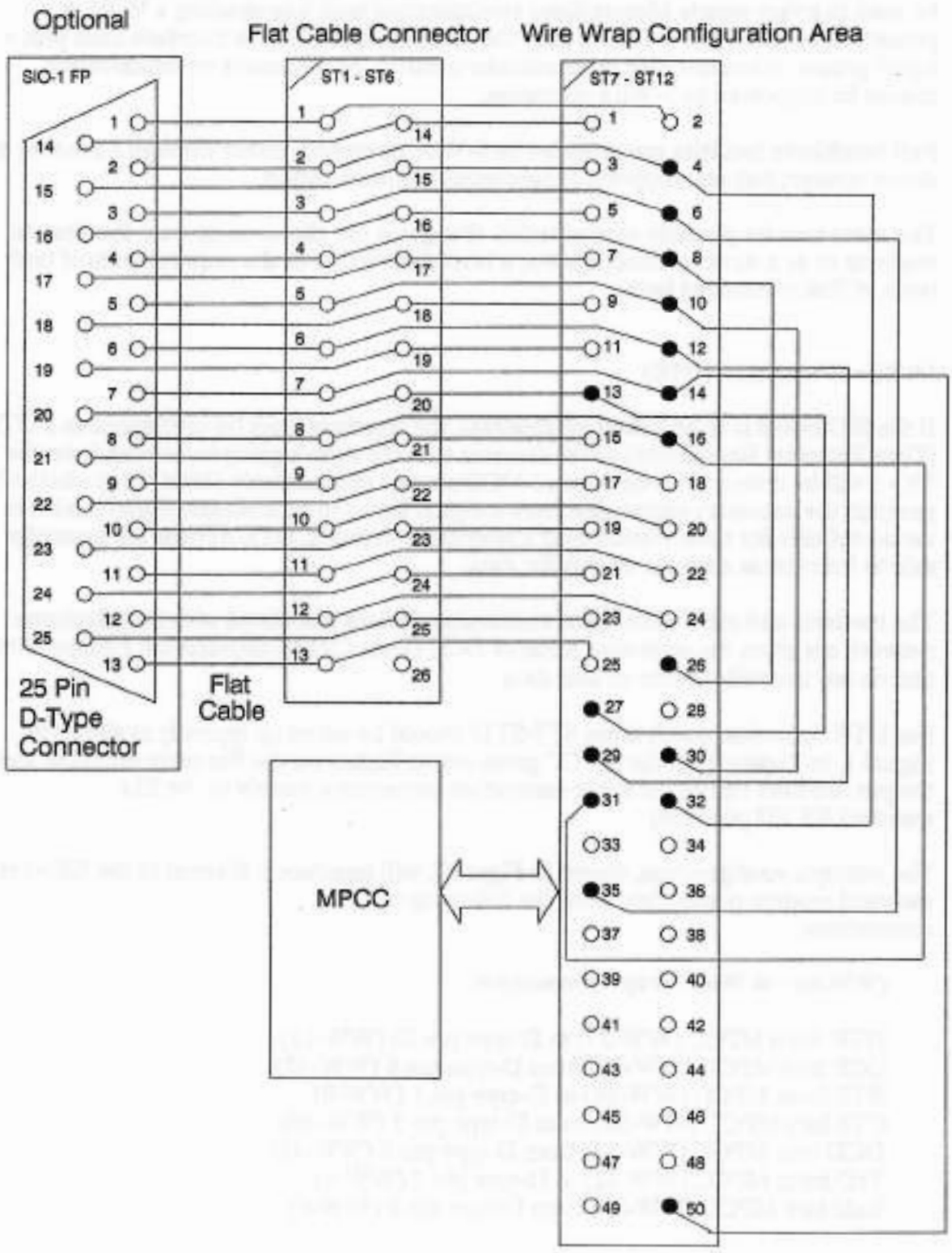
For DTE operation, patch areas ST7-ST12 should be wired up typically as shown in Figure 7, ie Txdata from the MPCC going out to Txdata on the flat cable etc (note that the pin numbers on the flat cable connectors correspond exactly to the EIA standard RS 232 pin-outs)

The example configuration, shown in Figure 7, will interface a channel of the SIO-1 to a standard modem connection using the following signal connections:

(WW-nn) = Wire Wrap - pin number.

DTR from MPCC (WW-27) to D-type pin 20 (WW-13)
DSR into MPCC (WW-29) from D-type pin 6 (WW-12)
RTS from MPCC (WW-26) to D-type pin 4 (WW-8)
CTS into MPCC (WW-30) from D-type pin 5 (WW-10)
DCD into MPCC (WW-31) from D-type pin 8 (WW-16)
TxD from MPCC (WW-32) to D-type pin 2 (WW-4)
RxD into MPCC (WW-35) from D-type pin 3 (WW-6)

Figure 7. DTE (Modem) Connection



Notes on Modem Connection

For modem connection it is not necessary to convert a stream of transmitted data into a stream of receive data for the receiving device, the modem itself makes the switch.

A modem connection makes other assumptions, which may or may not be realised depending on the handshaking level of which the modem is capable. The first of these is the interaction of the Data Terminal Ready/Data Set Ready signals.

Data Terminal Ready is a signal which should be raised by DTE devices at power up and simply indicates that the interface is powered up and functional. The modem will see this Data Terminal Ready and will respond with an equivalent signal called Data Set Ready. The patch area can be used to simulate this handshake, should either of these signals not be available.

The second of these handshake signals is the Request To Send/Clear To Send (RTS/CTS) pair. (Note: The term Clear To Send (CTS) has in recent years also been referred to as Ready For Sending (RFS)). A DTE, wishing to transmit, will raise its Request To Send which will cause the modem to activate the data carrier. When the carrier has stabilised, the modem will return Clear To Send indicating that the DTE can begin transmitting data. RTS/CTS interaction is of particular importance when using a Multipoint datacomms network employing "switched carrier".

Note: Request To Send must remain active throughout the transmission.

It is conceivable that the SIO-1 could be interfaced to a modem which is not capable of returning Clear To Send in which case the outgoing Request To Send can simply be patched across to Clear To Send.

A third interface signal, which may or may not be present, is the Data Carrier Detect signal. Data Carrier Detect is asserted by a DCE when it detects an incoming carrier ie a remote device has raised its Request To Send line and is about to transmit. The communication controller can use this level signal to prepare to receive incoming data.

It is worth mentioning at this point the existence of Null modems. The term "null modem" refers to a device used to extend the physical distance between DTE's without using the normal modulation techniques employed by conventional modems. The null modem performs regeneration of the digital signals in each direction preventing signal rise and fall times from degrading appreciably. Null modems also perform pin reversal of the various interface control and data signals for correct DTE-to-DTE operation.

Direct Connection (DCE)

If the SIO-1 board is to be linked by direct connect means, the SIO-1 interface must be configured to look and act like a DCE and some of the functions normally performed by the DCE must be simulated on the patch area. For all the connections mentioned below, it is assumed that the direct connect cable in use is a 1:1 set up i.e. Pin 1 of the D-type goes to Pin 1 of the opposite D-type, etc.

The first of the simulations is to perform the Txdata/Rxdata switch which is done by taking Txdata from the MPCC and connecting it to the Rxdata input line and vice versa with the incoming Rxdata line. (see Figure 8.)

The second is the simulation of the Request To Send/Clear To Send handshake. This can be done in either of two ways depending on whether Hardware Flow Control is necessary.

Devices, such as serial printers, can normally buffer only small amounts of data prior to printing. Therefore, such devices tend to exercise control over how the host system is allowed to send data, ie they will only allow the host to send a block of data if the printer buffer is currently empty or at least capable of storing the maximum size of a data block. Printers use the Request To Send from the host to exercise this control, only returning Clear To Send when ready. This facility is called Hardware Flow Control and to create this handshake, jumper the outgoing Request To Send (Host RTS) to the printers incoming Clear To Send. In the same way, jumper the printer's Request To Send to the Host Clear To Send. If Hardware Flow Control is not required and the need is simply to simulate the DCE signals for satisfying handshake requirements, the outgoing Request To Send can simply be looped round to Request To Send.

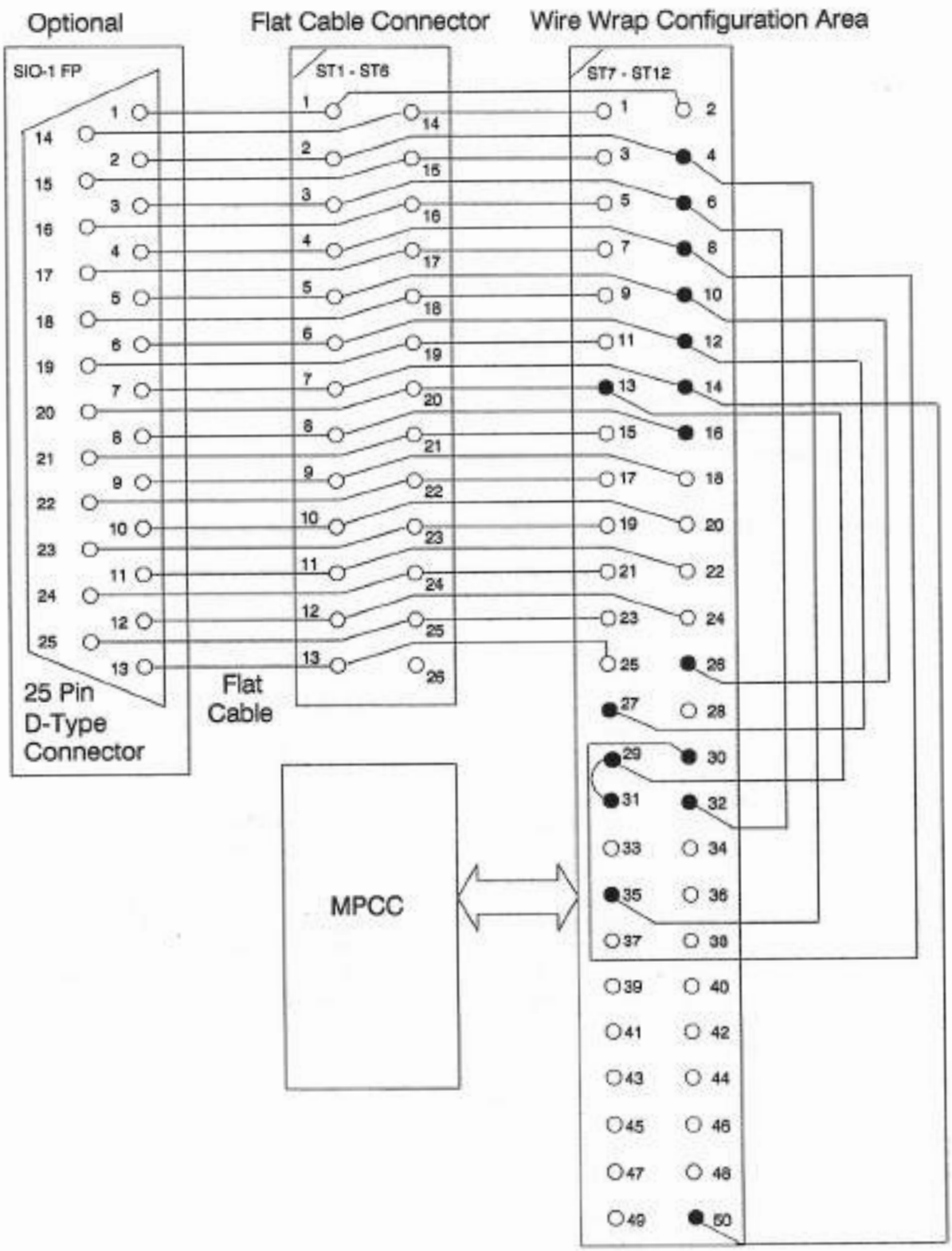
On a direct connect system, with no modems physically present, the various DCE control signals (Data Terminal Ready, Data Set Ready, Data Carrier Detect) must be simulated on the CN connector. Figure 8 shows a typical method for accomplishing this, although in practice it is likely that unless the communication firmware has been specifically written to verify these control lines, some of these signals can be ignored in a direct connect set-up.

The example shown in Figure 8 demonstrates a DCE configuration for interfacing one channel of the SIO-1 to another DTE using a 1:1 direct connect cable using the following signal connections:

(WW-nn) = Wire Wrap pin no.

DTR from MPCC (WW-27) to D-type pin 6 (WW-12)
DSR into MPCC (WW-29) from D-type pin 20 (WW-13)
RTS from MPCC (WW-26) to D-type pin 5 (WW-10)
CTS into MPCC (WW-30) from D-type pin 4 (WW-8)
DCD into MPCC (WW-31) from WW-29 (derived from incoming DTR)
TxD from MPCC (WW-32) to D-type pin 3 (WW-6)
RxD into MPCC (WW-35) from D-type pin 2 (WW-4)

Figure 8. DCE (Direct Connect) Configuration



Programming Example

Install the following wire wrap connections on the wire wrap area of MPCC 6:

For DCE:
02 - 14 - 50
26 - 30 - 31
32 - 6 display or printer data input
35 - 4 display or printer data input

For DTE:
02 - 14 - 50
26 - 30 - 31
32 - 6 display or printer data input
35 - 4 display or printer data input

INITMPCC: Initialize an MPCC
CHARINPUT: Input one character
STRINGOUT: Output of a string

The code starting at test causes an infinite stringout.

```
                ORG             $1000;
MPCCBASE:       EQU             $B00140     !       BASE ADR OF MPCC6
                BRA.L   TEST;
!               INITIALIZE FOR POLLING RECEIVE AND TRANSMIT

INITMPCC:       MOVE.L  A0,-(A7);           !
                MOVE.L  MPCCBASE,A0;        !       LOAD MPCC BASE ADR
                MOVE.B  #$1,$21(A0);        !       RESET RECEIVER
                MOVE.B  #$1,$29(A0);        !       RESET TRANSMITTER
                MOVE.B  #$00,$19(A0);       !       PSR1            ASYNCHR, 8 BIT,
                MOVE.B  #$5E,$39(A0)        !       PSR2 2 STOP BITS
                MOVE.B  #$8C,$1D(A0);       !       BRDR1           96
                MOVE.B  #$00,$3D(A0);       !       BRDR2           BAUD
                MOVE.B  #$1C,$1F(A0);       !       CCR INTERNAL CLOCK SELECT
                MOVE.B  #$00,$3F(A0);       !       ECR  NO PARITY
                MOVE.B  #$00,$25(A0);       !       DISABLE RECEIVER INTERRUPT
                MOVE.B  #$00,$2D(A0);       !       DISABLE TRANSMIT INTERRUPT
                MOVE.B  #$00,$35(A0);       !       DISABLE SER.INTERF.INTERR
                MOVE.B  #$80,$31(A0);       !       ASSERT RTS OUTPUT
                MOVE.B  #$00,$21(A0);       !       RECEIVER INTERFACE ENABLE
                MOVE.B  #$80,$29(A0);       !       TRANSMIT INTERFACE ENABLE
                MOVE.L  (A7)+,A0;
                RTS

!               INPUT ONE CHARACTER INTO D

CHARIN:         MOVE.L  A,0-(A7);
WAITRDA:        MOVE.L  MPCCBASE,A0; 0      !       LOAD MPCC BASE ADR
                BTST.B  #$07,$01(A0);       !       TEST RDA BIT
                BEQ.S   WAITRDA;
                MOVE.B  $03(A0),D0;         !       READ DATA MPCC - D0
                RTS;
```

```
                RTS;

                SUBROUTINE TO DUMP A STRING

                STOP TRANSMISSION:      XOFF    ($13)
                RESTART:        XON     ($11)

                START :  (A1)
                END:     (A2)

STRINGOUT:      MOVE.L  A0,-(A7);
                MOVE.L  MPCCBASE,A0;    !       LOAD MPCC BASE ADR
TEXTCHAR:       CMP.L   A1,A2;          !       COMPARE IF COMPLETED
BUFFERFULL:     BTST.B  #$07,$09(A0);   !       TEST TDRA FLAG
                BEQ.S   BUFFERFULL;     !       BRANCH IF BUFFER FULL
                BTST.B  #$07,$01(A0);   !       TEST RDA FLAG
                BEQ.S   OUTPUT;         !       BRANCH IF NO CHAR REC'D.
                CMPI.B  #$13,$03(A0);   !       TEST RECEIVED DATA
                BNE.S   OUTPUT;         !       BRANCH IS NO XOFF
OFFLOOP:        BTST.B  #$07,$01(A0);   !       TEST RDA FLAG
                BEQ.S   XOFFLOOP;       !       BRANCH TO WAIT XON CHAR
                CMPI.B  #$11,$03(A0);   !       TEST RECEIVED DATA
                BNE.S   XOFFLOOP;       !       BRANCH TO WAIT XON CHAR
OUTPUT:         MOVE.B  (A1)+,$0B(A0);  !       TRANSMIT CHAR
                BRA.L   NEXTCHAR;       !       CONTINUE WITH NEXT CHAR
STRINGEND:      MOVE.L  (A7)+,A0
                RTS;

TEST:           BSR.L   INITMPCC;
TESTLOOP:       LEA.L   STRING1,A1;
                LEA.L   STRING2,A2;
                LSR.L   STRINGOUT;
                BRA.S   TESTLOOP;

STRING1         DC.B    $0A;
                DC.B    $0D;
                DC      'ABCDEFG';

                DC.B    $0A;
                DC.B    $0D;

STRING2         DC.B    $00;
```

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To obtain copies of circuit diagrams, please sign and complete two copies of this form and forward to:

The Contracts Manager Radstone Technology plc Water Lane Towcester Northants NN12 7JN	or	The General Manager Radstone Technology Corp 20 Craig Road Montvale New Jersey 07645-1737

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In consideration of our supplying you with information concerning the PME product range for the purpose of allowing all user functions to be fully understood, it is agreed as follows:-

1. As used in this agreement:

   (a) "our information" shall mean all documents, ideas, know-how and other information supplied by us to you (whether disclosed to you orally, in documentary or other material form, by demonstration or otherwise) for the purpose referred to above;

   (b) "proper use" shall mean use solely for the purpose referred to above; and

   (c) "third party" shall include any parent, subsidiary or affiliated company of your Company.

2. All our information shall be treated by you as confidential, shall not be used by you except for proper use, shall not be disclosed to any person within your Company who is not directly concerned in its proper use, and shall not be disclosed to any third party without our prior written consent, except for such information as you can prove to our reasonable satisfaction:-

   (a) is already known to you at the date hereof and is or becomes free of restriction on disclosure and use (and you have advised us of the fact), or

   (b) is generally known or freely available to the public (except by reason of any breach by you of your obligations hereunder), or

   (c) has been disclosed to you, free of restriction on disclosure and use, by a third party who was entitled to make such unrestricted disclosure.

3. You will take such precautions and make such arrangements as are reasonably necessary to protect our information (and in any event no less than those you would take and make to protect your own confidential information). You will inform such of your employees as are concerned in its proper use of the confidential nature of our information, and you will prohibit each of them from making copies of any of it.

4. In the event that you do not purchase or discontinue purchase of the product, you will promptly and in any event, not later than 3 months after such event, and without further request, return to us all the documents and other material containing our information.

5 This Agreement shall be governed by and construed in accordance with the law of England.

..... For and on behalf of
Radstone Technology plc

Please send me a copy of the circuit diagrams for this product.

AGREED
For and behalf of .....Company name

Name .....(Please print)

Signed .....

Title .....

Date .....

Address .....

.....

.....

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To obtain copies of circuit diagrams, please sign and complete two copies of this form and forward to:

The Contracts Manager	or	The General Manager
Radstone Technology plc		Radstone Technology Corp
Water Lane		20 Craig Road
Towcester		Montvale
Northants		New Jersey
NN12 7JN		07645-1737

If your company has already entered a Confidentiality Agreement with Radstone Technology for PME products, no signature is required.

Confidentiality Agreement

In consideration of our supplying you with information concerning the PME product range for the purpose of allowing all user functions to be fully understood, it is agreed as follows:-

1. As used in this agreement:

   (a) "our information" shall mean all documents, ideas, know-how and other information supplied by us to you (whether disclosed to you orally, in documentary or other material form, by demonstration or otherwise) for the purpose referred to above;

   (b) "proper use" shall mean use solely for the purpose referred to above; and

   (c) "third party" shall include any parent, subsidiary or affiliated company of your Company.

2. All our information shall be treated by you as confidential, shall not be used by you except for proper use, shall not be disclosed to any person within your Company who is not directly concerned in its proper use, and shall not be disclosed to any third party without our prior written consent, except for such information as you can prove to our reasonable satisfaction:-

   (a) is already known to you at the date hereof and is or becomes free of restriction on disclosure and use (and you have advised us of the fact), or

   (b) is generally known or freely available to the public (except by reason of any breach by you of your obligations hereunder), or

   (c) has been disclosed to you, free of restriction on disclosure and use, by a third party who was entitled to make such unrestricted disclosure.

3. You will take such precautions and make such arrangements as are reasonably necessary to protect our information (and in any event no less than those you would take and make to protect your own confidential information). You will inform such of your employees as are concerned in its proper use of the confidential nature of our information, and you will prohibit each of them from making copies of any of it.

4. In the event that you do not purchase or discontinue purchase of the product, you will promptly and in any event, not later than 3 months after such event, and without further request, return to us all the documents and other material containing our information.

5 This Agreement shall be governed by and construed in accordance with the law of England.

..... For and on behalf of
Radstone Technology plc

Please send me a copy of the circuit diagrams for this product.

AGREED
For and behalf of .....Company name

Name .....(Please print)

Signed .....

Title .....

Date .....

Address .....

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