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PMV 68 AIP-1
Manual

Revision A

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Chapter 1 - Introduction

Scope

This manual describes the PMV 68 AIP-1. The AIP-1, in common with all other PMV 68 modules, is available in five versions/build standards (under the following product codes):

Military Conduction Cooled	PMV68 AIP1-xyzMI
Military Air Cooled	PMV68 AIP1-xyzMA
Rugged Conduction Cooled	PMV68 AIP1-xyzRI
Rugged Air Cooled	PMV68 AIP1-xyzR
Commercial	PMV68 AIP1-xyzE

where xyz is the variant number.

PMV 68 AIP-1

The AIP-1 Analog Input Board interfaces directly to the VMEbus and provides the user with 32 single-ended / 16 differential analog input channels.

This manual includes a full description of the features of the AIP-1, and instructions on how to configure, install and operate the board. Example programs are provided to illustrate the use of the board in a standard VMEbus system.

The main features of the PMV 68 AIP-1 are:

- 32 single-ended/16 differential analog input channels with 12 bit resolution
- Up to 50kHz throughput for one channel (20ms period) with software gain set to x1, otherwise 33kHz (30ms period)
- Analog input section optically isolated from the VMEbus
- Random channel order selection using scan list
- Hardware Configurable Input Gain for all channels (x1, x10,x100, user selectable)
- Software Programmable Channel Gain for individual channels (x1, x10, x100)
- On-board user selectable sample rate generator
- 4 interrupt sources (Half full, Block full, Single sample, Programmable Stop flag)
- 7 levels of interrupt (software programmable)
- 4 trigger options (internal, external, event, software)
- 2 data acquisition modes (continuous, transient)
- 2 operating modes (polling, interrupt)
- Software board reset
- One of the Radstone PMV 68 family

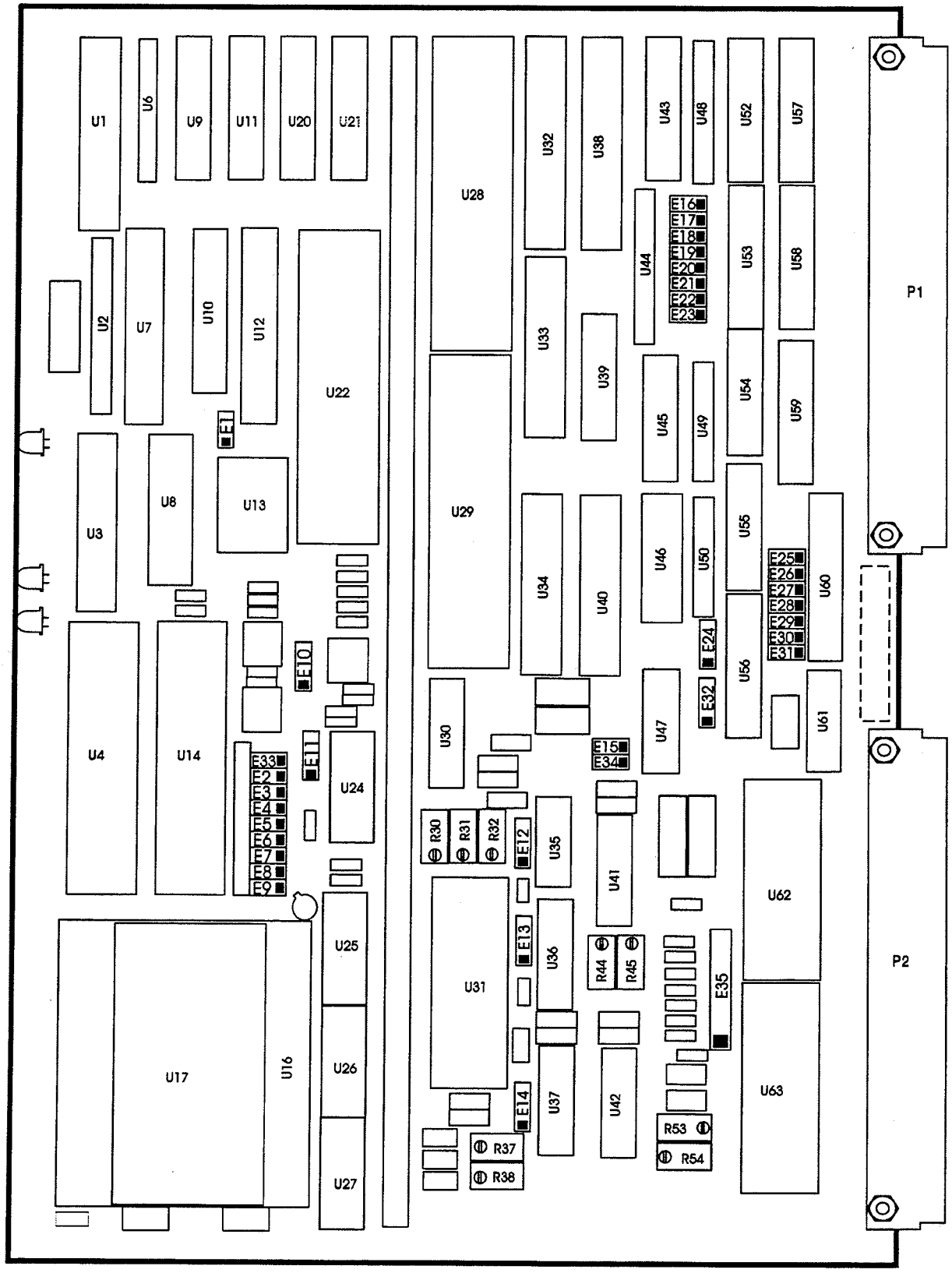
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Figure 1 - PMV 68 AIP-1

TBA

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Figure 2 - PMV 68 AIP-1 Board Layout



■ Indicates pin 1

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PMV 68 Family

The AIP-1 is a member of the PMV 68 VMEbus family, which is a range of high performance processor, memory and I/O boards. PMV 68 satisfies the demands of today's military system designers for reliable, high performance, modular processing systems. It is complemented by Air Transportable Racking (ATR) boxes of various sizes, plus the necessary software and hardware development facilities. For up-to-date details of this ever growing range, please contact your supplier. The major features of PMV 68 include:

- Totally VMEbus compatible family of modules
- Multiprocessor dual bus architecture
- Communications interfaces
- 32-bit architecture
- ATR box compatible (per IEEE Std 1101.2-1992)
- Commercial VMEbus rack compatible
- EPROM stored Built In Test Equipment (BITE) programs
- Monitor (PLUM-4) supplied as standard
- Five 100% software compatible build standards

Mechanical Overview

All PMV 68 modules come in five electrically compatible build standards, each carefully tailored to a particular set of requirements and environments. All five standards fully support the power and versatility of the VMEbus, so no matter how large or diversified your project, MIL-STD-VME assures absolute compatibility at all stages of development. Due to the common circuit design, this manual describes a 'generic' standard, the exception being the individual mechanical specifications of each standard. A short description of each standard follows:

PMV 68MI

At the top of the range, the MI-style complies with the most stringent military design rules and represents the highest level of reliability and environmental resistance available. Designed primarily for use in sealed ATR chassis, MI-style boards feature MIL-STD-454 qualified components, an integral thermal management layer and incorporate a central stiffening bar for additional strength. Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. MI-style boards comply fully with IEEE Std. 1101.2-1992.

MI-style boards are designed to withstand environments involving extremes of temperature, shock and vibration.

Careful attention to design details ensures that the MI-style remains compatible with standard Commercial VMEbus racks.

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PMV 68MA

Produced to the same strict military guide lines and specifications as the MI-style boards, using screened military components, MA-style boards are designed for mounting in conventional, rugged or custom VMEbus racking systems. The boards are mechanically stiffened and cooling is by forced air.

PMV 68RI

Mechanically identical to the MI-style, the RI-style is populated with wide temperature range, industrial grade ceramic packaged devices offering a 100% compatible, economical alternative to MI-style, for use in Radstone's ATR boxes and other conduction cooled environments.

PMV 68R

R-style boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional air-cooled racking systems. These rugged boards consist of a double-Eurocard size printed wiring board fitted with wide temperature range, hermetically packaged, industrial grade ceramic components and incorporate a centre stiffening bar.

PMV 68E

E-style provides the ideal cost effective method of complete system development. As software compatibility throughout the build standards is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to target style only in the final stages of testing.
Each E-style assembly comprises a double-Eurocard size printed wiring board with high quality commercial (plastic encapsulated) ICs. The boards survive the same levels of shock and vibration as the MA and R-styles. E-style boards are designed for blown air cooling.

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PMV 68 AIP-1 Functional Overview

The AIP-1 Analog Input Board is supplied as a single 6U card, and is electrically and mechanically compatible with the VMEbus specification.

The AIP-1 provides 32 single-ended / 16 differential analog inputs with fully programmable gain amplification (PGA) on all channels. Optical Isolation of the VMEbus from all inputs insulates the bus and the user's valuable system components from the effects resulting from the accidental application of large voltages. This feature makes the AIP-1 ideally suited to industrial applications where a high degree of bus isolation is required. All analog inputs are accessible via VME connector P2.

Three LEDs on the front panel provide a visual indication of the current board status. The **Oversample** LED illuminates **YELLOW** whenever the sample rate exceeds 60kHz. The **Halt** LED illuminates **GREEN** to indicate that the conversion process is halted. The **SYS-FAIL FAIL** LED illuminates **RED** on initial power up and can be extinguished by an appropriate VME access.

The order in which analog inputs are sampled by the AIP-1 is controlled by entering channel addresses into a 64 byte programmable Scan List (see Chapter 5). When operating in transient mode (see Chapter 6), the AIP-1 cycles through consecutive entries in the Scan List until all 64 elements have been accessed, halts automatically and waits to be re-initialised. When operating in continuous mode (see Chapter 6), the AIP-1 cycles continuously through consecutive entries in the Scan List until halted by the CPU.

The rate at which the inputs are sampled, or scanned, is determined by one of four software selectable sources :

- Trigger signal generated by an internal timer
- Trigger signal generated by an external timer (and applied to connector P2)
- Initiated by an external event signal and continuing at a rate determined by an internal timer
- Software generated

The AIP-1 memory map occupies 512 consecutive byte locations in the VMEbus short address space as illustrated in Figure 3.

As each channel is sampled, the instantaneous analog value acquired is applied to a 12 bit analog-to-digital converter (ADC) which generates a 12 bit digital code that is proportional to the original analog signal. The digital codes are stored in consecutive locations of the 64 word converted data memory (see Figure 3).

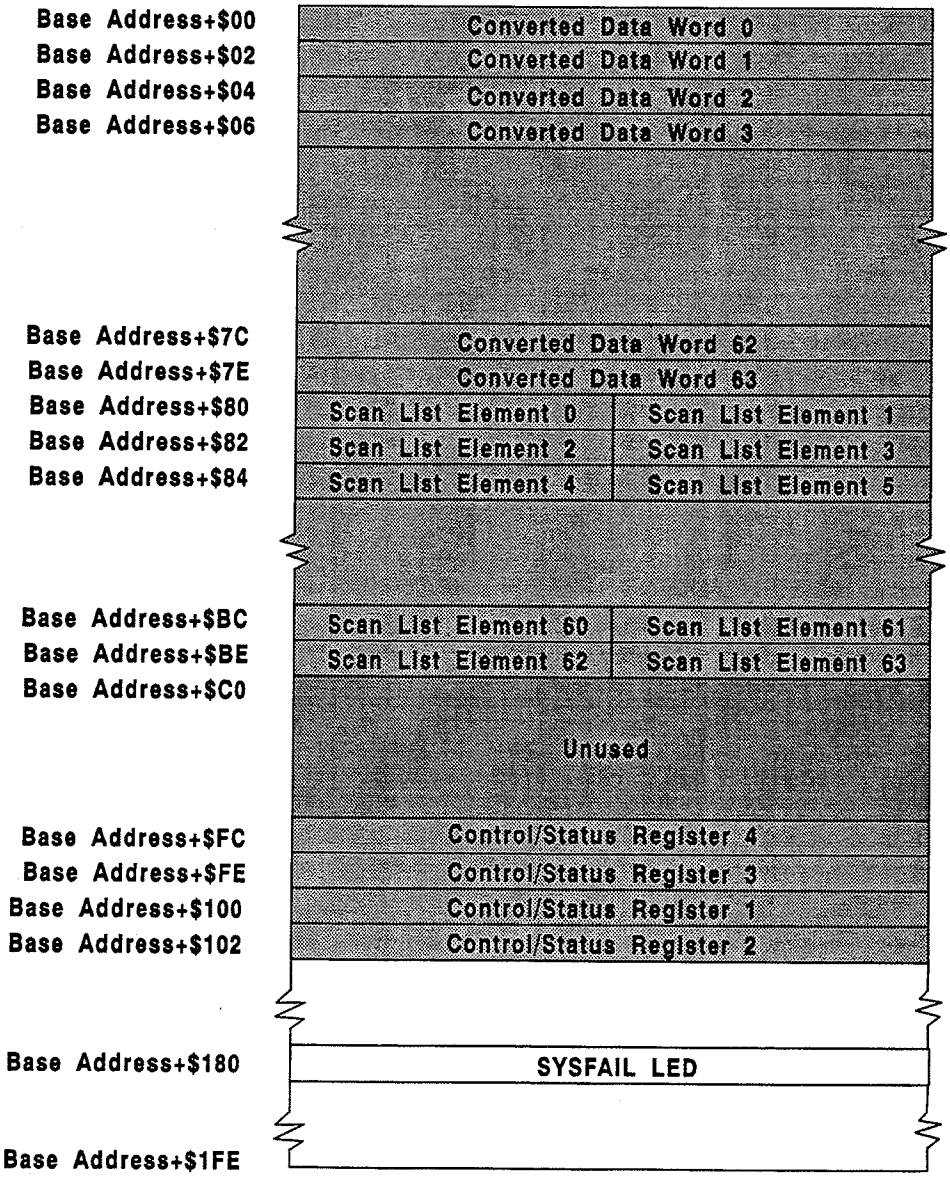
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Four Control/Status Registers are used to configure the software programmable options of the AIP-1. These software programmable options include the trigger signal source, the data acquisition mode of the AIP-1 (continuous or transient) and the operating mode of the AIP-1 (polling or interrupt). Using a combination of the control registers and link E32, the AIP-1 can be configured to generate an interrupt on any of seven interrupt levels whenever any of four events occurs :

- Each time converted data is stored
- When the AIP-1 converted data memory is half-full or full
- When the AIP-1 converted data memory is full only
- When a programable stop bit in the SCAN list is encountered

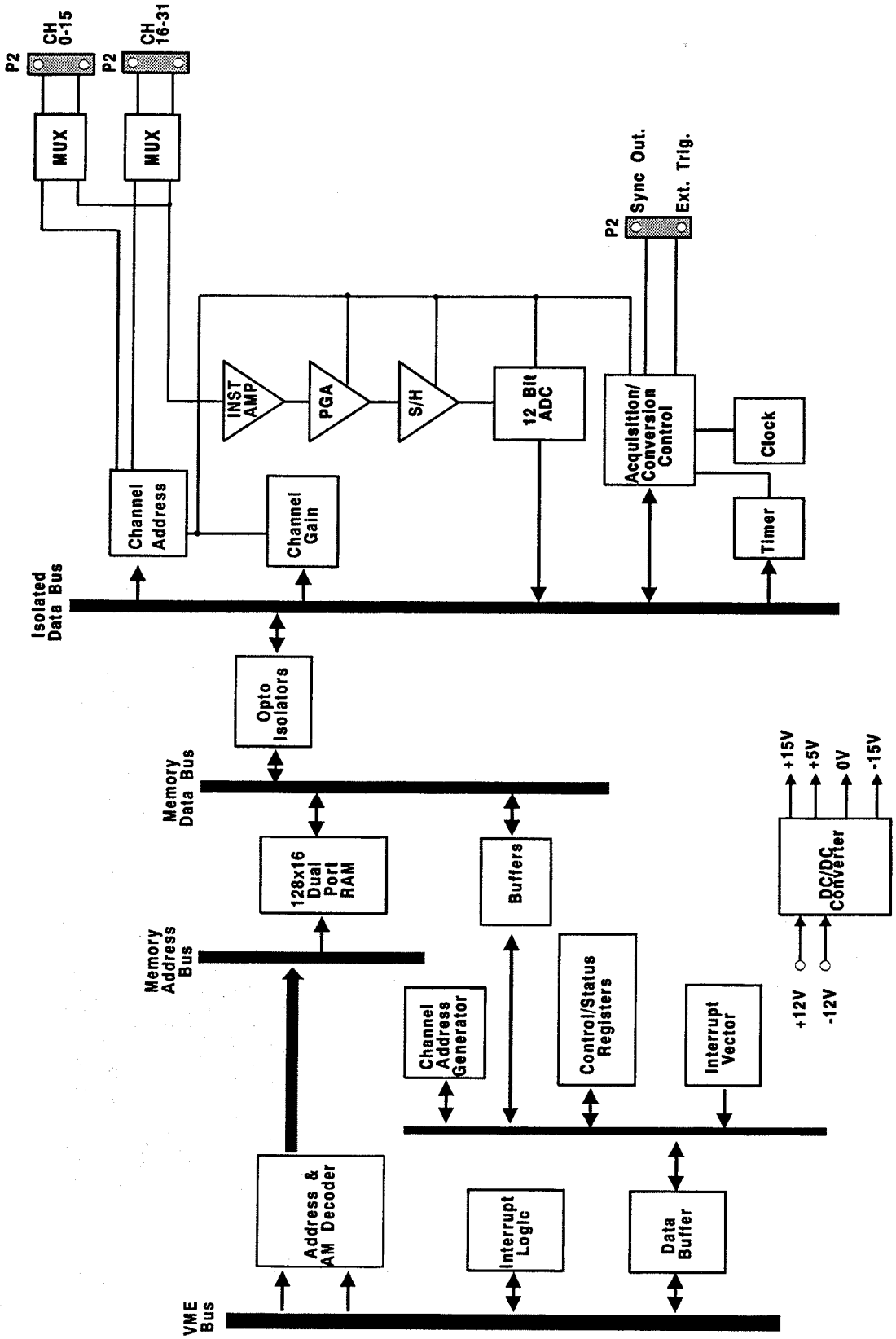
Alternatively, by checking or polling the status registers of the AIP-1, the CPU can determine the state of the board independently and can be programmed to react to specific conditions.

Figure 3 - AIP-1 General Memory Map



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Figure 4 - AIP-1 Block Diagram



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Conventions

This manual adopts the following conventions:

Throughout this manual, bits are numbered from 0 to n, where 0 is the least significant bit and n the most significant.

Signal names follow the ANSI/IEEE Std. 1014 - 1987. Signal names ending in * are active low, all others are active high. GND and V_{CC} mean zero volt and five volt supply rails. Also "longword", "word" and "byte" mean a thirty-two bit word, a sixteen bit word and an eight bit word respectively.

The $ prefix indicates hexadecimal values.

Related Documents

VMEBus Specification ANSI/IEEE Std 1014-1987

IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards IEEE Std 1101.2-1992

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Chapter 2 - Specifications

Common Specifications

This section details the specifications common to all versions of the PMV 68 AIP-1.

VME Interface

Board Type	Slave
Addressing Modes	Standard A24 Short A16
Data Transfers	Word D16 Byte D08 (odd or even)
Data Transfer Rate	3.6Mbytes/s
DSA low to DTACK low	250ns
DSA high to DTACK high	150ns
Signal Drive Current	as defined by VMEbus Specification (Rev.C)
Signal Loads	as defined by VMEbus Specification (Rev.C)

Input Characteristics

Number of Channels	32 single-ended / 16 differential
ADC Gain Ranges (jumper selectable)	0 to 10V, ±5V, ±10V
Amplifier Gain Ranges:	
Jumper Programmable	1, 10, 100
Software Programmable	1, 10, 100
Maximum Input Voltage without damage	±25V (power OFF), ±35V (power ON)
Input Impedance	10MΩ (channel ON), >10MΩ (channel OFF)
Bias Current	300nA
Field to Bus Isolation	250V dc

Transfer Characteristics

Resolution	12 bits
Throughput	50kHz maximum (20µs period) programmable gain of 1 33kHz maximum (30µs period) all other gains

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Accuracy

		Typical
System Errors at +25°C - Jumper Programmable Mode	Gain=1 : ±0.05% FSR	(<± 0.01% FSR)
System Errors at +25°C - Software Programmable Mode	Gain=1 : ±0.05% FSR	(<± 0.01% FSR)
	Gain=10 : ±0.2% FSR	(<± 0.01% FSR)
	Gain =100:	(< ± 0.1% FSR)
A/D Converter Linearity	±1/2 LSB	
Differential Linearity	±1/2 LSB	
Gain Error	adjustable to zero	
Offset Error	adjustable to zero	
Monotonic	0°C to 70°C	E-style
	-40°C to 85°C	RI & R-styles
	-55°C to 85°C	MI & MA-styles

Accuracy Over Temperature

		Typical
System Accuracy Drift	510ppm/°C	(7ppm/°C for 0Volt inputs)

Note: Boards operating over the full rugged or military temperature range will have some change in zero offset at the temperature extremes. If an unused input were to be linked to the users 0 Volts this would provide an opportunity to allow software compensation for variations in zero offset over the operating temperature range.

Dynamic Accuracy

Sample/Hold Aperture Delay	25ns
Sample/Hold Aperture Jitter	±300ps
Feedthrough (10V pk-pk @ 100kHz)	0.01%
CMRR G=1	100dB
Channel Crosstalk	-75dB at 1kHz for OFF channel to ON channel

Electrical

Two 96-way DIN41612 compatible connectors that mate with rack mounted backplane connectors form the electrical connection to the board.

Current Consumption

Typical +5V ± 5% @ 1.2 A
± 12V ± 5% @ 300mA per rail

Voltage Supply Requirements

+5V ±0.25V DC total excursion, including all transients.
V ripple (5V) = 50mV RMS (max) contained within the total excursion.
± 12V ±1Volt per rail

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Safety Requirements

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.

Mechanical

Weight

The approximate weights of the different styles of the PMV 68 AIP-1 are as follows:

MI/RI style	=	700g (25oz)
MA/R style	=	620g (22oz)
E style	=	500g (18oz)

Dimensions

All five build standards of the AIP-1 board are compatible with ANSI/IEEE Std 1014-1987 VMEbus Double Eurocard Standard. This allows all styles of assembly to be fitted in any commercial VMEbus development chassis.

Figures 5 and 6 show basic VME board dimensions. The dimensions are in millimetres, with inches (in parentheses) for general guidance only.

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Figure 5 - VME Dimensions for MA, R and E Styles

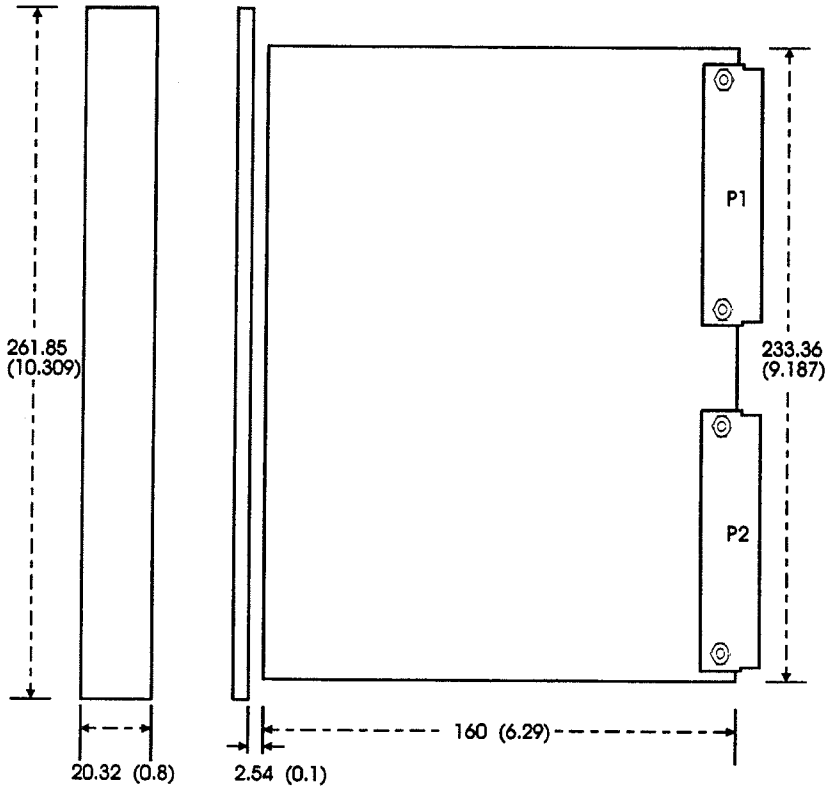
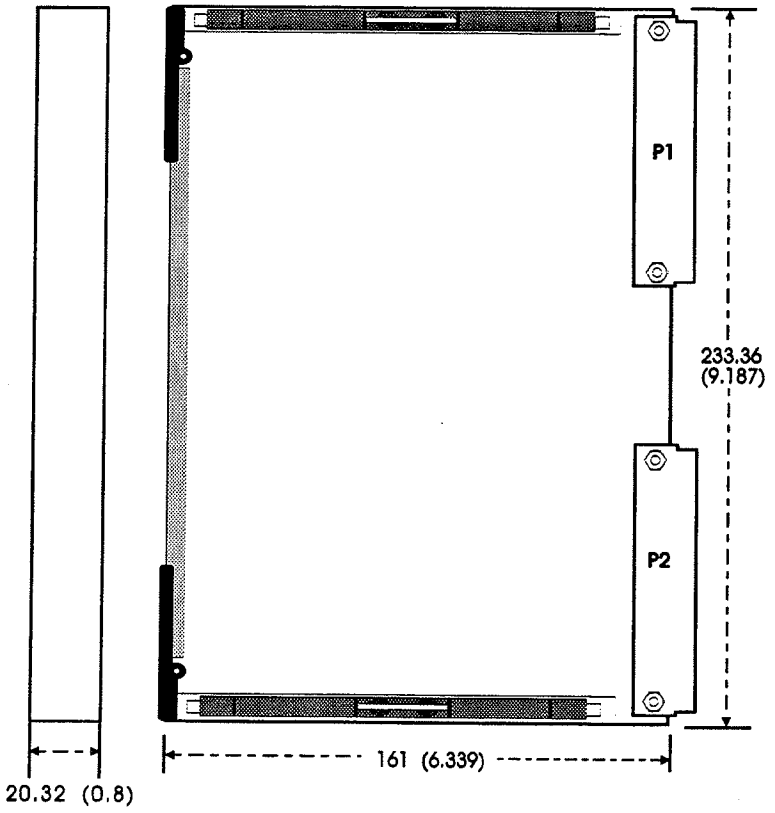


Figure 6 - VME Dimensions for MI and RI Styles



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PMV 68MI Specification

Mechanical

Each MI-style assembly has a Heat Management Layer (HML) bonded to a multilayer printed wiring board. ICs are mounted astride rungs of the HML which conducts heat to the edges of the assembly. The unit may be secured in a rack by two screw driven wedgelocks. These clamp the HML to the rack 'cold wall' at the thermal interface on the two short edges of the assembly.

Environmental

In common with other PMV 68MI modules the PMV 68MI AIP-1 can withstand the following conditions:

MIL-STD-810E Test	Method	Procedure	Comments
Low pressure (altitude)	500.3	I, II & III	Storage and operational tests to 50,000 ft. Also rapid decompression to maximum altitude.
High temperature	501.3	I & II	Maximum storage 105°C #Maximum operating 85°C
Low temperature	502.3	I & II	Minimum storage -62°C #Minimum operating -55°C
Temperature shock	503.3	I	Rapid change over range of operational and storage temperatures
Humidity	507.3	III	Up to 95%RH with varying temperature, 10 cycles 240 hours minimum
Salt fog	509.3	I	Continuous exposure to mist with 5% salt solution for 48 hours
Acceleration	513.4	I & II	Structural and operational tests. Acceleration levels up to 13.5g
Vibration	514.4	I	Category 5 equipment. Vibration spectrum Fig 514.4-8. 15 to 2,000 Hz to 0.1g ^{2}/Hz (RMS level = 12g approx.)
Shock	516.4	I	Test pulse giving the spectrum of Fig. 516.4-1 approximating to a perfect sawtooth of Fig. 516.4-4 at the level of 40g 11ms.
		VI	Bench handling

Measured at the thermal interface to the module

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Reliability

Using MIL-HBK-217F notice 1 as a data base and the parts count method, the following estimates have been made of the Mean Time Between Failure (MTBF) for the MI-style AIP-1.

Environment	Ground Mobile	Naval Sheltered	Airborne Inhabited Cargo
Temperature	45°C	40°C	55°C
Failure Rate (Failures/million hours)	12.420	10.118	12.315
MTBF (Hours)	80,511	98,825	81,196

Environmental Stress Screening

The MI-style AIP-1 is subjected to a Reliability Burn-in according to Radstone specification VV68102899 ESS Requirements for PMV 68 Military CCAs.

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PMV 68MA Specification

MA-style boards are built to the same design and using the same military qualified components as MI-style boards, but lack the HML required for conduction cooling. Forced air convection cools the boards.

The PMV 68MA AIP-1 can withstand the following conditions (highlights show differences from the MI-style):

Environment	Specification	Method	Procedure	Comments
Low pressure (altitude)	MIL-STD-810E	500.3	I, II & III	Storage and operational tests to 50,000 ft. Also rapid decompression to maximum altitude
High temperature	MIL-STD-810E	501.3	I & II	Maximum storage 105°C **Maximum operating 85°C with air flow of 600 ft/min Maximum operating 70°C with air flow of 300 ft/min**
Low temperature	MIL-STD-810E	502.3	I & II	Minimum storage -62°C Minimum operating -55°C
Temperature shock	MIL-STD-810E	503.3	I	Rapid change over range of operational and storage temperatures
Humidity	MIL-STD-810E	507.3	III	Up to 95%RH with varying temperature, 10 cycles 240 hours minimum
Salt fog	MIL-STD-810E	509.3	I	Continuous exposure to mist with 5% salt solution for 48 hours
Vibration	**MIL-STD-810E**	**514.4**	**I**	**Fig 514.4-17 swept sine 5g 5-500Hz**
	MIL-STD-202F	**201A**	**I**	**Constant amplitude swept sine 0.06 inch double amplitude 10-55Hz**
Shock	**MIL-STD-202F**	**213**	**J**	**30g 11msec half sine**
	MIL-STD-810E	516.4	VI	Bench handling

Acceleration figures are not applicable for MA-style AIP-1.

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Reliability

Using MIL-HBK-217F notice 1 as a data base and the parts stress method, the following estimates have been made of the MTBF for the MA-style AIP-1.

Environment	Ground Mobile	Naval Sheltered	Airborne Inhabited Cargo
Temperature	45°C	40°C	55°C
Failure Rate (Failures/million hours)	TBA	TBA	TBA
MTBF (Hours)	TBA	TBA	TBA

Environmental Stress Screening

The MA-style AIP-1 is subjected to a Reliability Burn-in according to Radstone specification VV68102899 ESS Requirements for PMV 68 Military CCAs.

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PMV 68RI Specifications

RI-style boards can survive the same environment as the MI-style boards with the following operating and storage temperatures:

Maximum storage temperature	100°C
Maximum operating temperature	65°C
Minimum storage temperature	-50°C
Minimum operating temperature	-40°C

Reliability

Using MIL-HBK-217F notice 1 as a data base and the parts count method, the following estimates have been made of the MTBF for the RI-style AIP-1.

Environment	Ground Mobile	Naval Sheltered	Airborne Inhabited Cargo
Temperature	45°C	40°C	55°C
Failure Rate (Failures/million hours)	68.606	37.867	43.710
MTBF (Hours)	14,576	26,408	22,878

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PMV 68R Specification

R-style boards have the same mechanical build standard as MA-style boards. They can withstand the same environment when conformally coated (an option that must be specified separately), apart from the storage and operational temperatures. Wide temperature range, ceramic packaged, industrial components replace full military qualified components.

The differences from the MA specification are as follows:

High temperature

Maximum storage temperature	100°C.
Maximum operating temperature	85°C with an airflow of 600 ft/min.
	70°C with an airflow of 300 ft/min.

Low temperature

Minimum storage temperature	-50°C
Minimum operating temperature	-40°C

Reliability

Using MIL-HBK-217F notice 1 as a data base and the parts count method, the following estimates have been made of the MTBF for the R-style AIP-1.

Environment	Ground Fixed	Naval Sheltered
Temperature	40°C	40°C
Failure Rate (Failures/million hours)	19.574	37.867
MTBF (Hours)	51,088	26,408

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PMV 68E Specification

The E-style boards use commercial grade, plastic packaged components.
The PMV 68E AIP-1 can withstand the following conditions:

Altitude

-1000 to +50,000 feet (-300 to +15,000 Meters approximately)

High temperature

Maximum storage temperature	100°C.
Maximum operating temperature	70°C with an airflow of 600ft/min.
	55°C with an airflow of 300ft/min.

Low temperature

Minimum storage temperature	-50°C
Minimum operating temperature	0°C

Temperature shock

±10°C/minute

Humidity

95% non-condensing

Vibration

Swept sine 5g 5 to 500 Hz

Mechanical shock

30g for 11 milliseconds (half-sine)

Reliability

Using MIL-HBK-217F notice 1 as a data base and the parts count method, the following estimates have been made of the MTBF for the E-style AIP-1.

Environment	Ground Benign	Naval Sheltered
Temperature	30°C	40°C
Failure Rate (Failures/million hours)	9.164	51.321
MTBF (Hours)	109,117	19,485

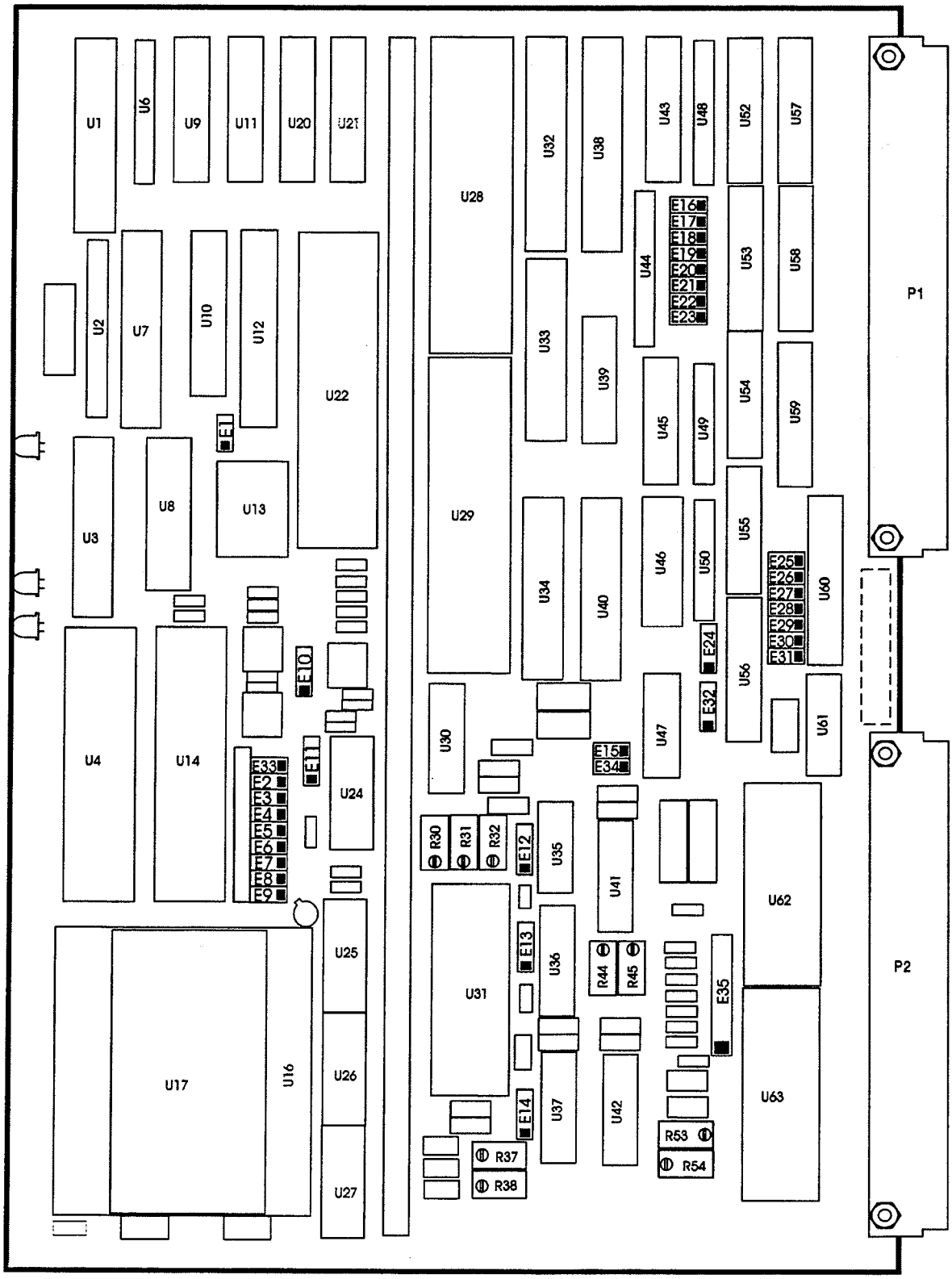
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Chapter 3 - Hardware Configuration

Figure 7. Jumper Location



■ Indicates pin 1

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Introduction

The AIP-1 Analog Input Board has a number of user-definable options which are selected using a series of jumpers. Boards are shipped from the factory with default options configured as indicated in the table below.

E16 to E19, E21, E22, E25 to E31	Memory Map Base Address Selection	Standard Addressing - $C00000
E24 pin 1-2	Address Modifier Code Response	Standard Addressing, no response to AM Codes
E11 pin 2-3	Sign Extension/Oversampling Response	Sign Extension
E2, E3, E4, E6, E8, E9	Base Trigger Period Selection	5µs (frequency 200kHz)
E35, pin 2-3, 4-5, 6-7	Single-ended/Differential Input Selection	Single-ended
No jumper	Hardware Configurable Input Gain Selection	x1
E12 pin 1-2 E13 pin 1-2	Input Range Selection	±10V
E 10 pin 2-3	Digital Output Code Selection	Offset Binary
E32 pin 2-3	ProgrammableHalf/Stop flag	Respond to Half/Stop Flag

Preparing the Board

The AIP-1 is sensitive to the build up of static electricity and normal anti-static precautions should be observed when unpacking or handling the board.

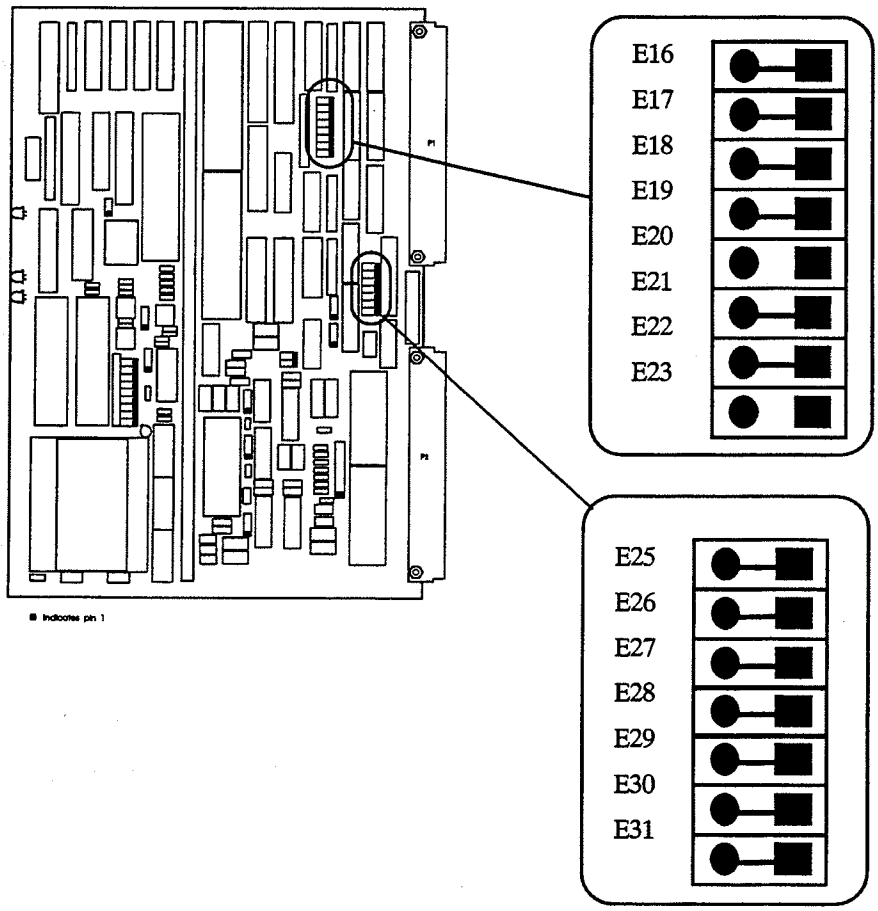
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Changing the Base Address

Jumpers E16 to E23 — upper byte, E25 to E31 — middle byte

The AIP-1 occupies 256 consecutive word locations within the system. It may be located on any 256 word boundary within the short or standard address space of the VMEbus, provided it does not conflict with the location of any other device already installed in the system. The location of the AIP-1 is altered by setting its base address using jumpers indicated in Figure 8.

Figure 8 - Base Address Default Setting



The AIP-1 is shipped from the factory with a base address of $C00000. There are 15 individual jumpers corresponding to address lines A09 to A23. Address lines A00 to A08 are set within the hardware of the AIP-1, hence the location of memory map is automatically restricted to a 256 word boundary.

Note: The base address selected for the AIP-1 will be required when programming the board.

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Table 1 summarises how the configuration of jumpers is used to alter the base address of the AIP-1. Removing a jumper sets the corresponding address bit to one (1). Inserting a jumper sets the corresponding address bit to zero (0).

Table 1 - Summary of Base Address Options

E23 A23	E20 A22	E18 A21	E16 A20	E17 A19	E19 A18	E21 A17	E22 A16	E29 A15	E28 A14	E26 A13	E27 A12	E30 A11	E31 A10	E25 A09	Base Address
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	$FFFE00
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	$FFFC00
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	$FFFA00
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	$FFF800
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	OUT	$FFF600
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	IN	$FFF400
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	OUT	$FFF200
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	IN	$FFF000
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	OUT	OUT	$FFEE00
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	OUT	OUT	IN	$FFEC00

and so on, until.....

IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	IN	IN	OUT	$001200
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	IN	IN	IN	$001000
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	OUT	$000E00
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	IN	$000C00
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	IN	OUT	$000A00
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	IN	IN	$000800
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	OUT	$000600
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	IN	$000400
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	OUT	$000200
IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	IN	$000000

Default Base Address = $C00000

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Example : To select a Base Address of $FF0200

Binary equivalent of $FF0200 = 1111 1111 0000 0010 0000 0000

Address lines A08-A00 are fixed, therefore we are only concerned with A23-A09 = 1111 1111 0000 001

OUT=1 and IN=0, therefore the required configuration =

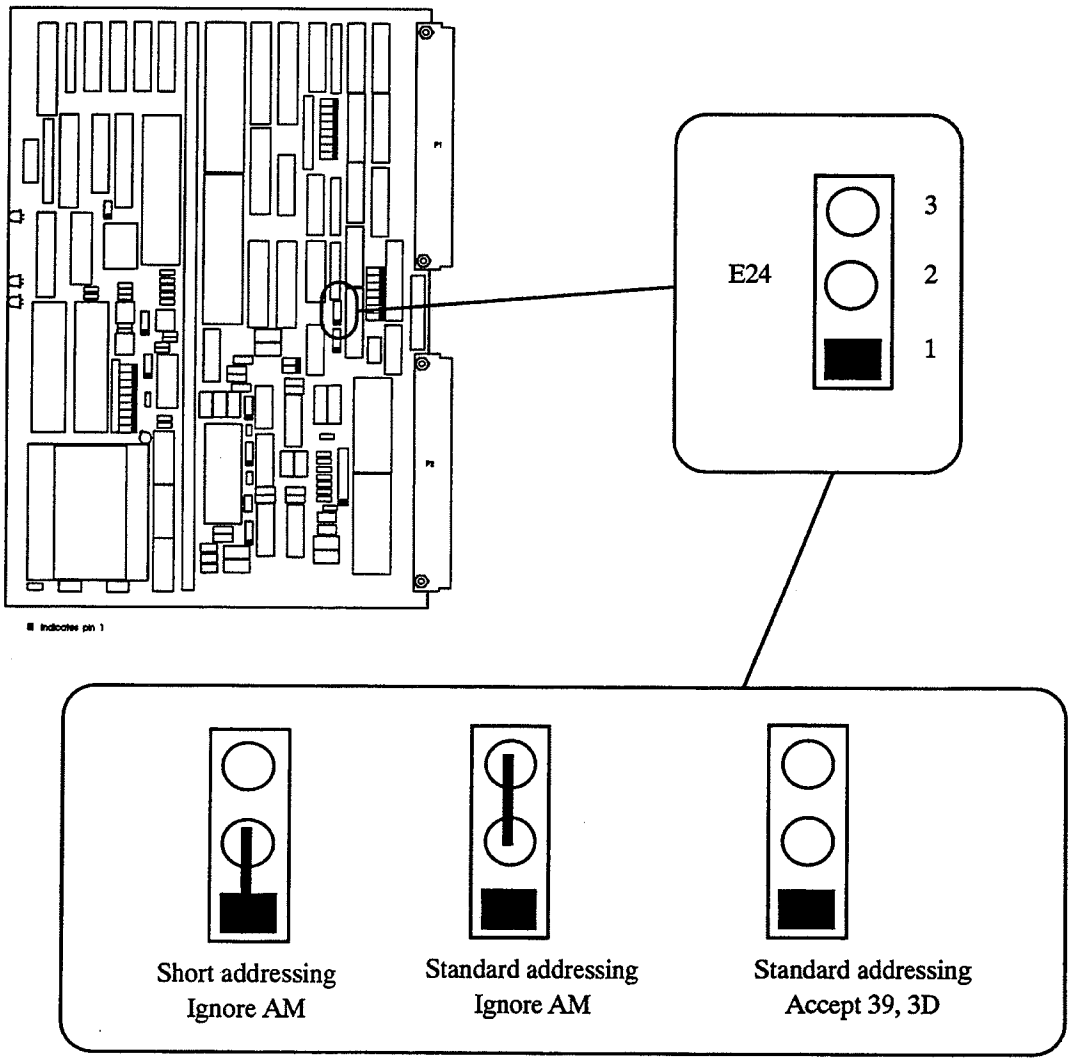
E23	E20	E18	E16	E17	E19	E21	E22	E29	E28	E26	E27	E30	E31	E25	Address
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	IN	IN	IN	IN	IN	IN	OUT	FF0200H

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Changing the Address/Address Modifier Code Response (E24)

Jumper E24 is used to define the way in which the AIP-1 will respond to addresses placed on the address bus. The AIP-1 may be located in either the short or standard address space of the VMEbus and accessed with or without the use of address modifiers.

Figure 9. Address Modifier Response Position



Short Address Decoding (ignore Address Modifiers)

With pins 1 and 2 linked the AIP-1 will only respond to 16bit (short) addresses and will not be affected by address modifier codes. Ensure that the base address of the AIP-1 locates the board in the short address space when configured in this way.

Standard Address Decoding (ignore Address Modifiers)

With pins 2 and 3 linked the AIP-1 will respond to either 16bit (short) addresses and 24bit (standard) addresses, but will not be affected by address modifier codes.

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Default Address Modifier Response

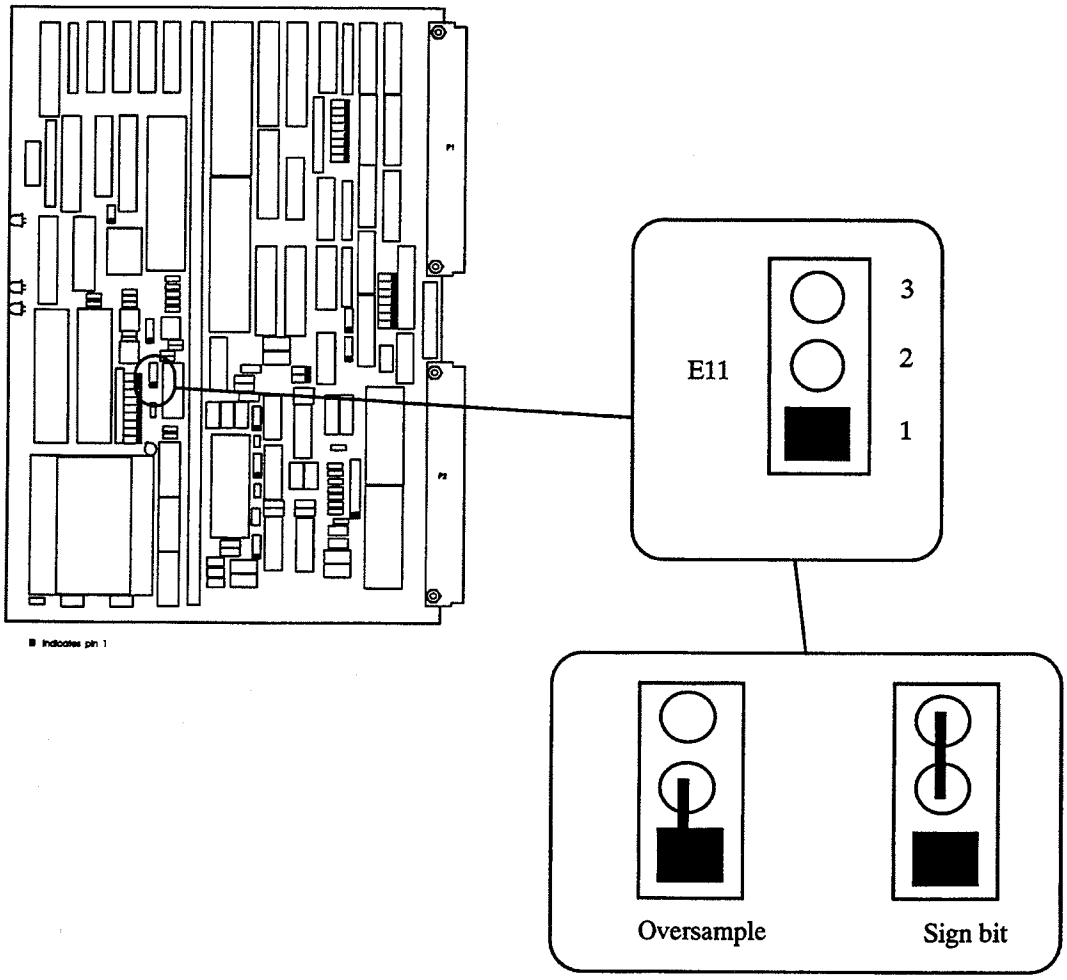
With both jumpers removed, the AIP-1 will respond to 24bit (standard) addresses with an address modifier code of either 39 (standard non-privileged data access) or 3D (standard supervisory data access).

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Selecting Sign Extension/Oversampling (E11)

Analog signals applied to the AIP-1 are converted into 12bit digital codes, representing the magnitude of the signal, by a 12bit analog-to-digital converter. However, the digital codes are stored in 16bit memory locations, which means that the 4 most significant bits are available to either sign extend the data, or to be used to indicate when an oversampling condition occurs. E11 is used to select between these two options.

Figure 10 - Sign extension / Oversampling



When the sign-extension option is selected, the sign bit of the 12bit digital code (ie. bit 12) is repeated in the 4 most significant bits of the 16bit word so that the 12bit codes can be used in integer arithmetic without requiring any further manipulation.

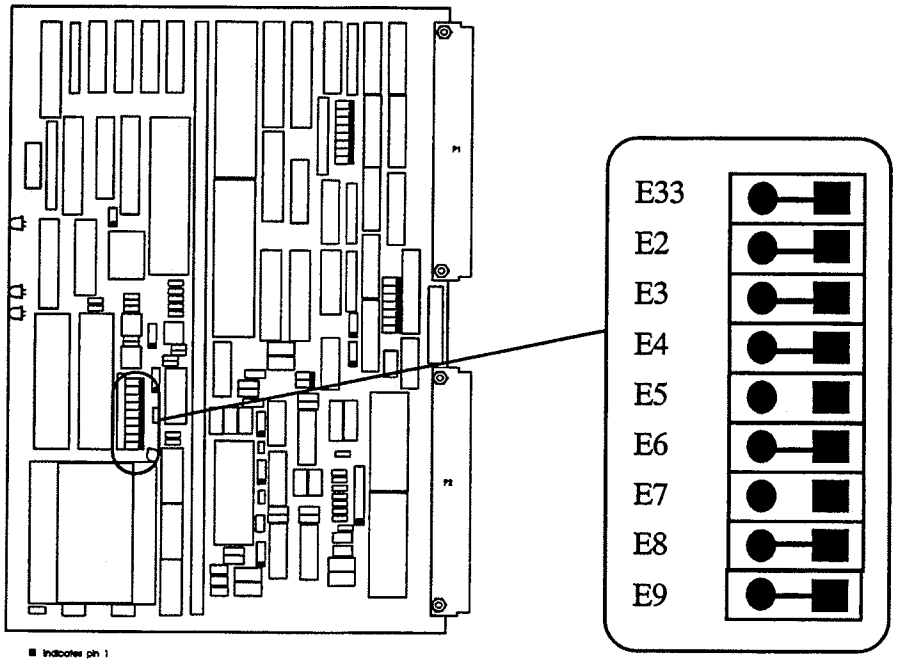
When the oversampling option is selected, the four most significant bits of each byte of data are normally set to 1111. If an oversampling condition occurs, these bits are reset to 0000. A program may be written which detects this change and alerts the CPU to the error. (Oversampling occurs when the trigger signal, which determines the frequency with which the AIP-1 samples the analog inputs, has a frequency higher than the maximum sample frequency of the board - approximately 60kHz. Oversample selection is only allowed for external triggering)

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Changing the Base Sample Period (E2 to E9)

The rate at which the AIP-1 samples its analog inputs is determined by a trigger signal which synchronises the internal operation of the board. This trigger signal may be generated by one of four sources (see 'Control/Status Register 3 - Trigger Source Selection' in Chapter 5), one of which is an internal timer arrangement.

Figure 11. Default Base Sample Period Link configuration

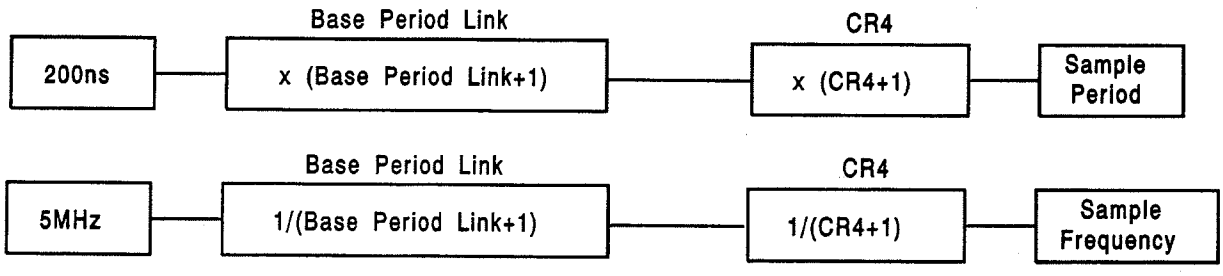


When the internal trigger is selected its period is derived as a multiple of two components:

1. Base Sample Period (set using jumpers E2 to E9)
2. Sample Period Multiplier (software selected using Control Register 4)

E2 to E9 function as a frequency pre-scaler, dividing the master frequency generated by an on-board quartz crystal to generate a signal with a period in the range 400ns and 51.2µs, in 200ns intervals.

Figure 12 - Deriving the Sample Period



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The combination of base trigger frequency and trigger frequency multiplier is used to provide extremely sensitive control over the sample rate of the AIP-1, however, this arrangement does not prevent the user from selecting a trigger frequency greater than the maximum sample rate of the board (50kHz).

Base period	Control Reg 4	Trigger period	Trigger frequency	
$00, $01, $02	Illegal state	Illegal state	Illegal state	Illegal state
$18	$05	30µs	33kHz	
$FF	$FF	13.1ms	76.3Hz	Maximum setting

To determine the configuration of base period links for a given sample period:

- Select a base sample period (Tb) and sample period multiplier (Tm) which multiplied together give the required trigger period.
- Determine Tm and reprogram as shown in 'Control/Status Register 4' (Chapter-5)
- link decode (decimal)=$(Tb/200x10^{-9})-1$

where link decode (decimal) is the decimal equivalent of the hex code which defines the configuration of base period.

Example: To select an internal sample period of 100µsec

choose base sample period (Tb) of **10µsec** and sample period multiplier (Tm) of 10

link decode (dec) + 1 = $(Tb/200 \times 10^{-9}) = (10 \times 10^{-6})/(200 \times 10^{-9}) = 50$

link decode (dec) = 50 - 1 = 49

link decode (hex) = $31 = 00110001

E8	E6	E9	E7	E5	E4	E2	E3
0	0	1	1	0	0	0	1

Tm entered into CR4 = $OA - 1 = 0001001

Alternative Decode calculation

An alternative method for calculating the Base sample Link Decode is given below:

step 1 — determine the decimal value of the required base sample period
step 2 — deduct 200ns from this required value
step 3 — using the following binary table make up the value.
Note: the values shown exist when the link is not made

E8 =	25.6µs	(msb)
E6 =	12.8µs	(bit6)
E9 =	6.4µs	(bit5)
E7 =	3.2µs	(bit4)
E5 =	1.6µs	(bit3)
E4 =	0.8µs	(bit2)
E2 =	0.4µs	(bit1)
E3 =	0.2µs	(bit0)

Example:

A prescaler period of 10µsec is required subtract 200ns, this leaves a period required of 9.8µs

Fit all links except E9, E7, E3

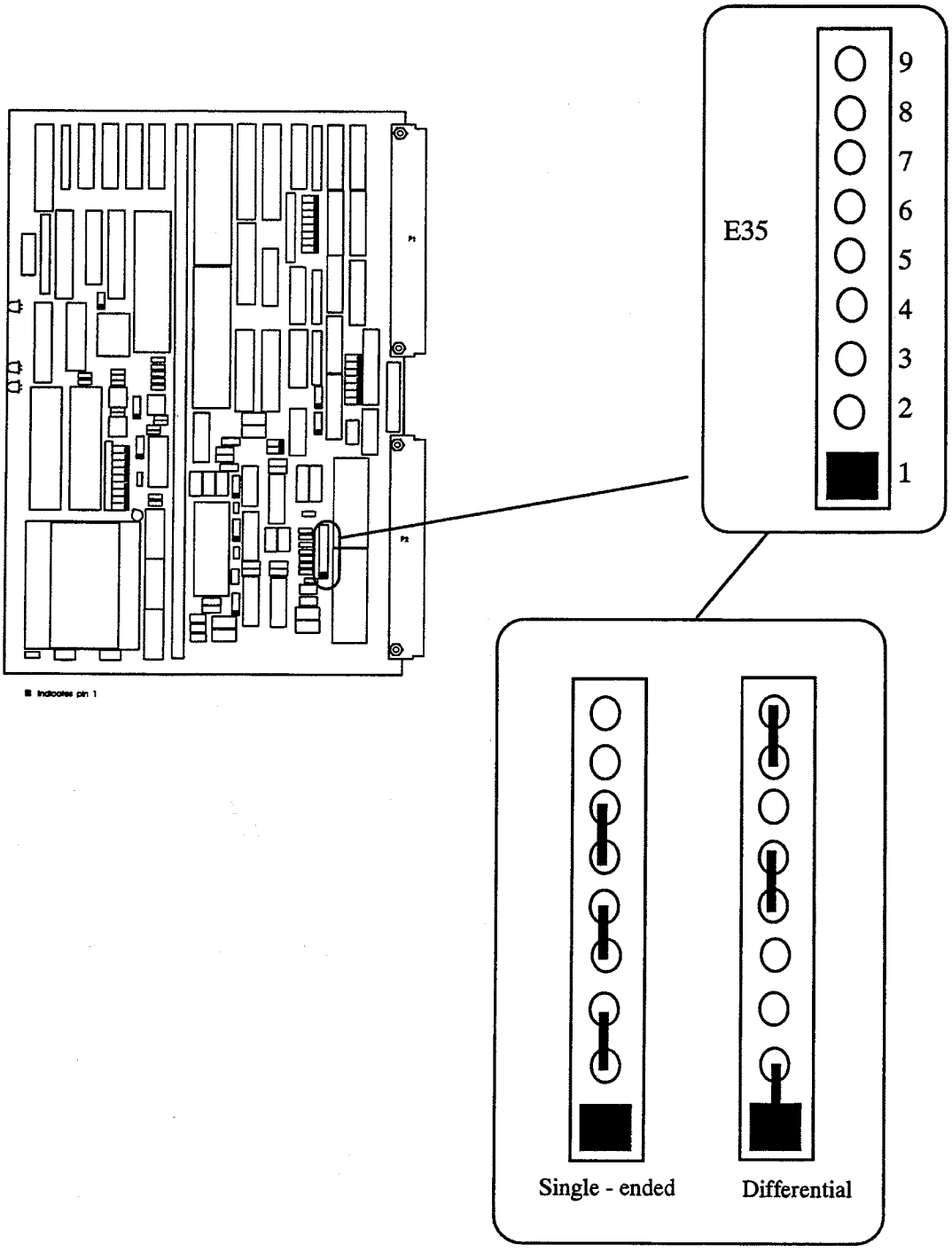
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Single-Ended or Differential Configuration (E35)

The AIP-1 can be configured to accept either 32 single-ended analog inputs, or 16 differential analog inputs, using link E35.

Although single-ended configuration provides a much larger number of inputs, this configuration suffers from the possibility of errors caused by ground currents flowing between the signal source and the input amplifier. These errors may become significant when detecting low input signals.

Figure 13 - Single-ended / Differential Inputs (link E35)

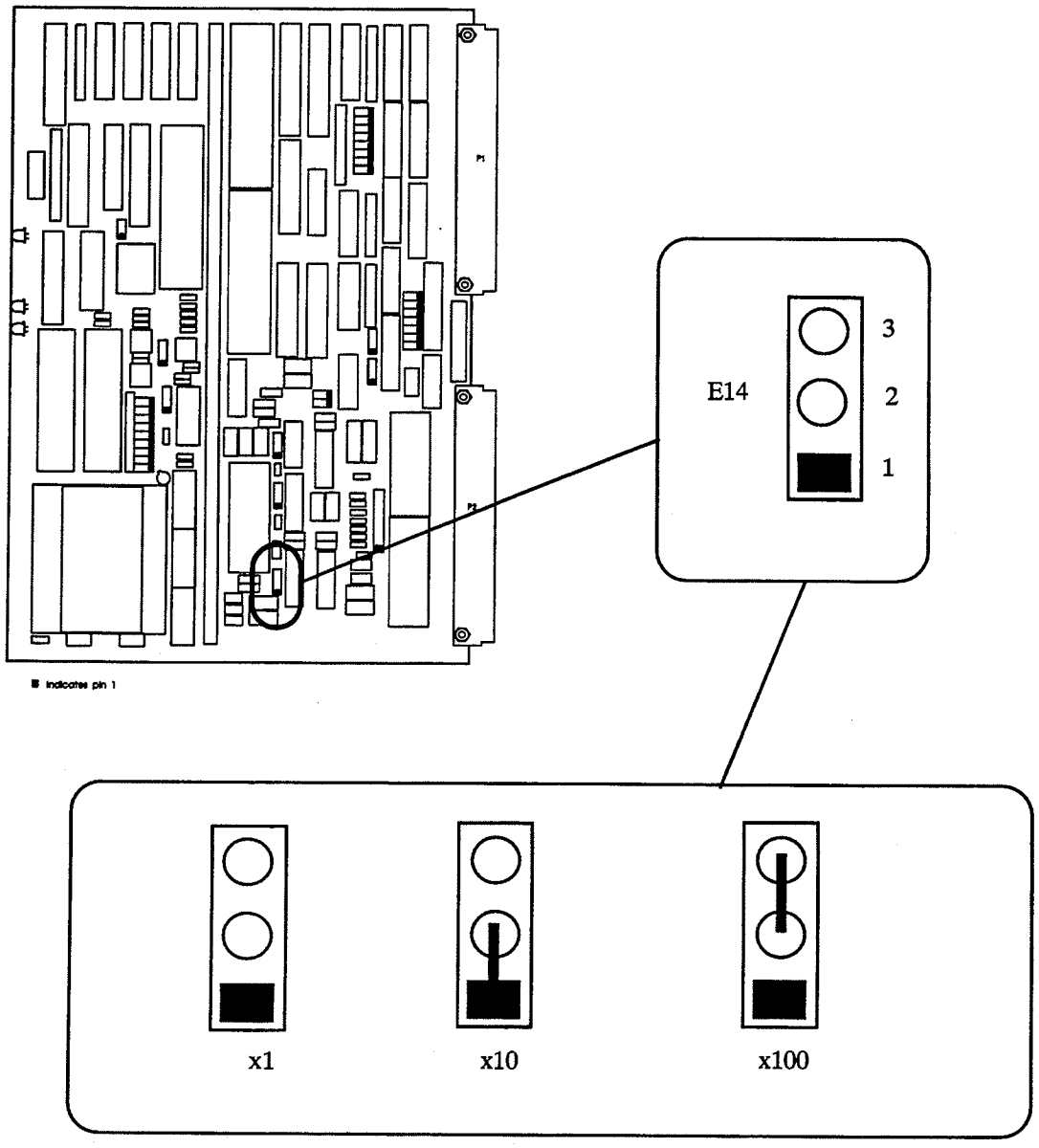


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Changing the Input Amplifier Gain (E14)

An instrumentation amplifier is used to set the input gain of all channels. It provides a fixed gain in the range 1 to 100. Input gains of x1, x10 and x100 are set using E14 as shown in Figure 14. The AIP-1 is shipped from the factory with E14 set to select an input gain of x1.

Figure 14. Input Gain selection (E14)



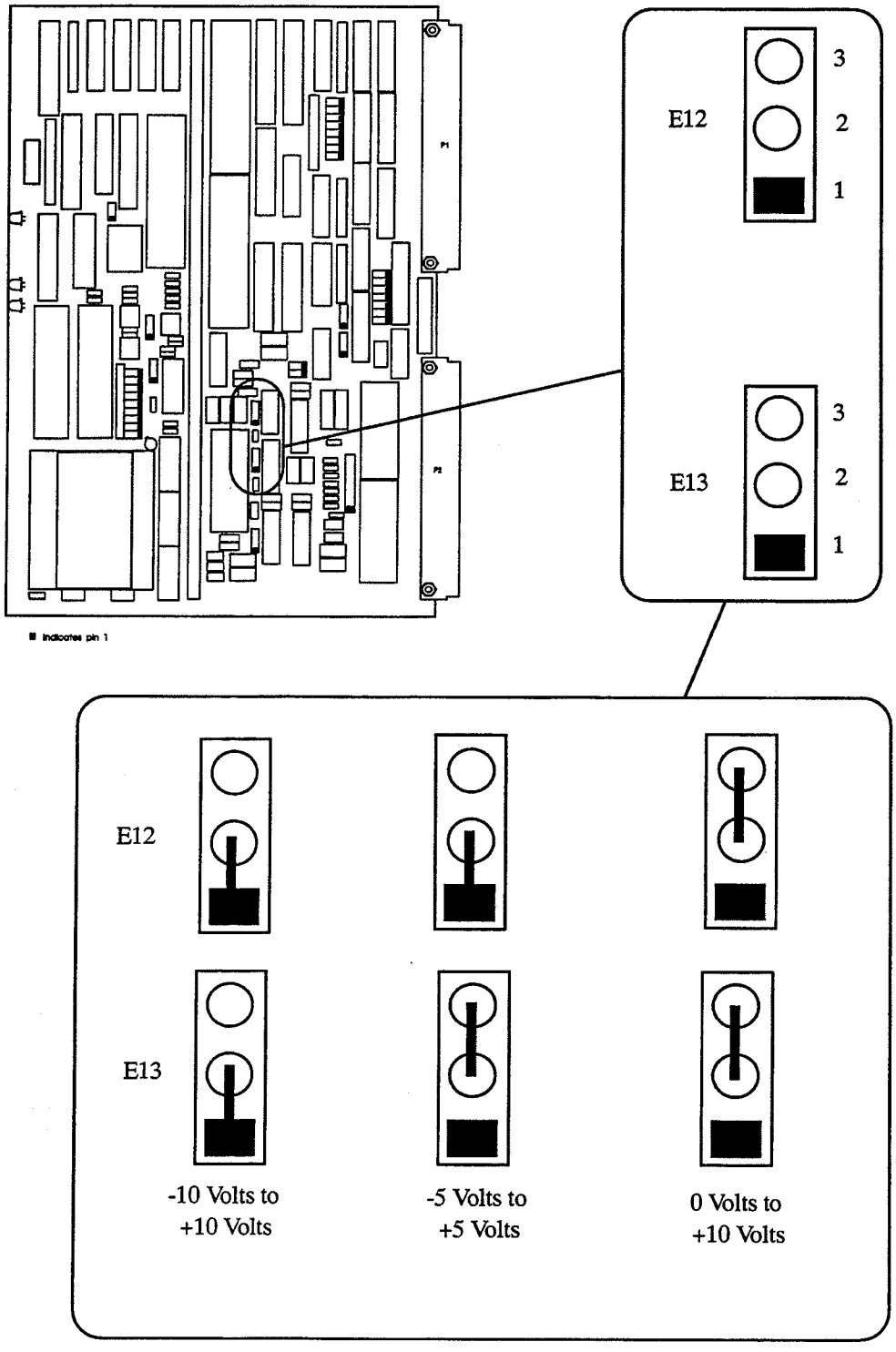
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Changing the Analog Input Range (E12 & E13)

There are three analog input ranges available on the AIP-1 : 0 to 10V, ±5V and ±10V.

The AIP-1 is shipped with its analog inputs configured for operation in the ±10V range. This may be changed using the jumpers and the corresponding input ranges shown in Figure 15.

Figure 15. Input Range Selection



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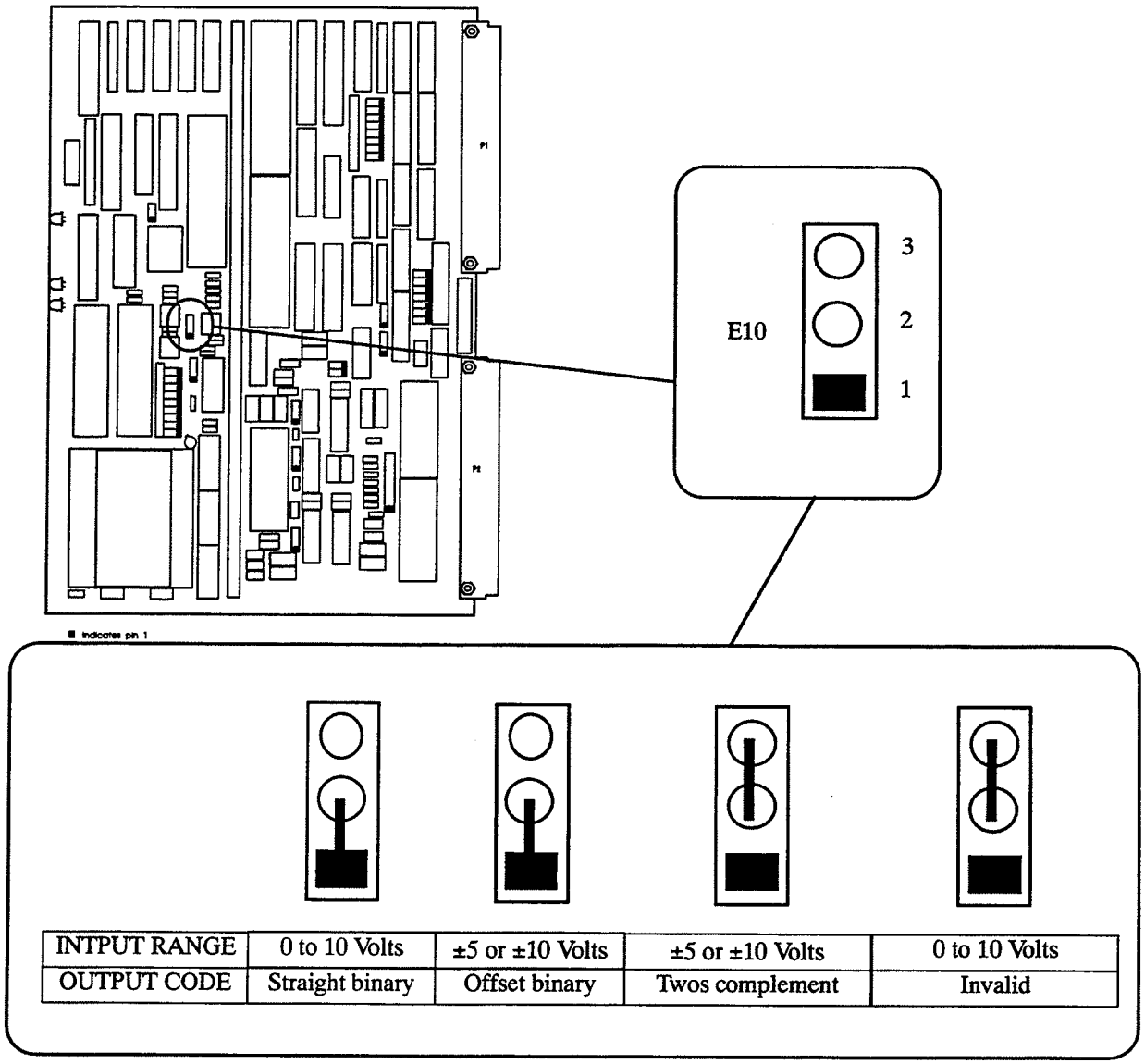
Selecting the Digital Code Format (E10)

Analog signals applied to the AIP-1 are converted into 12 bit digital codes representing the signal magnitude. The format of these codes is selected using jumper E10.

There are three possible digital code formats, and the required configuration is dependent in part on the analog input range selected (see 'Converting Analog Voltages to Digital Codes' in Chapter 7)

- Unipolar (0 to 10V) range : straight binary
- Bipolar (5V or 10V) : offset binary or 2's complement

Figure 16. Digital Output Format (E10)



INTPUT RANGE	0 to 10 Volts	±5 or ±10 Volts	±5 or ±10 Volts	0 to 10 Volts
OUTPUT CODE	Straight binary	Offset binary	Twos complement	Invalid

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Straight Binary Format

If a unipolar input range (0 to 10V) has been selected, the straight binary digital code format is required.

Offset Binary Format

Offset Binary format may be selected for either of the bipolar ranges, ±5V or ±10V. This format has the same true magnitude relationship as straight binary, however the offset from zero provides an indication of sign.

2's Complement Format

2's Complement format may be selected for either of the bipolar ranges, ±5V or ±10V.

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Selecting Half Full Flag or Programmable End Stop (E32)

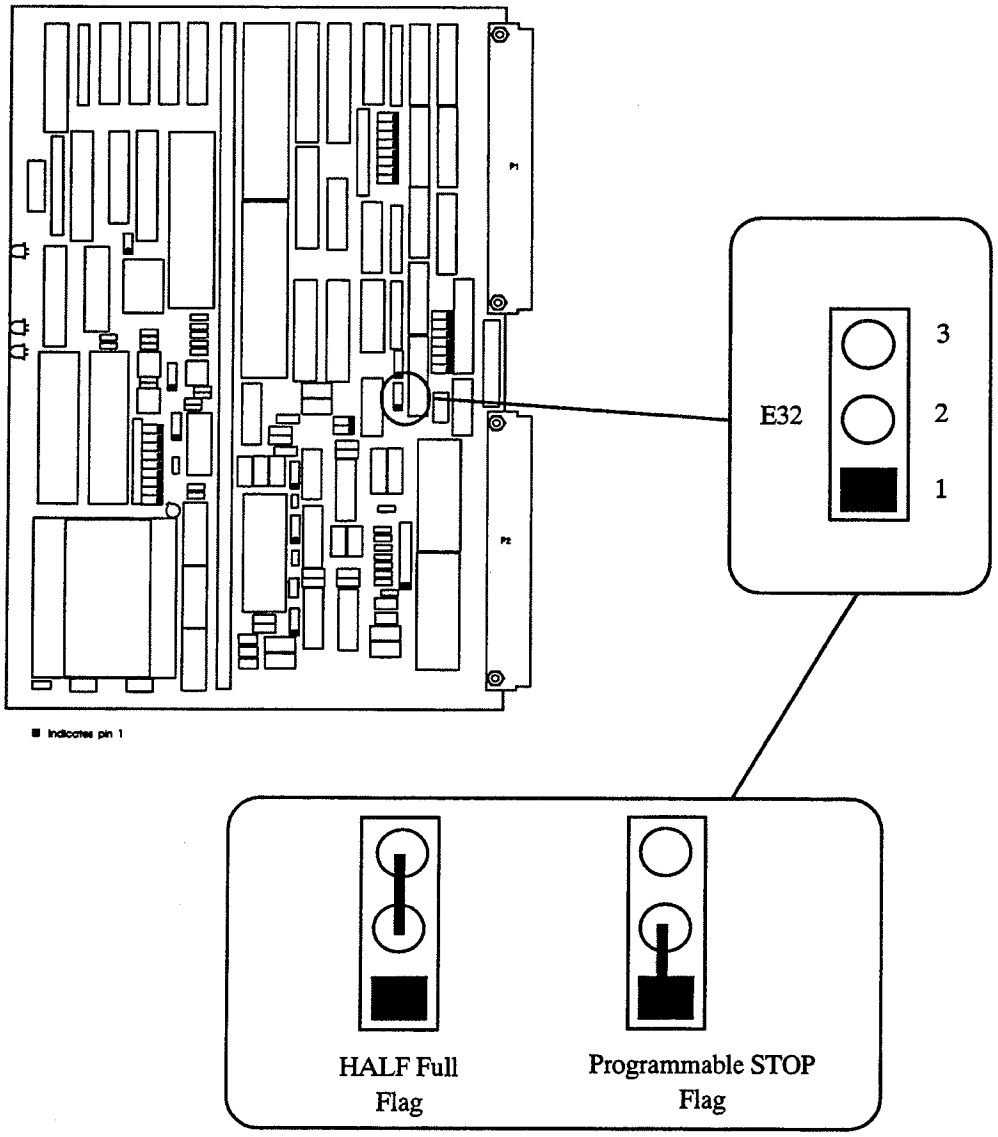
The status of AIP-1 during samples can be determined by reading Control/Status register 2. Three flags have been provided to give instant indication of sample progress. These are:

FULL flag
HALF Full flag
Programmable End STOP flag

The functional description of each flag is detailed in Chapter 5 - Software Configuration.

The Half Full Flag and Programmable End STOP Flag occupy the same bit in Control/Status register 2 (bit D13).

Figure 17. Half full / Programmable End Stop Flags (E32)



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Selecting the Internal Ground Analog Input (E15)

For calibration purposes it is possible to short the input of the Sample and Hold device to the Analog Ground by linking E15 pin1 to pin 2.

Note: Links E33 and E34 are for factory use only.

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Chapter 4 - Cables and Connections

Connecting the AIP-1

Ensure that power to the VMEbus system is turned off before installing the AIP-1. The AIP-1 is sensitive to the build-up of static electricity, therefore normal anti-static precautions should be observed when handling the board.

Communication between the AIP-1 and the VMEbus is performed via the P1 Connector on the rear of the board. To install the AIP-1 in the VMEbus system, carefully align connectors P1 and P2 with the corresponding J1 and J2 connectors on the VMEbus backplane and press firmly home.

The 32 channels of analog input are accessed via the VME backplane P2 connector

The external trigger and SYNC output signals are also on the VME P2 connector.

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Connector Pin Assignments

P1 Pin Assignment

The 96-way P1 connector on the AIP-1 mates with the J1 connector on the VMEbus backplane

Table 2 - Connector P1 Pin Assignment

Pin	(a)	(b)	(c)
1	D00	BBSY	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22

Pin	(a)	(b)	(c)
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT*(1)	A16
23	AM4 GND	A15	
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V +5V	+5V	

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Errata: Table 2 on page 4-2 has been printed incorrectly. The correct layout for this table is given below.

Connector Pin Assignments

P1 Pin Assignment

The 96-way P1 connector on the AIP-1 mates with the J1 connector on the VMEbus backplane

Table 2 - Connector P1 Pin Assignment

Pin	(a)	(b)	(c)
1	D00	BBSY	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22

Pin	(a)	(b)	(c)
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK(1)	A17
22	IACKOUT*	SERDAT*(1)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

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Single-ended Analog Input Connections

Up to 32 analog inputs can be connected to the AIP-1 when it is operated in single-ended mode. The pin assignments for the analog input connector P2 is shown in Table 3.

Unused inputs should be connected to analog ground 0VA.

Table 3 - Single-ended Analog Input Connections

Pin	(a)	(b)	(c)
1	LOC (0)	N/C	LOC (1)
2	LOC (2)	N/C	LOC (3)
3	N/C	Reserved	N/C
4	N/C	N/C	See note
5	0VA	N/C	0VA
6	IN0	N/C	IN8
7	IN16	N/C	IN24
8	0VA	N/C	OVA
9	IN1	N/C	IN9
10	IN17	N/C	IN25
11	0VA	N/C	0VA
12	IN2	N/C	IN10
13	IN18	N/C	IN26
14	0VA	N/C	0VA
15	IN3	N/C	IN11
16	IN19	N/C	IN27
Pin	**(a)**	**(b)**	**(c)**
17	0VA	N/C	0VA
18	IN4	N/C	IN12
19	IN20	N/C	IN28
20	0VA	N/C	0VA
21	IN5	N/C	IN13
22	IN21	N/C	IN29
23	0VA	N/C	0VA
24	IN6	N/C	IN14
25	IN22	N/C	IN30
26	0VA	N/C	0VA
27	IN7	N/C/	IN15
28	IN23	N/C	IN31
29	0VA	N/C	0VA
30	SYNC	N/C	EXT TRIG

0VA is 0 Volts with respect to the analogue inputs IN0 to IN31.

0VA is isolated from the 0 Volts of the VMEbus.

Note: Pin C4 has a short track connecting it to Link E34. During normal use E34 should not be made (it is used only for factory test purposes) however, any signal taken to this pin on the backplane may induce a small amount of noise in the analog circuit particularly if the signal has fast edges or carries high frequency R.F. noise.

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Differential Analog Input Connections

Up to 16 analog input signals can be connected to the AIP-1 when it is operated in differential mode. Noise interference can be mimimised by connecting the AIP-1 in the manner illustrated in Table 4.

Table 4 - Differential Analog Input Connections

Pin	(a)	(b)	(c)
1	LOC (0)	N/C	LOC (1)
2	LOC (2)	N/C	LOC (3)
3	N/C	Reserved	N/C
4	N/C	N/C	See Note
5	0VA	N/C	0VA
6	IN0+N/C	IN8+	
7	IN0-	N/C	IN8-
8	0VA	N/C	OVA
9	IN1+N/C	IN9+	
10	IN1-	N/C	IN9-
11	0VA	N/C	0VA
12	IN2+N/C	IN10+	
13	IN2-	N/C	IN10-
14	0VA	N/C	0VA
15	IN3+N/C	IN11+	
16	IN3-	N/C	IN11-

Pin	(a)	(b)	(c)
17	0VA	N/C	0VA
18	IN4+N/C	IN12+	
19	IN4-	N/C	IN12-
20	0VA	N/C	0VA
21	IN5+N/C	IN13+	
22	IN5-	N/C	IN13-
23	0VA	N/C	0VA
24	IN6+N/C	IN14+	
25	IN6-	N/C	IN14-
26	0VA	N/C	0VA
27	IN7+N/C	IN15+	
28	IN7-	N/C	IN15-
29	0VA	N/C	0VA
30	SYNC	N/C	EXT TRIG
31	0VA	N/C	0VA
32		N/C	

GND is 0 Volts with respect to the VMEbus.

0VA is 0 Volts with respect to the analogue inputs IN0+ to IN15+, IN0- to IN15-.

0VA is isolated from GND.

Note: Pin C4 has a short track connecting it to Link E34. During normal use E34 should not be made (it is used only for factory test purposes) however, any signal taken to this pin on the backplane may induce a small amount of noise in the analog circuit particularly if the signal has fast edges or carries high frequency R.F. noise.

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Errata: Table 4 on page 4-4 has been printed incorrectly. The correct layout for this table is given below.

Differential Analog Input Connections

Up to 16 analog input signals can be connected to the AIP-1 when it is operated in differential mode. Noise interference can be mimimised by connecting the AIP-1 in the manner illustrated in Table 4.

Table 4 - Differential Analog Input Connections

Pin	(a)	(b)	(c)
1	LOC (0)	N/C	LOC (1)
2	LOC (2)	N/C	LOC (3)
3	N/C	Reserved	N/C
4	N/C	N/C	See Note
5	0VA	N/C	0VA
6	IN0+	N/C	IN8+
7	IN0-	N/C	IN8-
8	0VA	N/C	OVA
9	IN1+	N/C	IN9+
10	IN1-	N/C	IN9-
11	0VA	N/C	0VA
12	IN2+	N/C	IN10+
13	IN2-	N/C	IN10-
14	0VA	N/C	0VA
15	IN3+	N/C	IN11+
16	IN3-	N/C	IN11-

Pin	(a)	(b)	(c)
17	0VA	N/C	0VA
18	IN4+	N/C	IN12+
19	IN4-	N/C	IN12-
20	0VA	N/C	0VA
21	IN5+	N/C	IN13+
22	IN5-	N/C	IN13-
23	0VA	N/C	0VA
24	IN6+	N/C	IN14+
25	IN6-	N/C	IN14-
26	0VA	N/C	0VA
27	IN7+	N/C	IN15+
28	IN7-	N/C	IN15-
29	0VA	N/C	0VA
30	SYNC	N/C	EXT TRIG
31	0VA	N/C	0VA
32		N/C	

GND is 0 Volts with respect to the VMEbus.

0VA is 0 Volts with respect to the analogue inputs IN0+ to IN15+, IN0- to IN15-.

0VA is isolated from GND.

Note: Pin C4 has a short track connecting it to Link E34. During normal use E34 should not be made (it is used only for factory test purposes) however, any signal taken to this pin on the backplane may induce a small amount of noise in the analog circuit particularly if the signal has fast edges or carries high frequency R.F. noise.

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External Trigger/ SYNC Signal Connections

External trigger signals are applied to the AIP-1 via P2. The SYNC output is also accessed via connector P2 as shown in Figure 18.

Figure 18 - External Trigger/SYNC Connections

SYNC	P2 Row a pin 30
EXT. TRIG.	P2 Row c pin 30

Note: SYNC and EXT. TRIG. are referenced with respect to 0VA (P2 Row a pin 31 and Row c Pin 31)

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Chapter 5 - Software Configuration

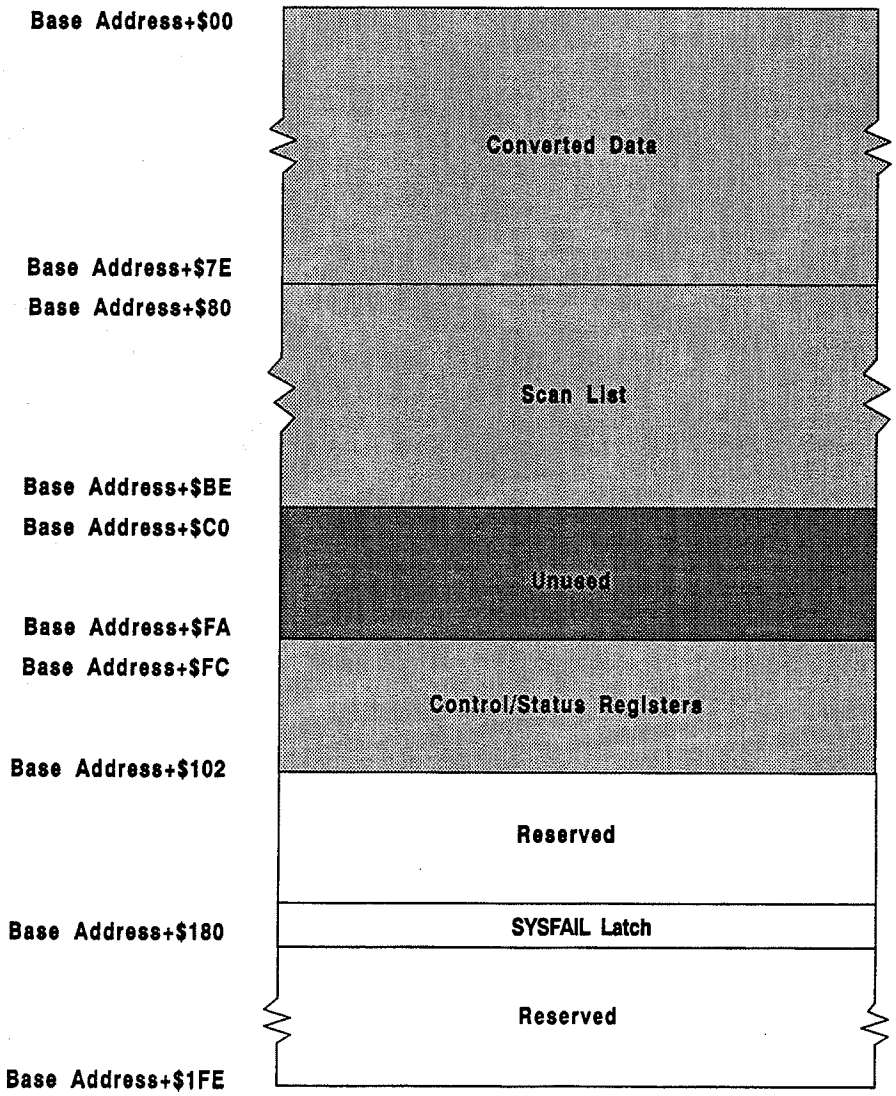
Introduction

The AIP-1 Memory Map occupies 256 consecutive word locations within the VMEbus short or standard address space, and is divided into six sections:

1. SYS FAIL latch
2. Control and Status Registers
3. Unused
4. Scan List
5. Converted Data Memory
6. Reserved

The location of the memory map within the address space of the VMEbus is controlled by setting the base address of the AIP-1 using jumpers (see Chapter 3).

Figure 19 - Simplified Memory Map

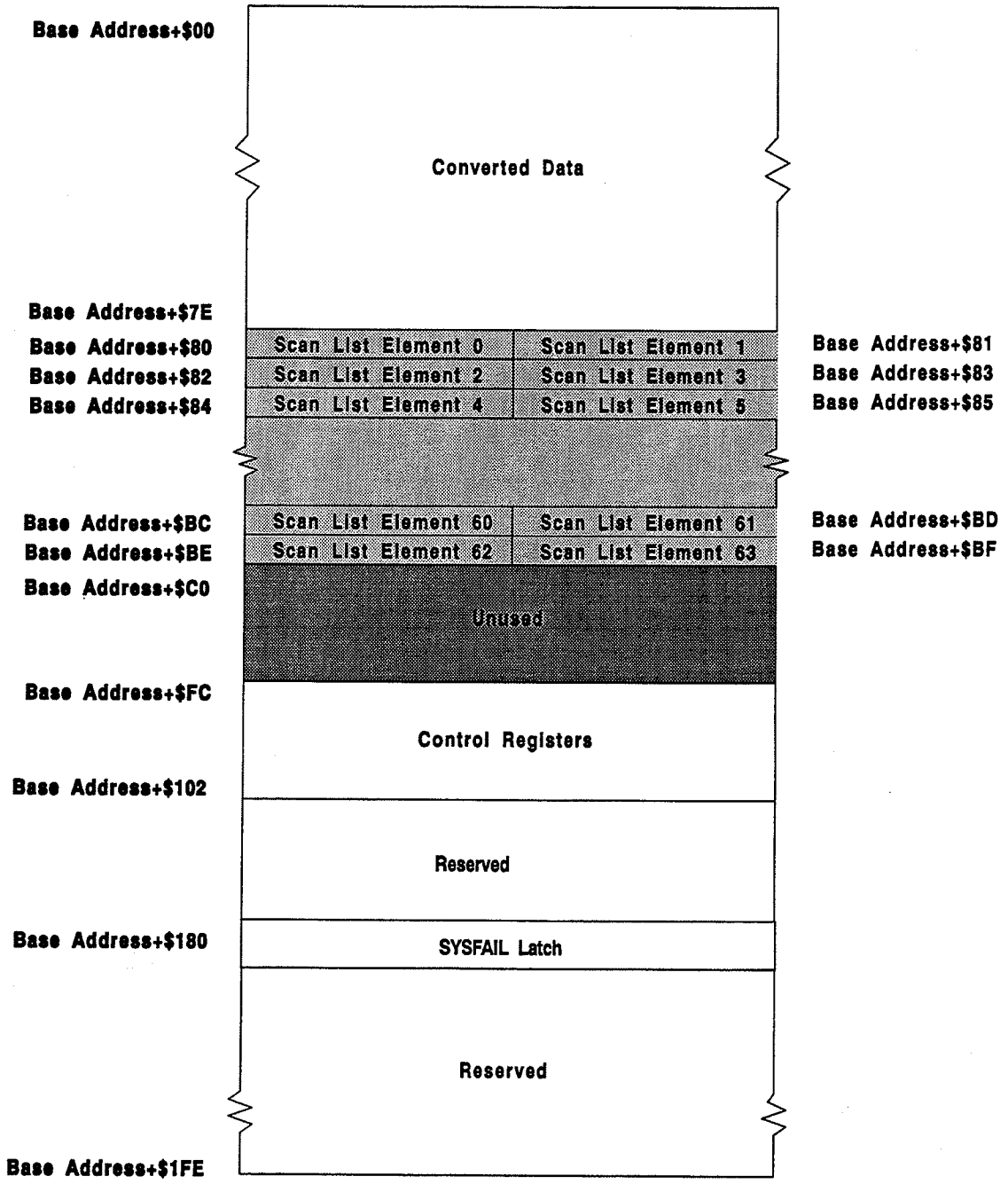


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Setting up the Scan List

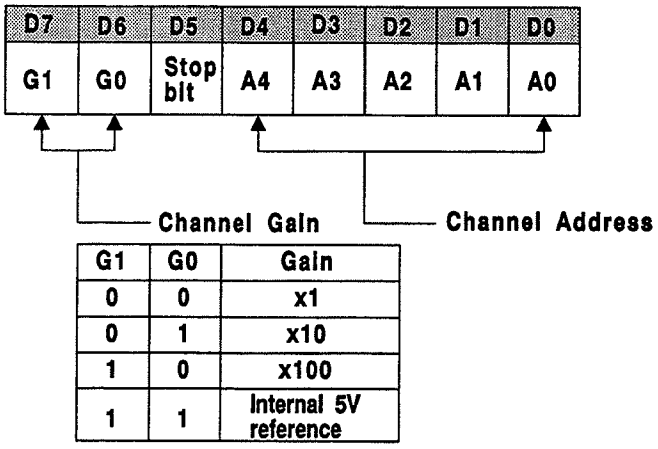
The Scan List defines the order in which the analog inputs are sampled. It consists of 64 consecutive byte locations, called Scan List Elements, located in the AIP-1 memory map between `Base Address + $80` and `Base Address + $BE`.

Figure 20 - Memory Map showing Scan List Elements



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Figure 21 - Scan List Element



G1	G0	Gain
0	0	x1
0	1	x10
1	0	x100
1	1	Internal 5V reference

Each Scan List Element contains a 5 bit binary address which is used to select one of the input channels, a 2 bit binary code which defines the associated software programmable gain, plus a stop bit. The Scan List Elements should be programmed by the user before the AIP-1 starts to sample analog input data.

The 32 input channels are numbered between 00 and 31, and have 5 bit binary addresses in the range 00000 to 11111 as shown in Table 5. By entering a sequence of binary channel addresses into the scan list, together with the desired gain for each channel, it is possible to program the AIP-1 to sample its input channels in any order.

For example :

To sample Channel 05 continuously, the binary address 00101 should be entered into every Scan List Element in the Scan List.

To sample each channel once and in order, each of the binary addresses in Table 6 should be entered into the corresponding Scan List Element.

When a channel is sampled, the converted digital code is stored in the corresponding 16 bit word location in the converted data memory of the AIP-1. The relationship between each scan list element and locations in the converted data memory is detailed in Table 6.

For more information regarding the storage of converted data, see the 'Storing Converted Data' section in this chapter.

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Table 5 - Programming the Scan List

Sample Channel No.	D4	D3	D2	D1	D0
$00	0	0	0	0	0
$01	0	0	0	0	1
$02	0	0	0	1	0
$03	0	0	0	1	1
$04	0	0	1	0	0
$05	0	0	1	0	1
$06	0	0	1	1	0
$07	0	0	1	1	1
$08	0	1	0	0	0
$09	0	1	0	0	1
$0A	0	1	0	1	0
$0B	0	1	0	1	1
$0C	0	1	1	0	0
$0D	0	1	1	0	1
$0E	0	1	1	1	0
$0F	0	1	1	1	1
$10	1	0	0	0	0
$11	1	0	0	0	1
$12	1	0	0	1	0
$13	1	0	0	1	1
$14	1	0	1	0	0
$15	1	0	1	0	1
$16	1	0	1	1	0
$17	1	0	1	1	1
$18	1	1	0	0	0
$19	1	1	0	0	1
$1A	1	1	0	1	0
$1B	1	1	0	1	1
$1C	1	1	1	0	0
$1D	1	1	1	0	1
$1E	1	1	1	1	0
$1F	1	1	1	1	1

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Table 6 - Valid Scan List Addresses

Scan List Element	Scan List Element Address	Converted Data Storage Address
$00	Base+$80	Base+$00
$01	Base+$81	Base+$02
$02	Base+$82	Base+$04
$03	Base+$83	Base+$06
$04	Base+$84	Base+$08
$05	Base+$85	Base+$0A
$06	Base+$86	Base+$0C
$07	Base+$87	Base+$0E
$08	Base+$88	Base+$10
$09	Base+$89	Base+$12
$0A	Base+$8A	Base+$14
$0B	Base+$8B	Base+$16
$0C	Base+$8C	Base+$18
$0D	Base+$8D	Base+$1A
$0E	Base+$8E	Base+$1C
$0F	Base+$8F	Base+$1E
$10	Base+$90	Base+$20
$11	Base+$91	Base+$22
$12	Base+$92	Base+$24
$13	Base+$93	Base+$26
$14	Base+$94	Base+$28
$15	Base+$95	Base+$2A
$16	Base+$96	Base+$2C
$17	Base+$97	Base+$2E
$18	Base+$98	Base+$30
$19	Base+$99	Base+$32
$1A	Base+$9A	Base+$34
$1B	Base+$9B	Base+$36
$1C	Base+$9C	Base+$38
$1D	Base+$9D	Base+$3A
$1E	Base+$9E	Base+$3C
$1F	Base+$9F	Base+$3E

Scan List Element	Scan List Element Address	Converted Data Storage Address
$20	Base+$A0	Base+$40
$21	Base+$A1	Base+$42
$22	Base+$A2	Base+$44
$23	Base+$A3	Base+$46
$24	Base+$A4	Base+$48
$25	Base+$A5	Base+$4A
$26	Base+$A6	Base+$4C
$27	Base+$A7	Base+$4E
$28	Base+$A8	Base+$50
$29	Base+$A9	Base+$52
$2A	Base+$AA	Base+$54
$2B	Base+$AB	Base+$56
$2C	Base+$AC	Base+$58
$2D	Base+$AD	Base+$5A
$2E	Base+$AE	Base+$5C
$2F	Base+$AF	Base+$5E
$30	Base+$B0	Base+$60
$31	Base+$B1	Base+$62
$32	Base+$B2	Base+$64
$33	Base+$B3	Base+$66
$34	Base+$B4	Base+$68
$35	Base+$B5	Base+$6A
$36	Base+$B6	Base+$6C
$37	Base+$B7	Base+$6E
$38	Base+$B8	Base+$70
$39	Base+$B9	Base+$72
$3A	Base+$BA	Base+$74
$3B	Base+$BB	Base+$76
$3C	Base+$BC	Base+$78
$3D	Base+$BD	Base+$7A
$3E	Base+$BE	Base+$7C
$3F	Base+$BF	Base+$7E

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Unlike the hardware configurable input gain, which is set using jumper E14 and affects all 32 input channels, (see Chapter 3) the software programmable channel gain set within each Scan List Element is associated solely with the channel individually addressed by the element. The software programmable channel gain therefore allows signals of vastly different magnitudes to be handled simultaneoulsy by the AIP-1. Bits D6 and D7 of the Scan List Element can be used to set the software programmable channel gain to x1, x10 or x100 as shown in Table 7.

Table 7 - Channel Gain Selection

G1	G0	Gain
0	0	x1
0	1	x10
1	0	x100
1	1	Internal 5V reference

Note: The hardware configurable input gain and the software programmable channel gains are cumulative.

ie. an input gain of x10 (set using jumper E14) associated with a channel gain of x100 (set in the Scan List Element) will result in an overall gain of 1000. Hence by combining the two gain options it is possible to achieve overall gains in the range x1 to x10000 (see Table 9).

Table 8 - Valid Input/Channel Gain Combinations

Input Gain (TBA)	Channel Gain (Scan List)	Overall Gain	Maximum Voltage Range 0-10V
x1	x1	1	10V
x1	x10	10	1V
x1	x100	100	0.1V
x10	x1	10	1V
x10	x10	100	0.1V
x10	x100	1000	0.01V
x100	x1	100	0.1V
x100	x10	1000	0.01V
x100	x100	10000	0.001V

Caution: The combination of low input voltages and high input gains (in the range 1000-10000) may effect the achievable accuracy adversely.

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Stop bit

Bit 5 position is used in conjunction with link E32 to provide a programable stop bit. The Half full flag is normally fed by a signal which detects that the Scan list pointer is at the halfway mark. If link E32 selects the programmable end stop instead of the Half full flag, then, whenever a stop bit is encountered during the sending of a Scan list element, it is routed to Control/Status register 1 in place of the Half full flag. A stop bit exists when Bit position 5 in a Scan list element is programmed to a logic 1.

More than 1 stop bit can be programmed if required, for example, 4 stop bits could be programmed throughout the 64 elements at intervals 16 elements apart, this would give 4 'Quarter full' flags. The more usual use for the stop flag is as a boundary flag generating an interrupt where the number of programmed Scan list elements is small and/or the Timebase value required is sufficiently large that time is wasted waiting for the Full or Half full flags to set. The occurance of a stop bit does not actually stop the sampling, it is merely notification that (in its normal use) the required Scan list elements have all been sampled.

The stop flag (Control Register 2 bit 13) has the same affect as, and is reset in the same way as, the Half flag, eg the flag is reset following a read of any location in the Converted data area, and by a software reset, also, as a stop flag is asserted, it will clear the Full flag if that is asserted, and Poll mode is selected (see the section on Control/Status register 2).

Note - when operating in interrupt mode using the programmable stop flag it will be necessary to clear out all Scan list bit 5 locations (stop bits) which are not needed, this includes those after the last required stop bit, the scan will continue sampling after detecting a stop bit, any and every further detected stop bit will generate an interrupt.

Programming the stop bit

To achieve the higher throughput rate, the sampling and conversion functions are overlapped, this means that the SCAN LIST DATA sent out for sampling is not in step with the CONVERTED DATA being returned. At any given time, converted data coming back from the analog section will be for scan data passed several samples previously. To program a stop therefore, place the stop bit in the SCAN list location which is 1 address after the required sample count.

Example:

5 samples are required, SCAN list locations 0,1,2,3,4 are programmed with the required sample data (but no stop bits), the remaining SCAN list locations (5 to 63) are first cleared so that all stop bits are unprogrammed, then, since the required sample count is 5, a stop bit is programmed into location 6 of the scan list.

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Scan List Pointer

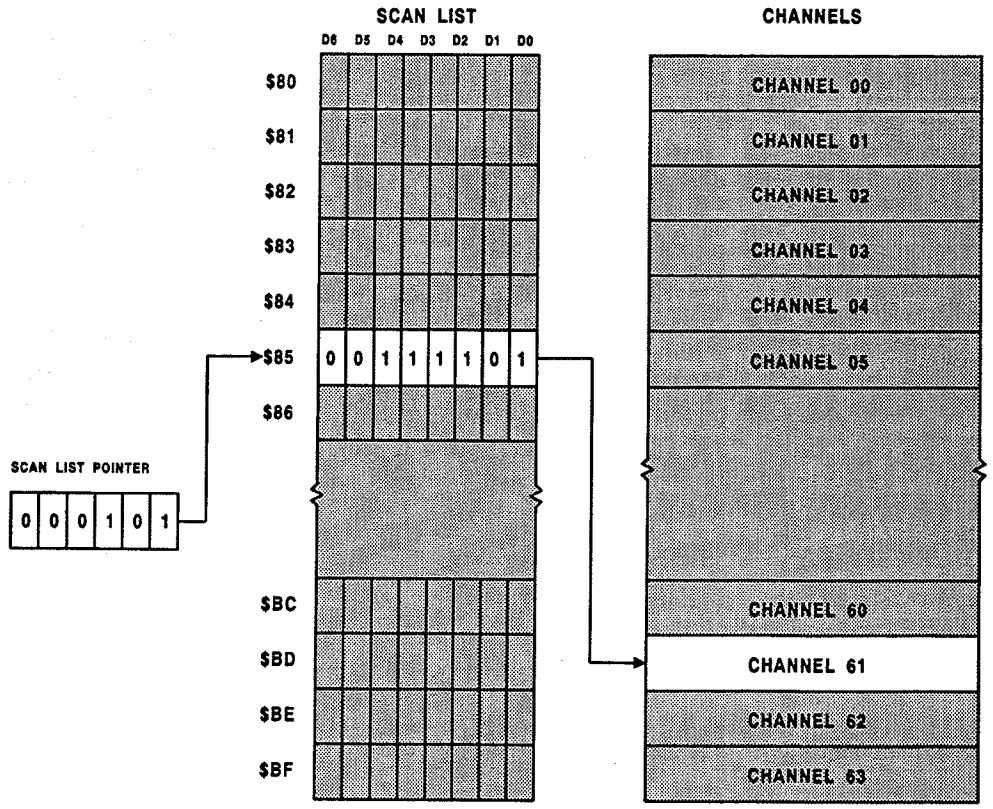
The Scan List Pointer is a special 6 bit register used as an address when accessing the Scan List Elements . It is also used as an adress when storing converted data. A scan list element points to a channel to be sampled (see Figure 22)

When input sampling is initiated by clearing Control/Status Register 2 the Scan List Pointer reads -3 ($3D). Each time a channel is sampled, the Scan List Pointer is incremented so that it points to the next consecutive Scan List Element. This process continues until the Scan List Pointer has passed through all 64 elements of the scan list and points to the last Scan List Element+1 ($00). When the last channel has been sampled, the condition of the Scan List Pointer is determined by the data acquisition mode of the AIP-1:

If the AIP-1 is operating in Transient Mode (see 'Continuous/Transient Mode Selection (D11)' in this chapter) the Scan List Pointer is not reset when it reaches the last Scan List Element ($3F) and the AIP-1 halts automatically showing 0 when read.

If the AIP-1 is operating in Continuous Mode (see 'Continuous/Transient Mode Selection (D11)' in this chapter), the Scan List Pointer is reset each time it reaches the Last Scan List Element ($3F) and continues to step through the Scan List until the AIP-1 is halted by the CPU, or a software reset is generated.

Figure 22 - Scan List Pointer



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When a scan is first initiated, the lower 6 bits of CONTROL/STATUS register 2 start counting from -4 (HEX 3C). For this reason, a poll of the status register, taken immediately after starting a sample, will give a value of $3C or $3D in its lower 6 bits (depending on how soon afterwards the status is read). Converted data storing will not take place until the scan list pointer reaches 0, Similarly the VALID_DATA flag will not occur until the scan list pointer reaches 0. The POINTER is however still a true indicator to the progress of the scan since it always points to the next word to be written to, ie it reflects the address of the element in the SCAN list which is currently being converted. There should be no problem unless the pointer is being monitored for values of hex 3D,3E,3F if this is the case, it should be monitored for a value of 0 first. (Note that once the first scan is underway, ie the SCAN LIST POINTER has passed through 0, it behaves normally, ie in CONTINUOUS mode scanning, any value of SCAN POINTER is valid once it has passed through the first scan, the value of the SCAN LIST pointer will always be 1 count ahead of the current element address whose data is currently being sampled).

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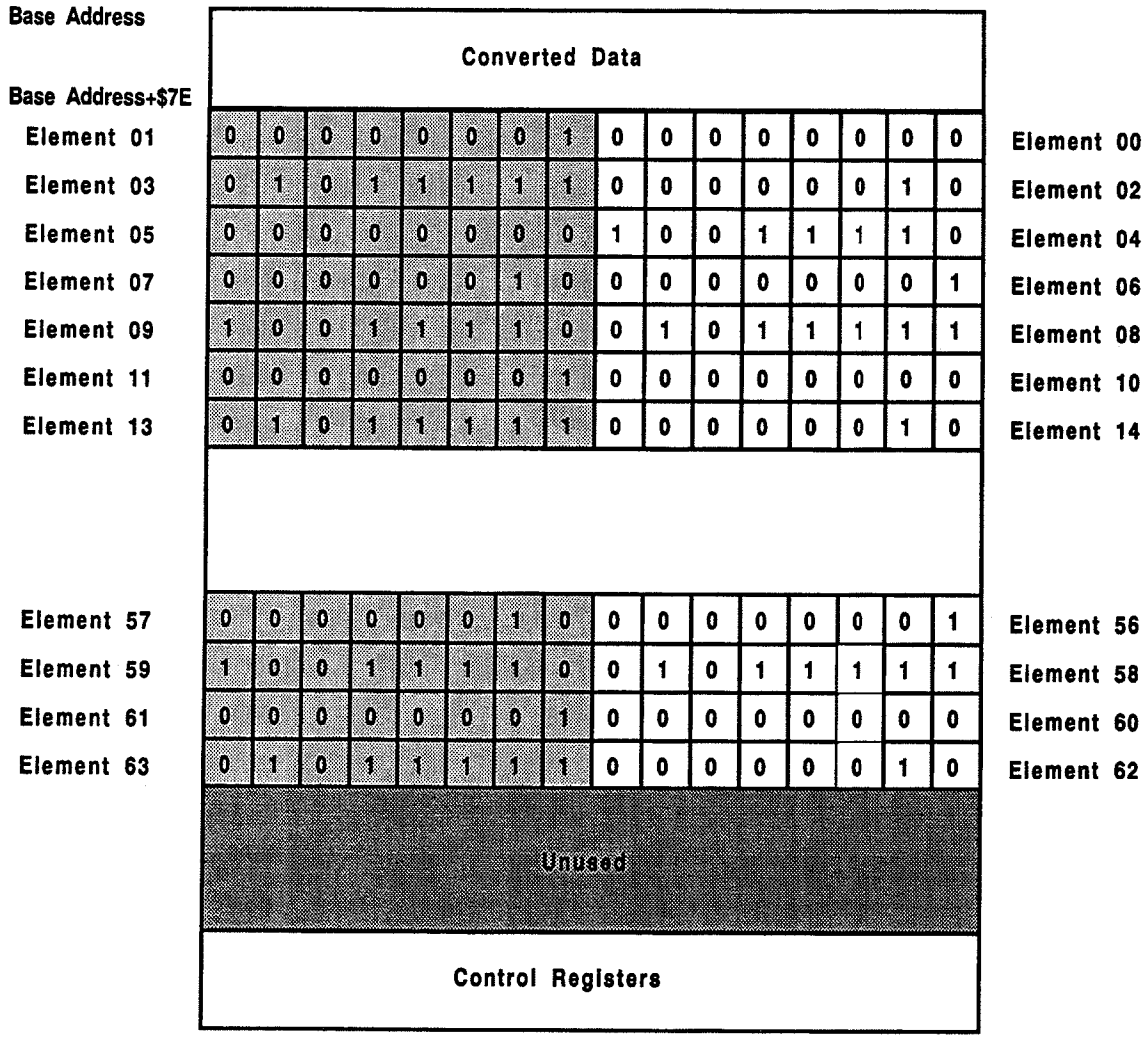
Example : Programming The Scan List

To sample five analog inputs repetitively, in the following order :

```
Channel 00 (gain=x1)      :   00000000
Channel 01 (gain=x1)      :   00000001
Channel 02 (gain=x1)      :   00000010
Channel 31 (gain=x10)     :   01011111
Channel 30 (gain=x100)    :   10011110
```

Enter the binary codes into the Scan List as shown in Figure 23.

Figure 23 - Programming the Scan List

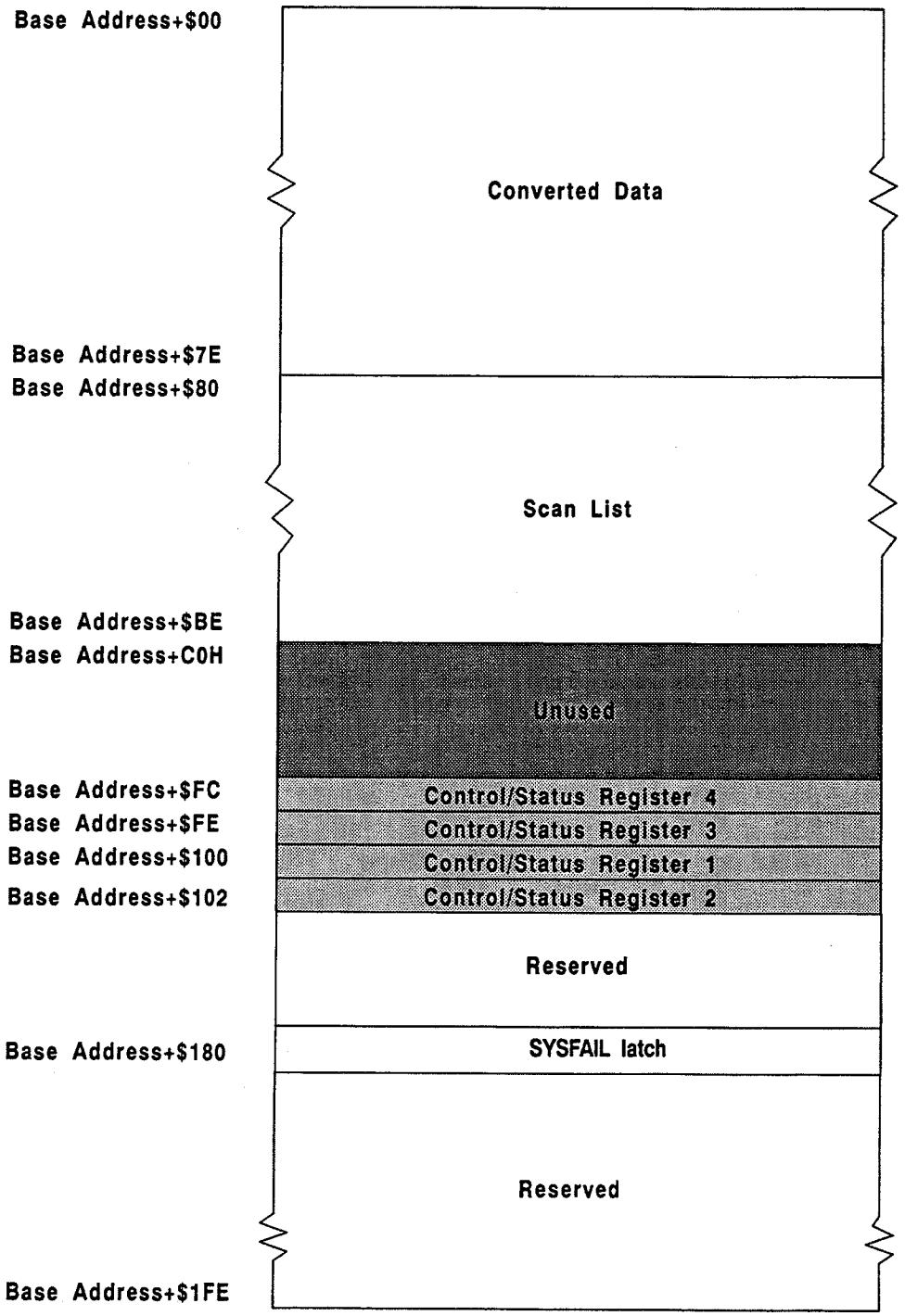


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AIP-1 Control/Status Registers

Software control of the AIP-1 is performed via four control/status registers, which are first programmed by the user, and then may be interrogated by the CPU during operation to determine the current status of the board.

Figure 24 - Memory Map showing Control Registers



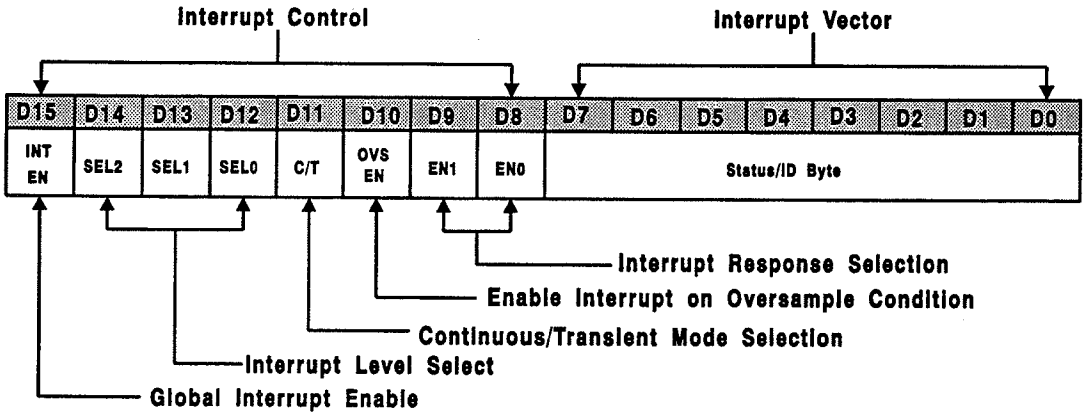
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Control/Status Register 1 - Interrupt Response

Control/Status Register 1 is located at an offset of $100 from the base address of the AIP-1. It is used to select the data acquisition mode of the AIP-1 (continuous or transient mode) and to configure its interrupt response.

Control/Status Register 1 should be programmed as part of the initialisation procedure of the AIP-1. Once programmed it may be read at any time to determine the current status of the board.

Figure 25 - Control/Status Register 1



Interrupt Status/ID Byte (D0-D7)

The least significant byte (D0-D7) of Control Register 1 contains the status/ID byte that represents the interrupt vector supplied during a valid interrupt cycle, as defined by the ANSI/IEEE Std. 1014-1987.

Interrupt Response (D8-D9)

The conditions which cause the AIP-1 to generate an interrupt across the VMEbus are defined using bits D8 and D9 of Control Register 1. These conditions, and the corresponding configuration of D8 and D9, are specified in Table 9.

Oversample Response (D10)

Table 9 - Interrupt Response

D9	D8	Interrupt Response
0	0	No Interrupt
0	1	Interrupt each conversion
1	0	Interrupt on data memory **half-full** or **full** (or if link selected, when programmed stop bit is encountered).
1	1	Interrupt on data memory **full**

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When bit D10 of Control Register 1 is set to logic 1, the AIP-1 will generate an interrupt across the VMEbus whenever the external trigger causes an oversample condition.

Table 10 - Oversample Response

D10	Interrupt Response
0	Disable interrupt on oversample condition
1	Enable interrupt on oversample condition

Continuous/ $\overline{\text{Transient}}$ Mode Selection (D11)
With bit D11 of Control Register 1 set to logic 0, the AIP-1 operates in transient mode, so that it cycles once through the scan list (see 'Operating the AIP-1 in Transient Mode' and 'Operating the AIP-1 in Continuous Mode' sections in Chapter 6) and then halts. With bit D11 set to logic 1, the AIP-1 operates in continuous mode, so that it cyles continuously through the scan list at a rate determined by the trigger signal, until halted.

Table 11 - Continuous/Transient Mode Selection

D11	Continuous/Transient Mode
0	Transient Data Acquisition Mode
1	Continuous Data Acquisition Mode

Interrupt Level Selection (D12-D14)
The combination of these three bits is used to select the interrupt request level for the AIP-1.

Table 12 - Interrupt Level Selection

D14	D13	D12	Interrupt Level
0	0	0	No Interrupt Response
0	0	1	$\overline{\text{IRQ1}}$ driven
0	1	0	$\overline{\text{IRQ2}}$ driven
0	1	1	$\overline{\text{IRQ3}}$ driven
1	0	0	$\overline{\text{IRQ4}}$ driven
1	0	1	$\overline{\text{IRQ5}}$ driven
1	1	0	$\overline{\text{IRQ6}}$ driven
1	1	1	$\overline{\text{IRQ7}}$ driven

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Global Interrupt Enable (D15)

Setting bit D15 to logic 1 enables all interrupts and the AIP-1 responds according to the configuration of the other bits in Control/Status Register 1.

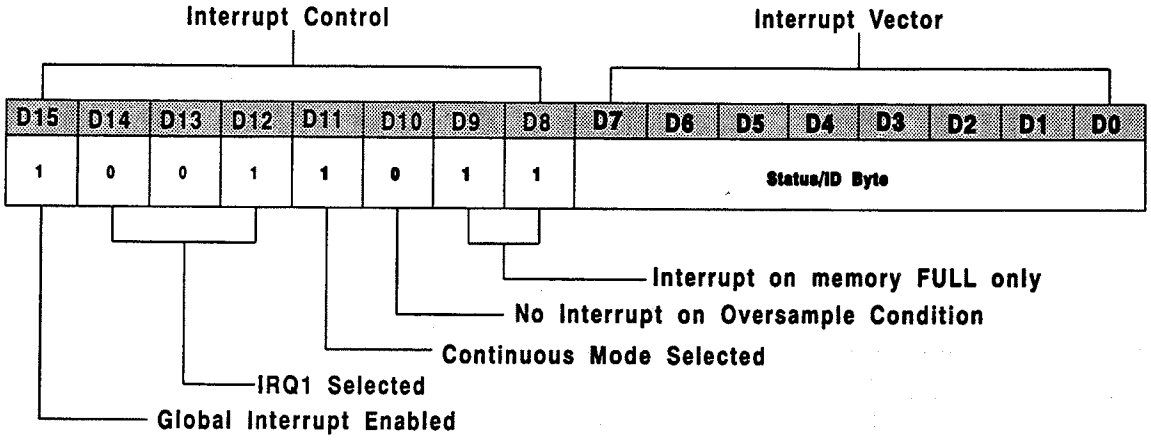
Table 13 - Global Interrupt Enable

D15	Global Interrupt Enable
0	AIP Interrupts Disabled
1	Interrupts enabled - response determined determined by the configuration of bits D8-D9 and D12-D14

Example - Programming Control/Status Register 1

To configure the AIP-1 to scan its inputs continuously and to generate an interrupt on IRQ1 only when the data memory becomes full.

Figure 26 - Programming Control/Status Register 1



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Control/Status Register 2 - I/O Section Control and Sysreset Response

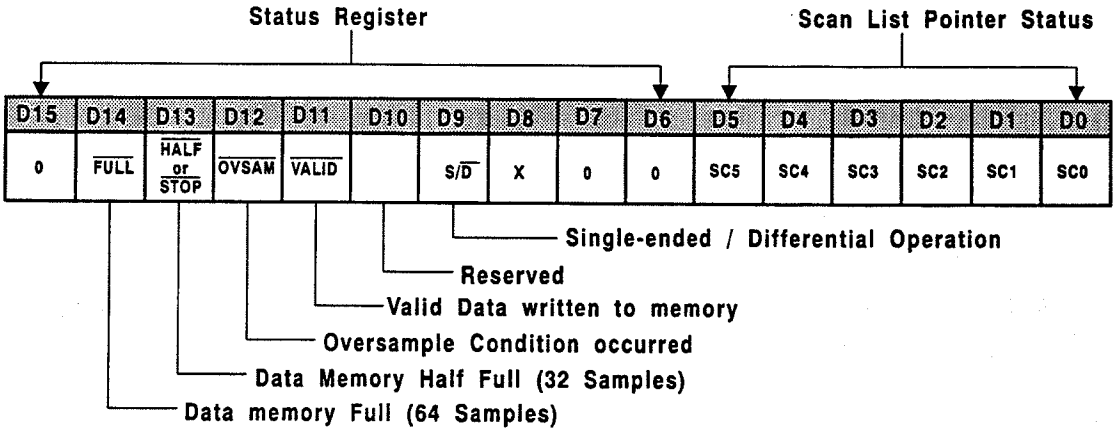
Control/Status Register 2 is located at an offset of $102 from the base address of the AIP-1. It is used to initiate the analog data sampling process and performs the function of a software reset.

Control/Status Register 2 must be accessed at the conclusion of the initialisation procedure of the AIP-1 in order to start the board. Once the AIP-1 is operating, control/status register 2 may be read at any time to determine the current status of the board. It contains a record of the current contents of the Scan List Pointer which indicates the next Scan List Element to be accessed (see 'Scan List Pointer' in this chapter) and the flags required to control the AIP-1 when configured to operate in a polling mode.

Writing to any bit in Control/Status Register 2 starts the input sampling process of the AIP-1. The Scan List Pointer and all status flags are cleared and sampling is initiated on the first channel at a rate determined by selection of the trigger signal. **The preferred method of initiating the AIP-1 is to clear Control/Status Register 2 by writing logic 0 to all bits.**

Writing to Control/Status Register 2 when the AIP-1 is operating also performs the function of a software reset. The Scan List Pointer, the $\overline{\text{HFULL}}$ and $\overline{\text{FULL}}$ flags are cleared (to logic 1) and the channel address contained in the first Scan List Element is passed to the channel multiplexer arrangement which selects the first channel to be sampled.

Figure 27 - Control/Status Register 2



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Scanlist Pointer (D0-D5)
The current contents of the Scan List Pointer (ie. the address of the next Scan List Element to be read) is reflected in bits D0 to D5 of Control/Status Register 2. These bits change only after converted data has been written into memory.

Single Ended / Differential Mode (D9)
Bit D9 reflects the configuration of the analog front end, indicating whether single-ended or differential inputs are being processed. Bit D9=1 indicates that single-ended mode has been selected. Bit D9=0 indicates that differential mode has been selected.

Bit D10 Reserved

Table 14 - Single-ended/Differential Mode

D9	Input Mode
0	Differential Mode selected
1	Single-ended Mode selected

Data Valid (D11)

Bit D11 becomes active (logic 0) when valid data has just been written into any location of the on-board converted data memory. It remains active until cleared (logic 1) by reading Control Status Register 1.

Note that the flag is cleared **after** being read.

Oversample (D12)
Table 15 - Data Valid Indicator

D11	DATA VALID Indicator
0	Valid Data available
1	No new converted data

Bit D12 is set to logic 1 to indicate that the sampling process is occuring normally. If an Oversample condition occur (ie. the sample rate exceeds 60kHz), then Bit D12 will be cleared to logic 0, but only when using the external trigger.

The Oversample condition, and therefore bit D12, is only reset by writing to Control/Status Register 2 to initiate a software reset of the AIP-1.

Table 16 - Oversample Indicator

D12	OVERSAMPLE Indicator
0	Oversample has occured
1	Conversions proceeding normally

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Memory Status (D13 and D14)
The status of bits D13 and D14 indicates the quantity of converted data currently stored in the converted data memory.

Table 17 - Memory Status

D14 (Full)	D13 (HFull)	Memory Status
0	1	Full = 64 samples
1	0	Half-full = 32 samples

FULL flag: Indicates that the converted data memory is full and needs to be transferred out of RAM.

Set (to logic 0) by: A count of 64 data words having been written to data memory (specifically when the outputs of the SCAN list pointer point to address 63 whilst converted data is being written to DPM).

Cleared (to logic 1) by: In Transient mode, cleared by Software Reset (writing to C/S reg 2) or hardware reset.

In Continuous mode with interrupt on either FULL or HALF FULL flag enabled (ie inten1=1), cleared by reading status reg 2 OR SoftwareReset. (Note that the former will be post read).

In Continuous mode with interrupts disabled (inten1=0 inten0=0), cleared by Software Reset OR when half full flag is set (ie using the same signal as that which is used to set the half full flag, the half full flag being set will NOT itself clear the FULL flag).

HALF FULL flag: Indicates that the converted data memory is half full and needs to be transferred out of RAM

Set (to logic 0) by: A count of 32 data words having been written to data memory. (specifically when the outputs of the SCAN list pointer is pointing to address 31 whilst converted data is being written to DPM).

Cleared (to logic 1) by: Any read of converted data.

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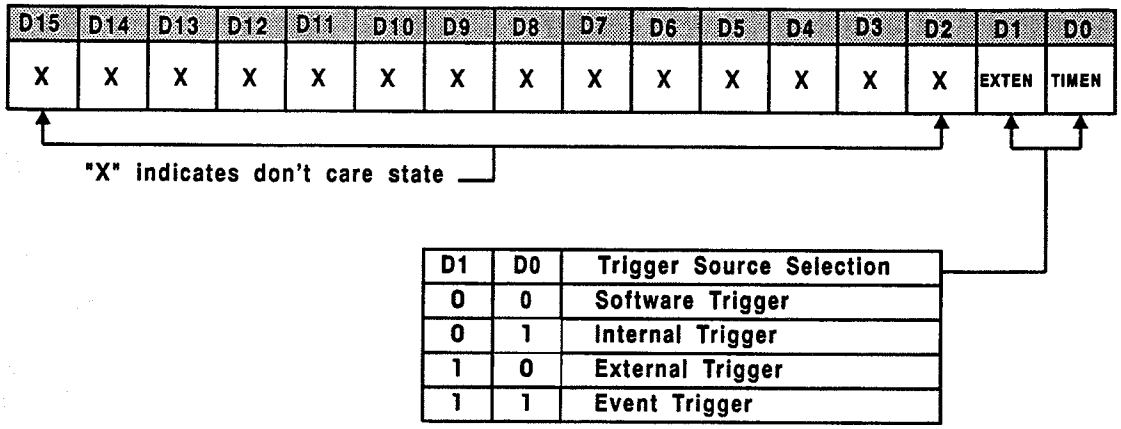
Control/Status Register 3 - Trigger Source Selection

Control Register 3 is located at an offset of $0FE from the base address of the AIP-1 memory map. It is used to select the source of the trigger signal which determines the rate at which the AIP-1 samples its analog inputs. There are four possible trigger sources to select from:

1. Trigger generated by reading converted data from data memory (software trigger)
2. Trigger generated by on-board timer (internal trigger)
3. Trigger generated by external signal (external trigger)
4. Trigger initiated by external event which starts on-board timer (event trigger)

Software Trigger (EXTEN=0,TIMEN=0)

Figure 28 - Control/Status Register 3



D1	D0	Trigger Source Selection
0	0	Software Trigger
0	1	Internal Trigger
1	0	External Trigger
1	1	Event Trigger

The rate at which the analog input channels are sampled is entirely controlled by the program which reads the digital codes previously stored in the data memory. Each time any location in the data memory is read, the next input channel contained in the scan list is sampled. Note that 4 software trigger pulses need to occur before the return of valid data, during this time the VALID DATA bit will remain inactive.

Software triggering is initiated by performing 4 single "dummy" reads from the converted data memory. The data acquired by these read operations should be discarded. At the conclusion of each read cycle a software trigger is generated. Further reads of converted data will result in converted data from the channel identified by the current Scan List Element being stored.

The AIP-1 remains inactive after the conclusion of each conversion cycle until any location in the converted data memory is read. The end of the conversion cycle can be detected by polling bits D10 and D11 in Control/Status Register 2, or configuring the AIP-1 to generate an interrupt when conversion is complete.

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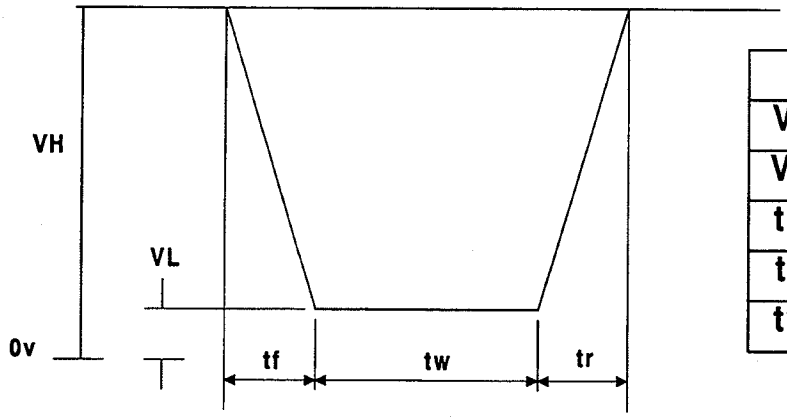
Internal Trigger (EXTEN=0,TIMEN=1)
The AIP-1 may be configured to generate an internal trigger signal based upon a quartz crystal and counter combination (see 'Changing the Base Sample Period' in Chapter 3 and 'AIP-1 Control/Status Registers' section in this Chapter).

External Trigger (EXTEN=1,TIMEN=0)
A TTL compatible signal conforming to the timing diagram shown in Figure 30, may be used as an external trigger applied to pin 30 of connector P2 Row c. The conversion cycle is initiated on the falling edge of the external trigger signal.

An "oversampling" condition will occur if the frequency of the external trigger signal exceeds the maximum sample frequency of the AIP-1. In this event the O/S LED on the front panel will be illuminated and Bit D12 of Control/Status Register 2 will be cleared (logic 0). If the Oversample option has been selected using jumper (TBA), then the Bits 13 - 15 of any converted data words will be cleared. The oversample condition remains active until the host CPU issues a software reset which sets bit D12 of the register to logic 1 and resets the O/S LED.

Note that the oversample flag reflects the logic throughput rate and not the Analog throughput rate and will set (go low) on rates greater than 60kHz.

Figure 29 - External Trigger Timing Diagram



	MAX	MIN
VL	0.5V	-10.0V
VH	+25V	+3.5V
tR	20nS	-
tF	20nS	0nS
tw	15uS	300nS

Event Trigger (EXTEN =1, TIMEN=1)
A single TTL compatible pulse signal, which conforms to the timing diagram in Figure 30, applied to pin 30 of connector P2 Row c will initiate the conversion process on the AIP-1 which will then continue under the control of the internal trigger.

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Control/Status Register 4 - Sample Period Multiplier

The rate at which the AIP-1 samples its analog inputs is determined by a trigger signal which synchronises the internal operation of the board. This trigger signal may be generated by one of four sources (see 'Control/Status Register 3 - Trigger Source Selection' in this chapter), one of which is an internal timer arrangement. When the internal trigger is selected, its period is derived as a multiple of two components :

1. Base Sample Period (set using Links E2 - E9 - see 'Changing Base Sample Period' section in Chapter 3)
2. Sample Period Multiplier (software selected using Control/Status Register 4)

The first 8 bits of Control/Status Register 4 contain the **Sample Period Multiplier + 1** (maximum value $FF)

Figure 30 - Deriving the Sample Period

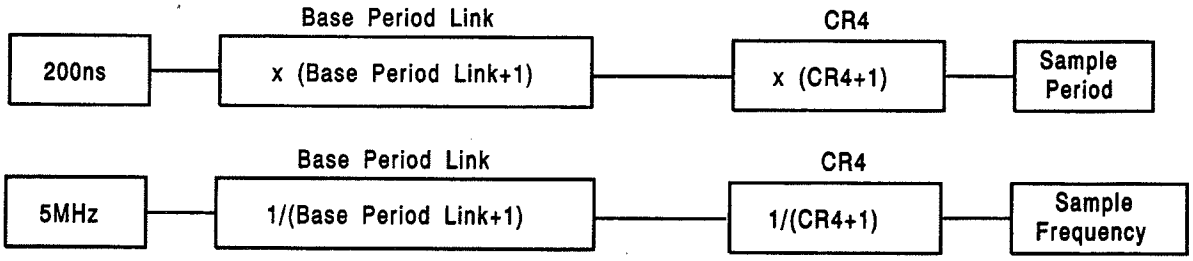
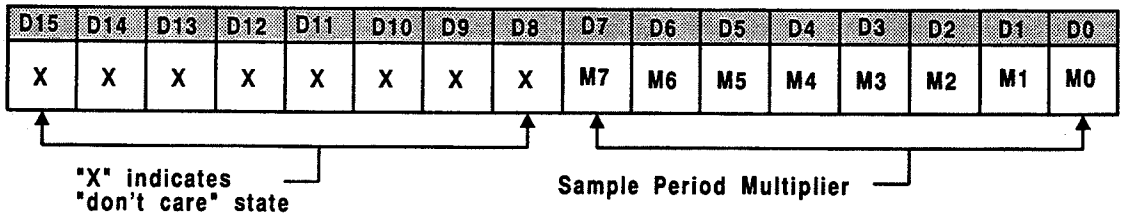


Figure 31 - Control/Status Register 4



See 'Changing Base Sample Period' in Chapter 3 for example of setting up the time base.

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Sysfail Latch

A simple one bit latch driving a front panel LED is provided so that basic VME access can be verified visually as an automatic process.

Clearing the latch (extinguishing the LED) is accomplished by writing any byte of data to location: BASE ADDRESS + $181

Setting the latch (illuminating the LED) is accomplished by writing any byte of data to location: BASE ADDRESS + $180

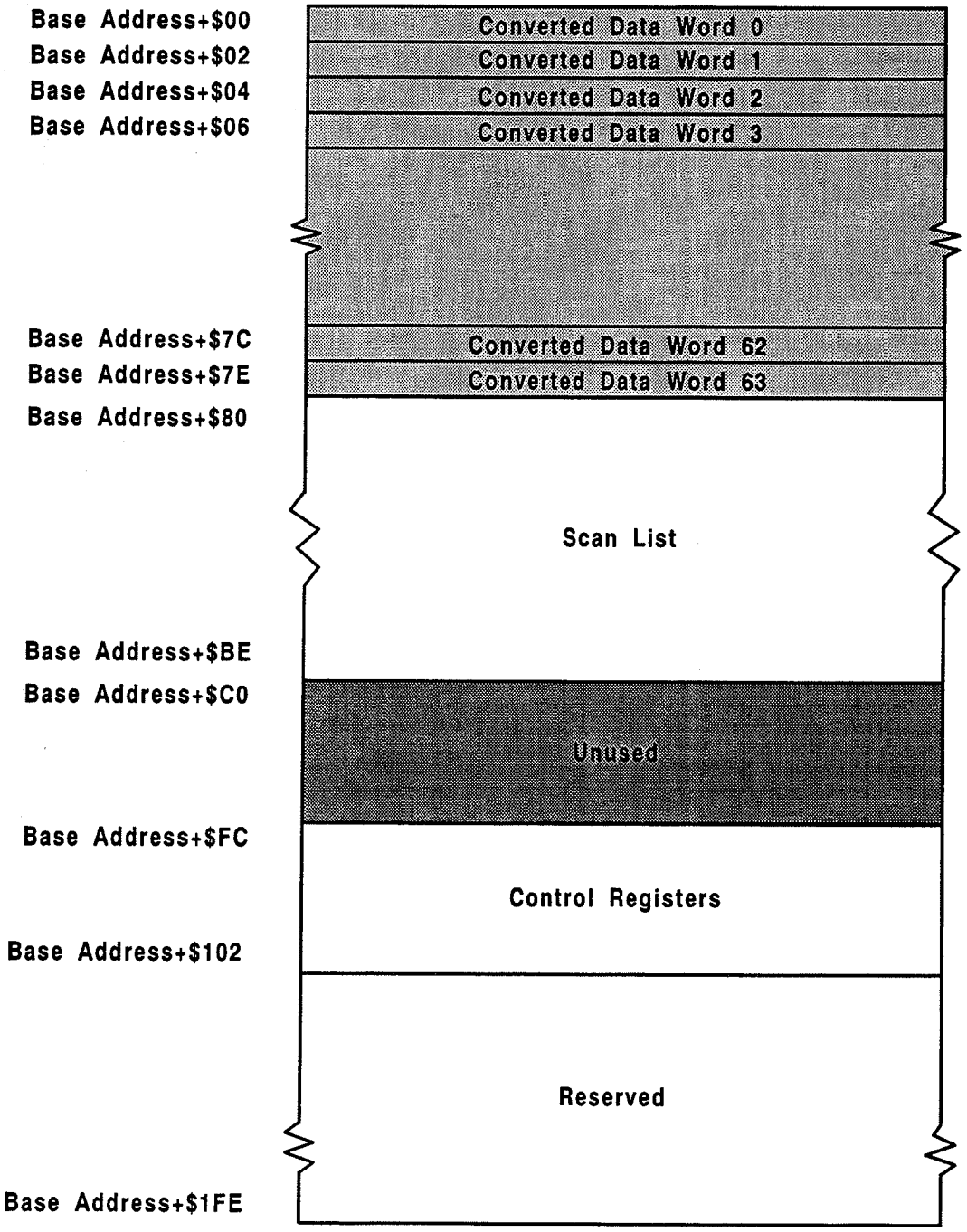
The latch is also set during power up, or whenever a VME System Reset signal is issued. If, following power up or reset, the VME Master is programmed to clear this Sysfail latch, the Sysfail LED on the front panel (red LED at the top) will extinguish. This system would provide for a simple visual indication that, following system reset, basic VME access to the card is possible. Further automated testing of the AIP-1 card could also be provided as required, and the Sysfail latch could be set to provide visual indication of a failed test.

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Storing Converted Data

When each analog input is sampled, the instantaneous analog voltage is converted into an equivalent 12 bit digital code which is stored in the **converted data memory**. The converted data memory is located between **Base Address+$00** and **Base Address +$7F** in the AIP-1 memory map as shown in Figure 32.

Figure 32 - Memory Map showing Converted Data Memory



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The data acquired from the channel whose address is entered in Scan List Element 00 is stored in Converted Data Location 00 (Base Address+$00)

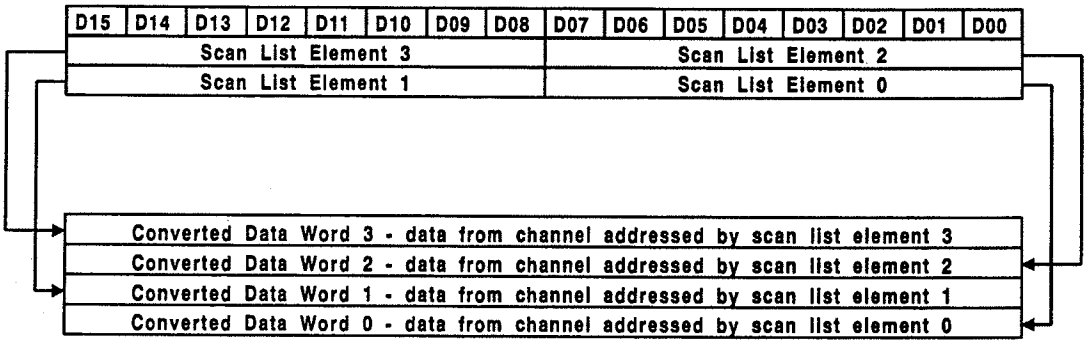
The data acquired from the channel whose address is entered in Scan List Element 01 is stored in Converted Data Location 01 (Base Address+$02)

The data acquired from the channel whose address is entered in Scan List Element 03 is stored in Converted Data Location 03 (Base Address+$04)

and so on .....

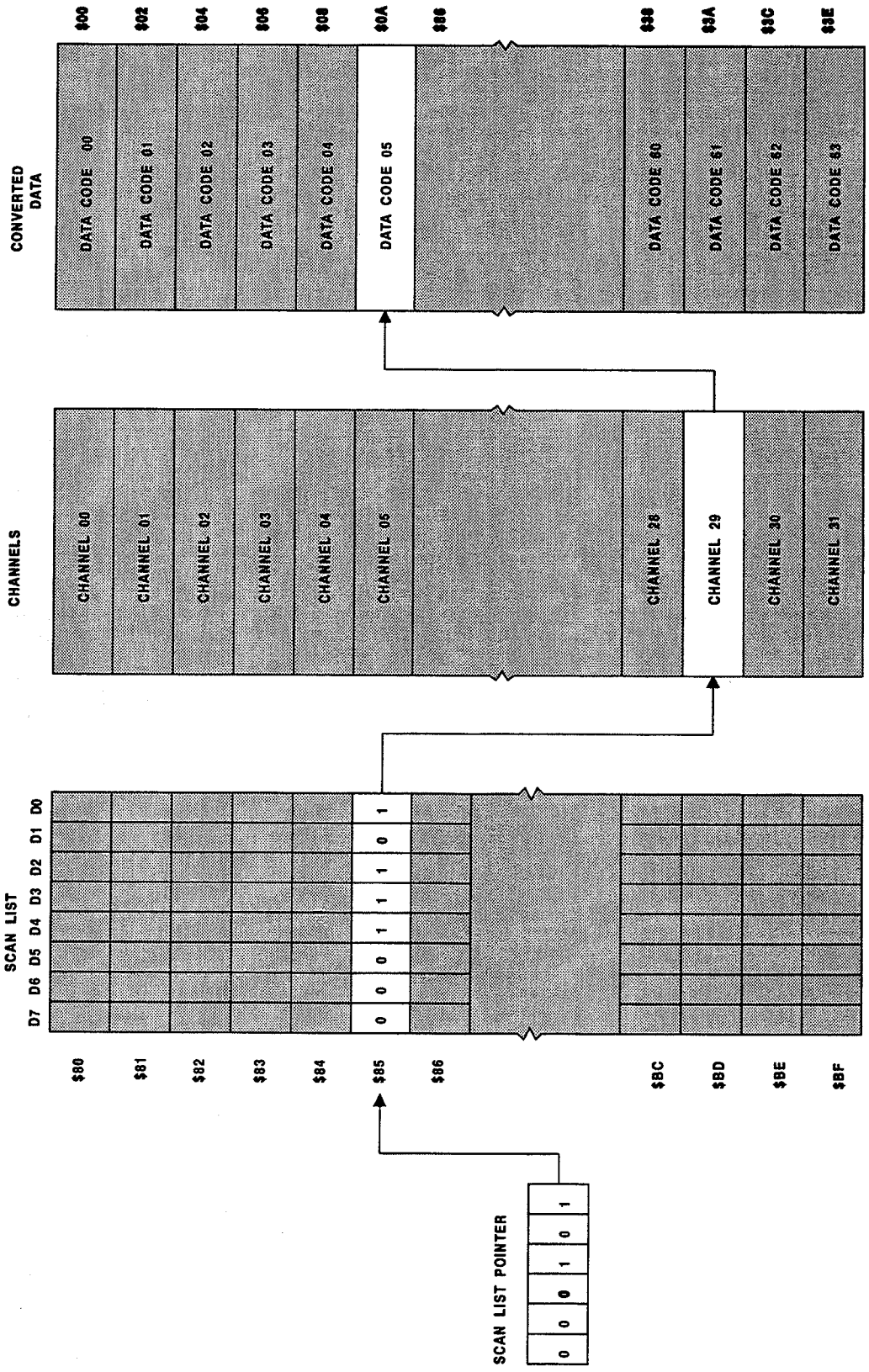
The relationship between the Scan List and Converted Data storage is illustrated in Figures 33 and 34. A list of Valid Scan List Addresses and Converted Data Storage Addresses is provided in Table 6.

Figure 33 - Converted Data Storage



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Figure 34 - Converted Data Storage



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Chapter 6 - Operating the AIP-1

Before attempting to operate the AIP-1 Analog Input Board in a VMEbus system, ensure that it has been configured as described in the preceding chapters.

Checklist

- Check that the hardware configurable options have been set (see Chapter 3)

  Base Address Selection - Jumpers E16 to E23 and E25 to E31

  AM Code Response - Jumper E24

  Sign Extension/Oversampling Response - Jumper E11

  Base Trigger Period - Jumper E2 to E9

  Single-ended/Differential Input Selection - Jumper E35

  Hardware Configurable Input Gain Selection - Jumper E14

  Input Range Selection - Jumpers E12, E13

  Output Code Selection - Jumper E10

  Programmable/Half flag E32

- Ensure that the AIP-1 has been inserted into the VMEbus system correctly and is fed by the correct signals (see Chapter 4).

- Check that the software configurable options have been set (see Chapter 5)

  Status/ID Byte - Control/Status Register 1

  AIP-1 Interrupt Response - Control/Status Register 1

  Continuous/Transient Mode - Control/Status Register 1

  Interrupt Level Selection - Control/Status Register 1

  Global Interrupt Enable - Control/Status Register 1

  Trigger Source Selection - Control/Status Register 3

  Internal Trigger Period Multiplier - Control/Status Register 4

- Ensure that the scan list elements have been programmed with the desired channel order and associated channel gains, stop bits (clearout unused stop bits).

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Initiating the Conversion Process

When the conversion process is initiated, the AIP-1 samples up to 32 analog voltages in an order defined by the contents of its Scan List (see 'Setting up the Scan List' section in Chapter 5) and at a rate determined by the selected trigger signal (see 'Control/Status Register 3 - Trigger Source Selection' in Chapter 5). Each sampled voltage is converted into an equivalent digital code, and this code is stored in the converted data memory before the next analog voltage is sampled. If the AIP-1 is operating in Continuous Mode this process is repeated continuously until the AIP-1 is halted.

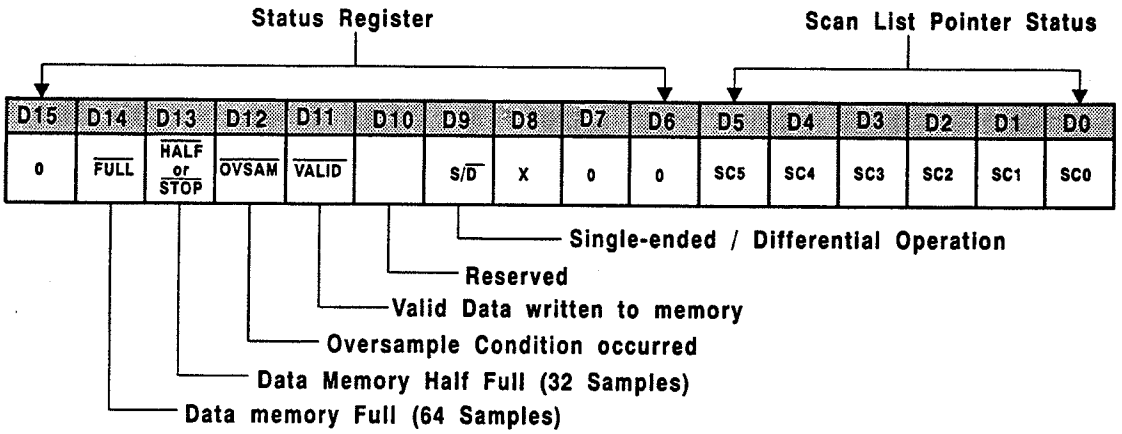
The conversion process is initiated by writing to any bit of Control/Status Register 2. It is recommended that the AIP-1 is started by clearing Control/Status Register 2.

Software Reset

Once the conversion process has been initialised, the AIP-1 may be reset at any time by issuing a software reset. This is performed by writing to any bit of Control/Status Register 2.

The Scan List Pointer is reset to $3C, all flags in Control/Status Register 2 are cleared, and the conversion process starts again at the first Scan List Element.

Figure 35 - Control/Status Register 2



The Front Panel LEDS

There are three LEDS on the front panel of the AIP-1, which provide a visual indication of the current status of the board.

Oversample LED

The middle LED is labelled "O/S" and will illuminate YELLOW whenever an oversample condition occurs, ie. whenever the sample rate exceeds 60kHz (16µS conversion period).

The **Oversample LED** will remain illuminated until the oversample condition is cleared, by altering the sample rate and issuing a software reset by writing to Control/Status Register 2.

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Halt LED

The lower LED is labelled "Halt" and will illuminate GREEN whenever the conversion process is halted.

If the AIP-1 is operating in Transient Mode the conversion process is automatically halted when 32 channels have been sampled, and the Halt LED is illuminated. The Halt LED will also be illuminated should the AIP-1 be halted for any reason before the last channel has been sampled. If the AIP-1 is operating in continuous mode, channels will be sampled continuously and the Halt LED will remain off unless some external event halts the AIP-1 artificially.

SYSFAIL LED

The top Fail LED illuminates RED on initial power up. Unless cleared under user control, this LED will remain illuminated (see Chapter 5 — Software Configuration).

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Operating the AIP-1 in Transient Mode

The AIP-1 Analog Input Board is configured to operate in Transient Mode by setting bit D11 of Control/Status Register 1 to logic 0.

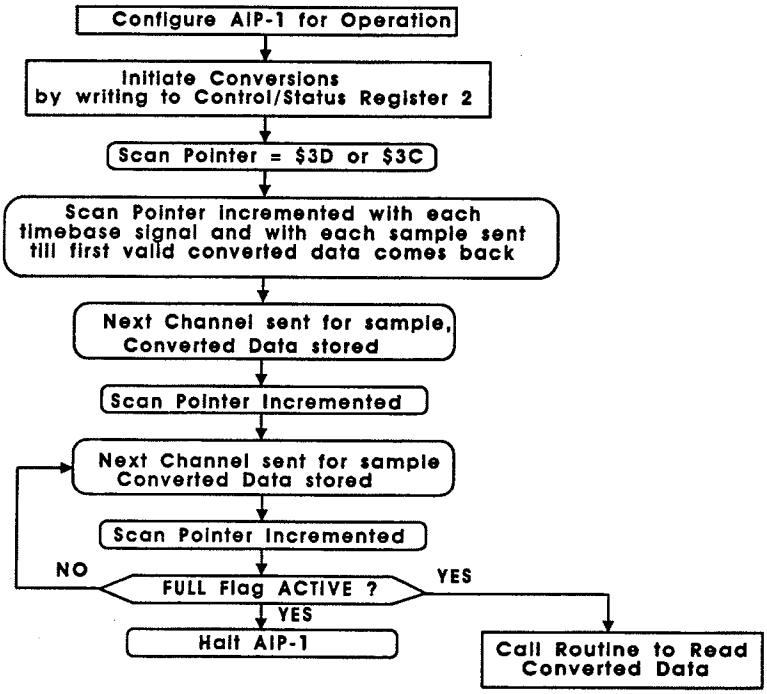
The conversion process is initiated by writing to Control/Status Register 2. 64 channels are sampled in an order defined by the contents of the Scan List and each sampled voltage is converted to an equivalent digital code which is stored in one of the converted data memory locations before the next channel is sampled.

When the last channel (defined in Scan List Element 63) has been sampled, the FULL Flag (bit D14 in Control/Status Register 2) is activated and the AIP-1 automatically halts. The AIP-1 will remain in this state, with the Halt LED illuminated, until a software reset is issued (by writing to Control/Status Register 2) or a hardware reset is performed. A software or hardware reset performed either when the AIP-1 is halted, or when the AIP-1 is still sampling input channels, resets the Scan List Pointer to 00 and clears all the flags in Control/Status Register 2. Following a sofware reset the conversion process begins again at Scan List Element 00.

The activation of the FULL flag may be detected by polling Control/Status Register 2, or by configuring the AIP-1 to generate an interrupt in this event. Once the FULL flag is detected, the CPU may read all the digital codes contained within the converted data memory as a single block of data. Reading the converted data clears the FULL flag.

The sequence of events which occur when the AIP-1 is operating in Transient Mode are illustrated in Figures 36 and 38.

Figure 36 - Polling the AIP-1 in Transient Mode



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Operating the AIP-1 in Continuous Mode

The AIP-1 is configured to operate in Continuous Mode by setting bit D11 in Control/Status Register 1 to Logic 1.

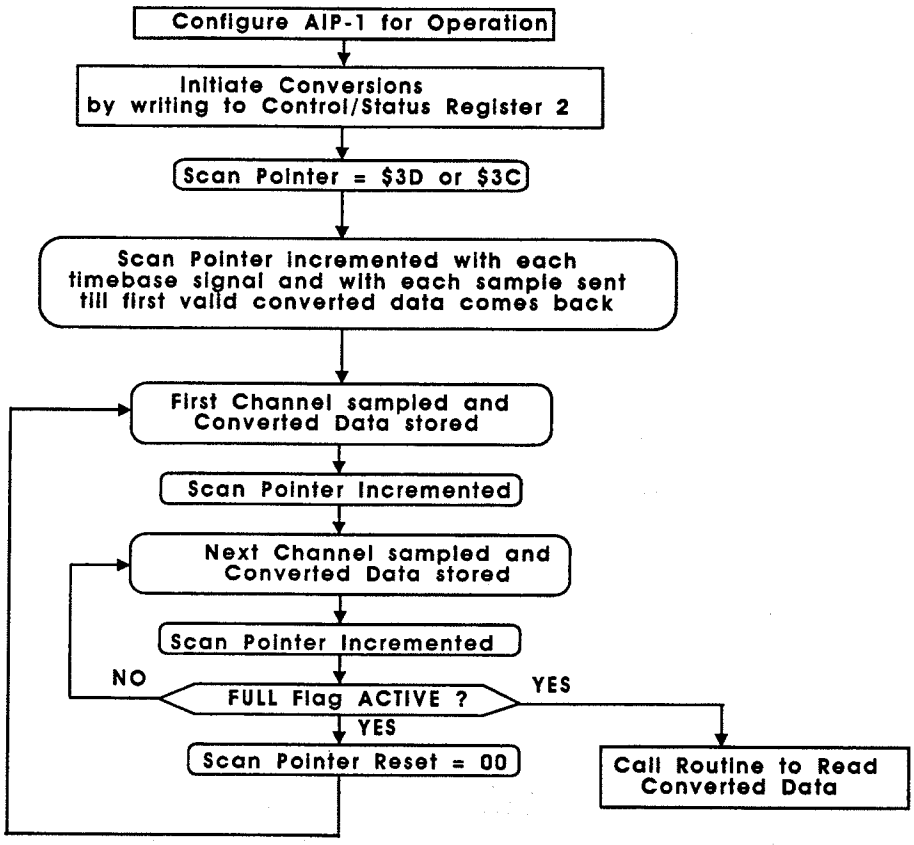
At first, the AIP-1 operating in Continuous Mode behaves exactly as it did in Transient Mode. The conversion process is initiated by writing to Control/Status Register 2, and the AIP-1 samples the channels in the order defined in the Scan List. The difference occurs when the 64th channel is sampled. When the AIP-1 is operating in Continuous Mode, the Scan List Pointer is reset each time all 64 channels are sampled, and the conversion process is repeated.

Each time the first Scan List Element is accessed, the resulting converted data is stored in the first converted data memory location. As a result, the AIP-1 starts to overwrite previously stored data whenever the Scan List Pointer is reset to 00.

To avoid losing essential data when operating in Continuous Mode, therefore, the converted data must be read before the last channel is sampled.

A sequence controlled by detecting the activation of the HALF- FULL flag (bit D13 of Control/Status Register 2) and the FULL flag (bit D14 of Control/Status Register 2) is used to ensure that valid data is read before it may be overwritten. This sequence of events is illustrated in Figures 37 and 39.

Figure 37 - Polling the AIP-1 in Continuous Mode



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Operating the AIP-1 in Interrupt Mode

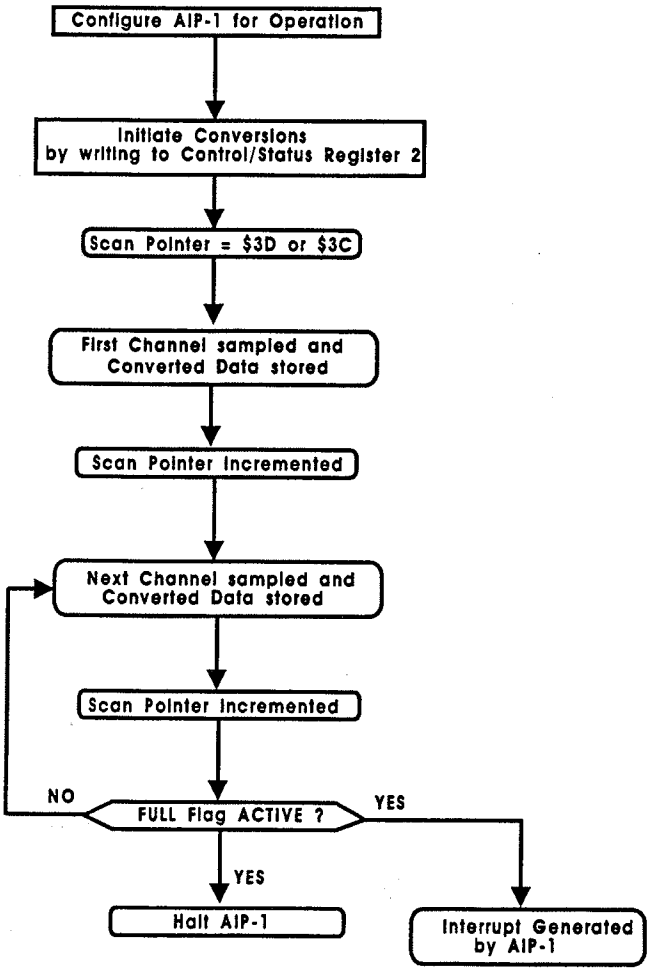
The AIP-1 is configured to operate in Interrupt Mode by setting bit D15 in Control/Status Register 1 to Logic 0.

When configured in this mode, the AIP-1 generates an interrupt on the VME Priority Interrupt Bus each time a specific event occurs. The full interrupt response (interrupt source, interrupt level, status/ID Byte, etc.) of the AIP-1 should be defined in Control/Status Register 1 before the conversion process is initiated (see 'Control/Status Register 1 - Interrupt Response' in Chapter 5).

There are three event combinations, one of which may be selected to result in the generation of an interrupt.

Interrupts may therefore be used to synchronise access to the converted data so that it is not overwritten.
Note : After an interrupt is generated, all further interrupts are disabled until the CPU services the original interrupt.

Figure 38 - Using Interrupts in Transient Mode

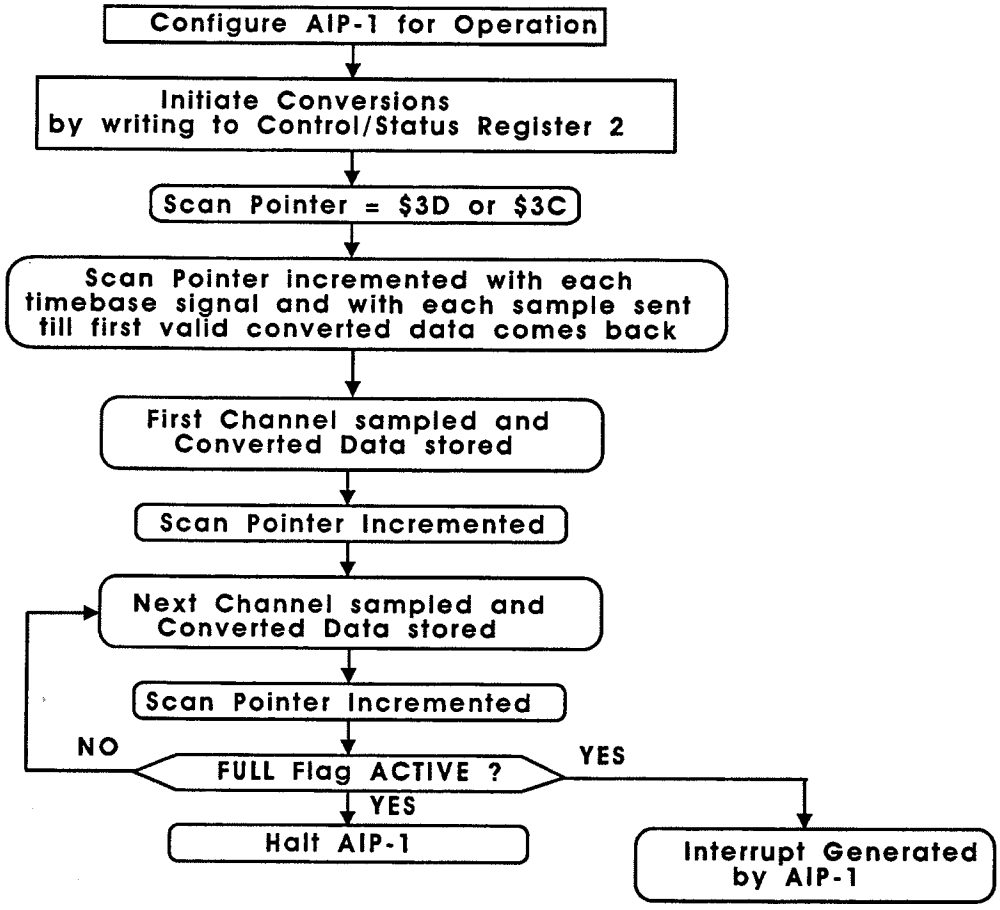


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When an interrupt is generated in response to the activation of the HALF-FULL Flag, the first 32 words of converted data must be read to clear the flag and to enable further interrupts. The process of using interrupts to control the AIP-1 operating in either Transient or Continuous Mode is illustrated in Figures 38 and 39.

In transient mode, when an interrupt is generated in response to the activation of the FULL flag, the second 32 words of converted data should be read and if required a software reset issued (by writing to Control/Status Register 2) to clear the flag and to enable further interrupts.

Figure 39 - Using Interrupts in Continuous Mode



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Operating the AIP-1 in Polling Mode

The AIP-1 is configured for operation in Polling Mode by setting Bit D15 in Control/Status Register 1 to Logic 1.

The CPU is able to detect that the converted data memory is either Half-full or Full, by polling bit D13 (half-full) or if link selected,the programmed stop bit and bit D14 (full) in Control/Status Register 2.

Both flags are cleared by the action of reading converted data, however, the FULL flag is inhibited by an active HALF-FULL flag. To ensure the correct operation of the AIP-1 in Polling Mode, it is therefore essential that, once the HALF-FULL flag is activated, the first 32 words of converted data are read before the converted data memory becomes full.

The process of polling the AIP-1 in Transient Mode is illustrated in Figure 40 and the process of polling the AIP-1 in Continuous Mode is illustrated in Figure 39.

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Chapter 7 - Reading the Analog Inputs

Before attempting to access the input data acquired by the AIP-1 Analog Input Board it must be configured and the conversion process initiated as described in the earlier chapters of this Manual.

Checklist

- Ensure that the hardware configurable options have been set (see Chapter 3)
- Ensure that the software programmable options have been set (see Chapter 5)
- Ensure that the Scan List has been programmed (see Chapter 5)
- Ensure that the conversion process has been initiated by writing to Control/Status Register 2 (see Chapter 5 and Chapter 6)

Converting Analog Voltages to Digital Codes

As each channel is sampled, the instantaneous analog voltage is held, and converted to a digital code by a 12 bit analog to digital converter. The exact relationship between the instantaneous analog input voltage and the digital output code is dependent on the output code format selected (see Chapter 3).

There are three coding scheme options :

Straight binary for the unipolar range (0 - 10V)

Offset binary for the bipolar ranges (±5V and ±10V)

Two's complement for the bipolar ranges (±5V and ±10V)

Figures 40, 41 and 42 illustrate the graphical relationship that exists between each of the coding schemes and the analog input voltage.

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Figure 40 - Straight Binary Coding

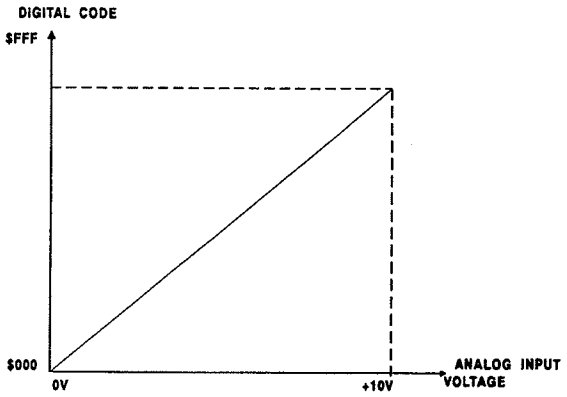


Figure 41 - Offset Binary Coding

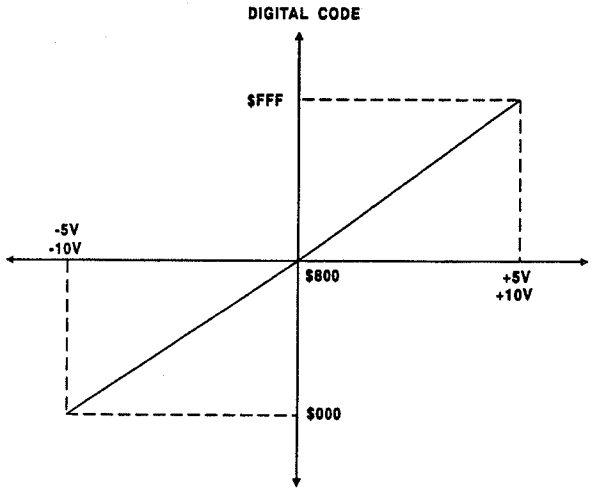
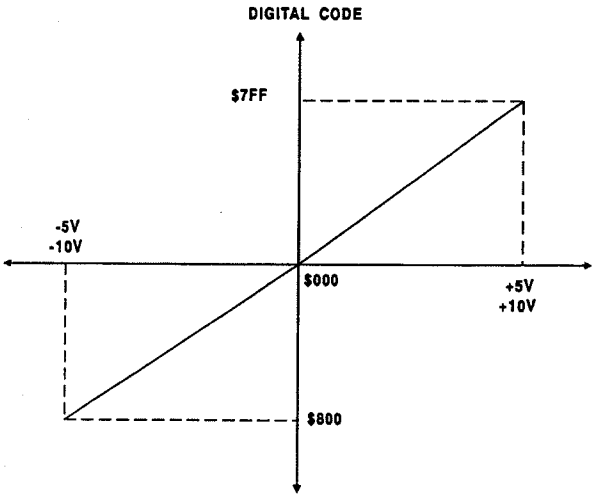
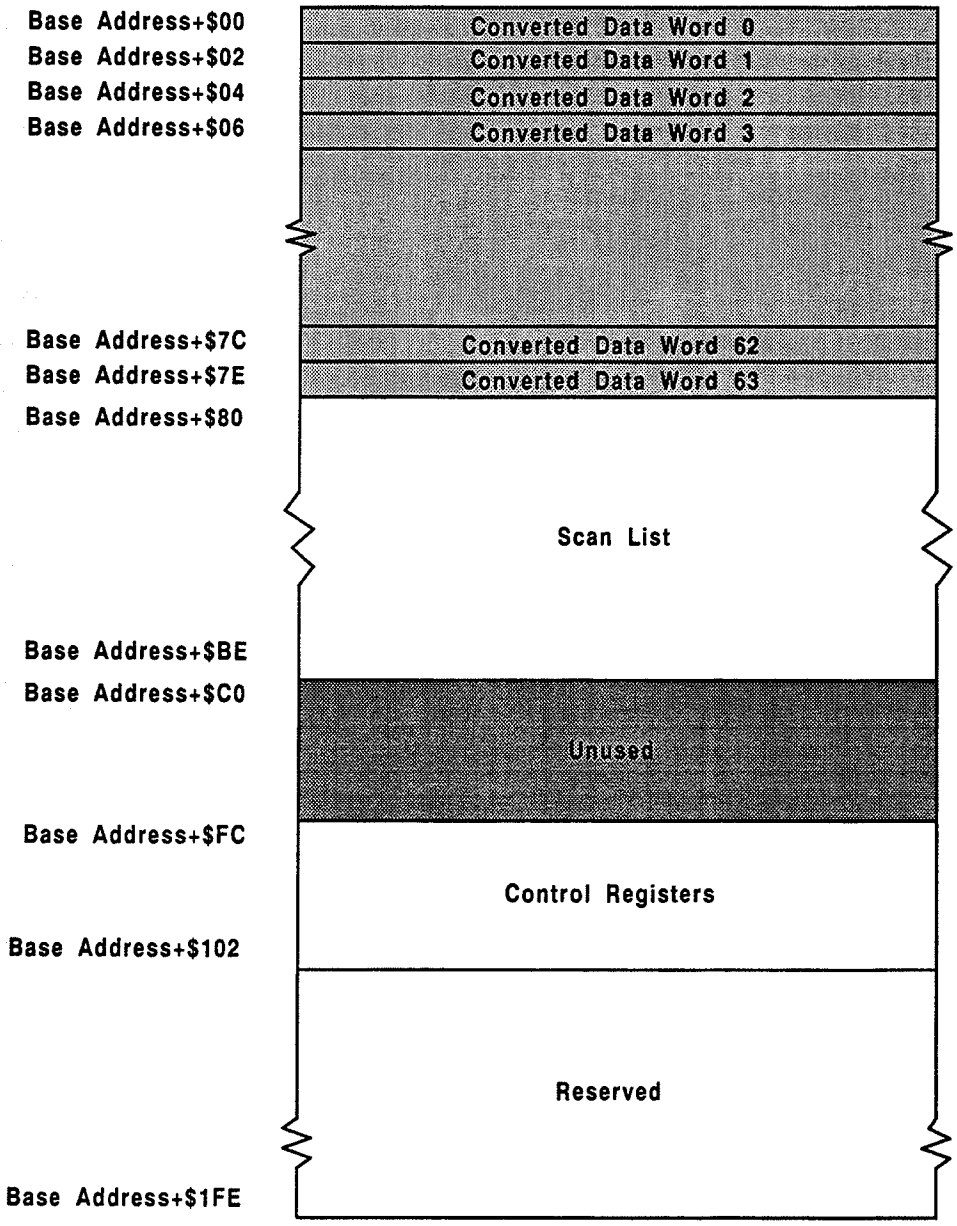


Figure 42 - Two's Complement Coding



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Figure 43 - Memory Map showing Converted Data Memory



Converted Data Storage

The 12 bit digital codes representing the analog input voltages are stored in 64 x 16 bit word locations between Base Address +$00 and Base Address + $7F.

Each Scan List Element has a unique location in the converted data memory associated with it, and this relationship is illustrated in Figure 44 and summarised in Table 18 overleaf.

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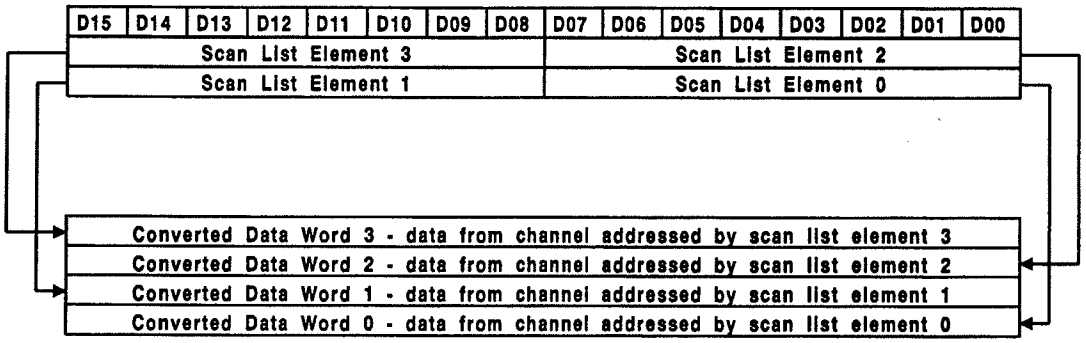
Table 18 - Valid Scan List Addresses

Scan List Element	Scan List Element Address	Converted Data Storage Address
$00	Base+$80	Base+$00
$01	Base+$81	Base+$02
$02	Base+$82	Base+$04
$03	Base+$83	Base+$06
$04	Base+$84	Base+$08
$05	Base+$85	Base+$0A
$06	Base+$86	Base+$0C
$07	Base+$87	Base+$0E
$08	Base+$88	Base+$10
$09	Base+$89	Base+$12
$0A	Base+$8A	Base+$14
$0B	Base+$8B	Base+$16
$0C	Base+$8C	Base+$18
$0D	Base+$8D	Base+$1A
$0E	Base+$8E	Base+$1C
$0F	Base+$8F	Base+$1E
$10	Base+$90	Base+$20
$11	Base+$91	Base+$22
$12	Base+$92	Base+$24
$13	Base+$93	Base+$26
$14	Base+$94	Base+$28
$15	Base+$95	Base+$2A
$16	Base+$96	Base+$2C
$17	Base+$97	Base+$2E
$18	Base+$98	Base+$30
$19	Base+$99	Base+$32
$1A	Base+$9A	Base+$34
$1B	Base+$9B	Base+$36
$1C	Base+$9C	Base+$38
$1D	Base+$9D	Base+$3A
$1E	Base+$9E	Base+$3C
$1F	Base+$9F	Base+$3E

Scan List Element	Scan List Element Address	Converted Data Storage Address
$20	Base+$A0	Base+$40
$21	Base+$A1	Base+$42
$22	Base+$A2	Base+$44
$23	Base+$A3	Base+$46
$24	Base+$A4	Base+$48
$25	Base+$A5	Base+$4A
$26	Base+$A6	Base+$4C
$27	Base+$A7	Base+$4E
$28	Base+$A8	Base+$50
$29	Base+$A9	Base+$52
$2A	Base+$AA	Base+$54
$2B	Base+$AB	Base+$56
$2C	Base+$AC	Base+$58
$2D	Base+$AD	Base+$5A
$2E	Base+$AE	Base+$5C
$2F	Base+$AF	Base+$5E
$30	Base+$B0	Base+$60
$31	Base+$B1	Base+$62
$32	Base+$B2	Base+$64
$33	Base+$B3	Base+$66
$34	Base+$B4	Base+$68
$35	Base+$B5	Base+$6A
$36	Base+$B6	Base+$6C
$37	Base+$B7	Base+$6E
$38	Base+$B8	Base+$70
$39	Base+$B9	Base+$72
$3A	Base+$BA	Base+$74
$3B	Base+$BB	Base+$76
$3C	Base+$BC	Base+$78
$3D	Base+$BD	Base+$7A
$3E	Base+$BE	Base+$7C
$3F	Base+$BF	Base+$7E

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Figure 44 - Converted Data Memory Addressing



Accessing Converted Data

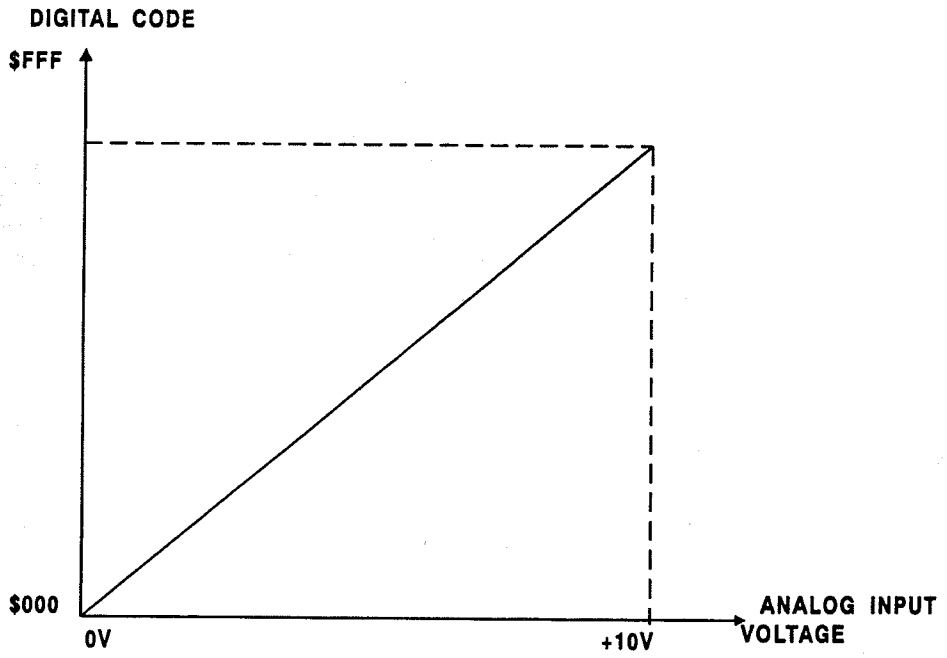
Dual port memory allows direct access to the converted data stored by the AIP-1. Data is read using word accesses across the VMEbus.

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Interpreting Straight Binary Codes

A simple graphical relationship exists between the analog input voltage and the straight binary coding scheme as illustrated in Figure 45 and Table 19.

Figure 45 - Straight Binary Coding



The mathematical equation relating analog input voltages to straight binary codes is :

Input Voltage = (10 x Code)/(4096 x Gain)

where

Code = the decimal equivalent of the digital output code

Gain = the overall input gain (channel gain x input gain)

Table 19 - Straight Binary Code Examples

0 - 10 V Scale

	Voltage	Code	Resolution
Negative Full Scale	0	$000	2.44mV
Midscale	+5V	$800	2.44mV
Positive Full Scale	+9.9976	$FFF	2.44mV

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Example 1 - straight binary

An analog input voltage in the range 0 - 10V is applied to an input channel with a channel gain of x1, and an input gain of x1. The AIP-1 generates a digital output code of $3FF. The corresponding input voltage may be calculated as follows :

Code = decimal equivalent of $FF = 1023 decimal

Gain = channel gain x input gain = 1 x 1 = 1

Input Voltage = (10 x 1023) / (4096 x 1) = 2.498V

Example 2 - straight binary

An analog input voltage in the range 0 - 10V is applied to an input channel with a channel gain of x10 and an input gain of x1. The AIP-1 generates a digital output code of 800H.

The corresponding input voltage may be calculated as follows :

Code = decimal equivalent of $800 = 2048 decimal

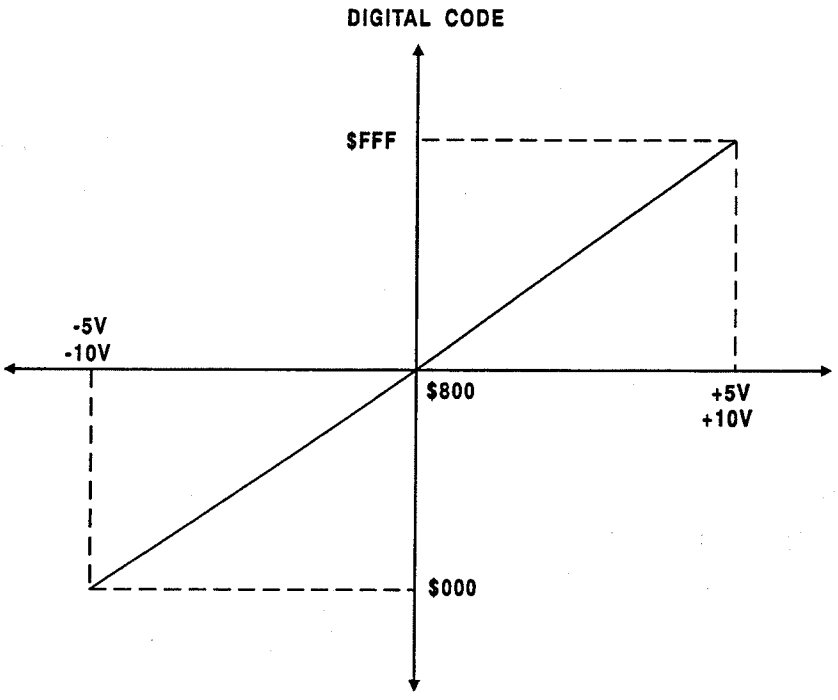
Gain = channel gain x input gain = 10 x 1 = 10

Input Voltage = (10 x 2048) / (4096 x 10) = 0.5V

Interpreting Offset Binary Codes

A simple graphical relationship exists between the analog input voltage and the offset binary coding scheme as illustrated in Figure 46 and Table 20.

Figure 46 - Offset Binary Coding



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Table 20 - Offset Binary Code Examples

±5V Scale

	Voltage	Code	Resolution
Negative Full Scale	-5V	$000	2.44mV
Midscale	0V	$800	2.44mV
Positive Full Scale	+4.9976	$FFF	2.44mV

±10V Scale

	Voltage	Code	Resolution
Negative Full Scale	-10V	$000	4.88mV
Midscale	+0V	$800	4.88mV
Positive Full Scale	+9.9951	$FFF	4.88mV

The mathematical equation relating analog input voltages to offset binary codes is :

Input Voltage x Gain = ((2 x R_{max} x Code)/(4096)) - Range

where

Code = the decimal equivalent of the digital output code

Gain = the overall input gain (channel gain x input gain)

Rmax = 5 for ±5V range and 10 for ±10V

Range = 5 for ±5V and 10 for ±10V

Example 3 - offset binary

An analog input voltage in the range ±10V is applied to a channel with an input gain of x10 and a channel gain of x10. The AIP-1 generates an output code of $FFF. The corresponding input voltage may be calculated as follows :

Code = decimal equivalent of $FFF = 4095 decimal

Gain = channel gain x input gain = 10 x 10 = 100

R_{max} = 10 for ±10V range

Range = 10 for ±10V range

Input Voltage x 100 = ((2 x 10 x 4095) / 4096) - 10 = 9.9951V

Input Voltage = 9.9951/100 = 99.95mV

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Example 4 - offset binary

An analog input voltage in the range ±5V is applied to a channel with an input gain of x1 and a channel gain of x100. The AIP-1 generates an output code of $0FE. The corresponding input voltage may be calculated as follows :

Code = decimal equivalent of $0FE = 254 decimal

Gain = channel gain x input gain = 1 x 100 = 100

R_{max} = 5 for ±5V range

Range = 5 for ±5V range

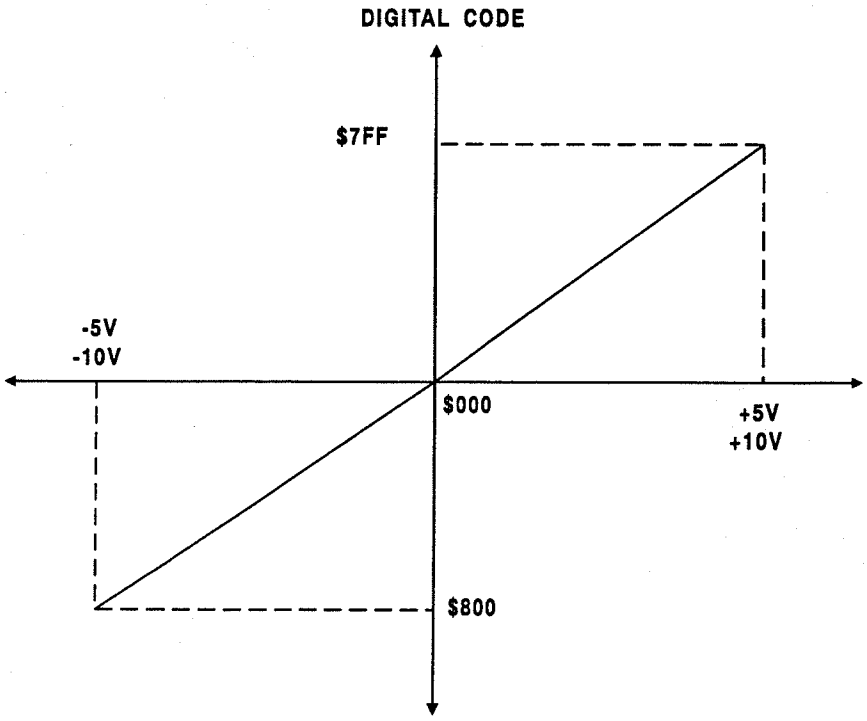
Input Voltage x 100 = ((2 x 5 x 254) / 4096) - 5 = -4.3799V

Input Voltage = -4.3799/100 = 43.799mV

Interpreting Twos Complement Codes

A simple graphical relationship exists between the analog input voltage and the two's complement coding scheme as illustrated in Figure 47 and Table 21.

Figure 47 - Two's Complement Coding



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Table 21 - Twos Complement Code Examples

±5V Scale

	Voltage	Code	Resolution
Negative Full Scale	-5V	$000	2.44mV
Midscale	0V	$800	2.44mV
Positive Full Scale	+4.9976	$FFF	2.44mV

±10V Scale

	Voltage	Code	Resolution
Negative Full Scale	-10V	$000	4.88mV
Midscale	+0V	$800	4.88mV
Positive Full Scale	+9.9951	$FFF	4.88mV

There are two mathematical equations relating analog input voltages to two's complement codes, dependent on the value of the most significant bit :

for msb = 1,

equation 1 : Input Voltage = (2/Gain) x (R_{max} x Code/4096) - R_{max}

for msb = 0

equation 2 : Input Voltage = (2 x R_{max} x Code)/(Gain x 4096)

where

Code = the decimal equivalent of the digital output code

Gain = the overall input gain (channel gain x input gain)

Rmax = 5 for ±5V range and 10 for ±10V

Example 5 - two's complement

An analog input voltage in the range ±10V is applied to a channel with an input gain of x1 and a channel gain of x1. The AIP-1 generates an output code of $800. The corresponding input voltage may be calculated as follows :

Code = decimal equivalent of $800 = 254 decimal

msb = 1, therefore equation 1 applies

Gain = channel gain x input gain = 1 x 1 = 1

R_{max} = 10 for ±10V range

Input Voltage = (2 x10 x 2048)/(1 x 4096) - 10 = -10V

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Example 6 - two's complement

An analog input voltage in the range ±5V is applied to a channel with an input gain of x10 and a channel gain of x1. The AIP-1 generates an output code of $7FF. The corresponding input voltage may be calculated as follows :

Code = decimal equivalent of $7FF = 2047 decimal

msb = 0, therefore equation 2 applies

Gain = channel gain x input gain = 10 x 1 = 10

R_{max} = 5 for ±5V range

Input Voltage = (2 x5 x 2047)/(10 x 4096) = 0.49976V

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Appendix A - AIP1 Code Examples

The following examples are source code for a C compiler

AIP-1 Example Code 1

*/This program sets the AIP-1 card to run in transient mode with the internal timer selected. It polls the VALID DATA flag to determine the start of sampling, then uses the HALF and FULL flag to indicate the availability of converted data.

The converted data is fetched when ready, and is stored in data_array

/*

```
# define BASE_ADDRESS        0x1C00000 /* for CPU-1A VME access          */
# define CONV_DATA           (BASE_ADDRESS + 0x000)
# define SCAN_ADDR           (BASE_ADDRESS + 0x080
# define TIMER               (BASE_ADDRESS + 0x0FC)
# define TRIGGER             (BASE_ADDRESS + 0x0FE)
# define CONTROL_REG         (BASE_ADDRESS + 0x100)
# define STATUS_REG          (BASE_ADDRESS + 0x102)
# define SOFT_TRIGGER        0
# define INTERNAL_TRIG       1
# define EXTERNAL_TRIG       2
# define EVENT_TRIGGER       3
# define VALID_DATA_BIT      0x800
# define HALF_FLAG_BIT       0x2000
# define FULL_FLAG_BIT       0x4000
# define TRANSIENT_MODE      0
# define ARRAY_LENGTH        64
typedef unsigned char        Uchar;
typedef unsigned short       Ushort;
typedef unsigned long        Ulong;
unsigned short status;       /*output of board status register          */
unsigned short converted_array[ARRAY_LENGTH];
unsigned short test_word;    /* word sent out to board                  */
```


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```
main()    {
/* The function proceeds as follows:
      Set up for a transient sample
      Initiate the sample
      Monitor the Status register looking first for VALID DATA then HALF
      flag
      Fetch first 32 samples
      Monitor the Status register looking for FULL flag
      Fetch last 32 samples
*/
int index;
            /* Fill up SCAN LIST */
for (index =0;index  64;index++)
      *((Uchar *) (SCAN_ADDR + index +1)) = 0;  /* channel 0, gain =1 */

            /* Initialise converted data array */
for (index = 0;index  ARRAY_LENGTH;index++ )
      converted_array[index] = 0;

            /* Set up sample parameters */
*((Ushort *) TIMER) = 100;   /* set up AIP TIMER                          */
*((Ushort *) TRIGGER) = 1;   /* set up TRIGGER select                     */
*((Ushort *) CONTROL_REG)= TRANSIENT_MODE; /* set control register */
*((Ushort *) STATUS_REG) = 0;                /* START SAMPLING           */

            /* Wait for Valid Data bit */
do {
      status = (*((Ushort *) STATUS_REG));    /* fetch status            */
      status = (status & VALID_DATA_BIT);   /* remove all but VALID DATABIT
      from status */
      } while (status != 0);  /* Flags in status register are active low */

                  /* Wait for HALF flag */
do {
      status = (*((Ushort *) STATUS_REG));      /* fetch status          */
      status = (status & HALF_FLAG_BIT);  /* remove all but HALF FLAGBIT
      from status */
      } while (status != 0);  /* Flags in status register are active low */
```


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```
            /* Get first 32 words of converted data */
for (index = 0;index  <32;index++) {
            /* read converted data */
      test_word = *((Ushort *) (CONV_DATA + index + index));
            /* store converted data */
      converted_array[index] = test_word;
}
            /* Wait for FULL flag */
do {
      status = (*((Ushort *) STATUS_REG));      /* fetch status          */
      status = (status & FULL_FLAG_BIT);  /* remove all but FULL FLAG BIT
      from status */
      } while (status != 0);  /* Flags in status register are active low */


            /* Get last 32 words of converted data */
for (index = 32;index  <64;index++) {
            /* read converted data */
      test_word = *((Ushort *) (CONV_DATA + index + index));
            /* store converted data */
      converted_array[index] = test_word;
      }
}
```


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AIP-1 Example Code 2

/*This program sets up the 1st 3 scan list elements to sample channel 0 with a gains of 1, then 10, then 100, and sets up the 4th scan list element to sample channel 0, but displays the result as a voltage.

This program sets the AIP-1 card to run in transient mode with the internal timer selected. It polls the VALID DATA flag to determine the start of sampling, then uses the HALF flag to indicate the availability of converted data.

```
*/
# define BASE_ADDRESS        0x1C00000 /* for CPU-1A VME access        */
# define CONV_DATA           (BASE_ADDRESS + 0x000)
# define SCAN_ADDR           (BASE_ADDRESS + 0x080)
# define TIMER               (BASE_ADDRESS + 0x0FC)
# define TRIGGER             (BASE_ADDRESS + 0x0FE)
# define CONTROL_REG         (BASE_ADDRESS + 0x100)
# define STATUS_REG          (BASE_ADDRESS + 0x102)
# define SOFT_TRIGGER        0
# define INTERNAL_TRIG       1
# define EXTERNAL_TRIG       2
# define EVENT_TRIGGER       3
# define VALID_DATA_BIT 0x800

# define HALF_FLAG_BIT 0x2000
# define FULL_FLAG_BIT 0x4000

# define TRANSIENT_MODE      0
# define CONTINUOUS_MODE 0x800
# define ARRAY_LENGTH 64
# define CONVERSION_FACTOR1 (20000000/4096) /* microvolts per resolution */

      /* The above value is true only for an ADC input configuration of
      +10 Volts to -10 Volts */

# define CONVERSION_FACTOR2 (10000000/4096) /* microvolts per resolution*/

       /* The above value is true only for an ADC input configuration of 0
      to +10 Volts */

typedef unsigned char       Uchar;

typedef unsigned short      Ushort;

typedef unsigned long       Ulong;

unsigned short status;      /* output of board status register */

unsigned short converted_array[ARRAY_LENGTH];

unsigned short test_word;                  /* word sent out to board     */

unsigned short returned_word;              /* word returned from board   */

unsigned char test_byte;                   /* byte sent out to board     */

unsigned char returned_byte;               /* byte returned from board   */

char  key;
```


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/* Function to convert from 12 bit signed integer to long integer */

```
convert_toint(temp)
int temp;

      {
      int extended;

      if (temp> = 0x800) {                /* (exclude positive numbers) */
            extended = (temp & 0xF000);/* look for wrong extended value */
            if (extended != 0xF000) {
                  printf("ERROR in extended sign, data returned = %x",temp);
                  printf("\n Press any key to continue; \n");
                  key = getchar();              /* pause screen   */
                  temp = (temp | 0xF000); /* correct the value before
                  returning */
                  }
            temp = temp | -4096;     /* converted data is now in temp */
            }
      return(temp);
      }
```

/* Function to convert from a HEX integer (assumed to represent a voltage value) to a millivolt based decimal number where the ADC input range is -10 Volts to +10 Volts */

```
conv_to_millvlts1(temp)
int temp;

      {
      temp = temp * CONVERSION_FACTOR1;
      temp = temp / 1000;
      return(temp);
      }
```

/* Function to convert from a HEX integer (assumed to represent a voltage value) to a millivolt based decimal number where the ADC input range is 0 to +10 Volts */

```
conv_to_millvlts2(temp)
int temp;

      {
      temp = temp * CONVERSION_FACTOR2;
      temp = temp / 1000;
      return(temp);
      }
```


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CALIBRATION DISPLAY PROCEDURE

/* Only ADC gain calibration can be carried out. The instrumentation amplifiers are programmed with fixed gain resistors, therefore amplifier gain calibration does not exist */

```
calibrate() {

int count,index,answer;

      printf("\n");

      printf("\n  ------------------------------------------");

      printf("\n  CALIBRATION PROCEDURE - Display facility");

      printf("\n  ------------------------------------------");
      printf("\n");

      printf("\n");

      printf("\n Enter 1    for 0 to +10 Volts or -5 to +5 Volts input
      range");

      printf("\n Enter 2    for -10 Volts to +10 Volts input range");

      printf("\n\n    Enter required option   ");

      key = getchar();                          /* pause screen   */

      key = getchar();  printf("\n");

/*            SAMPLE AND DISPLAY RELEVANT CONVERTED DATA                */
                  /* Set up sample parameters */

*((Ushort *) TIMER) = 250;                  /* set up AIP TIMER */
*((Ushort *) TRIGGER) = INTERNAL_TRIG;      /* set up TRIGGER select */
*((Ushort *) CONTROL_REG) = TRANSIENT_MODE;/* set control register */

            /* Fill up scan list with chan zero, gain = 1 */

for (index =0;index  64;index++)

      *((Uchar *) (SCAN_ADDR + index)) = 0;  /* sample channel 0, gain=1 */

            /* Set up scan list - first 4 elements */

/* first element already done */

*((Uchar *) (SCAN_ADDR + 0)) = 0x00;        /* sample channel 0, gain=1 */
*((Uchar *) (SCAN_ADDR + 1)) = 0x40;        /* sample channel 0, gain=10 */
*((Uchar *) (SCAN_ADDR + 2)) = 0x80;        /* sample channel 0, gain=100 */
*((Uchar *) (SCAN_ADDR + 3)) = 0x00;        /* sample channel 0, gain=1 */

count = 0;

do {

                  /* Start sampling */

*((Ushort *) STATUS_REG) = 0;
```


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```
/* Wait for Valid Data bit */
do {
      status = (*((Ushort *) STATUS_REG));      /* fetch status */
      status = (status & VALID_DATA_BIT); /* remove all but VALID DATA BIT
      from status */
      } while (status != 0); /* Flags in status register are active low */
            /* Wait for FULL flag */
do {
      status = (*((Ushort *) STATUS_REG));      /* fetch status */
      status = (status & HALF_FLAG_BIT);  /* remove all but HALF FLAG BIT
      from status */
      } while (status != 0); /* Flags in status register are active low */
            /* read back converted data */
get_converted();
            /* display 1st 4 converted data results */
printf("Gain of 1 = %4x  ",(converted_array[0]));
printf("Gain of 10 = %4x  ",(converted_array[1]));
printf("Gain of 100= %4x  ",(converted_array[2]));
if (key == '1') {
      answer = (converted_array[3]) & 0x0FFF;
      printf("Source = %6d mv",(conv_to_millvlts2(answer)));
      }
if (key == '2') {
      answer = convert_toint(converted_array[3]);
      printf("Source = %6d mv",(conv_to_millvlts1(answer)));
      }
printf("\n");
count++;
} while (count  600);
}
```


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```
/*                          GET CONVERTED DATA                          */
get_converted() {
int index;
      for (index = 0;index < 64;index++)  /* initialise array */
            converted_array[index] = 0;
      for (index = 0;index < 64;index++) {
                  /* read converted data */
            test_word = *((Ushort *) (CONV_DATA + index + index));
                  /* store converted data */
            converted_array[index] = test_word;
            }
      }
/*                          MAIN ROUTINE                                */
```

/* The preceding program is arranged to give 600 lines of display then exit, this allows the program to be included in a general AIP-1 support program if required. The following function merely recalls the display as required */

```
main(){
      do    {
            calibrate();
            printf("\n Enter ~ to exit, any other key to continue\n");
            key = getchar();  /* pause screen   */
            } while (key != '~');
      }
```


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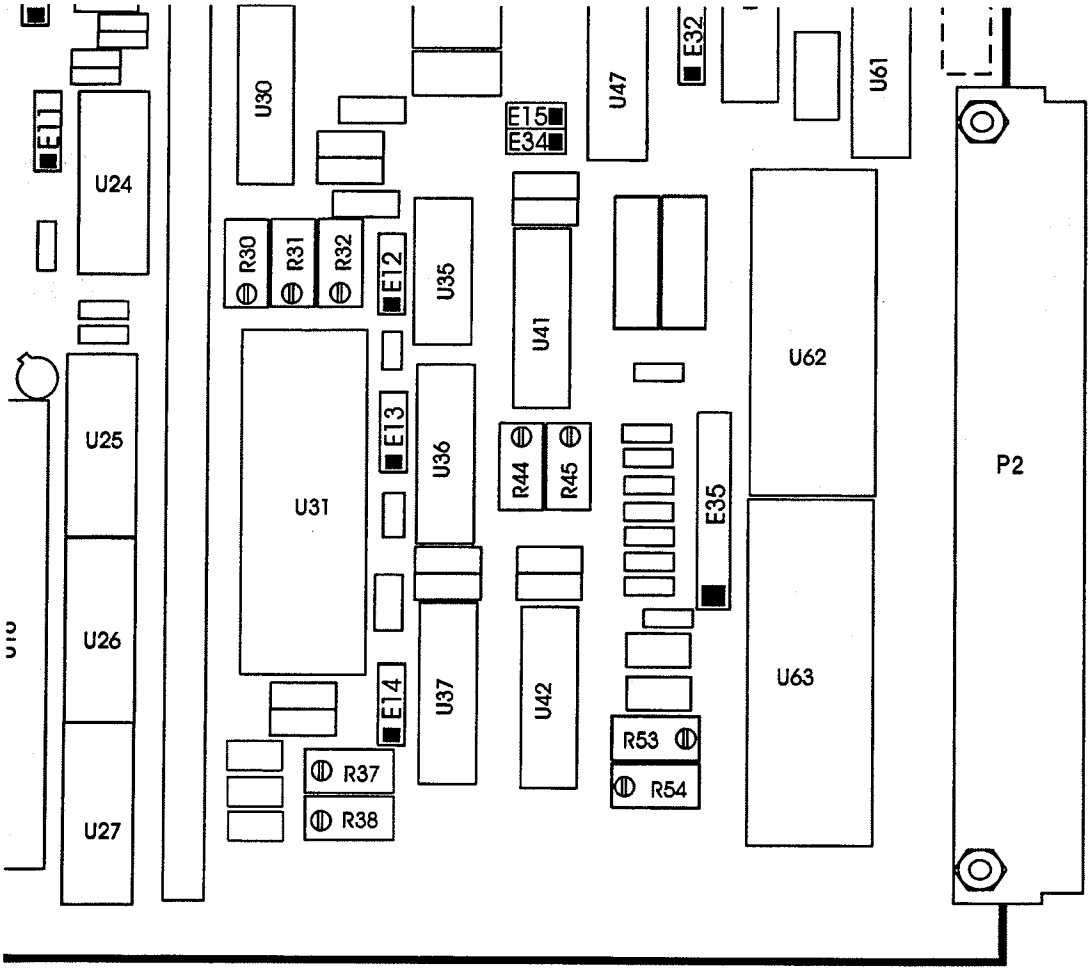
Appendix B - Calibration

Before attempting to calibrate the AIP-1, allow approximately 15 minutes after power-up to ensure that the board has reached its thermal equilibrium.

The calibration procedure requires a voltage source capable of 0.002% accuracy. (Alternatively, a less accurate voltage source may be used, provided it is monitored using a digital voltmeter capable of 0.002% accuracy.) Calibration is performed by applying known voltages to Channel 00 only. All other channels should be connected to analog GND.

Figure 48 shows the position of the potentiometers which should be adjusted as the calibration voltages are applied.

Figure 48 Calibration potentiometers



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The AIP-1 card has been designed to take advantage of the low drift characteristics available from instrumentation amplifiers. The long term offset and gain changes are not expected to be significant, and furthur calibration should not be necessary. Calibration is possible however using the procedure given below (Note that boards sealed with a conformal coat will become vulnerable to any atmospheric pollution and moisture ingress if the conformal coat is broken).

The calibration process requires constant monitoring of the converted data. The software program provided in Chapter 8 as Example program 2 is designed to carry out the necessary monitoring. When run, it provides 4 columns of data, each column being a necessary measurement used within the calibration procedure.

The calibration must be carried out in the sequence shown, otherwise offsets will simply move around rather than be eliminated.

The board assumes an initial configuration to which slight changes are made as the calibration proceeds.

Calibrating the board needs access to link E15, and to all the trimpots located in the analogue area adjacent to the P2 connector.

Initial Board Set Up

Channel 00 (In0) must be driven by a power supply capable of providing a voltage range of -10 Volts to +10 Volts, and monitored by a Digital Volt Meter capable of 0.002 % resolution over the same range. This power supply will be referred to as the voltage source.

Initial link configuration (the VME address, AM code select, and timebase prescaler are all assumed to be set up to working values and are not included here):

Remove any link on E14.

Fit the following push fit multiple links:

E10 pins 1 and 2	(sets 'straight binary')
E11 pins 2 and 3	(select 'sign')
E12 pins 2 and 3	(0 to 10 Volts)
E13 pins 2 and 3	(0 to 10 Volts)
E32 pins 2 and 3	(selects HALF flag)
E35 pins 2 and 3	(selects single ended inputs)
E35 pins 4 and 5	(selects single ended inputs)
E35 pins 6 and 7	(selects single ended inputs)

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Calibration Procedure

In the following procedure the ADC offset is Calibrated first, then Link Gain amplifier, then ADC Gain, then programmable amplifiers.

Calibrate ADC - Unipolar Range - Offset

Step 1 —Fit internal Gnd link E15

While monitoring channel 0 - adjust R30 through a decode of 2 down to a decode of 0, noting the amount of adjustment on the potentiometer required to move from 2 to 1. Then continue the adjustment into 0 by half this amount (if using sample 2 program, use the channel 0, gain = 1 display column). This calibrates the ADC w.r.t. the analogue 0 Volts.

Step 2 —Remove E15 link

Adjust the voltage source to +1.221mV.

Calibrate Link Gain Amplifier - Offset

Step 3 —Fit link E14 pins 2 and 3 (provides link selectable gain of X100)

Adjust R53 (input offset) until channel 0 has equal quantities of 0 and 1 (if using sample 2 program, use the channel 0, gain = 1 display column).

(If insufficient adjustment is available and this is the first time step 5 has been encountered, move on to step 4.)

Step 4 —Remove link E14 pins 2 and 3 (provides link selectable gain of X1)

Adjust R54 (O/P offset) until channel 0 has equal quantities of 0 and 1 (if using sample 2 program, use the channel 0, gain = 1 display column).

Repeat Steps 3 and 4, until no adjustment is necessary.

Calibrate ADC - Unipolar Range - Gain

Step 5 —Adjust the voltage source to +9.993 Volts

Adjust R32 until channel 0 shows equal quantities of $FFFE and $FFFF (if using sample 2 program, use the channel 0, gain = 1 display column, or use the right hand column and look for a matching voltage).

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Calibrate ADC - Bipolar Range - Offset

Step 6 —Set ADC to Bipolar -10 to +10 Volts (-5 to +5 Volts)

by moving: link at E10 pins 1+2 to E10 pins 2+3
link E12 pins 2+3 to E12 pins 1+2
link E13 pins 2+3 to E13 pins 1+2 (leave link)

Ensure links E14 and E15 are removed.

Step 7 —Adjust the voltage source to -9.9976 Volts (-4.9988 Volts)

Adjust R31 until channel 0 shows equal quantities of $8000 and $8001 (if using sample 2 program, use the channel 0, gain = 1 display column, or use the right hand column and look for a matching voltage).

Step 8 —Adjust the voltage source to +9.993 Volts (+4.9963 Volts)

Observe channel 0 which should show equal quantities of $07FE and $07FF (if using sample 2 program, use the channel 0, gain = 1 display column, or use the right hand column and look for a matching voltage).

Step 9 —Adjust the voltage source to +2.442 (+1.221mV)

Observe channel 0 which should show equal quantities of 0000 and 0001 (if using sample 2 program, use the channel 0, gain = 1 display column, or use the right hand column and look for a matching voltage).

Calibrate Programable Gain Of 10 Amplifier

Step 10 —Adjust the voltage source to +0.0mV

Adjust R45 (input offset) until channel 0 is midway through the 0 decode (if using sample 2 program, use the channel 0, gain = 1 display column).

(If insufficient adjustment is available adjust R44 instead.)

Calibrate Programable Gain Of 100 Amplifier

Step 11 —Retain the voltage source at +0.0mV

Adjust R37 (input offset) until channel 0 is midway through the 0 decode (if using sample 2 program, use the channel 0, gain = 1 display column).

(If insufficient adjustment is available adjust R38 instead.)

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Copies of circuit diagrams for this product may be obtained subject to a Confidentiality Agreement being made. For details please contact:

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