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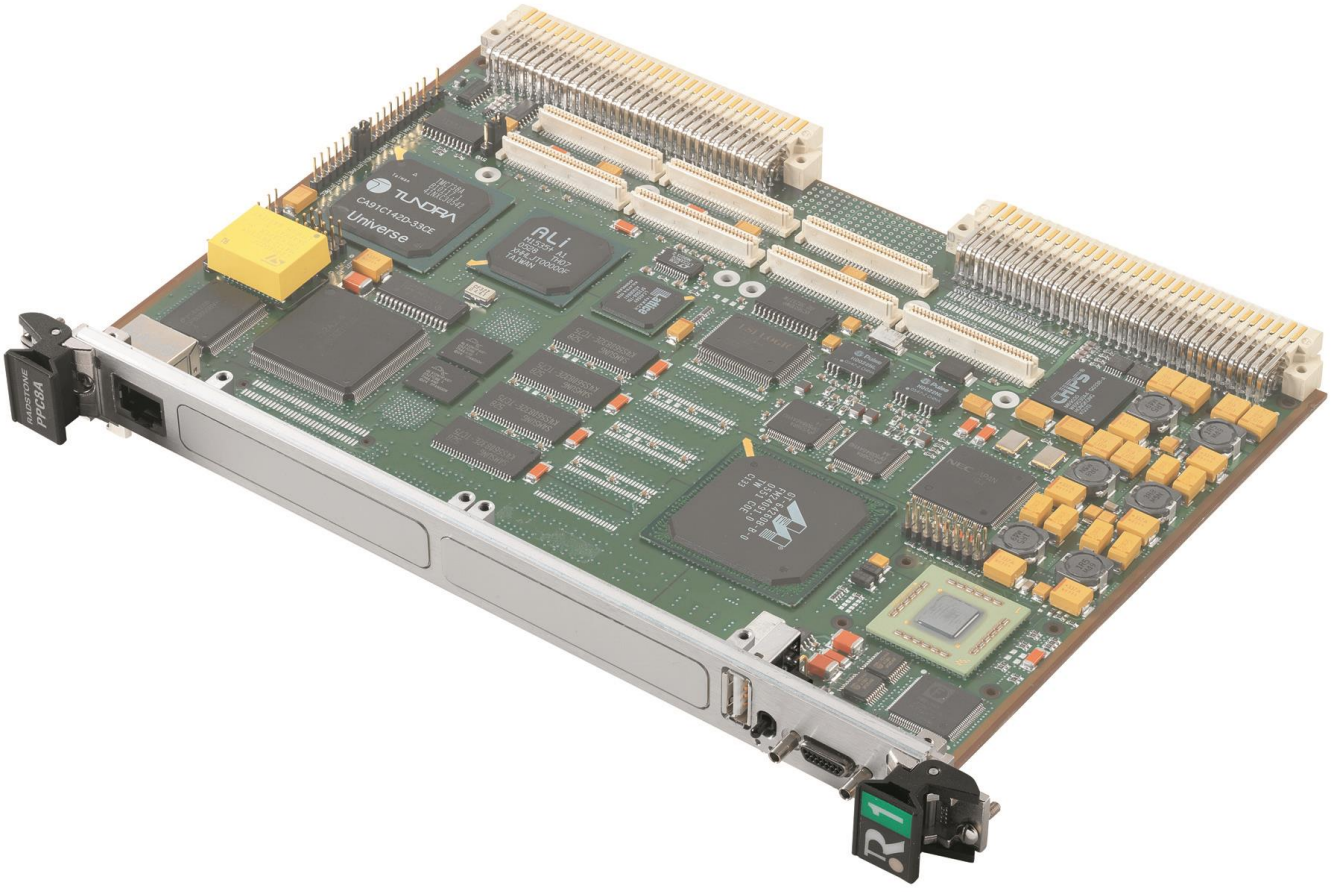
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Hardware Reference Manual

PPC8A 6U VME Single Board Computer

Edition 8DG

Publication No. PPC8A-0HH/8DG



abaco SYSTEMS

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Preface

This manual contains hardware details for the Abaco Systems PPC8A (Rev 4 & 5 Artwork) single board computer. The information contained in this document must be used in conjunction with the PowerX product Manual.



LINK

PowerX Range Hardware Reference Manual, publication PPC-0HH.

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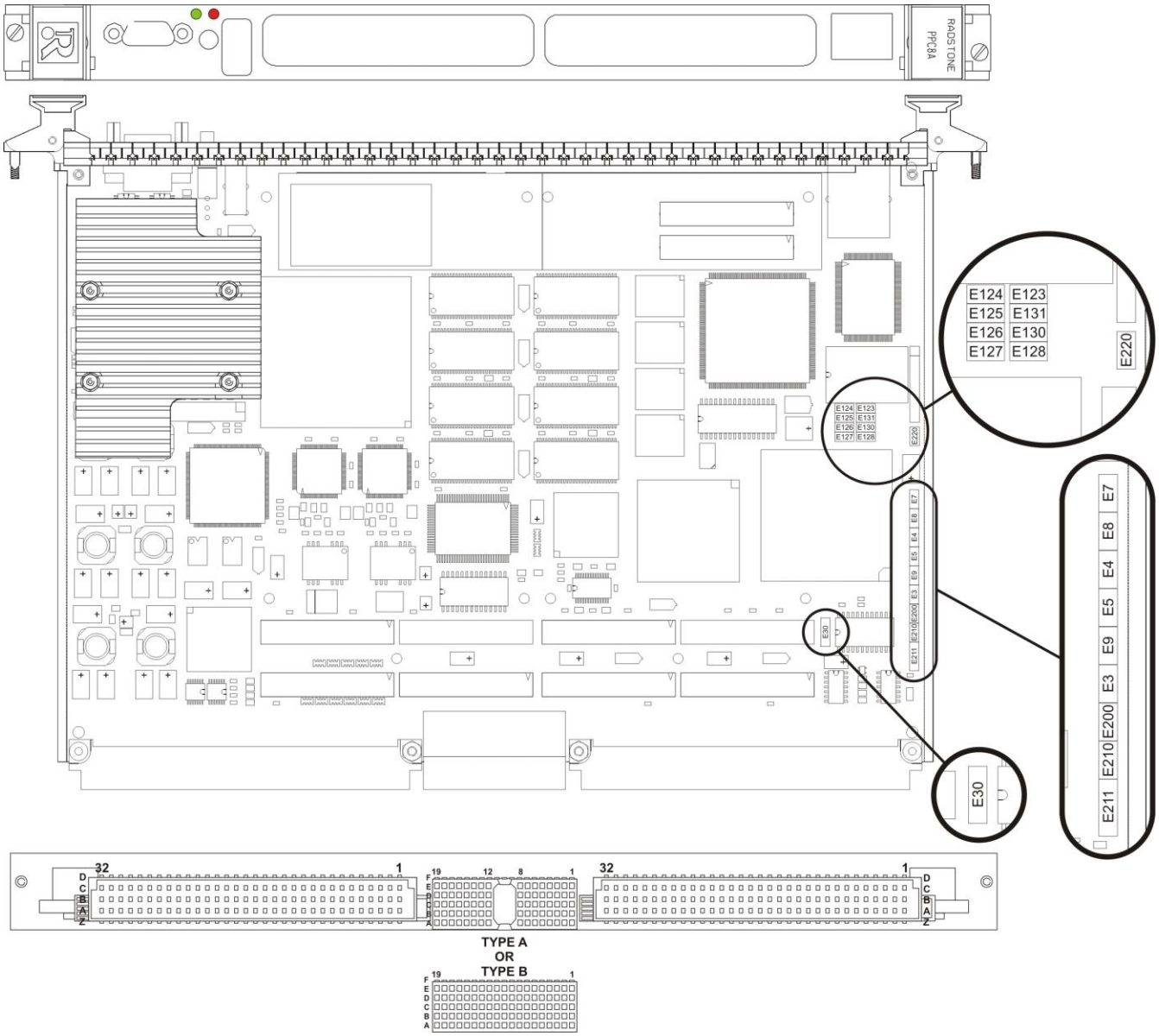
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1 • Link Settings

This section describes the configuration of link fields. The board is delivered with push-on jumpers.

Figure 1-1 Link Locations



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Table 1-1 Default Link Settings

Link	Setting	Silkscreen	Action
E30	Open	VIO	Used to select the PCI Signaling Voltage of the PMC sites If the PPC8A is powered-up with no jumper fitted on E30, it may remain in reset
E211	Open	None	This is for factory use only
E210	Open	NVWP	NVRAM areas write protect. When a jumper is fitted on this link, writes to both NVRAM areas are blocked
E200	Open	P1AW	Used to connect the Flash JTAG Autowrite signal between the backplane (P1) and the JTAG Scan Bridge
E3	Open	WRUR	User Flash Area Write Enable. Has no effect on hardware; software feature only
E9	Open	WRBT	Boot Flash Area Write Enable. Has no effect on hardware; software feature only
E5	Open	PWEN	Flash Protection Password Visibility Enable. Fitting a jumper on this link causes the Flash protection password to become visible to software in EPLD register space
E4	Open	BTVME	Boot From VME. Fitting a jumper on this link enables the PPC8A to be accessed from VME for programming purposes (holds the CPU in reset)
E8	Open	BTAT	Boot from Alternative Region. Changes the region from which Boot Code is fetched
E7	Open	BTREC	Boot from Recovery (BANC) Region. Changes the region from which Boot Code is fetched
E124	Open	SLOT_ID 3	Identification Link Bit 3 (no longer ORed with the Geographical Address bits from P1)
E125	Open	SLOT_ID 2	Identification Link Bit 2 (no longer ORed with the Geographical Address bits from P1)
E126	Open	SLOT_ID 1	Identification Link Bit 1 (no longer ORed with the Geographical Address bits from P1)
E127	Open	SLOT_ID 0	Identification Link Bit 0 (no longer ORed with the Geographical Address bits from P1)
E123	Open	ECC_REQ	SDRAM ECC Protect disable. If a jumper is fitted on this link, it instructs the software to disable ECC protection of the SDRAM banks (if the software supports this function)
E131	Open	JTAG_MODE	Enable JTAG Interface[a]
E130	Open	RST_EN	Front Panel Reset Switch Disable. If this field is linked, the front panel reset switch is disabled
E128	Open	SC_TRM	On-card SCSI Terminator Enable Request. SCSI Termination can be enabled by software if this link is open
E220	Open	LNKSEL	Geographical ID select If linked, the Geographical Address reported in the EPLD Registers is controlled from the IDENT_LINKS (E124-E127) rather than the Geographical Address bits from the P1 connector

a. If the JTAG interface is enabled, the TCK pin on P1 *must* be pulled low for the card to operate correctly.



TIPS

Before changing any of these link options, see the appropriate section(s) in the following pages.

If you are about to install your board and power-up for the first time, leaving your board in the default configuration (as above) – except link E30, will enable board operation to be proved before tackling any configuration issues.

1.1 Factory Use Only Link (E211)

These pins are for factory use only and must always be left unconnected.

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1.2 Flash Password Visibility Link (E5 (PWEN))

This link enables or disables the visibility of the password used by the Spansion (AMD) Flash Persistent Protection, Password Mode sector locking scheme. The link's function is ORed with the PASSW_EN_BP~ signal from P0-A2 and/or P2-Z1. See the Flash section for details of operation.

Table 1-2

Setting	Function
In	Password Visible
Out (default)	Password Hidden

1.3 Flash Write Enable Links (E3 (WRUR) and E9 (WRBT))

Each link enables or disables erasure/reprogramming of a section of the Flash. E3 controls the User Flash and E9 controls the System Flash. However the links no longer have any effect on hardware and are purely retained for software legacy. See the Flash section for details of operation.

Table 1-3

Setting	Function
In	Enables erasure/reprogramming of the section of Flash
Out (default)	Disables erasure/reprogramming of the section of Flash

1.4 VME Boot Link (E4 (BTVME))

This link holds the CPU in reset to allow a VME master to program boot code to the Flash devices. To program the boot code into the Flash devices, the VME master needs to program both the Universe and the GT-64260B to enable a window from VME into the Flash devices.

Table 1-4

Setting	Function
In	VME programming mode
Out (default)	Normal boot mode

Use of this link relies on the default Universe II configuration (see the VMEbus Interface Configuration section).

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1.5 Flash Boot Image Select Links (E7 (BTREC) & E8 (BTAT))

The System Flash is divided into four sections, with all sections accessible all the time. Using these links, the four sections can be swapped around in the CSBOOT memory map. This allows for up to four boot images to be programmed into Flash: Normal, Alternate, Second Alternate and a factory-blown Boot Recovery image, with the links selecting which image is used at boot time. The state of the links is reflected in the Memory Configuration Register (port 0x0804). Normally, these links are not fitted and the PPC8A boots from the default boot area in Flash (see the Flash section for details of operation). However, when either of the links are fitted, the PPC8A boots from an alternate boot image. After boot time, the link setting can be overridden by software to select the different images. These links only affect Flash accesses via Discovery 1, Chip Select Boot (CSBOOT).

Table 1-5

E7 (BTREC)	E8 (BTAT)	Function
Out (default)	Out (default)	Normal Flash boot image operation
Out	In	Alternate Flash boot image
In	Out	Recovery Boot image
In	In	Second Alternate Flash boot image

1.6 VIO (PCI Signaling) Voltage Selection Link (E30 (VIO))

Table 1-6

Pins 1 - 2	Pins 2-3	Function
Out (default)	Out (default)	PPC8A held in reset
In	Out	PMC VIO voltage is set to 3.3-Volts
Out	In	PMC VIO voltage is set to 5-Volts



CAUTION

If no jumper is fitted on E30, such that the VIO voltage is not specified, the PPC8A is held in reset. Some legacy PMCs short VIO to VCC (PMC9100), which will both source VIO with 5 Volts and allow the PPC8A to exit the reset state. However, if such a card is installed and the E30 link is set to 3.3V, the PPC8A and/or PMC may be damaged.

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1.7 Board ID Links (E124, E125, E126, E127)

These links form a 4-bit board ID that may be read from the ID Link register (see the EPLD Register (0x0864/0x0880) section). The links are decoded as follows:

Table 1-7

Board ID	Links			
	E124	E125	E126	E127
15 (default)	Out	Out	Out	Out
14	Out	Out	Out	In
13	Out	Out	In	Out
12	Out	Out	In	In
11	Out	In	Out	Out
10	Out	In	Out	In
9	Out	In	In	Out
8	Out	In	In	In
7	In	Out	Out	Out
6	In	Out	Out	In
5	In	Out	In	Out
4	In	Out	In	In
3	In	In	Out	Out
2	In	In	Out	In
1	In	In	In	Out
0	In	In	In	In



NOTE

The ID Links are no longer logically ORed with the Geographical Address Signals from the backplane. See the VME section for more detail.

1.8 On-board SCSI Terminator Enable Link (E128 (SC_TRM))

This link enables or disables the on-board SCSI terminators, as follows:

Table 1-8

Setting	Function
In	Enable on-board SCSI terminator
Out (default)	Disable on-board SCSI terminators

If using the SCSI bus, it is recommended to locate the PPC8A at one end and enable the terminator by fitting a jumper on this link. If the PPC8A is placed somewhere other than at the end of the SCSI bus, ensure that no jumper is fitted on this link.



CAUTION

Fitting a jumper on this link when the PPC8A is not located at the end of a SCSI bus may cause erroneous SCSI operation. An on-card EPLD based control register bit can be used to enable SCSI termination even if the no jumper is fitted on this link.

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1.9 Enable Front Panel Reset Switch Link (E130 (RST_EN))

This link enables or disables the front panel reset/abort switch, as follows:

Table 1-9

Setting	Function
In	Disable reset switch
Out (default)	Enable reset switch

NOTE

The function of this link is the opposite of most other Abaco PPC cards.

1.10 ECC Enable Link (E123 (ECC_REQ))

This link enables or disables ECC protection on the SDRAM, as follows:

Table 1-10

Setting	Function
In	Disables ECC
Out (default)	Enables ECC

NOTE

This link only provides status information in register 0x0866; the software running on the PPC8A controls the operation of ECC, so it is possible that the software may not support this feature.

1.11 JTAG Scan Bridge Enable Link (E131 (JTAG_MODE))

This link is used to enable the on-card JTAG Scan Bridge. When enabled, this device allows external control of all the on-card JTAG circuitry via P1, row Z pins.

Table 1-11

Setting	Function
In	Enables JTAG Scan Bridge
Out (default)	Disables JTAG Scan Bridge

NOTE

With the JTAG Scan Bridge enabled, the Processor BDM header (P8), is not usable due to a drive clash between the BDM and the JTAG Scan Bridge. P8 should only be used when no jumper is fitted on this link.

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1.12 JTAG Autowrite Routing Link (E200 (P1AW))

This link is used to connect the backplane pin, P1-Z13 to the Autowrite input of the on-card JTAG Scan Bridge. As P1-Z13 is a VME reserved signal, its use as JTAG Autowrite must be optional. Autowrite is a signal used by some JTAG controller equipment to speed up the JTAG programming of Flash memory.

Table 1-12

Setting	Function
In	P1-Z13 is connected to Scan Bridge
Out (default)	P1-Z13 is isolated

1.13 Board ID Source Select Link (E220 (LNKSEL))

The five-bit Geographical Address ID and the four on-card links are no longer combined in hardware. The two buses are routed to the on-card EPLD and are available in two separate registers. This link controls which of the two sources are reported in the main Geographical Address ID register (0x0864) and which is reported in a new EPLD register (0x0880).

Table 1-13

Setting	Function
In	Main Board ID is sourced from links
Out (default)	Main Board ID is sourced from backplane



NOTE

The rack position input to the JTAG Scan Bridge is always sourced from the backplane Geographical Address ID bits.

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2 • Functional Description

2.1 Introduction

The PPC8A is a highly integrated, VMEbus processor using the PowerPC MC7448 RISC CPU with 1 MByte integrated L2 cache. The product offers an extensive range of standard functions including processors clocked at 1000 MHz, user SDRAM up to 1024 MBytes on-board with ECC, 128/256 MBytes of Flash, on-board serial, parallel, and two channels of 10/100BASE Ethernet to the rear, one 10/100/1000BASE-T Ethernet port to a dedicated front-mounted RJ45, an Ultra-SCSI peripheral interface controller, a 64-bit VMEbus interface, USB 1.1 and USB 2.0, and optional video.

Expansion capabilities are provided by two, 64-bit/66 MHz, PCI interface PMC slots. PMC (IEEE P1386.1) provides an industry-standard, high-speed (528 MBytes/second) local expansion bus, designed for graphics, high-speed communications (e.g. ATM, FDDI, ISDN, etc.), multi-media and user-defined custom functions. PCI has established itself as the leading local interconnect standard, and the wide availability of compatible devices, coupled with its adoption on an array of platforms, ensures that PCI-based modules are both high-performance and low cost.

The highly-integrated nature of the PPC8A makes it a true single board computer. In many ways, the PPC8A resembles a high-performance PC motherboard, although in a more rugged, lower profile and more compact form factor.

The PPC8A has been designed to be a plug-in replacement of the PowerXpress family of SBCs, which previously offered the PPC1A and PPC6. To enhance the connection capabilities, the PPC8A uses 5-row P1 and P2 connectors, but still retains the PPC basic pinout.

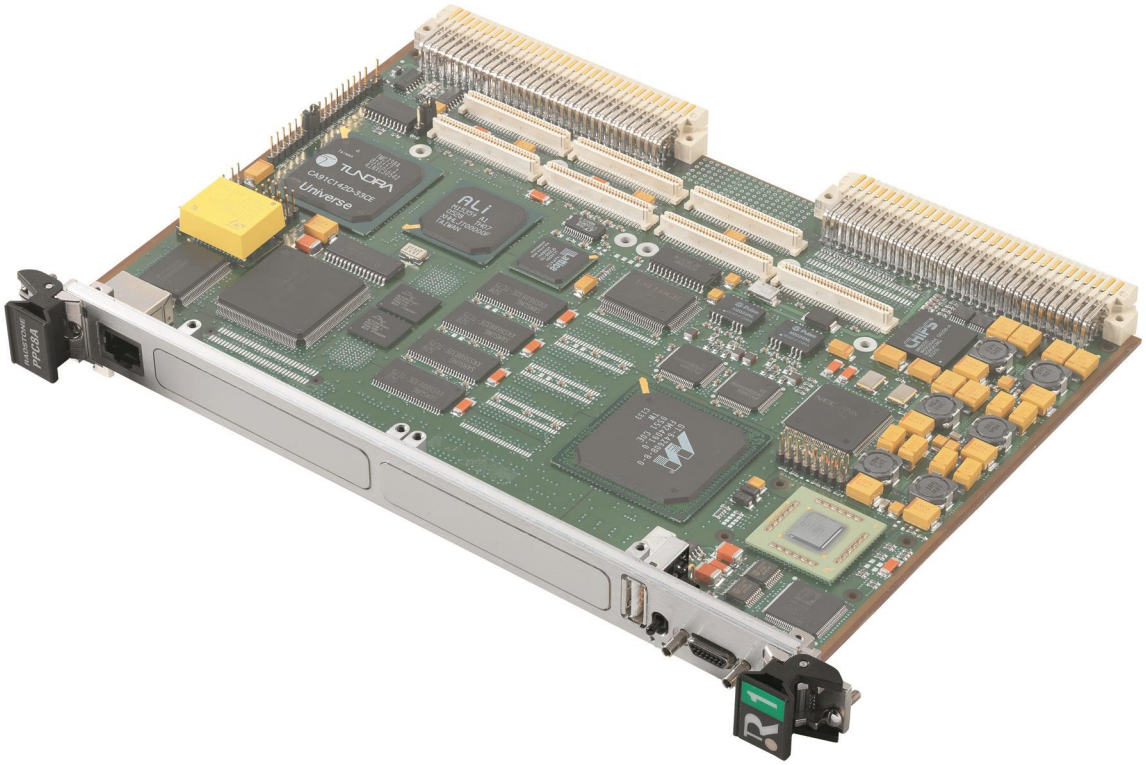
2.2 Migrating from Rev 1 Artwork Boards

New features for rev 4 and 5 boards include:

- PowerPC Processor migration to MC7448 @ 1000 MHz
- Flash banks now use Spansion S29GL-N devices, which affects bank size and software protection scheme
- Keyboard/Mouse or USB 1.1 is now software selectable (not a build option)
- GPIO (Floppy) or Parallel Port is now software selectable (not a build option)
- GPIO default pullup changes
- An Elapsed Time Indicator device added
- Improved COM3/COM4 RS232 Mode signal set
- Separation of Slot ID/Geographical Signal buses
- Inclusion of a 1-wire, unique serial number device
- Inclusion of JTAG Scan Bridge

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Figure 2-1 PPC8A General View



NOTE

Rev 4 board shown – heatsink removed

2.3 Features

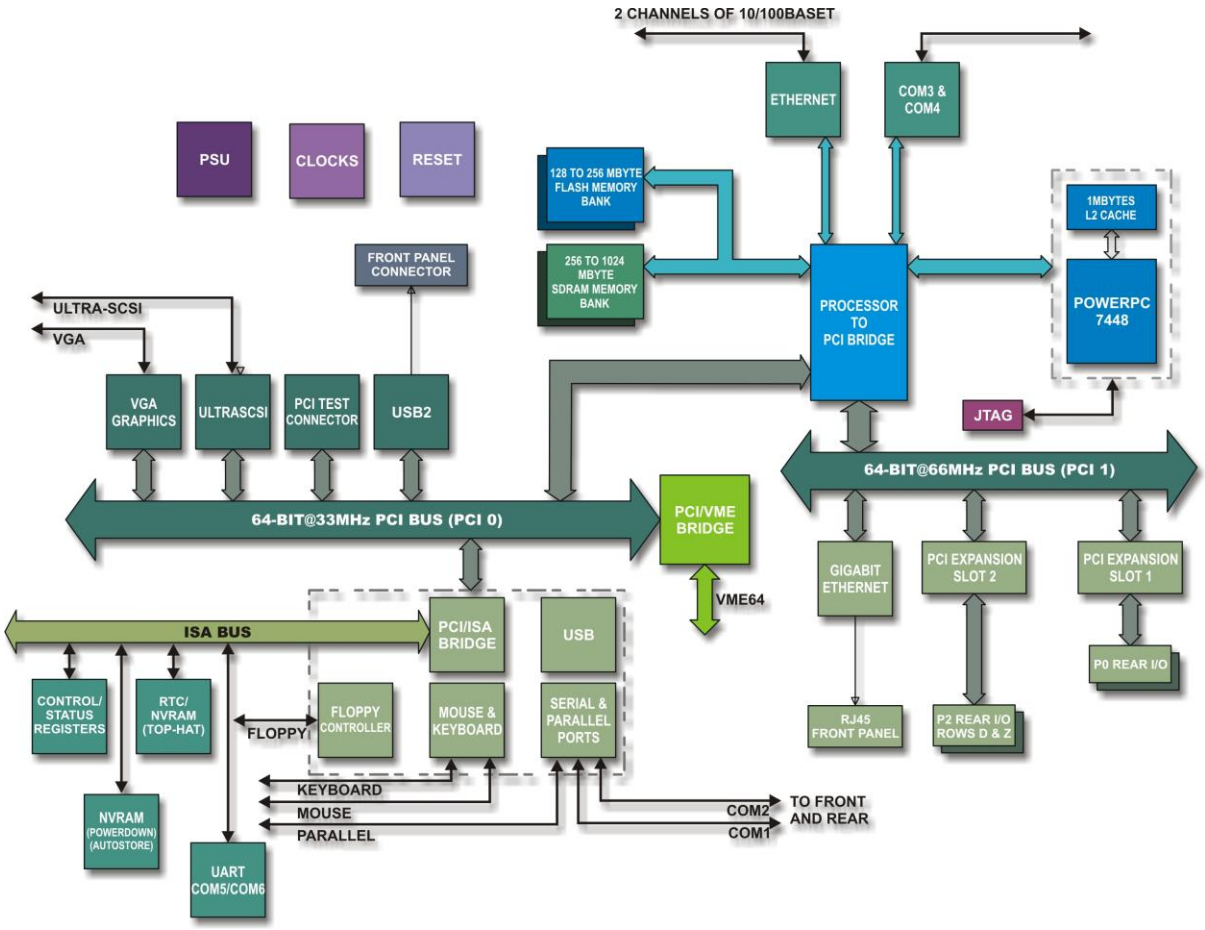
- PowerPC MC7448 CPU at 1000 MHz with 1 MByte of on-chip L2 cache
- Up to 1024 MBytes of SDRAM with optional ECC for memory intensive applications
- 128 or 256 MBytes of NOR Flash ROM (512 MBytes is a future option - depending on device availability)
- Two 64-bit/66 MHz PCI expansion slots on-board give system expansion using IEEE P1386.1 standard single- or double-width PMCs
- Three on-board Ethernet controllers: two 10/100BASE-T to the rear, one 10/100/1000BASE-T to a dedicated front RJ-45 connector
- Four USB 1.1 ports: two to the front, two to the rear (software selected over PS2 style Keyboard/Mouse)
- Two USB 2.0 capable ports: one to a dedicated, front mounted, Type A socket, the second routed to P0
- 32 KBytes of NOVRAM (Simtek SRAM shadowed by EEPROM)
- Real Time Clock (TOD/calendar) with top-hat style battery and 8 KBytes of Battery Backed SRAM
- Ambient Temperature Sensor

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- Elapsed Time Indicator (ETI) with 'powered hours' and 'number of switch-ons' registers
- Ultra-SCSI I/O processor
- Two RS232 serial I/O channels up to 115.2 Kbaud (COM1/COM2)
- Two RS485/422/RS232 software selectable serial I/O channels up to 1 Mbaud (COM3/4)
- Two RS232/RS422 serial I/O channels up to 115.2 kbaud (COM5/6)
- Parallel printer port (optional over GPIO/Floppy port)
- 17-bit wide GPIO interface
- Keyboard/mouse interface (optional over USB 1.1)
- Floppy disk controller (uses same I/O as GPIO)
- VME64 interface using Tundra Universe II VMEbus interface chip
- Single slot 6U VME form factor for reduced system cost and slot count
- Range of 3U rear-mounting I/O modules
- ANSI/VITA 1-1994 VME64 and VME64 extensions (5 row P1 and P2) compatible
- Two build standards (Level 1 or Level 2)
- Abaco COTS software support includes BIT, Boot firmware, BSPs and ESPs (with BCS) for LynxOS/LynxOS HA, Tornado II/VxWorks and Integrity
- Wide range of shrink-wrapped application software available
- Optional software maintenance giving automatic software revision updates and technical support
- Optional hardware and on-board firmware configuration management service giving a unique part number requiring customer authorization for changes in product revision status

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Figure 2-2 PPC8A Block Diagram



NOTE

Flash block = 128 to 256 and SDRAM = 256 to 1024 MBytes.

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2.4 PowerPC Platform

The PowerPC Platform is an example implementation of a philosophy designed to allow software compatibility across different platforms based on the PowerPC processor. Aiming to achieve an open standard, the PowerPC Platform encourages the use of industry standard components and buses, and a wide range of operating systems.

As well as providing a detailed hardware design specification, the PowerPC Platform also embodies a software mechanism that allows the hardware to be isolated from the application by abstraction layers. It is these abstraction layers (in effect very low-level system drivers) that are the key to differentiation, scalability and future-proofing. Operating systems, applications and drivers can 'sit' on these layers without needing to be aware of the underlying hardware (other than general functionality). This is fundamentally different from PCs, which use a BIOS that ultimately constrains operating systems and applications alike.

The major purpose of the PowerPC Platform architecture "... is to give direction to system designers, while still enabling differentiation in areas where real value can be added, thus allowing the PowerPC microprocessor industry to build a reusable body of OS and application software...". The knowledge that both operating system and application programs will run on any host that complies with the PowerPC Platform architecture provides security for today's valuable software investments, as well as expansion capabilities for the future.

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2.5 PowerPC Processors

2.5.1 MC7448

The PowerPC MC7448 is a 32-bit superscalar RISC processor, clocked at 1000 MHz, with the following features:

- A 32-bit implementation of the PowerPC architecture
- 32 KByte, 8-way set associative instruction and data caches
- 64-bit external data bus
- On-chip 32 KByte instruction and data caches running at core speed
- On-chip 1024 KByte L2 cache running at core speed
- Enhanced branch prediction capabilities
- MMU and integral FPU

The PowerPC MC7448 implements a fully static architecture and offers sophisticated power management capabilities. As a result, the PPC8A has a maximum power consumption of less than 20 Watts at 1000 MHz.

Table 2-1

PowerPC CPU	CPU Frequency	Specint95	Specfp95
MC7448	1000 MHz	43.79	31.63

The processor has a 32-bit physical address bus and a 64-bit data bus.

Table 2-2

Processor Type	Bus Frequency	Core Frequency
MC7448	100 MHz	1000 MHz

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2.6 PCI

PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. PCI provides a synchronous 32 or 64-bit multiplexed address and data bus at speeds of 33 or 66 MHz, allowing burst data transfers to 528 MBytes/second. The PPC8A uses PCI to provide a high-speed backbone for local interconnection of on-board devices (processor, VGA, Ultra-SCSI, Southbridge and VME64, all of which have direct PCI connectivity). The Tundra Universe II chip provides full PCI to VME bridge capability.

As well as local interconnection of on-board devices, PCI also allows communication with optional mezzanine expansion modules (PMCs). The PCI mezzanine format also provides 64 I/O pins for user definition. A range of PMCs are available from Abaco, including high-performance graphics, MIL-STD-1553, asynchronous serial, Fast Ethernet, Flash memory, Fiber Channel and ATM, all fully compliant with the IEEE P1386.1 standard.

Using the PCI to PCI bridge device on the PMCPCI bridge card (see below), the PPC8A can maintain concurrent bus operation. This allows applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

2.6.1 PCI Bridge and Memory Controller

The Marvell GT-64260B Discovery 1 provides the CPU to Memory-PCI bridge. This interfaces the processor to the SDRAM, Flash and the two PCI buses.

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2.6.2 PCI Expansion Bus

Two PMC slots are provided as standard on the PPC8A. These PCI slots are 64 bits wide and run at 66 MHz. If a PMC is fitted that is not capable of running at 66 MHz, then the PPC8A will reduce the frequency to 33 MHz for both PCI slots.

For those configurations requiring additional PCI functionality, the PMC to PCI Bridge card (PMCPCI) bridges the on-board PCI bus out via the P0 connector, allowing use of a range of P0 PMC carriers, or interfacing the PPC8A directly to Abaco's range of DSP boards.

To connect the PPC8A to P0-based carrier cards such as the P0CC1, a series of P0 add-on backplanes are available. These are PCBs for attaching to a system backplane that has J0 connectors fitted. The following variants are available:

Table 2-3

Variant	PCI Backplane Slots	Master Slots	P0CC1 Slots
P0BP1-502	2	1	1
P0BP1-503	3	1	2
P0BP1-504	4	1	3
P0BP1-505	5	1	4

The P0BP1 backplane must be soldered onto the J0 system backplane, and can be used with either type A or type B J0. These backplanes are intended to have a host SBC with PMCPCI card plugged into the master slot, which is the left-most slot of the P0 PCI backplane. For further information about P0 backplanes, contact Abaco.



NOTES

The on-card 10/100/1000BASE-T Ethernet interface uses the same PCI bus as the PMC sites. Fitting a 33MHz PMC may impact on Gigabit Ethernet bandwidth.

PPC8A rev 4 and rev 5 boards include the ability for software to monitor the status of the EREADY signal (J12-58 and J22-58). This wired-OR signal can be used by a mezzanine card to delay PCI Bus enumeration by the PPC8A host software. This feature is to cater for PMCs where the PCI interface is realized in a slow loading, large FPGA device.

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2.6.3 PCI Configuration

The boot process must configure the base address and space type (memory or I/O) of all the PCI attached peripherals. The memory requirements of each PCI device are given in the appropriate device descriptions in this section.

Each PCI device also has several registers located in PCI configuration space, which is accessed by the processor through the GT64260B PCI bridge and memory controller using the CONFIG_ADDR and CONFIG_DATA registers. A full description of PCI configuration can be found in the GT64260B specifications.

The device number mapping for the PCI bus 0 attached to the GT64260B is as follows:

Table 2-4

Device	Function
0 to 15	Not implemented
16	Not implemented
17	Not implemented
18	Southbridge
19	Not implemented
20	Universe II VME controller
21	Graphics
22	SCSI Controller
23	Not implemented
24	USB 2.0
25 to 31	Not implemented

The device number mapping for the PCI bus is as follows:

Table 2-5

Device	Function
0 to 22	Not implemented
23	PMC1
24-25	Not implemented
26	PMC2
27	Not implemented
28	Gigabit Ethernet
29 to 31	Not implemented

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2.6.4 PCI Buses

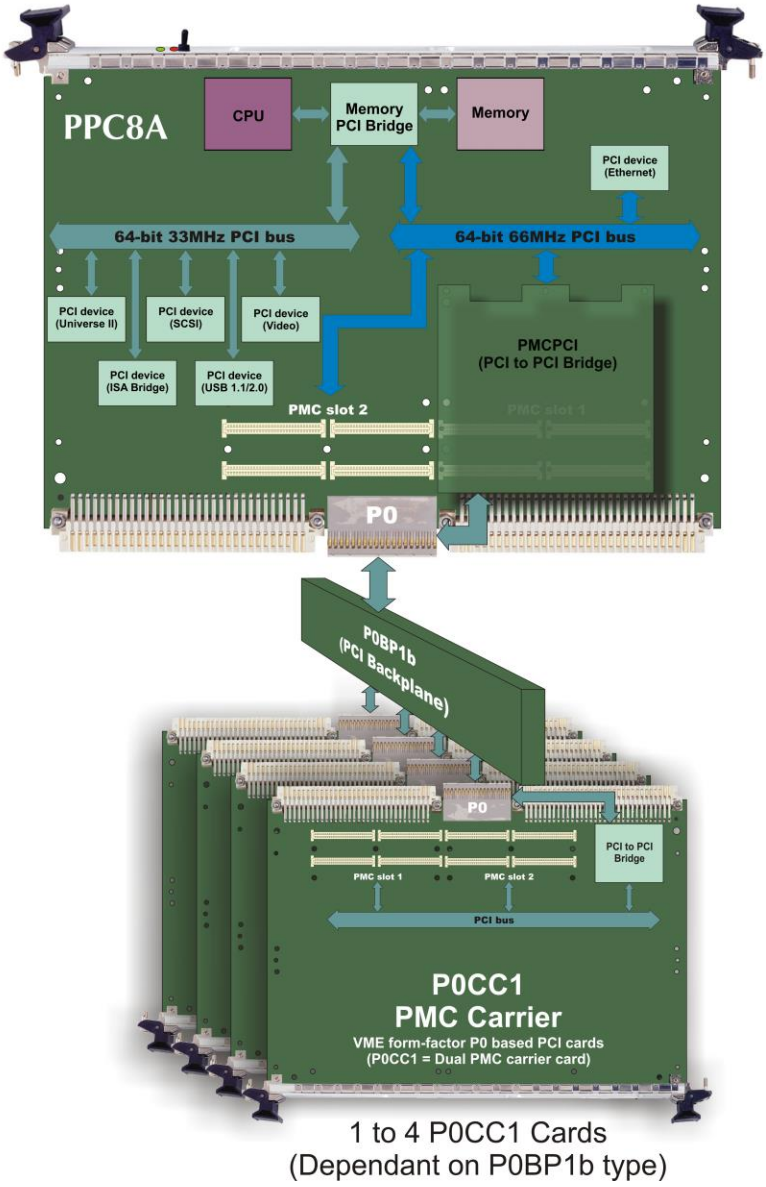
There are two PCI buses on the PPC8A.

PCI0 is connected to all the on-board PCI devices. This bus is implemented as a 64-bit PCI bus running at 33 MHz (64-bit to Universe device only). This gives a burst rate up to 264 MBytes/second between PCI agents.

PCI1 is the PCI bus routed to the two PMC sites, the CPU Host bridge interface and the on-card 10/100/1000BASE-T Ethernet Interface. This bus is implemented as a 64-bit PCI bus running at up to 66 MHz. This gives a burst rate up to 528 MBytes/second between PCI agents. The PMC sites may be occupied in any order as this bus is terminated at both ends by the Host Bridge and Gigabit Ethernet MAC respectively.

The PCI bus structure of the PPC8A is shown below:

Figure 2-3 PCI Bus Diagram



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2.7 Memory/PCI Bridge (Host Bridge)

The Memory/PCI Bridge on the PPC8A is provided by a Marvell GT64260B Discovery 1 device. This device provides:

- Host Bridge between the processor bus and the two PCI buses
- SDRAM memory controller and Flash interface (see the Memory section)
- Two 10/100 Ethernet MACs (See the Ethernet Section)
- Two Serial channels (COM3 and COM4)
- MPP GPIO interface

2.7.1 Serial Ports COM3/COM4

The GT64260B Host Bridge provides two, high speed serial ports capable of both synchronous and asynchronous operation. The two channels are routed through dedicated, software selectable RS232/RS422/485 transceivers, which provide the following signal set:

Table 2-6

COM3/COM4	
RS232	RS422
TXD	TXDA
DTR	TXDB
RTS	RTSA
DEZ2 (for test use only)	RTSB
RXD	RXDA
DSR	RXDB
CTS	CTSA
DCD	CTSB
TT_CLK	TT_A
N/A	TT_B
RT_CLK	RT_A
N/A	RT_B
ST_CLK	ST_A
N/A	ST_B

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2.7.2 MPP GPIO Interface

The MPP Interface on the GT64260B Host Bridge can provide a wide range of features. The PPC8A design uses these signals to provide:

- Two PCI Arbiters for the on-card PCI buses
- On-chip Watchdog interface
- COM3/4 RS232 Mode DSR inputs
- On-chip counter extenders
- PMC Site EREADY monitoring
- 1-Wire, unique serial number device interface. Dallas – DS2411

2.8 Memory

2.8.1 Memory Maps

The PPC8A supports programmable memory maps. No memory maps are provided in this manual as no memory locations are fixed in hardware. See the manuals for the software that is installed on the PPC8A for more information.

2.8.2 Level 2 Cache

The PPC8A provides 1024 KBytes (1 MByte) of L2 cache, integral to the MC7448 processor. This memory operates at CPU core speed (1000 MHz on a 7448).

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2.8.3 SDRAM

The following table shows the options available for SDRAM on the PPC8A:

Table 2-7

SDRAM Size	Banks	SDRAM Device Organization
256 MBytes	1	32M x 8
512 MBytes	2	32M x 8
1024 MBytes	2	64M x 8

The SDRAM is protected by eight ECC bits per 64 data bits. All single bit, double bit and nibble errors can be detected, and single bit errors can be corrected.

Following a hard reset, the GT64260B Controller must be set up for the size and number of banks of SDRAM and the appropriate number of wait states to match the SDRAM speed. This is done by the standard Boot firmware. The size of the SDRAM may be checked by reading the Memory Configuration Register (see the Control and Status Registers section).

At least 100µs must have elapsed from the negation of reset before enabling the SDRAM. After being enabled, the SDRAM must not be accessed until at least 8 refreshes have occurred. If ECC is to be enabled, then it is necessary to initialize the SDRAM to set-up valid ECC bits.

SDRAM access times from the processor, for a 32-byte burst are as follows:

Table 2-8

Bus Speed	Clocks Access	Data Transfer Rate
100 MHz (no page hit)	16:1:1:1	168 MBytes/second
100 MHz (pipelined)	5:1:1:1	400 MBytes/second
100 MHz (pipelined & page hit)	2:1:1:1	640 MBytes/second

SDRAM access times from the PCI, referenced to the 33 MHz PCI clock, for a 32-byte burst with no interference from L1 or L2 caches, are as follows:

Table 2-9

Action	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate
Burst Read	2:1:1:1:1:1:1:1	118 MBytes/second
Burst Write	2:1:1:1:1:1:1:1	118 MBytes/second

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2.9 Flash

The GT64260B Controller is used to interface to one or two banks of NOR Flash, realized using two, Spansion S29GL-N devices per bank, resulting in 128 MBytes per bank and producing a total of 256 MBytes if both banks are populated. The Operating System Board Support Package makes the migration from Intel to Spansion Flash invisible to application code, however users who have produced their own Flash drivers should familiarize themselves with the device using the Spansion datasheet – available at http://www.spansion.com.

2.9.1 Flash Protection

The protection mechanism has shifted from hardware to software. For Rev 1 Artwork boards, links were used to control the programming pin on the Flash devices. For Rev 4 Artwork and above, the Persistent Password Mode, sector protection capabilities of the Spansion devices has been used to greatly improve the control and flexibility of Flash protection. For more information, see the Persistent Protection, Password Mode section in the Spansion S29GL-N Datasheet.

The current password required to lock/unlock Flash sectors is stored in the EPLD registers accessed through CS0 of the Discovery 1 Bridge. Link E5 (PWEN) or the backplane signal PASSW_EN_BP~ can be used to hide or reveal the current password, making it unnecessary for the OS, BSP or application code to contain the actual password (see the E5 definition and EPLD registers via CS0 for more detail).

The E3 (WRUR) and E9 (WRBT) links are retained for legacy but do not affect Flash protection in any way.

The Flash has a write capacity of 100,000 cycles per block (128 KByte block size) and the software must write to the Flash as 32-bits.

PPC8A is shipped with the Spansion devices set to Persistent Protection, Password Mode with most the sectors of the 8 MByte Boot Area locked, and the remaining User area and BIT result sectors unlocked.



NOTE

Flash data Integrity cannot be guaranteed if a hard reset occurs during a Flash write cycle.

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2.9.2 System Flash

The top 8 MBytes of Bank 0 has been designated as the System Flash. This area is further divided into four to produce Normal Boot, Alternative Boot, Second Alternative Boot and Recovery (BANC) Boot regions. Each of the 2 MByte areas (256 KBytes in the case of Recovery) can be selected as the boot code source region, with links E7 and E8 being the mechanism for selecting the required area. Address modification using the links is only applicable when the region is accessed through GT64260B output, CSBOOT. Flash accesses through GT64260B output, CS3, are not affected by the links and the Flash is addressed 'as-is'.

2.9.3 Normal Boot

This area is used as the main default boot area of the PPC8A. This area is typically where user put their boot firmware, and is selected for booting by leaving the E7 (BTREC) and E8 (BTALT) links without jumper fitted. The PPC8A is shipped with these sectors locked.

To write to this area, it may be necessary to unlock the Normal Boot Flash sectors, which requires the fitting of a jumper on link E5 (PWEN) or the pulling low of the backplane signal PASSW_EN_BP~.

2.9.4 Alternate Boot

This area normally contains a backup or alternate boot image, and can be useful when developing boot code, as it provides the ability to switch to a 'known-to-be-good' image if the Normal Boot area becomes unusable. If an alternate boot image is not required, this area can be used to hold User data or for extended boot code. This area is selected for booting from when a jumper is fitted on link E8 (BTALT) but link E7 (BTREC) is left without a jumper fitted.

To write to this area, it may be necessary to unlock the Alternate Boot Flash sectors which requires the fitting of a jumper on link E5 (PWEN) or the pulling low of the backplane signal PASSW_EN_BP~.

2.9.5 Second Alternate Boot

This area normally contains data. If required, a second alternate boot image can be programmed into this area and is selected by fitting a jumper on both link E7 (BTREC) and link E8 (BTAT).

To write to this area, it may be necessary to unlock the Second Alternate Boot Flash sectors, which requires the fitting of a jumper on link E5 (PWEN) or the pulling low of the backplane signal PASSW_EN_BP~.

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2.9.6 Recovery Boot or BANC (Boot Area – Non-Corruptible)

This area contains a simple boot image (PPCBoot) that is designed to allow recovery of the card when all the other boot areas have been rendered unusable. Fitting a jumper on link E7 (BTREC) and leaving E8 (BTAT) without a jumper fitted causes this area to become the source of boot code.

The recovery area is programmed in the factory and cannot be modified by the user. No link settings can make this area writeable.

The recovery image only uses 256 KBytes of the 2 MByte Recovery area. The remaining space is an unlocked area and may be used to store BIT results, but is only accessible via CS3 as all accesses to this area via CSBOOT are redirected into the top 256 KBytes.

2.9.7 User Flash

All but the top 8 MBytes of the Flash region is designated User Flash and is accessed through CS3 of the GT64260B Host Bridge. These sectors are shipped unlocked, but can be locked at user discretion using the sector protection password available in EPLD registers off GT64260B Bridge, CS0.

2.9.8 Flash Programming from VME

Fitting a jumper on link E4 (BTVME) allows the PPC8A to have new boot firmware programmed via the VMEbus. This link is intended for factory use only. Normally, if the Boot firmware gets corrupted, the Recovery boot option should be used to restore the Boot firmware.

This link holds the on-board processor in reset as this is required when the on-board Flash contents are unknown and new boot firmware is required to be loaded into the Flash from VME.

To load new firmware from VME, the VME master relies on the reset configuration of the Universe. The register set of the Universe appears at address 0x8000 0000 on VME, by default. The VME master uses these registers to set up windows onto the PCI bus from VME.

The GT64260B has its register set available at address 0x1400 0000. The PowerPC's boot Flash can be accessed at address 0xFFF0 0000 on PCI. These areas will need mapping onto VME to allow access of the Flash memory.

The Flash memory can be read from or written to, but may require Flash sectors to be unlocked before erasure/reprogramming can be performed. Writes to the Flash memory should always be done as 32-bit word writes.

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The boot area that can be accessed at 0xFFF0 0000 depends on the Boot link (E7 and E8) settings.



NOTE

The Recovery boot area cannot be write-enabled by configuration of the Boot links (E7 and E8). This area is factory programmable only.

Once you have programmed the boot section of the Flash, remove the jumper from link E4 and carry out a hard reset. Normal booting now occurs from the Flash and both User and Boot sections are accessible again at their normal addresses.

2.9.9 NOVRAM

The PPC8A design includes two areas of NOVRAM:

Simtek – STK14C88: 32-KBytes, accessed via the Southbridge ISA Bus. The device consists of SRAM shadowed by EEPROM and includes the ability to perform auto-storing at power-down. The device is mapped as four pages of 8 KBytes, with page selection via two bits in the EPLD register at offset 0x0820.

STMicro - M48T18: 8-KBytes, also accessed via the Southbridge ISA Bus. The Real-Time Clock device contains battery-backed SRAM, using the 'snap-hat' (M4T28) battery to provide backup power.

2.10 Ethernet Interfaces

There are three Ethernet interfaces within the PPC8A design:

- The GT64260B Bridge device provides two, 10/100BASE-T ports routed via on-card PHYs and magnetics to the P2 connector
- A National Semiconductor DP83820/83865 chipset provides a 1000/100/10BASE-T interface to a dedicated front panel RJ45 connector

Automatic packet deletion on receive (runt packets or after a collision) and packet re-transmission after a collision on transmission are supported. This minimizes bus traffic by removing unnecessary accesses to shared memory. The network addresses (Ethernet numbers) are factory configured.

Front and Rear connections are detailed in the Connectors section. Associated status LEDs are mounted on the rear of the board near the front edge (see the Software Programmable LEDs section). The default functions of these LEDs are link status, TX activity, RX activity status, and link speed, but they may be overridden by the software.

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2.11 SCSI Scripts Processor

The NCR53C860 SIOP executes commands, in the form of SCSI scripts. It has a PCI interface and a DMA controller, which are used to access the scripts and data held in system memory. The SIOP can transfer data at 20 MBytes/second synchronously or 14 MBytes/second asynchronously. Connection to the SCSI bus is made through the P2 connector. The pinout is given in the Connectors section.

The PPC8A has an on-board active SCSI terminator, which may be enabled or disabled with a jumper (see the E128 description in the Link Settings section). The SCSI specification allows a maximum cable stub length of
10 cm. If the SCSI bus connections are taken directly from the backplane J2 connector, then the PPC8A may be located anywhere on the SCSI bus and the terminator should only be enabled if the PPC8A is at the end of the SCSI bus. Otherwise, the PPC8A must be at the end of the SCSI bus and the terminator must be enabled.

A software programmable SCSI Activity LED (LED DS217) is mounted on the back of the board. See the Software Programmable LEDs section and the SCSI Activity LED Register description for more details.

2.12 VGA Graphics Processor



NOTE

Due to component obsolescence, this feature is no longer available.

2.13 USB

A NEC uP720101 PCI-USB device provides two USB 2.0 ports. One is routed to a dedicated, vertical, type A, front mounted socket. The second is routed to P0 (see the P0 pinout).

Four USB 1.1 ports are available from the Southbridge. Two ports are routed to the front P19 connector and two are routed to the rear and are software selectable over Keyboard/Mouse.

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2.14 PMC Sites

The PPC8A has two sets of connectors ({J11, J12, J13, J14} and {J21, J22, J23, J24}) that allow standard PMCs to be connected to the PCI bus. The PPC8A can accept either air-cooled or conduction cooled PMCs, if adequate cooling is provided. Air-cooled PMCs are defined in the IEEE 1386 Standard. Front panel I/O is fully supported.

The PMC I/O connectors are routed to the backplane connectors to allow backplane I/O. J14 (PMC site 1) is connected to P0 and J24 is partially connected to P2 and the center rows of P0.

The PPC8A supports the EREADY signal for use with PMCs that use a slow loading FPGA to realize their PCI interface. Such PMC designs can hold EREADY low to hold off PCI enumeration by the host OS until the PCI interface is ready to participate in the enumeration process. A separate EREADY signal is provided for each PMC site.

Fitting a PMCPCI card (must be fitted in PMC slot 1) allows the PCI bus to come out to the backplane via P0.

2.15 VMEbus Interface

The Tundra Semiconductors CA91C142D Universe II PCI to VME bridge provides the VMEbus interface. This complies with the VME64 specification and provides:

- All slot 1 (system controller) functions
- Interrupt control
- A DMA controller
- Interprocessor communications
- Block transfer support

The Specification section details the VMEbus compliance and basic VMEbus performance of the PPC8A.



NOTE

The Universe II does not self-address.

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2.15.1 VMEbus Master Access

Four general-purpose, software-programmable PCI slave images are available for access to the VMEbus.

- These can all be configured to access VMEbus A32, A24 or A16 address space
- An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address
- The start and end addresses of the A32, A24 and A16 PCI slave images may be set on any 64 KByte boundary in PCI memory or I/O space that is not allocated to other PCI-attached devices or the user Flash
- One image may be set on 4 KByte boundaries to accommodate access to A16 space

One further, special purpose, PCI slave image allows mapping of A16 and A24 space.

- This slave image uses a 64 MByte window, aligned to any 64 MByte address in PCI memory space
- The window is divided into four 16 MByte quadrants
- The top 64 KBytes of each quadrant maps to A16 space, while the rest of each quadrant maps to A24 space
- The Address Modifiers generated are software configurable for each quadrant

VMEbus master cycles may be coupled or write posted.

- Coupled cycles are retried on the PCI bus until the Universe II has ownership of the VMEbus and are not terminated on the PCI bus until all data has been transferred over the VMEbus
- Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred

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2.15.2 VMEbus Slave Access

Four general-purpose, software-programmable VMEbus slave images are available.

- These may all be defined in VMEbus A32, A24 or A16 space
- An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address
- The start and end addresses of the A32, A24 and A16 images may be set on any 64 KByte boundary

One further, special purpose, VMEbus slave image, the Register Access Slave Image, allows a VMEbus master to access to the Universe II control and status registers.

VMEbus slave accesses to the PPC8A may be coupled, write posted or pre-fetched block read.

- Coupled slave transfers can only proceed once the slave posted write FIFO is empty
- Slave posted write cycles are queued in a FIFO until the PCI bus is available for the data to be transferred

2.15.3 VME Slave Address Configuration

The board ID should be set up according to the system slot into which the board is inserted, as shown in the following table. The board ID also sets the board's VME slave addresses, so take care to avoid an address clash with other boards in the system.

Table 2-10

Slot	Slot 1 Functions	Board ID	A32 Address	A24 Address
1	Yes	0	0x0000 0000	0x00 0000
2	No	1	0x1000 0000	0x40 0000
3	No	2	0x2000 0000	0x80 0000
4	No	3	0x3000 0000	0xC0 0000
5	No	4	0x4000 0000	None
6	No	5	0x5000 0000	None
7	No	6	0x6000 0000	None
8	No	7	0x7000 0000	None
9	No	8	0x8000 0000	None
10	No	9	0x9000 0000	None
11	No	A	0xA000 0000	None
12	No	B	0xB000 0000	None
13	No	C	0xC000 0000	None
14	No	D	0xD000 0000	None
15	No	E	0xE000 0000	None
16	No	F	0xF000 0000	None

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NOTE

Any change to the Board Slot ID or Board ID links will require the hardware registers to be 're-learned' if BIT is not to fail.

2.15.4 VMEbus Slot Identification

The operating system can determine the rack position of the PPC8A by reading slot ID information from the on-card EPLD register at offset 0x0864. When n o jumper is fitted on the LNKSEL link, this register reflects the status of the five signals from the backplane P1 connector. If a jumper is fitted on the LNKSEL link, the register at offset 0x0864 reflects the status of the on-card Slot ID links (E124-E127). The bus not reported at offset 0x0864 is reported in a new register at offset 0x0880. See the EPLD register definitions for more information.

NOTES

When the on-card links are selected as the source, ID4 is always reported as '0'.

The JTAG Scan Bridge uses the Slot ID information from the backplane P1 signals regardless of the LNKSEL link.

2.15.5 VMEbus Interface Configuration

Several operating features of the Universe II VME interface are set at power-up or reset by surface mount links. Apart from local register access, these may all be overridden by software. The default settings are:

Table 2-11

Operating Feature	Setting
Register access slave image from VMEbus	Enabled in A32 space at 0x8000 0000
VME CR/CSR slave image	Disabled
PCI slave image 0	Enabled in PCI memory space at 0xF000 0000 to 0xFFFF FFFF
Local register access	PCI I/O space
Auto-ID scheme	Disabled

Changing the default power-up options requires surface-mount rework tools and would normally only be done by Abaco. Further details are available from technical support.

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2.16 Utility I/O and Auxiliary Function Bus

To take full advantage of low-cost, industry standard components, general purpose I/O and auxiliary functions are implemented through a Southbridge bus interface. Facilities provided include:

- Floppy disk controller
- GPIO
- Serial Channels COM1 and COM 2
- Parallel Port
- Keyboard/mouse interface
- USB 1.1
- Serial Channels COM5 and COM 6
- NOVRAM
- IDE Interface
- Audio

2.16.1 Southbridge

An ULI-M1535+ provides a bridge from the PCI bus to the ISAbus for connection of native I/O devices. This device also provides the following functions:

Table 2-12

Function	Equivalent to Function of
7 channel DMA between ISAbus and PCI bus	Two 83C37s
Timer block	One 82C54
Interrupt controller	Two 8259s
PCI bus arbiter	-
Four USB 1.1 Ports	-

The Southbridge positively decodes some I/O cycles on the PCI bus for internal resources. It subtractively decodes and claims all PCI memory and I/O cycles not claimed by other PCI targets, and forwards them to the ISAbus.

Apart from the Southbridge, there are no other ISAbus masters in the PPC8A architecture.

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2.16.2 Floppy Disk Controller

Connection to the FDC is through P2 and uses the same lines as the GPIO interface. The pinout is given in the Connectors section. The FDC is software compatible with the DP8473, 765A and NS82077. The Parallel Port must not be enabled by software at the same time as the GPIO or Floppy Port.

2.16.3 GPIO

The Floppy Disk port can be configured, by software, to operate as General Purpose In/Out. There are 17 lines: GPIO(0:14) and GPIO(16:17) with on-card pullups (1K0 to 5V) on GPIO(0:13). The remaining lines and not pulled in either direction and can be pulled low externally if a default of '0' is required.

The Parallel Port must not be enabled by software at the same time as the GPIO or Floppy Port.

2.16.4 Serial Channels (COM1/COM2)

The Ultra I/O provides two serial channels (COM1 and COM2) containing FIFOs, software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 115.2 kbaud, including the MIDI data rate.

Connection to the serial ports is primarily through the P2 connector, although access may be obtained through front panel connector, P19. See the Connectors section for pinouts.

- COM1 supports TXD, RXD, CTS, RTS to rear (P2) but only TXD, RXD to front (P19)
- COM2 supports TXD, RXD, CTS, RTS to both rear (P2) and front (P19)

Both COM1 and COM2 support RS232 only.

2.16.5 Serial Channels (COM5/6)

The PPC8A contains a 16750 compatible, dual channel UART, providing two additional serial channels, which is accessed through the Southbridge ISA Bus. The interface can be enabled/disabled under software control as well as configured for RS232 or RS422. COM5 and COM6 ports must be assigned together as either RS232 or as RS422; they cannot be defined individually.

Table 2-13

COM 5/6	
RS232	RS422
TXD	TXD-
RTS	TXD+
RXD	RXD-
CTS	RXD+

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2.16.6 Parallel I/O

The parallel port includes extended capabilities conforming to IEEE P1284. Connection to the parallel port is through the P2 connector. The pinout is given in the Connectors section. The GPIO or Floppy Port must not be enabled by software at the same time as the Parallel Port.

2.16.7 Keyboard and Mouse Controller

A PS/2-compatible Keyboard and Mouse interface with Phoenix BIOS is integrated into the Ultra I/O. Connections to the mouse and keyboard are through either the P2 connector or the front panel, P19 connector. See the Connectors section for pinouts. The Keyboard/Mouse port can be enabled at the same time as USB 1.1, however hardware only permits one of the two interfaces to be routed to the front or rear connectors at any one time. Routing to front and rear is independently controlled via software. See the EPLD register at offset 0x0870 for more detail.

2.16.8 USB 1.1 Ports

The keyboard/mouse signals can be optionally replaced by four USB 1.1 ports. USB 1.1, Port 0 and 1 routed to the front connector, P19 and USB 1.1 ports 2 and 3 routed to P2. The routing is controlled by software. See the EPLD register at offset 0x0870 for more details

2.16.9 I/O Option selection

The GPIO (Floppy Port) or Parallel Port is no longer selected via a hardware build option. The cards are built with both interfaces and it is up to software to enable the desired interface. Software must *not* enable both interfaces simultaneously

The same is true for the Keyboard/Mouse or USB 1.1 option. The PPC8A design uses software controlled analog switches to route either Keyboard/Mouse or USB 1.1 to front and/or rear independently. The hardware prevents both types of interface from being routed out at the same time.

2.16.10 NOVRAM

See the Memory section.

2.16.11 IDE Interface

The Southbridge can provide two ATA-100 IDE channels, but these are not currently supported.

2.16.12 Audio

The Southbridge includes an Audio controller, but this is not currently supported.

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2.17 Watchdog Timers

The PPC8A contains a Maxim MAX706 microprocessor supervisory circuit with a Watchdog timer. Once enabled, this timer must be re-triggered every 1.6 seconds or a hard reset results. The trigger control register is one the EPLD based registers. See EPLD Registers at offsets 0x082C and 0x0828 for more detail.



NOTE

Once this bit is enabled as an output, software needs to write to the trigger register to keep the board from resetting. Disabling the re-trigger output, once enabled, does not disable the Watchdog.

The GT64260B also contains a Watchdog timer. This timer has a programmable timeout interval. The Watchdog output pin needs to be enabled in the GT64260B as MPP bit 9 before the Watchdog can reset the PPC8A.

2.18 Software Support

Abaco's software strategy for PowerX boards allows fully integrated system-level solutions to be realized easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of the PowerX family, so providing a common look, feel and interface for technology inserts.

2.18.1 Boot Firmware

Developed as an integral part of the Abaco PowerX strategy, the Boot firmware provides a foundation layer to interface between the raw Abaco board hardware, with its highly programmable device set-ups and flexibility, and the supported Operating Systems, which require a straight-forward booting and device interface model.

The PPC Boot Firmware includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialization, PCI display/interrogation utilities and other valuable features for system integrators.

Memory or other speed and feature enhancements are seamlessly absorbed by the Boot firmware, giving the same look and feel to the O/S and the user application as the Abaco hardware models advance. This allows the constant use of latest technology in required areas without system impact. Where particular operating systems define the use of alternate boot methods (e.g. VxWorks bootroms), the Boot firmware technology is absorbed into such boot methodology.

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2.18.2 Built In Test

PPC BIT probes from the lowest level of discrete on-board hardware up to Line Replaceable Unit level within a system, ensuring a high degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialization tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

2.18.3 Background Condition Screening

BCS supplements the BIT initialization test coverage with further health screening that can co-exist with a standard COTS Operating System. In contrast to a traditional BIT-style test (the intensity and coverage of which makes it destructive to operating systems), the configurable BCS package allows functions such as periodic check-summing, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in Flash in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.

2.18.4 Operating System Support

In-house porting expertise for PowerX based boards is focused on key operating systems, including Wind River Systems' Tornado II/VxWorks, and LynxOS from LynuxWorks. Hardware support code is delivered by Abaco, to complement the main operating system code shipped by the O/S vendor.

Other operating system ports (including Integrity from Green Hills Systems), drivers for third party hardware and layered products, are provided through strategic partnerships with dedicated third party vendors, able to offer products and services complementary to the Abaco range. In this way, development environments and debug tools that are part of the above software products, are made available for use on Abaco's flexible hardware architectures. Contact Abaco for availability of these offerings.

2.18.5 BSPs and ESPs

Board Support Packages provide 'standard' support for the above operating systems, as defined by the operating system vendors. Abaco also provide Enhanced Support Packages, for comprehensive hardware support *in addition* to that defined by the operating system vendors. ESP features may be added or removed as desired during development.



NOTES

Hardware should be accessed only through mechanisms provided by the Operating System's 'Hardware Independence' mechanism (BSP, HAL, residual data, etc.), and not directly by application software.
If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.
Abaco-supported Operating Systems guarantee compatibility at the application level through the Hardware Independence mechanisms mentioned above.

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2.19 Resetting the PPC8A

There are two types of reset that may be applied to the PPC8A: 'Hard' and 'Soft'.

2.19.1 Hard Reset

This causes the processor to begin executing code from address 0xFFF0 0100 in the System Flash. The following table summarizes events that may cause a hard reset:

Table 2-14

Source		Action	SYSRESET~ Generation
Hardware Events	Power-on	Hard reset all devices	Yes
	Received SYSRESET~		No
	Watchdog time-out		If System Controller
	Front-panel hard reset		
	P0 (where fitted) hard reset signal (pin C1)		
Software Events	SW_LRST bit	Hard reset excluding VMEbus Interface	No
	VCSR bit		
	SW_SYSRESET bit	Hard reset if System Controller	If System Controller

The SW_LRST, VCSR and SW_SYSRESET bits are in the Universe II PCI-VME bridge. The front panel hard reset may be disabled under software control or by fitting a jumper across link P31 pins 3 and 4.



NOTE

Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled. Similarly, integrity of Flash or EEPROM data cannot be guaranteed if a hard reset occurs during a Flash or EEPROM write cycle, respectively.

See the SDRAM section for SDRAM initialization requirements following a hard reset.

2.19.2 Soft Reset

This causes the processor to reach a recoverable state and then branch to either 0x0000 0100 or 0xFFF0 0100, depending on the IP bit in the processor's Machine State Register. The following table summarizes events that may cause a soft reset:

Table 2-15

Hardware Events	Front-panel Soft Reset
	P0 (where fitted) soft reset signal (pin C2)
	P8 (on-board connector) soft reset signal (pin 11)
Software Events	HOT_RESET bit in ISA-bridge

The front panel soft reset switch may be disabled under software control or by fitting a jumper across link P31 pins 3 and 4.

The standard boot firmware does not support the use of soft reset.

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2.19.3 VMEbus Remote Reset

Another VME master may reset the PPC8A via the Universe II control registers. This causes a hard reset.

2.19.4 Watchdog Reset

If enabled and triggered (via the Watchdog Control Register), the watchdog causes a hard reset unless re-triggered (via the Watchdog Trigger Register) every 1.6 seconds.

2.20 JTAG

The PPC8A Rev 4 & 5 board artwork cards include a JTAG Scan Bridge (Firecron JTS06BU) which interfaces with the five VME64 JTAG signals (P1-Row Z) and provides six separate, secondary chains to control/monitor the on-card devices.

By default, the Scan Bridge is disabled, allowing the PPC8A to operate normally. Fitting a jumper on the E131 link enables the device and allows external JTAG test equipment access to test and/or reprogram the card as necessary.



NOTE

If a jumper is fitted on the E131 link, the backplane *must* pull TCK (P1-Z3) low for the PPC8A to function normally, i.e. when the JTAG interface is enabled but not in use.

All the JTAG chain connections are routed to connector P1, row Z (see the Connectors section for more details).

- TRST, input, P1-Z1
- TCK, input, P1-Z3
- TMS, input, P1-Z9
- TDI, input, P1-Z7
- TDO, output, P1-Z5
- AUTOWRITE, input, P1-Z13



NOTE

As P1-Z13 is a VME64 reserved pin, the AUTOWRITE signal can be isolated from the Scanbridge by the removal of the jumper from the E200 link.

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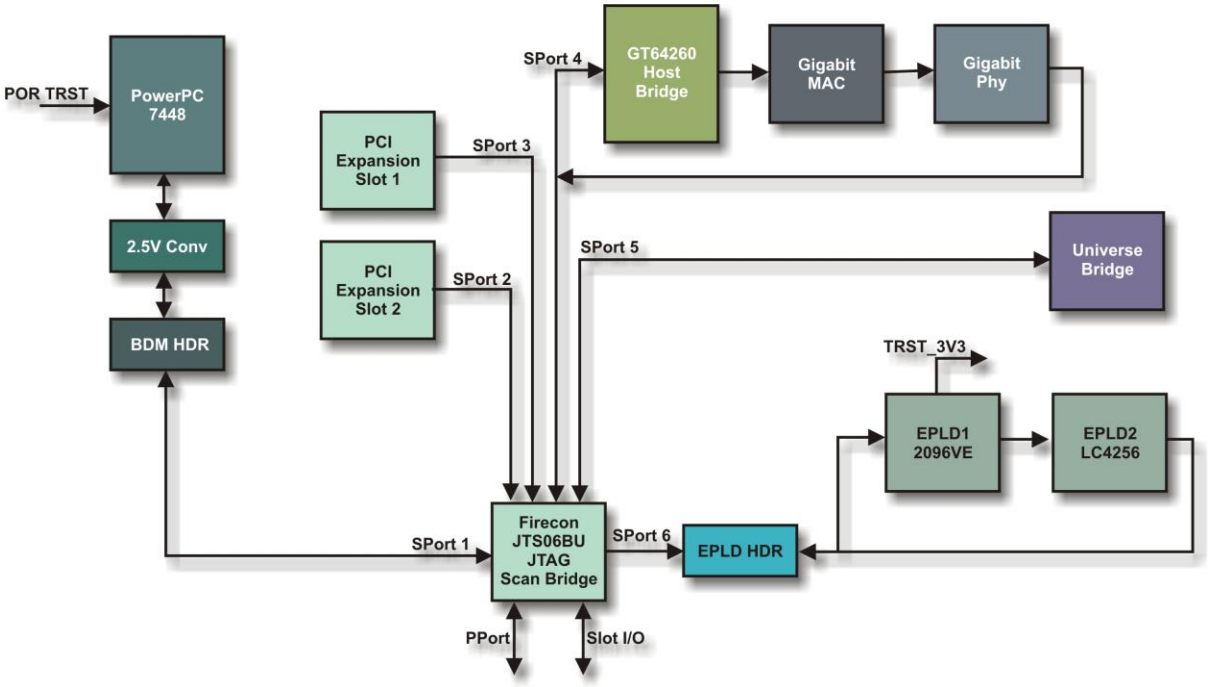
2.20.1 JTAG Clock Frequencies

Different parts in the JTAG chain may have different maximum TCK frequencies. The PPC8A has the following clock limitations:

Universe II	⇒ 20 MHz
GT64260	⇒ 3 MHz
PowerPC MC7448	⇒ 33 MHz

The JTAG clock should not exceed the maximum clock frequency of the slowest element in the JTAG chain. Using the data from the above components, the chain clock frequency should not exceed 10 MHz.

Figure 2-4 JTAG Interconnect



The Scan Bridge secondary TAPs are connected to the on-card devices as shown in the diagram, above.

Each PMC Site is on its own TAP, permitting the use of both 5V and 3.3V signaling PMCs to be used without damage.

The VME Bridge (Universe IID) is on its own TAP - to facilitate VME Boundary Scan testing using the minimum of on-card devices.

The BDM header to the processor can only be used when the Scan Bridge is disabled.

For more information on using the JTAG interface in a deployed system, contact Technical Support.

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2.21 Front Panel Sockets, Switches and Indicators

This section describes the features found on the PPC8A front panel.

2.21.1 PMC Slots

There are two PMC slots in the front panel. However, if you have not ordered PMCs for the sites, then Abaco will fit blanking plate(s) in the slot(s) for EMC protection.

If you are fitting a non-Abaco PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPC8A mechanics. This will be the case for Abaco PMCs.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel will fill the slot and will usually provide connection to the module. PMCs are delivered with a full kit of parts for mounting them.

2.21.2 Reset/Abort Switch

A momentary action toggle switch is fitted to allow generation of a hard reset or abort.

2.21.3 USB 2.0 Type A Vertical

A dedicated USB 2.0 socket from the on-card USB 2.0 controller.

2.21.4 Gigabit Ethernet RJ45

A dedicated RJ-45 socket fed from the on-card 10/100/1000BASE-T Ethernet interface.

2.21.5 Software Programmable LEDs

The PPC8A has four software programmable LEDs, mounted on the rear of the card.

DS200 is a red LED, visible through the front panel, lit by default.
DS201 is a green LED, visible through the front panel, off by default.
DS215 is a yellow LED, off by default.
DS216 is a yellow LED, off by default.
Control register 0x820 controls these LEDs.

2.21.6 SCSI LED

A yellow LED, DS217 shows SCSI activity under software control. Control register 0x808 can be used to control this LED.

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2.21.7 Gigabit Ethernet Status LEDs

Five yellow LEDs, DS202 to DS206 reflect the status of the on-card Gigabit Ethernet Interface.

DS202: lit when operating at 1000BASE link speed.
DS203: lit when operating at 100BASE link speed.
DS204: lit when operating at 10BASE link speed.
DS205: lit when the link is operating in Full Duplex mode.
DS206: lit when the link is good.

2.21.8 10/100 Ethernet Channel 0 Status LEDs

Four yellow LEDs, DS207 to DS210 reflect the status of the on-card 10/100BASE Ethernet Interface channel 0.

DS207: lit when link operating at 10BASE speed. Off indicates 100BASE speed.
DS208: indicates Receive data activity.
DS209: indicates Transmit data activity.
DS210: lit indicates that the link is good.

2.21.9 10/100 Ethernet Channel 1 Status LEDs

Four yellow LEDs, DS211 to DS214 reflect the status of the on-card 10/100BASE Ethernet Interface channel 1.

DS211: lit when link operating at 10BASE speed. Off indicates 100BASE speed.
DS212: indicates Receive data activity.
DS213: indicates Transmit data activity.
DS214: lit indicates that the link is good.

2.21.10 On-Card Supply Status LED

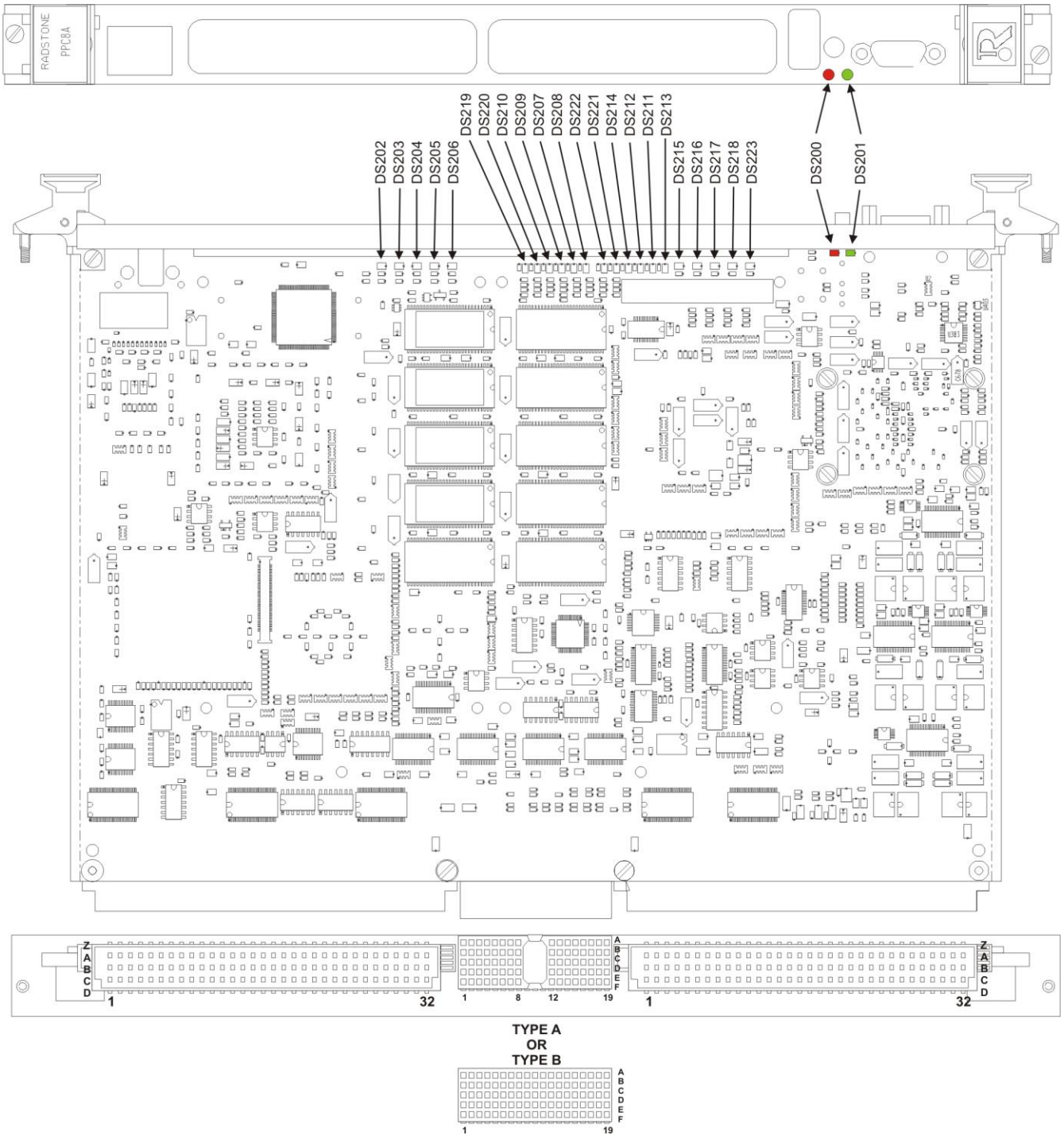
A single green LED, DS218, is used to indicate the status of the on-card power supplies. Lit indicates supplies are good.

2.21.11 JTAG Scan Bridge Enable Status LED

If the yellow LED, DS223 is lit, the on-card JTAG Scan Bridge is enabled and being accessed by off-card JTAG test equipment.

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Figure 2-5 LED Positions



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2.22 ISA Bus EPLD based Control and Status Registers

Table 2-16

ISA I/O Port	Description	Read/Write	ISA I/O Port	Description	Read/Write
0x0000 to 0x000F	Southbridge DMA 1 Control		0x0804	Memory Configuration	RO
0x0020 and 0x0021	Southbridge Interrupt 1 Control		0x0806	Memory Configuration Extend	RO
0x0040 to 0x0043	Southbridge Counter Control		0x0808	SCSI Activity LED	R/W
0x0060	Keyboard		0x080C	Equipment Present 1	RO
0x0061	Southbridge NMI Status and Control		0x080E	Equipment Present 2	RO
0x0064	Keyboard		0x0810	Equipment Present 3	RO
0x0071 and 0x0072	RTC	R/W	0x0818	Key Lock	RO
0x0078 to 0x007B	Southbridge BIOS Timer		0x0820	LEDS	R/W
0x0080 to 0x0090	Southbridge DMA Pages		0x0824	COMs	R/W
0x00A0 and 0x00A1	Southbridge Interrupt 2 Control		0x0826	RTS	R/W
0x00C0 to 0x00DE	Southbridge DMA 2 Control		0x0828	Reset	R/W
0x02E8 to 0x02EF	COM6	R/W	0x082C	Watchdog Trig	R/W
0x02F8 to 0x02FF	Southbridge COM2	R/W	0x0840	COM3/4/5/6 Enable, mode, loopback	R/W
0x03E8 to 0x03EF	COM5	R/W	0x0854	Board Revision	RO
0x03F8 to 0x03FF	Southbridge COM1	R/W	0x0858	Extended ID	RO
0x040A	Southbridge DMA Scatter/Gather	RO	0x0864	ID Link	RO
0x040B	DMA 1 Extended Mode	WO	0x0866	Motherboard Type	RO
0x0410 to 0x043F	Southbridge DMA Scatter/Gather		0x0868	Flash Write control	RO
0x0481 to 0x048B	Southbridge DMA High Pages		0x086A	Software Flash Write control	R/W
0x04D0 and 0x04D1	Southbridge Edge/Level Control		0x086E	Flash Control	R/W
0x04D6	DMA 2 Extended Mode	WO			

Where: R/W = Read/Write RO = Read Only WO = Write Only

The control and status registers exist for controlling or reading the status of the hardware. The addresses indicate the offset from ISA Bus I/O space base.

Certain registers are described in detail in the following pages. The others are registers in the ISA Bridge or other major devices, which are described in the detail in the appropriate device data sheet (which will also give the appropriate 'Type' column entry).

In the following register descriptions, the bit significance is shown in big-endian mode (i.e. from the viewpoint of the PowerPC 750 programmer) – that is the MSB is D0 and the LSB is D7.

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2.22.1 Memory Configuration Register (Port 0x0804)

This provides information on the memory fitment.

D0: Memory type:

1 = SDRAM (hard-coded, as the PPC8A can only use SDRAM).

D1: NVRAM type:

1 = NVRAM (hard-coded, as the PPC8A can only use NVRAM).

D2 to D5: Reserved, always read as '0'.

D6: SDRAM Bank 1 fitted:

0 = Fitted
1 = Not fitted.

D7: SDRAM Bank 0 fitted (hard-coded, as Bank 0 is always fitted).

2.22.2 Memory Configuration Extend Register (Port 0x0806)

This provides size information for the SDRAM and Flash memory banks.

D0 and D1: SDRAM Bank density:

Table 2-17

D0	D1	MBytes
0	0	1024
0	1	Reserved
1	0	256
1	1	512

D2 to D4: Reserved.

D5: Flash bank 2 present:

0 = Not populated
1 = Populated.

D6 and D7: Flash banks and size configuration:

Table 2-18

D6	D7	Device Size	Second Bank Populated	MBytes
0	0	512 Mbit	No	128
0	1	1024 Mbit	No	256
1	0	Reserved	N/A	Reserved
1	1	Reserved	N/A	Reserved
0	0	512 Mbit	Yes	256
0	1	1024 Mbit	Yes	512
1	0	Reserved	N/A	Reserved
1	1	Reserved	N/A	Reserved

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NOTE

One bank of Flash consists of two Spansion S29GL512N devices, each providing 16-bits of the 32-bit data width, to produce an array of non-volatile storage, 128-MBytes, 32-bits wide. The option to fit one or two banks of 1 GBit parts depends on 1 GBit devices becoming available.

2.22.3 SCSI Activity LED Register (Port 0x0808)

This allows control of the SCSI activity LED (DS217).

D0 to D6: Reserved.

D7: SCSI activity LED:

0 = LED off
1 = LED on.

2.22.4 Equipment Present Register 1 (Port 0x080C)

This provides information on hardware options and the state of the SCSI Terminator power fuse.

D0: Hardware ID0 (see the Motherboard Type Register for details)

D1: SCSI_FUSE_GOOD

0 = SCSI fuse bad
1 = SCSI fuse good.

NOTE

This is a re-settable fuse that re-engages when the overcurrent condition is removed.

D2: PRSNT1_2~ (BUSMODE1 PMC site 2):

0 = Slot 2 PMC present
1 = Slot 2 empty.

D3: PRSNT1_1~ (BUSMODE1 PMC site 1):

0 = Slot 1 PMC present
1 = Slot 1 empty.

D4: PCI1 bus speed (PMC PCI Bus M66EN signal):

0 = 33 MHz
1 = 66 MHz.

D5 and D6: L3 Cache Size (hardwired to 0x3, as 7448 has no L3 memory).

D7: Reserved, always reads '0'.

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2.22.5 Equipment Present Register 2 (Port 0x080E)

This provides information on hardware options fitted to the PPC8A.

D0: Universe II fitted:

1 = Fitted (hardwired as the VME Bridge is always fitted).

D1: Reserved, always reads '0'.

D2: COMs 3 to 6 fitted:

0 = Not fitted (PMC site 2 User rear I/O to P2)
1 = Fitted.

D3: USB 1.1 fitted:

1 = Fitted (hardwired as this is no longer a build option).



NOTE

The design includes software controlled analog switches that control whether Keyboard/Mouse or USB 1.1 is routed to front and/or read. See the register at offset 0x0870 for more information.

D4: LPT fitted:

1 = Fitted (hardwired as this is no longer a build option).

D5 and D6: L3 Cache speed (hardwired to 0x2, as the MC7448 does not support L3 memory).

D7: L3 Cache type:

0 = Standard data rate (hardwired as the MC7448 does not support L3 memory).

2.22.6 Equipment Present Register 3 (Port 0x0810)

This provides information on hardware options fitted to the PPC8A.

D0 to D3: Reserved. Always reads '0'.

D4: PMC I/O voltage:

0 = PMC Voltage link selectable (hardwired, see the E30 Link description).

D5: 3.3Volt PMC power:

0 = Powered by on-board power supply
1 = Power from taken from 3.3V pins on P0/VME connectors

D7 and D6: SCSI clock speed:

Table 2-19

D7	D6	Speed (MHz)
0	0	Reserved
0	1	40
1	0	80
1	1	Reserved

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2.22.7 Key Lock Register (Port 0x0818)

This provides information on the state of the keylock signal. See the Keylock section for more details.

D0 to D6: Reserved.

D7: Keylock

0 = Keylock signal low
1 = Keylock signal high.

2.22.8 LED Register (Port 0x0820)

This controls the four user LEDs fitted to the PPC8A. See the Software Programmable LEDs section for the location of these LEDs.

D0: SCSI_TERM_REQ:

0 = SCSI terminator not required (no jumper fitted on the SCSI link)
1 = SCSI terminator required (jumper fitted on the SCSI link).

D1: SCSI_TERM_EN:

0 = Disable SCSI terminator
1 = Enable SCSI terminator.



NOTE

If a jumper is fitted on the SC_TRM (E128) link, the on-card terminator is enabled regardless of this bit. If no jumper is fitted on the link, the terminator can be enabled, by software, using this bit.

D2 & D3: Selects the NVRAM page. The default is (0,0):



NOTE

The 32 KByte Simtek NVRAM device is accessed as four pages of 8 KBytes. These register bits control the upper two address lines to the device.

D4: DS215, Yellow 1:

0 = LED off, OFFLINE~ high (default at power-up)
1 = LED on, OFFLINE~ low.

D5: DS216, Yellow 2:

0 = LED off, SYSFAIL~ high (default at power-up)
1 = LED on, SYSFAIL~ low.

D6: DS200, Red and SYSFAIL~ (P0 B1) signal:

0 = LED off
1 = LED on (default at power-up).

D7: DS201, Green and SYSFAIL~ (P0 B2) signal:

0 = LED off (default at power-up)
1 = LED on.

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2.22.9 COMs Register (Port 0x0824)

This provides control for COM3 and COM4, the Clocks, and interface configuration.



NOTE

Software should select the required interface mode before the respective transceiver is enabled, to prevent the PPC8A from driving out a potentially damaging voltage.

D0: COM3_CLK_EN, enables the TSCLK3 signal out onto COM3_TT (transmit clock):

0 = Disabled
1 = Enabled.

D1: TSCLK3_EN:

0 = Disabled
1 = Enabled.

When enabled, COM3_RT (receive transmit clock) is linked to TSCLK3.

D2: COM3_RS232, selects the interface mode of COM3:

0 = RS232 (default)
1 = RS422.

D3: COM3_TX_EN, enables the COM3 interface transceiver:

0 = Disabled (default)
1 = Enabled.

D4: COM4_CLK_EN, enables the TSCLK4 signal out on to COM4_TT (transmit clock):

0 = Disabled
1 = Enabled.

D5: TSCLK4_EN:

0 = Disabled
1 = Enabled.

When enabled, COM4_RT (receive transmit clock) is linked to TSCLK4.

D6: COM4_RS232, selects the interface mode of COM4:

0 = RS232 (default)
1 = RS422.

D7: COM4_TX_EN, enables the COM4 Interface transceiver:

0 = Disabled (default)
1 = Enabled.

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2.22.10 RTS Register (Port 0x0826)

This provides options for when the COMs channel data transmitters are enabled.

D0: Controls the DEZ1 input to the COM3 buffer. RS232 mode only. (For test use).

D1: COM3 DTR output. RS232 mode only.

D3 & D2: COM3 transmitter function select:

Table 2-20

D3	D2	Transmit Function Selected
0	0	Not enabled
0	1	Enabled
1	0	Enabled by RTS3
1	1	Enabled by RTS3 & stretched

D4: Controls the DEZ1 input to the COM4 Buffer. RS232 mode only. (For test use).

D5: COM4 DTR output. RS232 mode only.

D7 & D6: COM4 transmitter function select:

Table 2-21

D7	D6	Transmit Function Selected
0	0	Not enabled
0	1	Enabled
1	0	Enabled by RTS4
1	1	Enabled by RTS4 & stretched

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2.22.11 Watchdog Register (Port 0x0828)

This controls the Watchdog reset features of the PPC8A.

D0: Last reset was a Watchdog:

0 = Normal reset
1 = Last board reset was caused by a Watchdog timeout.

D1: Enable NMI from GT-64260:

0 = Disabled
1 = NMI can be generated from the GT-64260B CPUINT output pin.

D2 to D5: Reserved. Reads as '0'.

D6: Watchdog enable:

0 = Trigger output disabled
1 = Trigger output enabled.

Once the trigger output is enabled, the Watchdog Trigger Register (0x082C) needs to be accessed every 1.5 seconds, or a hard reset of the entire PPC8A occurs. Also, once set to '1', it cannot be returned to '0' by software.

D7: RESET_SW_EN (output):

0 = Disable the front panel reset switch logic
1 = Enable the front panel reset switch logic.



NOTE

This bit has no effect if the switch logic is not present or if a jumper is fitted on the RST_EN (E130) link.

2.22.12 Watchdog Trigger Register (Port 0x082C)

This is a dummy register that is written to trigger the Watchdog.

D0 to D7: Don't care for writes; undefined for reads.



NOTE

Data written is not used and reads do not trigger the Watchdog.

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2.22.13 COM5/6 Control Register (0x840)

D0: COM5/6 enable:

0 = Transceiver disabled (default)
1 = Transceiver enabled.

D1: COM5/6 interface mode:

0 = RS232 mode (default)
1 = RS422 mode.

NOTE
This bit controls the mode of both COM5 and COM6. They cannot be set to different standards independently. COM5/6 does not support RS485 multidrop.

D2: COM5/6 loopback control:

0 = Loopback mode
1 = Normal mode (default).

NOTE
In loopback mode, the LTC1334 transceiver loops all transmitted data back onto the receiver signal, but all data is also transmitted off-card.

D3: Not used, returns '0'.

D4: COM3/4 loopback control:

0 = Loopback mode
1 = Normal mode (default).

NOTE
In loopback mode, the LTC1334 transceiver loops all transmitted data back onto the receiver signal, but all data is also transmitted off-card.

D5 to D7: Not used, returns '0'.

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2.22.14 Board Revision Register (Port 0x0854)

This provides information on the build state of the PPC8A.

D0 to D2: Number revision of hardware build state:

1 = Revision 1
2 = Revision 2
3 = Revision 3
4 = Revision 4
5 = Revision 5
All other values are reserved.

D3 to D7: Letter revision of hardware build state:

0x0 = Revision A
0x1 = Revision B
...
0x18 = Revision Y
0x19 = Revision YA
...
0x1F = Revision YG

2.22.15 Extended ID Register (Port 0x0858)

This provides the board hardware type.

D0 to D7: Board ID:

0x17 = PPC8A – 7448.

Any other pattern means the board is not a PPC8A

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2.22.16 Slot ID/Geographical Address Link Register (Port 0x0864)

This allows software to read the Board ID links (E124, E125, E126, E127) or the VME Geographical Address pins, depending on the status of the LNKSEL Link (E220). If no jumper is fitted on the LNKSEL link, this register reports the status of the lines from the backplane (P1). If a jumper is fitted on the LNKSEL link, this register reports the status of the four on-card links. The two sources are separate. The source not reported here is reported in a new register at offset 0x0880.

D0 to D2: Reserved

D3: '0'/GA4

0 = Line is low
1 = Line is high.



NOTE

Bit D3 returns '0' if the selected source is the on-card links (a jumper is fitted on LNKSEL).

D4: E124/GA3

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

D5: E125/GA2

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

D6: E126/GA1

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

D7: E127/GA0

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

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2.22.17 Motherboard Type Register (Port 0x0866)

This provides information on the type of motherboard and SDRAM ECC operation. The bits used in this register are compatible with the other members of the current Abaco PPC product range.

D0: HW_ECC enable (controlled by the ECC_REQ Link (E123)):

0 = Non-ECC mode
1 = ECC requested.

D1: PLL2 (see table below).

D2: ECC_TYPE:

1 = ECC (hardwired, as only ECC protection is supported).

D3: ECC capability:

1 = Card is ECC capable (hardwired, as ECC RAM device is always fitted).

D4: PLL1 (see table below)
D5: PLL0 (see table below)

Table 2-22

PLL2	PLL1	PLL0	Bus Speed (MHz)
1	1	1	Reserved
1	1	0	Reserved
1	0	1	Reserved
1	0	0	133
0	1	1	Reserved
0	1	0	100
0	0	1	66
0	0	0	Reserved

D6 and D7: Hardware ID2 and ID1 respectively. Used with Hardware ID0 (bit 0 of Equipment Present Register 1) to define the hardware type as follows:

Table 2-23

ID2 to ID0	Hardware Type
111	PPC1/PPC3
110	PPC2
101	PPC1A
100	PPC2A
011	PPC4
010	PPC4A
000	Use Extended ID

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2.22.18 Flash Write Protection Register (Port 0x0868)

This provides information on the Flash protection.

D0: Flash Protection Password Visibility Link (E5 (PWEN)):

0 = Jumper not fitted
1 = Jumper fitted.

D1: Status of the P2-Z1 or P0-A2, PASSW_EN_BP~ signal:

0 = Signal not active (pin high)
1 = Signal active (pin low).

D2: Flash Boot Write Enable Link status:

0 = Jumper not fitted
1 = Jumper fitted.

D3: Flash User Write Enable Link status:

0 = Jumper not fitted
1 = Jumper fitted.

D4: Always reads '0'.

D5: Writes to Flash Recovery section:

0 = Disabled
1 = Enabled.

D6: Writes to Flash Boot section:

0 = Disabled
1 = Enabled.

D7: Writes to Flash User section:

0 = Disabled
1 = Enabled.

NOTES

If a jumper is fitted on link E5 (PWEN) or the backplane signal PASSW_EN_BP is pulled low, the current Flash Protection Password at offsets 0x18 to 0x1F through CS0 becomes visible, otherwise the password register reads as "********".

Bits D2 to D7 are retained for legacy but do not have any impact on hardware Flash Protection for rev 4/5 boards.

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2.22.19 Flash Software Write Control Register (Port 0x086A)

This provides additional Flash write protection. It is used in conjunction with the E3, E5 and E9 links.

D0 to D5: Not used, always reads '0'.

D6: Boot Flash software write enable:

0 = Boot Flash write inhibited (default)
1 = Boot Flash write enabled.

D7: User Flash software write enable:

0 = User Flash write inhibited (default)
1 = User Flash write enabled.



NOTE

Bits D6 and D7 are retained for legacy, but do not have any impact on hardware Flash Protection for rev 4/5 boards.

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2.22.20 Flash Control Register (Port 0x086E)

This provides status and control signals for the Boot sections of the Flash devices.

When the PPC8A is reset, this register is reset to reflect the status of the Boot links (E8, E4 & E7). After boot, software can override these link settings by writing to bits D5 & D7 in this register.

Status signals BOOT_ALTERNATE, BOOT_FROM_VME and BOOT_RECOVERY show the real link settings. Signals SELECT_ALTERNATE and SELECT_RECOVERY show what image is really selected.

D0: NVRAM Write Protect:

0 = NVRAM is write protected
1 = Writes to NVRAM are enabled.

D1: BOOT_ALTERNATE (reflects the status of user link E8). This bit is read-only.

0 = Jumper not fitted
1 = Jumper fitted.

D2: VME_BOOT_MODE (reflects the status of user link E4):

0 = Jumper not fitted
1 = Jumper fitted.

This bit is read-only.

D3: BOOT_RECOVERY (reflects the status of user link E7):

0 = Jumper not fitted
1 = Jumper fitted.

This bit is read-only.

D4: Reserved. Reads '0'.

D5: SELECT_ALTERNATE (see table below).

D6: FLASH_CONTROL_WRITTEN:

0 = Register not written
1 = Register written.

D7: SELECT_RECOVERY

Table 2-24

SELECT_ALTERNATE	SELECT_RECOVERY	Area Selected
0	0	Main
0	1	Recovery (BANC)
1	0	Alternate
1	1	Extended

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2.22.21 Keyboard/Mouse and USB 1.1 Control Register (Port 0x0870)

This is used to control which on-card resource is routed out of the rear (P2) and the front I/O connector (P19).

NOTE

These bits do not enable/disable the Keyboard/Mouse or USB 1.1 on-card resources, only which resource is routed off card. If Keyboard/Mouse is routed out both front and rear, the same signals drive both ports. If USB 1.1 is selected, ports 0 and 1 are routed to the rear and ports 2 and 3 to the front - routing to front and rear are independent.

D0 to D3: Reserved.

D4: Enable Keyboard/Mouse to front (P19):

0 = Disabled (default)
1 = Enabled.

D5: Enable USB 1.1 to front (P19):

0 = Disabled (default)
1 = Enabled.

NOTE

Register bit D4 cannot be set if D5 is set, and vice versa.

D6: Enable Keyboard/Mouse to rear (P2):

0 = Disabled (default)
1 = Enabled.

D7: Enable USB 1.1 to rear (P2):

0 = Disabled (default)
1 = Enabled.

NOTE

Register bit D6 cannot be set if D7 is set, and vice versa.

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2.22.22 Alternative Geographical Address Register (Port 0x0880)

This reports the Slot ID bus not reported at 0x0864. If LNKSEL (E220) is open, this register reports the status of the on-card Slot ID links. If a jumper is fitted on the LNKSEL (E220) link, this register reports the status of the backplane Slot ID lines.

D0 to D2: Reserved.

D3: '0'/GA4

0 = Line is low
1 = Line is high.



NOTE

Bit D3 returns '0' if the selected source is the on-card links (no jumper is fitted on the LNKSEL link).

D4: E124/GA3

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

D5: E125/GA2

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

D6: E126/GA1

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

D7: E127/GA0

0 = Line is low/no jumper fitted on link
1 = Line is high/jumper fitted on link.

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2.23 EPLD-based Control and Status Registers on CS0

These are accessed via the GT64260B CS0 address window (see the GT64260B data sheet for more information on setting up this address window).

Table 2-25

CS0 I/O Port	Description	Type
0x0000	Board ID	RO
0x0002	Last reset source	RO
0x0003	Reset	R/W
0x0004 to 0x0007	Board ID string	RO
0x0018	Flash Protection Password - upper 32-bits	RO
0x001C	Flash Protection Password - lower 32-bits	RO

Where: R/W = Read/Write RO = Read Only.

In the following, the MSB is D0 and the LSB is D7.

2.23.1 Board ID Register (Port 0x0)

This provides the board hardware type.

D0 to D7: Board ID register:

0x17 = PPC8A.

Any other pattern means that the board is not a PPC8A.

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2.23.2 Last Reset Source Register (Port 0x2)

This provides information about what caused the last reset.

D0 to D2: Reserved.

D3: GT64260B Watchdog time out:

0 = Did not cause the last reset
1 = Caused the last reset.

D4: MAX706 Watchdog timeout:

0 = Did not cause the last reset
1 = Caused the last reset.

D5: Reset switch:

0 = Did not cause the last reset
1 = Caused the last reset.

D6: Universe:

0 = Did not cause the last reset
1 = Caused the last reset.

D7: RiscWatch connector reset driven:

0 = Did not cause the last reset
1 = Caused the last reset.

2.23.3 Reset Register (Port 0x3)

This provides a 4-bit register that is not cleared or changed on any reset apart from a power up (when it is cleared to '0').

D0 to D3: Reserved. Reads '0'.

D4 to D7: 4-bit register.

2.23.4 Board ID String Registers (Ports 0x4 to 0x7)

These provide a board ID string, which shows "PPC8" when read as a 32-bit value.

Table 2-26

Port	Bits	Value (Hex)	Value (ASCII)
0x4	D0 to D7	0x50	P
0x5	D0 to D7	0x50	P
0x6	D0 to D7	0x43	C
0x7	D0 to D7	0x38	8

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2.23.5 Flash Persistent Protection Password Registers (Ports 0x18 to 0x1F)

These provide a 64-bit string controlled by the state of the PWEN Link (E5) and/or the PASSW_EN_BP~ line (P0/P2). If either the link is fitted or the backplane line is low, the value returned is the current password programmed into the Flash Bank Persistent Mode Protection Password register. If the link field is open and the backplane signal is high, the read value is 0x2A2A2A2A2A2A2A2A (ASCII for "********").

2.24 EPLD-based Status Registers on CS1

These are accessed via the GT64260B CS1 address window (see the GT64260B data sheet for more information on setting up this address window).

Table 2-27

CS1 I/O Port (Hex)	Description	Type
0000 to 0003	Checker board 1	RO
0004 to 0007	Checker board 2	RO

Where: RO = Read Only.

2.24.1 Checker Board 1 Registers (Port 0x0 to 0x3)

These provide a checker board value of 0x5555 5555 when read as a 32-bit value.

2.24.2 Checker Board 2 Registers (Port 0x4 to 0x7)

These provide a checker board value of 0xAAAA AAAA when read as a 32-bit value.

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2.25 Interrupts and Error Reporting

The following table shows the various external interrupt sources to the processor and their relative priorities. It also shows whether the previous state of the processor is recoverable.

Table 2-28

Priority	Interrupt	Cause	Recoverability
0	System Reset	Power on, Hard reset	Non-recoverable
1	Machine Check	Address or Data Parity error, Machine Check Input (MCP~), Non-maskable Interrupt (NMI~)	Non-recoverable in most cases
2	System Reset	Soft reset	Recoverable unless Machine Check occurs
3	System Management Interrupt	SMI~ input	Recoverable unless Machine Check or System Reset occurs
4	External Interrupt	INT~ input	Recoverable unless Machine Check or System Reset occurs

2.25.1 System Resets

See the Resetting the PPC8A in this section.

2.25.2 Machine Check Exception

The Southbridge can be configured to drive the signal NMI in certain conditions. The hardware on the PPC8A routes this signal to the CPU as the MCP~ (Machine Check) interrupt.

The Southbridge can drive this signal due to the following conditions:

- PCI bus error
- PCI SERR~ signal driven active

The PCI SERR~ signal can be driven low by other PCI devices to report an error condition.

The processor may be configured to take a machine check exception or enter the checkstop state.

2.25.3 System Management Interrupt (SMI~)

The System Management Interrupt pin of the CPU is connected to the GT64260B. This allows the GT64260B to interrupt the processor for events such as an SDRAM parity error.

To allow the GT64260B to provide a SMI~ interrupt to the CPU, the output pin MPP[8] needs to be set to Int[0]* (see the GT64260B register MPP Control 1 - offset 0xF004). The events that can cause this interrupt to be driven are configured via register CPU Int[0]* (0xE60).

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2.25.4 External Interrupt (INT~)

The processor external interrupt pin (INT~) is asserted for a pending interrupt from the interrupt controller in the Southbridge.

Interrupt priorities and modes are assigned by the firmware running on the PPC8A.

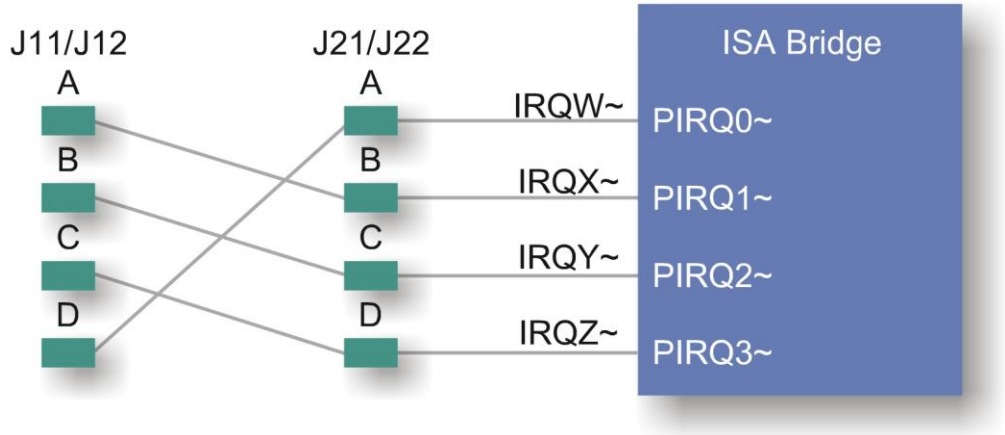
2.25.5 PCI Interrupts

There are four interrupt lines for the PMC expansion slots on the motherboard and the PMC carrier. These are connected to the PIRQ~ inputs of the interrupt controller. The PIRQ~ inputs may be routed to any IRQ that is set to level sensitive mode.

The interrupt routing follows the recommendations in the PCI specification and the PCI system design guide with a “rotation” between each slot.

The interrupt lines for the two on-board PMC slots are routed as shown below:

Figure 2-6 PCI Interrupts



Two single function PMCs (which always use INTA~) can use unique IRQs with appropriate programming of the interrupt controller.

2.26 Keylock

The keylock input signal allows the software to interrogate an external keyswitch. For example, the boot firmware could request a password if the keyswitch is in the locked position and a password is set up in the NVRAM.

The keylock signal defaults to high if no external connection is made.

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3 • Connectors

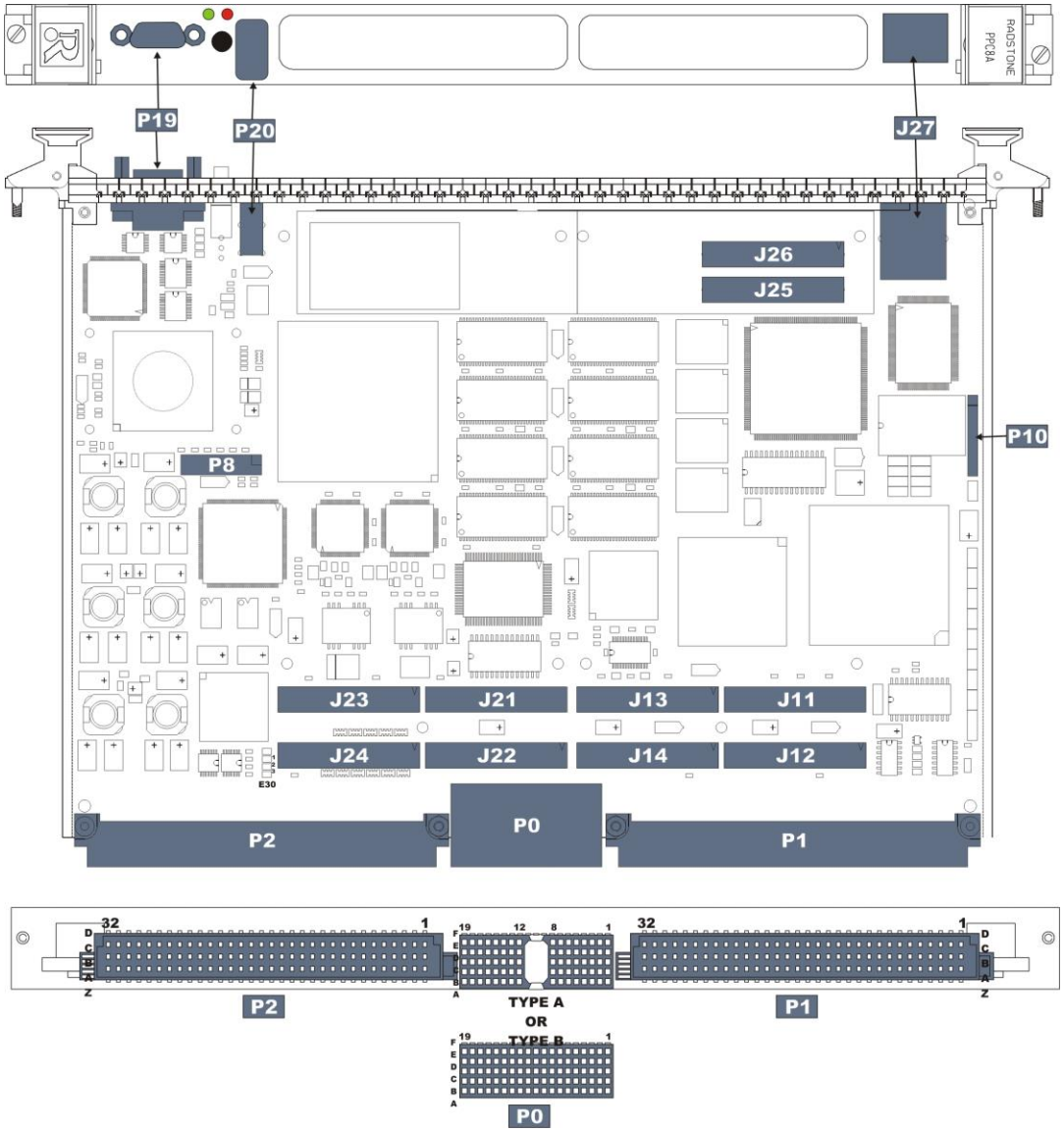
This section gives the pinouts and signal descriptions for the connectors on the PPC8A. The following table shows the function of the connectors on the PPC8A:

Table 3-1

Connector	Function
P1	VMEbus
P2	VMEbus and rear I/O
P0	PMC site 1 I/O
J11, J12, J13, J14	PMC (site 1)
J21, J22, J23, J24	PMC (site 2)
J25, J26	I/O expansion
J27	Ethernet (RJ45)
P8	RISCWatch
P10	EPLD JTAG Programming (factory use only)
P19	General I/O (keyboard, mouse, COMM1/2 etc.)
P20	USB 2.0

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Figure 3-1 Connector Positions



3.1 P1 Backplane Connector

The PPC8A P1 connector conforms to the VME64x standard. For pin assignments and signal descriptions, see the Standard Interfaces section.

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3.2 P2 Backplane Connector

3.2.1 Standard Pinout - J24 Connector Fitted

Table 3-2 P2 Pin Assignments

Pin	Row Z	Row A	Row B	Row C	Row D
1	PMC2_IO_2[1]	DB0~ (SCSI)	+5V	RX0+	PMC2_IO_1[1]
2	GND	DB1~ (SCSI)	GND	RX0-	PMC2_IO_3[1]
3	PMC2_IO_5[1]	DB2~ (SCSI)	Reserved	TX0+	PMC2_IO_4[1]
4	GND	DB3~ (SCSI)	A24	TX0-	PMC2_IO_6[1]
5	PMC2_IO_8[1]	DB4~ (SCSI)	A25	RX1+	PMC2_IO_7[1]
6	GND	DB5~ (SCSI)	A26	RX1-	PMC2_IO_9[1]
7	PMC2_IO_11[1]	DB6~ (SCSI)	A27	VSYNC[4]	PMC2_IO_10[1]
8	GND	DB7~ (SCSI)	A28	STROBE~[2]	PMC2_IO_12[1]
9	PMC2_IO_14[1]	DBP0~ (SCSI)	A29	LPTD0[2]	PMC2_IO_13[1]
10	GND	ATN~ (SCSI)	A30	LPTD1[2]	PMC2_IO_15[1]
11	PMC2_IO_17[1]	BSY~ (SCSI)	A31	LPTD2[2]	PMC2_IO_16[1]
12	GND	ACK~ (SCSI)	GND	LPTD3[2]	PMC2_IO_18[1]
13	PMC2_IO_20[1]	RST~ (SCSI)	+5V	LPTD4[2]	PMC2_IO_19[1]
14	GND	MSG~ (SCSI)	D16	LPTD5[2]	PMC2_IO_21[1]
15	PMC2_IO_23[1]	SEL~ (SCSI)	D17	LPTD6[2]	PMC2_IO_22[1]
16	GND	C/D (SCSI)	D18	LPTD7[2]	PMC2_IO_24[1]
17	PMC2_IO_26[1]	REQ~ (SCSI)	D19	ACK~[2]	PMC2_IO_25[1]
18	GND	I/O (SCSI)	D20	BUSY[2]	PMC2_IO_27[1]
19	PMC2_IO_29[1]	TERMPWR (SCSI)	D21	PERROR[2]	PMC2_IO_28[1]
20	GND	USBP0/MOUSE_CLK[3]	D22	SELECT[2]	PMC2_IO_30[1]
21	PMC2_IO_32[1]	USBP0~/MOUSE_DATA[3]	D23	AUTOFD~[2]	PMC2_IO_31[1]
22	GND	USB_5V/KBD_5V[3]	GND	ERR~[2]	PMC2_IO_33[1]
23	PMC2_IO_35[1]	USBP1/KBD_CLK[3]	D24	INIT~[2]	PMC2_IO_34[1]
24	GND	USBP1~/KBD_DATA[3]	D25	SLCTIN~[2]	PMC2_IO_36[1]
25	PMC2_IO_38[1]	COM2_TXD	D26	SPEAKER_OUT	PMC2_IO_37[1]
26	GND	COM2_RXD	D27	KEYLOCK_IN	PMC2_IO_39[1]
27	PMC2_IO_41[1]	COM2_RTS	D28	COM1_TXD	PMC2_IO_40[1]
28	GND	HSYNC[4]	D29	COM1_RXD	PMC2_IO_42[1]
29	PMC2_IO_44[1]	COM2_CTS	D30	COM1_RTS	PMC2_IO_43[1]
30	GND	RED[4]	D31	COM1_CTS	PMC2_IO_45[1]
31	PMC2_IO_46[1]	GREEN[4]	GND	TX1+	GND
32	GND	BLUE[4]	+5V	TX1-	+5V

[1] Indicates build option between PMC site 2 rear I/O and COM3/COM4/COM5/COM6 (see table 3-3).

[2] Indicates lines which could be Parallel Port or GPIO (Floppy) depending on software (see table 3-4).

[3] Indicates lines which could be Keyboard/Mouse or USB 1.1 depending on software.

[4] Video signals.

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3.2.2 COM3/4/5/6 Build Option Fitted

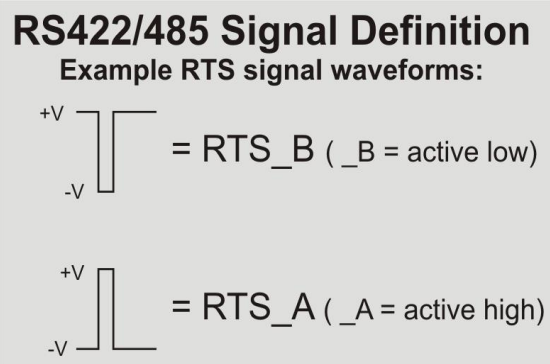
If the COM3/4/5/6 build-option is selected, P2 rows Z and D are as follows:

Table 3-3 P2 Pin Assignments

Pin	Row Z		Row D	
	RS422/485	RS232	RS422/485	RS232
1	PASSW_EN_BP~		COM3_TX_A	COM3_TXD
2	GND		COM3_TX_B	No Connection
3	EXTRESET		COM3_RX_A	COM3_RXD
4	GND		COM3_RX_B	No Connection
5	EXTABORT~		COM3_RTS_A	COM3_RTS
6	GND		COM3_RTS_B	No Connection
7	J24 Pin 11		COM3_CTS_A	COM3_CTS
8	GND		COM3_CTS_B	No Connection
9	COM4_TX_A	COM4_TXD	COM5_TX_A	COM5_TXD
10	GND		COM5_TX_B	COM5_RTS
11	COM4_TX_B	No Connection	COM6_TX_A	COM6_TXD
12	GND		COM6_TX_B	COM6_RTS
13	COM4_RX_A	COM4_RXD	COM5_RX_A	COM5_RXD
14	GND		COM5_RX_B	COM5_CTS
15	COM4_RX_B	No Connection	COM3_TT_A	COM3_CLKOUT
16	GND		COM3_TT_B	No Connection
17	COM4_CTS_A	COM4_CTS	COM3_ST_A	No Connection
18	GND		COM3_ST_B	No Connection
19	COM4_CTS_B	No Connection	COM3_RT_A	COM3_CLKIN
20	GND		COM3_RT_B	No Connection
21	J24 Pin 32		COM4_RTS_A	COM4_RTS
22	GND		COM4_RTS_B	No Connection
23	J24 Pin 35		COM6_RX_A	COM6_RXD
24	GND		COM6_RX_B	COM6_CTS
25	COM4_ST_A	No Connection	J24 Pin 37	
26	GND		J24 Pin 39	
27	COM4_ST_B	No Connection	COM4_TT_A	COM4_CLKOUT
28	GND		COM4_TT_B	No Connection
29	COM4_RT_A	COM4_CLKIN	J24 Pin 43	
30	GND		J24 Pin 45	
31	COM4_RT_B	No Connection	GND	
32	+5V		COM4_RT_B	No Connection

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Figure 3-2 RS422/485 Signal Definition



3.2.3 GPIO Pins

The following table shows alternate P2 row C pin functions:

Table 3-4 P2 Pin Assignments

Pin	GPIO	Floppy	LPT
8	GPIO0	RDATA~	STROBE~
9	GPIO1	WGATE~	LPTD0
10	GPIO2	WDATA~	LPTD1
11	GPIO3	HDSEL~	LPTD2
12	GPIO4	FD_DIR~	LPTD3
13	GPIO5	STEP~	LPTD4
14	GPIO6	DSKCHG~	LPTD5
15	GPIO7	DRV2~	LPTD6
16	GPIO8	DRV1~	LPTD7
17	GPIO9	MOT0~	ACK~
18	GPIO10	MOT1~	BUSY
19	GPIO11	WPROT~	PERROR
20	GPIO12	TRK0~	SELECT
21	GPIO13	INDEX~	AUTOFD~
22	GPIO14	DENSEL	ERR~
23	GPIO16	GPIO16 (ACGAME3)	INIT~
24	GPIO17	GPIO17 (ACGAME4)	SLCTIN~

NOTE

There is no connection to GPIO15 to the Southbridge from the P2 connector.
GPIO or Parallel Port (LPT) or Floppy selection is via software control of the Southbridge.

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3.3 P0 Backplane Connector

3.3.1 Type B (95-way)

P0 is routed to J14 and partially to J24.

NOTE

Due to the large amount of I/O required to be handled by the PPC8A, Type B connectors are preferred to the Type A (80-pin) shown overleaf, and are fitted by default if no type is specified.

Table 3-5 Type B P0 Pin Assignments

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1		P0_B1	EXTRESET~	USB2_VCC	USB2_GND	GND
2	PASSW_EN_BP~	P0_B2	EXTABORT~	USB2_DP2	USB2_DM2	GND
3	3.3V[a]	3.3V[a]	3.3V[a]	+5V	+5V	GND
4	PMC1_IO_5	PMC1_IO_4	PMC1_IO_3	PMC1_IO_2	PMC1_IO_1	GND
5	PMC1_IO_10	PMC1_IO_9	PMC1_IO_8	PMC1_IO_7	PMC1_IO_6	GND
6	PMC1_IO_15	PMC1_IO_14	PMC1_IO_13	PMC1_IO_12	PMC1_IO_11	GND
7	PMC1_IO_20	PMC1_IO_19	PMC1_IO_18	PMC1_IO_17	PMC1_IO_16	GND
8	PMC1_IO_25	PMC1_IO_24	PMC1_IO_23	PMC1_IO_22	PMC1_IO_21	GND
9	PMC2_IO_50	PMC2_IO_49	PMC2_IO_62	PMC2_IO_56	PMC2_IO_55	GND
10	PMC2_IO_48	PMC2_IO_47		PMC2_IO_64	PMC2_IO_63	GND
11	PMC2_IO_52	PMC2_IO_51	PMC2_IO_61	PMC2_IO_58	PMC2_IO_57	GND
12	PMC1_IO_30	PMC1_IO_29	PMC1_IO_28	PMC1_IO_27	PMC1_IO_26	GND
13	PMC1_IO_35	PMC1_IO_34	PMC1_IO_33	PMC1_IO_32	PMC1_IO_31	GND
14	PMC1_IO_40	PMC1_IO_39	PMC1_IO_38	PMC1_IO_37	PMC1_IO_36	GND
15	PMC1_IO_45	PMC1_IO_44	PMC1_IO_43	PMC1_IO_42	PMC1_IO_41	GND
16	PMC1_IO_50	PMC1_IO_49	PMC1_IO_48	PMC1_IO_47	PMC1_IO_46	GND
17	PMC1_IO_55	PMC1_IO_54	PMC1_IO_53	PMC1_IO_52	PMC1_IO_51	GND
18	PMC1_IO_60	PMC1_IO_59	PMC1_IO_58	PMC1_IO_57	PMC1_IO_56	GND
19	+5V	PMC1_IO_64	PMC1_IO_63	PMC1_IO_62	PMC1_IO_61	GND

a. The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on the VME P1 connector. If the external PMC option is fitted, then this is routed to the PMC connectors J12/J22, and capacitively decoupled to ground.

NOTE

Analog signals should not be routed through P0.

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3.3.2 Type A (80-way)

P0 is routed to J14.

NOTE

Due to the large amount of I/O required to be handled by the PPC8A, Type B (95-way) connectors are preferred to Type A, and are fitted by default no type is specified.

Table 3-6 Type A P0 Pin Assignments

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1		P0_B1	EXTRESET~	USB2_VCC	USB2_GND	GND
2	PASSW_EN_BP~	P0_B2	EXTABORT~	USB2_DP2	USB2_DM2	GND
3	3.3V[a]	3.3V[a]	3.3V[a]	+5V	+5V	GND
4	PMC1_IO_5	PMC1_IO_4	PMC1_IO_3	PMC1_IO_2	PMC1_IO_1	GND
5	PMC1_IO_10	PMC1_IO_9	PMC1_IO_8	PMC1_IO_7	PMC1_IO_6	GND
6	PMC1_IO_15	PMC1_IO_14	PMC1_IO_13	PMC1_IO_12	PMC1_IO_11	GND
7	PMC1_IO_20	PMC1_IO_19	PMC1_IO_18	PMC1_IO_17	PMC1_IO_16	GND
8	PMC1_IO_25	PMC1_IO_24	PMC1_IO_23	PMC1_IO_22	PMC1_IO_21	GND
9	Keying	Keying	Keying	Keying	Keying	
10	Keying	Keying	Keying	Keying	Keying	
11	Keying	Keying	Keying	Keying	Keying	
12	PMC1_IO_30	PMC1_IO_29	PMC1_IO_28	PMC1_IO_27	PMC1_IO_26	GND
13	PMC1_IO_35	PMC1_IO_34	PMC1_IO_33	PMC1_IO_32	PMC1_IO_31	GND
14	PMC1_IO_40	PMC1_IO_39	PMC1_IO_38	PMC1_IO_37	PMC1_IO_36	GND
15	PMC1_IO_45	PMC1_IO_44	PMC1_IO_43	PMC1_IO_42	PMC1_IO_41	GND
16	PMC1_IO_50	PMC1_IO_49	PMC1_IO_48	PMC1_IO_47	PMC1_IO_46	GND
17	PMC1_IO_55	PMC1_IO_54	PMC1_IO_53	PMC1_IO_52	PMC1_IO_51	GND
18	PMC1_IO_60	PMC1_IO_59	PMC1_IO_58	PMC1_IO_57	PMC1_IO_56	GND
19	+5V	PMC1_IO_64	PMC1_IO_63	PMC1_IO_62	PMC1_IO_61	GND

a. The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on the VME P1 connector. If the external PMC option is fitted, then this is routed to the PMC connectors J12/J22, and capacitively decoupled to ground.

NOTE

Analog signals should not be routed through P0.

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3.4 Backplane I/O Signal Descriptions

Table 3-7

Signal	Signal Description
DB0~ to DB7~	SCSI bus data
DBP~	SCSI bus data parity
ATN~	SCSI bus Attention
BSY~	SCSI bus Busy
ACK~	SCSI bus Acknowledge
RST~	SCSI bus Reset
MSG~	SCSI bus Message phase
SEL~	SCSI bus Select
C/D	SCSI bus Command/Data phase
REQ~	SCSI bus Request
I/O	SCSI bus I/O phase
TERMPWR	SCSI bus terminator power. Supplies power for external SCSI bus terminators. Rated at 1 Amp†
MOUSE_CLK	Mouse Clock. Clock drive for mouse
MOUSE_DATA	Mouse Data. Mouse data line
KBD_5V	Keyboard 5V. Supplies power for the keyboard and mouse or USB supply when USB is fitted. Rated at 1A†
KBD_CLK	Keyboard Clock. Clock drive for the keyboard
KBD_DATA	Keyboard Data. Keyboard data line
COM1/2/3/4/5/6_TXD	COM1/2/3/4/5/6 Transmit Data
COM1/2/3/4/5/6_RXD	COM1/2/3/4/5/6 Receive Data
COM1/2/3/4/5/6_RTS	COM1/2/3/4/5/6 Request-To-Send
COM1/2/3/4/5/6_CTS	COM1/2/3/4/5/6 Clear-To-Send
COM3/4_TT	COM3/4 Terminal timing
COM3/4_RT	COM3/4 Receive timing
COM3/4_ST	COM3/4 Send timing
KEYLOCK_IN	Keylock input. Used to detect the state of an external keyswitch. May be used to implement system password protection
SPEAKER_OUT	Loudspeaker Output. Outputs Timer2 Audio. May be used to drive 4Ω or 8Ω loudspeaker
nINIT	Parallel port INIT
nAUTOFD	Parallel port AUTOFD
SELECT	Parallel port SELECT
PERROR	Parallel port PERROR
BUSY	Parallel port BUSY
nACK	Parallel port ACK
D1 to D8	Parallel port data bits
nSTROBE	Parallel port STROBE
NSELECTIN	Parallel port Select In
nFAULT	Parallel port FAULT

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Signal	Signal Description
TX0±/TX1±	10/100BASE-T transmit data
RX0±/RX±	10/100BASE-T receive data
PASSW_EN_BP~	Global Flash Protection Password Visibility Enable
EXT_RESET~	External Reset (Hard Reset)
EXT_ABORT~	External Abort (Soft Reset)
USBPn/USBPn~	USB interface Port n
RED, GREEN, BLUE, VSYNC, HSYNC	VGA port
PMC2_IO_1 to PMC2_IO_46	I/O signals from PMC site 2
P0_B1	REDLED~ signal driven identically to the corresponding LED except that this signal has a separate buffer with a 180Ω series resistor. Defaults to low after reset
P0_B2	GREENLED~ signal driven identically to the corresponding LED except that this signal has a separate buffer with a 180Ω series resistor. Defaults to high after reset
PASSW_EN_BP~	Flash Write Protect password enable signal
EXTRESET~	Generates a Hard Reset. See the Resetting the PPC8A section for more details
EXTABORT~	Generates a Soft Reset. See the Resetting the PPC8A section for more details
3.3V	These pins are not connected to a 3.3V supply
+5V	+5 Volts DC power
PMC1_IO_1 to PMC2_IO_64	I/O signals from PMC site 1
PMC2_IO_48 to PMC_IO_52, PMC2_IO_55 to PMC_IO_58 and PMC2_IO_61 to PMC_IO_64	I/O signals from PMC site 2. PMC2_IO_48, PMC2_IO_50, PMC_IO_52, PMC2_IO_56, PMC2_IO_58, PMC2_IO_62 and PMC2_IO_64 are not available when a Fiber Channel PMC with rear I/O is fitted
GND	The DC voltage reference for the system

† This is a resettable fuse. The fuse rating is the current rating that the fuse can carry. In 20°C still air, the fuse trips at twice the rated current.

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3.5 PMC Connectors

J11/J21 and J12/J22 give the signals for 32-bit PCI.
J13/J23 give the signals for 64-bit PCI and J14/J24 give the user I/O signals.

3.5.1 J11/J21, J12/J22 and J13/23 Pin Assignments

These PPC8A PMC connectors conform to the IEEE standards. For pin assignments and signal descriptions, see the Standard Interfaces section.

NOTES

3.3V pins are connected to the PPC8A main 3.3V supply.

The PPC8A supports PMC clocking at speeds up to 66 MHz. However, if a PMC is fitted to the PPC8A that does not support the 66 MHz clocking speed, then *both* sites are limited to 33 MHz.

The PPC8A has two options for the VIO supply to the PMCs: 3.3 Volts or 5 Volts. The required voltage is controlled by link field E30, which is shipped with no jumper fitted. If left like this, the PPC8A processor sub-system may be held in reset. As both PMCs are routed to the same PCI bus, the VIO supply is then routed to both PMC sites.

As the PMC signaling voltage (VIO) is user selectable, PPC8A cards are shipped without PMC voltage keying pins.

WARNING

Check PMC VIO supply setting before installing any PMC to the PPC8A. The PPC8A and/or PMC may be damaged by a mismatch of VIOs.

CAUTION

Do not fit a PMC that requires more than 8 watts from the 3.3V supply.

3.5.2 J14 PMC I/O Pin Assignments

J14 is routed to P0 conform to ANSI/VITA 35-2000. For pin assignments, see the Standard Interfaces section or the ANSI/VITA document.

Figure 3-3 PMC Positions



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3.5.3 J24 PMC I/O and Partial P2 Option

J24 may be partially routed to the P2 connector, depending on the build option. If used, then COM3 and COM4 are no longer routed to P2. P2 now has the connections shown in the following table:

Table 3-8

Pin	PMC Signal	Connections		Pin	PMC Signal	Connections	
		P2	P0			P2	P0
1	PMC2_IO_1	D1		2	PMC2_IO_2	Z1	
3	PMC2_IO_3	D2		4	PMC2_IO_4	D3	
5	PMC2_IO_5	Z3		6	PMC2_IO_6	D4	
7	PMC2_IO_7	D5		8	PMC2_IO_8	Z5	
9	PMC2_IO_9	D6		10	PMC2_IO_10	D7	
11	PMC2_IO_11	Z7		12	PMC2_IO_12	D8	
13	PMC2_IO_13	D9		14	PMC2_IO_14	Z9	
15	PMC2_IO_15	D10		16	PMC2_IO_16	D11	
17	PMC2_IO_17	Z11		18	PMC2_IO_18	D12	
19	PMC2_IO_19	D13		20	PMC2_IO_20	Z13	
21	PMC2_IO_21	D14		22	PMC2_IO_22	D15	
23	PMC2_IO_23	Z15		24	PMC2_IO_24	D16	
25	PMC2_IO_25	D17		26	PMC2_IO_26	Z17	
27	PMC2_IO_27	D18		28	PMC2_IO_28	D19	
29	PMC2_IO_29	Z19		30	PMC2_IO_30	D20	
31	PMC2_IO_31	D21		32	PMC2_IO_32	Z21	
33	PMC2_IO_33	D22		34	PMC2_IO_34	D23	
35	PMC2_IO_35	Z23		36	PMC2_IO_36	D24	
37	PMC2_IO_37	D25		38	PMC2_IO_38	Z25	
39	PMC2_IO_39	D26		40	PMC2_IO_40	D27	
41	PMC2_IO_41	Z27		42	PMC2_IO_42	D28	
43	PMC2_IO_43	D29		44	PMC2_IO_44	Z29	
45	PMC2_IO_45	D30		46	PMC2_IO_46	Z31	
47	PMC2_IO_47		B10	48	PMC2_IO_48		A10
49	PMC2_IO_49		B9	50	PMC2_IO_50		A9
51	PMC2_IO_51		B11	52	PMC2_IO_52		A11
53	PMC2_IO_53			54	PMC2_IO_54		
55	PMC2_IO_55		E9	56	PMC2_IO_56		D9
57	PMC2_IO_57		E11	58	PMC2_IO_58		D11
59	PMC2_IO_59			60	PMC2_IO_60		
61	PMC2_IO_61		C11	62	PMC2_IO_62		C9
63	PMC2_IO_63		E10	64	PMC2_IO_64		D10



NOTE

P0 pins A9, A10, A11, C9, D9, D10 and D11 are not available if a Fiber Channel PMC with rear I/O is fitted.

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3.6 J27 Ethernet Connector (RJ45)

This is the industry standard pinout as described in IEEE802.3

Table 3-9

Pin	Signal
1	DA+
2	DA-
3	DB+
4	DC+
5	DC-
6	DB-
7	DD+
8	DD-

Where: DA+/DA- to DD+/DD- are the serial 10/100/1000BASE-T data pairs.

3.7 P8 BDM Connector

This allows the connection of software debugging tools that use the processor's JTAG port to control the operation of the processor.

CAUTION

P8 must not be used when the on-card JTAG Scan Bridge is enabled.

Table 3-10 P8 Pin Assignments

Pin	Signal	Pin	Signal
1	TDO_CPU	2	EMU~/QACK_IN~
3	TDI_CPU	4	TRST~
5	QREQ~	6	+3.3V pull-up
7	TCK	8	
9	TMS	10	
11	SRESET_CPU~	12	GND
13	HRESET_CPU~	14	
15	CHECKSTOP~	16	GND

For more information on JTAG, see the Functional Description section.

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Table 3-11 P8 Signal Descriptions

Signal	Description
TDO_CPU	Processor JTAG Test Data Out
EMU~	When connected to GND, creates QACK~ to the processor. This connection should be made with an emulator
TDI_CPU	Processor JTAG Test Data In
TRST~	Processor JTAG Test Reset
+3.3V PULL-UP	Power-on status signal to RISCWatch hardware
TCK	Processor JTAG Test Clock
TMS	Processor JTAG Test Mode Select
SRESET_CPU~	Processor Soft Reset
GND	Signal ground
HRESET_CPU~	Processor Hard Reset
CHECKKSTOP~	Processor Checkstop output
GND	Signal ground

3.8 P10 PLD Connector

This is the EPLD programming header and is for factory use only.

Table 3-12 P10 Pin Assignments

Pin	Signal
1	VCC
2	PLD_TDO
3	PLD_TDI
4	
5	KEYWAY
6	PLD_TMS
7	GND
8	PLD_TCK

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3.9 P19 I/O Port Connector

This 15-pin micro-D front panel connector combines the I/O Port connections for COM1, COM2, Mouse, Keyboard (or USB Ports 2/3) and speaker.

Table 3-13 P19 Pin Assignments

Pin	Signal	Pin	Signal
1	RXD1~	2	GND
3	TXD1~	4	RXD2~
5	SPEAKER†	6	GND
7	MOUSE_DATA~/USBP2~	8	KBD_DATA~/USBP3~
9	TXD2~	10	RTS2~
11	GND	12	CTS2~
13	KBD_5V	14	MOUSE_CLK~/USBP2
15	KBD_CLK~/USBP3		

† The speaker connection must be screened.

Table 3-14 P19 Signal Descriptions

Signal	Description
KBD_5V	Keyboard 5V. Supplies power for the keyboard and mouse. Rated at 300mA†
KBD_CLK	Keyboard Clock
KBD_DATA	Keyboard Data
MOUSE_CLK	Mouse Clock
MOUSE_DATA	Mouse Data
USBPn/USBPn~	USB Port n
TXDn~	Transmit Data COMn
RXDn~	Receive Data COMn
RTSn~	Request-To-Send COMn
CTSn~	Clear-To-Send COMn

† This is a resettable fuse. The fuse rating is the current rating that the fuse can carry. At 20°C still air, the fuse trips at twice the rated current.

NOTES

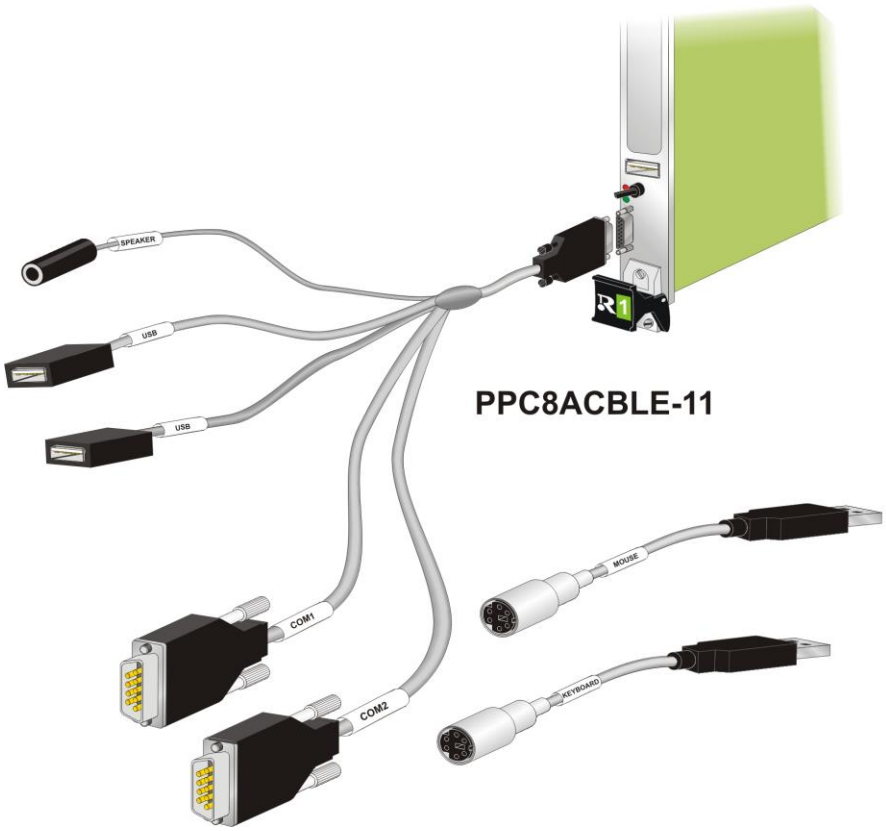
As the Keyboard/Mouse signals are the same as presented at the P2 connector, ***do not*** connect to both the P2 and P19 connection points at the same time.

The USB 1.1 ports routed to front and back are different ports from the Southbridge and so can be used simultaneously.

A custom cable for this connector is detailed in the following diagram:

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Figure 3-4 Front Panel I/O Connector



3.10 P20 USB 2.0 Type A Connector

This is an industry standard Type A USB connector for controllers and hubs.

Table 3-15

Pin	Signal
1	+5V
2	-DATA
3	+DATA
4	GND

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4 • Specifications

4.1 Mechanical Construction

Table 4-1

Weight	415g approx. There is no weight difference between the two build levels
Dimensions	The air-cooled PPC8A is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. For layout drawings, see the Standard Interfaces section

4.2 Local Resources

Table 4-2

Processor	PowerPC 7448 at 1000 MHz	
SDRAM	256 to 1024 MBytes with ECC	
L2 Cache	1024 KByte on-chip	
Flash	128/256 MBytes, with 8 MBytes reserved for Boot Flash banks	
RTC	ISA based RTC with top-hat style battery and 8 KBytes of battery-backed SRAM	
NVRAM	32 KBytes (SRAM shadowed by EEPROM)	
PCI (PMC)	64-bit, 33 MHz, 5V signaling (on-card only), 64-bit, 66 MHz, VIO link controlled to PMC sites	
SCSI	8-bit narrow Ultra-SCSI via the P2 connector	
Ethernet	3 off, two Ethernet 10/100BASE-T via the P2 connector, one 10/100/1000BASE-T to front RJ45	
USB 1.1/2.0	4 off, USB 1.1. Two to front and two to rear. Two USB 2.0, one to dedicated front Type A, second to rear (P0)	
IDE	To expansion connectors (still under development)	
Audio	To expansion connectors (still under development)	
PMC Slots	Air-cooled: Two 5V/3.3V, 66-bit/66-MHz IEEE P1386.1 compliant slots with front panel and P0 I/O, and restricted P2 I/O. EREADY support	
Serial I/O	Six serial I/O channels via the P2 connector (optional over second PMC site rear I/O)	
Keyboard and Mouse	PS/2 compatible Keyboard and Mouse interface via front and P2 connector (option over USB 1.1)	
Parallel I/O	Centronics style port via the P2 connector (software selectable over GPIO/Floppy)	
Floppy Disk Interface	MFM 1.44/2.88 MByte via P2 connector (uses GPIO signals)	
Counter/Timers	Eight 32-bit timers with a resolution of one bus clock (100 MHz)	
Reset/Abort switch	Front panel mounted	
Operating Systems	LynxOS, VxWorks/Tornado, Integrity, PBIT	
PCI Expansion	PCI through P0 via PMCPCI card	
I/O Modules	P2 (3U mounting) P25X606A	SCSI, Six serial, Parallel, floppy Mouse and keyboard (Or 2x USB 1.1 - requires USBX606) 2x Ethernet: 10/100BASE-T 15-way D-Type for optional Video
	P0	P0 Backplane Module (P07D8IO-11 or PMC specific P0 cards)

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4.3 EMC Regulatory Compliance and Safety

PPC8A is designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-1.

4.4 Power Requirements

Table 4-3

Supply Voltage	PPC8A-7448 256 MByte SDRAM	PPC8A-7448 512 MByte SDRAM
+5V +5 %, -2.5 %	4.5A	4.7A

These figures are based on a MC7448 running at 1000 MHz with a 100 MHz processor bus. The card was running a comprehensive memory test and gave measured values for +5V supply current of 4.1A.



NOTES

When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded, especially from the +5V supply.

The VME specification allows a maximum of 7.5 Amps to be drawn from the +5V supply in a single slot over the PPC8A's specified operating temperature range. It may not be possible to support all combinations of SDRAM and PMCs within this limit.

The PPC8A uses the undefined pins (rows A, C, D and Z) of the VMEbus P2 connector for I/O and power/ground connections. 3.3V from P1/P0 can be optionally routed to the 3V3 power pins of both PMC sites.



WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.



CAUTION

Only use the PPC8A in backplanes that supply power on both the J1 and J2 connectors.

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4.5 VMEbus Compliance

The PPC8A conforms to the ANSI/VITA 1-1994 standard for VME64.

Table 4-4

Master:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Slave:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Interrupt Handler:	D08(O), IH(1-7)
Interrupter:	I(1-7)
VMEbus Arbiter:	SGL, RRS, PRI, BCLR~ generation
VMEbus Requester:	ROR, RWD Early BBSY~ release Bus capture and hold
Bus Time-out Module:	16, 32, 64, 128, 256, 512, 1024 μS, disabled
Other Slot 1 Functions:	Slot 1 detector, IACK~ daisy chain driver, SYSCLK driver
Auto Slot ID:	VME64 specified and SCV64 compatible modes or geographical addressing via 5-row P1 connector

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4.6 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time Between Failures (MTBF) and Failures Per Million Hours (FPMH):

Table 4-5 PPC8A MTBF

Environment	Fail Rate (FPMH)	MTBF (Hours)
Ground benign 30°c	3.1830797	314,161
Ground fixed 40°c	10.10999	98,912
Ground mobile 45°c	27.46928	36,404
Naval sheltered 40°c	17.28301	57,860
Naval unsheltered 45°c	44.07775	22,687
Airborne inhabited cargo 55°c	25.28952	39,542
Airborne inhabited fighter 55°c	34.29919	29,155
Airborne uninhabited cargo 70°c	59.15771	16,904
Airborne uninhabited fighter 70°c	77.64975	12,878
Airborne rotary wing 55°c	74.10068	13,495
Space flight 30°c	2.6179898	381,972
Missile flight 45°c	45.15966	22,144
Missile launch 55°c	120.377	8,307

The predictions are carried out using MIL-HDBK-217F Notice 2, Parts Count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; πQ values have been modified according to the ANSI/VITA51.1 Specification.

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMCs.

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4.7 Product Codes

Table 4-6

PPC8A	-	X	X	X	X	X	X	X
								Software
							P0 Connector Options	3 = VxWorks
								4 = BIT/VxWorks
								5 = PPCBoot
								6 = BIT/PPCBoot
							0 = No P0	
						Comms Options/P2 PMC I/O	A = Type A	
							B = Type B	
						1 = 2 x 10/100BASE-T Ethernet, P2 PMC I/O, Graphics (no longer available)		
						2 = 2 x 10/100BASE-T Ethernet, P2 PMC I/O		
						B = 2 x 10/100BASE-T Ethernet & COM 3 & 4, COM 5 & 6, Graphics (no longer available)		
					Flash	C = 2 x 10/100BASE-T Ethernet & COM 3 & 4, COM 5 & 6		
						8 = 128MB		
				Memory		9 = 256MB		
						A = 512MB		
					4 = 256MB			
			Processor		5 = 512MB			
					6 = 1GB			
			E = 7447A @ 1.0GHz					
			F = 7447A @ 1.15GHz					
			H = 7448 @ 1.0GHz					
		Ruggedization Level						
		1, 2						

NOTES

P0 options are available on all build levels.

Due to the large amount of I/O required to be handled by the PPC8A, Type B (95-way) connectors are preferred to Type A (80-pin), and are fitted by default no type is specified.

4.8 P2 I/O Module

A compatible P2 backplane transition module for the PPC8A is the P25X606A. For installation instructions and pin assignments, see the I/O Modules manual.

LINK

I/O Modules Manual, publication number RT5154.

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5 • Troubleshooting

If you are experiencing a problem with your PPC8A, there follow some general suggestions of actions you may take, which may resolve the problem without the need to contact Abaco's technical support.

- Ensure that the board is firmly seated and secured in the rack and that all male/female connectors mate together correctly
- Check the links on the board, especially E30 and the system backplane
- If you are unsure of which link configuration to use, try the default configuration
- Check that the VME rack has terminators, if these are not built in (the manual for your rack should tell you whether the terminators are built in)
- Using a digital volt meter, check that the power supply is within VME limits on +5V, +12V and -12V



WARNING

Power supply problems should only be dealt with by qualified personnel.

- Check that there is only one board configured as system controller in a system and that this is in slot 1 of the rack
- Check that there are no vacant slots in the rack without jumpers (or that an automatic daisy chaining backplane is being used)
- Prove the PPC8A's operation in isolation before adding it into a multi-board system

If you are using the SCSI bus, then check that the cable stub length is less than 10 cm. You are also recommended to locate the PPC8A at one end and enable the bus terminator by fitting a jumper on link E128. If you want to use the PPC8A somewhere other than at the end of the SCSI bus, ensure that no jumper is fitted on this link. **Fitting a jumper on E128 when the PPC8A is not located at the end of a SCSI bus may cause erroneous SCSI operation.**

- If you have made your own cable for connection between P19 or P2 and a terminal/hyper-terminal, check that the pinout is correct
- Check that the terminal is set up for DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled)
- Ensure that air-cooled PPC8As receive sufficient airflow. If you need to operate your PPC8A on an extender card, this requires an additional fan to supply the necessary air flow
- If you are having problems programming the Flash, then check that either a jumper is fitted on the Flash Password Visibility Enable link (E5) or that the backplane signal, PASSW_EN_BP~ (P0-A2 or P1-Z1) is connected to GND. See the Flash section and the E5 link description for more details

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6 • Glossary



LINK

This glossary only features terms special to this manual. Explanations of more general terms can be found in the Glossary, publication number GLOS1.

CR/CSR Configuration ROM/Control and Status Register.

PPC8A Abaco's PowerPC-based processor card. The PPC8A is based on the PowerPC 7448 processor with integral L2 cache controller and uses SDRAM.

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