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Radstone PPC4B Manual

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Note: The revision state refers *only* to the manual, ***not*** the board.

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Chapter 1 - Introduction

Radstone's PPC4B, with its associated peripherals and software, is the latest addition to Radstone's PowerX family of VME-based PowerPC boards. It follows the Common Hardware Reference Platform architecture, ensuring compatibility with the abundance of CHRP-compliant software. Designed for users who require scaleable, high performance processors, sophisticated I/O subsystems and high levels of on-board integration, the PPC4B offers a cost-effective solution to a wide range of application requirements.

Like all Radstone's VME products, the PPC4B is available in a range of build styles, from Level 1 (Standard), suitable for a benign office-like environment, right through to Level 5 (Rugged Conduction-cooled), capable of withstanding the harshest of environments. All products are COTS/NDI, and make maximum use of low cost plastic packaged integrated circuits to ensure the most cost effective solution, whatever the market.

Local connection of Ultra-SCSI, Ethernet and VME64 uses a 32-bit 33 MHz PCI bus. The two IEEE P1386.1 PMC sites use another PCI bus running at 64-bit/66 MHz. The signalling voltage on this bus is user selectable for 5V or 3.3V signalling. PMCs available directly from Radstone include high performance graphics, MIL-STD-1553, serial, ATM, FLASH memory, Solid State Hard Disk, Fibre Channel, fast Ethernet and other communications. Additional PMC sites are available using a companion carrier card.

Radstone is a key member of the VITA standards committee, setting the standards for rugged conduction-cooled PMCs. In line with their recommendations, one of the two PMC sites on rugged conduction-cooled build standard product has the PMC I/O connected to P0, allowing direct backplane connection to all I/O. The other site may have its PMC I/O connected to P2, but this build option reduces the number of serial channels available to the user.

The PPC4B is the latest of Radstone's VME products to use 5-row connectors for P1 (VME), P2 (I/O) and P0 (PMC I/O). Like other boards in the PPCx range, the PPC4B can use the PMC-PCI bridge product to extend the board's PCI bus out via the P0 connector.

This flexibility, together with operating system support including VxWorks/Tornado and LynxOS are factors in making the PPC4B an ideal vehicle for applications such as communications, simulation, multi-media, real-time acquisition, terrain mapping, C^4, image processing and high performance graphics.

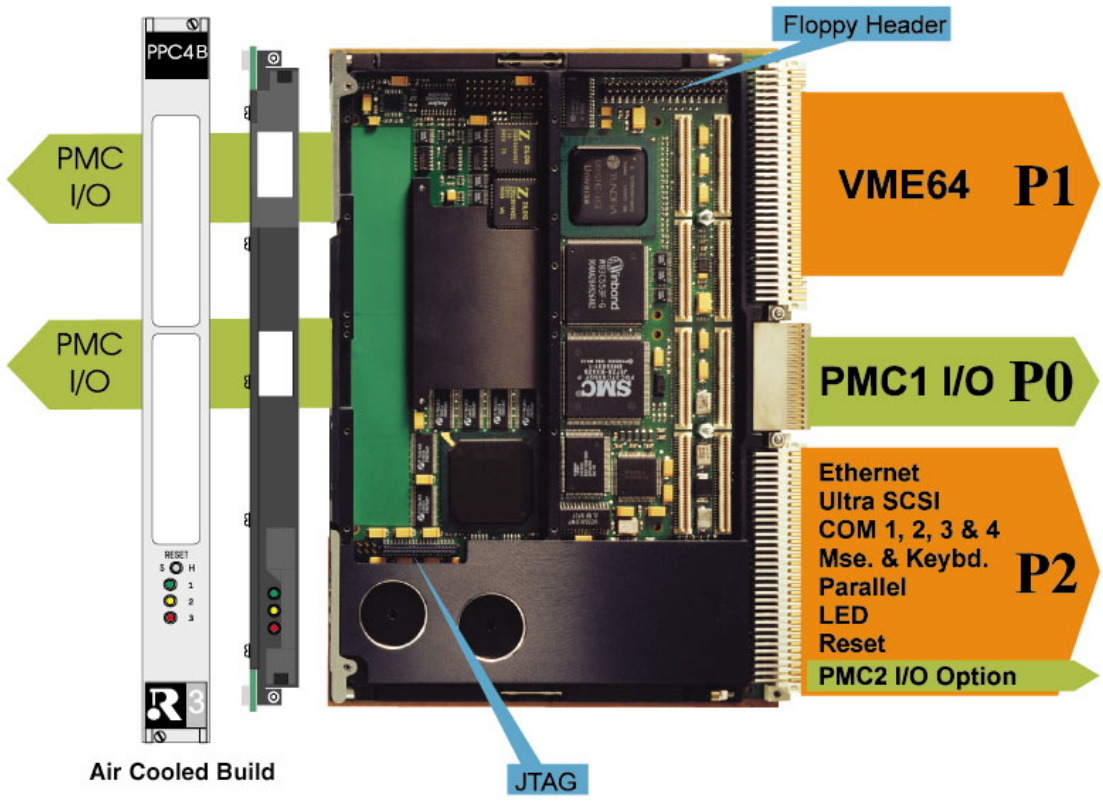
Input/Output

The PPC4B provides high-density rear I/O for systems requiring sealed box operation and simple card replacement routines for field maintenance.

Front panel I/O is limited to the two on-board PMC slots and also a Reset/Abort switch on the air-cooled builds of the board (see Figure 1-1). The PPC4B uses 5-row VME64 P1 and P2 connectors, as well as an optional P0 connector (type A or B can be specified) for rear access to the on-board PMC Slot 1. PMC Slot 2 is available via rows Z and D of the P2 connector.

The PPC4B has a wide variety of possible I/O connectivity including Ultra-SCSI, Ethernet, serial, mouse/keyboard and parallel/printer ports. To maximise the flexibility of connecting to these ports, a range of I/O modules are available, attached by a VME P2 or P0 transition module. Using rear I/O minimises the effort needed to remove boards from a rack, so improving maintainability and reliability.

Figure 1-1. PPC4B I/O



Software Support

Radstone's software strategy for PowerX allows fully integrated system-level solutions to be realised easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of the PowerX family, so providing a common look, feel and interface for technology inserts.

Radstone has invested more than 50 man-years of engineering talent into the PowerPC architecture so that customers can develop market-leading products using the O/S and development environment best suited to their long term program requirements.

SilverChip Boot Firmware

Developed as an integral part of the Radstone PowerX strategy, the SilverChip Boot firmware provides a foundation layer to interface between the raw Radstone board hardware, with its highly programmable device set-ups and flexibility, and the supported Operating Systems, which require a straight-forward booting and device interface model.

SilverChip includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialisation, PCI display/interrogation utilities and other valuable features for system integrators.

Memory or other speed and feature enhancements are seamlessly absorbed by SilverChip, giving the same look and feel to the O/S and the user application as the Radstone hardware models advance. This allows the constant use of latest technology in required areas without system impact. Where particular operating systems define the use of alternate boot methods (e.g. VxWorks bootroms), SilverChip technology is absorbed into such boot methodology.

Built In Test

PPC BIT probes from the lowest level of discrete on-board hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialisation tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

Background Condition Screening

BCS supplements the BIT initialisation test coverage with further health screening that can co-exist with a standard COTS Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic checksumming, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in FLASH in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.

Operating System Support

In-house porting expertise for PowerPC based boards is focused on key operating systems, including Wind River Systems' VxWorks/Tornado and LynuxWorks' LynxOS. Other operating system ports, drivers for third party hardware and layered products are provided through strategic partnerships with dedicated third party vendors, able to offer high quality products and services complementary to the Radstone range. In this way, state of the art development environments and debug tools that are part of the above software products are made available for use on Radstone's flexible hardware architectures.

Please contact Radstone for availability of other operating systems in addition to the standard VxWorks and LynxOS offerings.

VxWorks/Tornado

Wind River System's VxWorks/Tornado distributed real-time operating system includes integrated networking facilities and a complete software development environment for UNIX hosts. It features a fast, multitasking kernel with pre-emptive scheduling, inter-task communications, multiprocessor support, symbolic and source-level debugging, performance monitoring and an I/O file system.

The full range of facilities are supported by BSPs for all Radstone CPU types, which have been validated by both Radstone and Wind River for the greatest confidence and ease of use. To complement the BSPs, many of Radstone's I/O and graphics products are also supported by libraries and drivers.

LynxOS

Created by LynuxWorks, LynxOS is compatible with UNIX V.3. It is POSIX compliant and supports X.11 (X-Windows), Motif, NFS and TCP/IP. Unlike conventional UNIX, it is fully pre-emptive to ensure that application tasks can be rescheduled if a higher priority task is ready.

BSPs and ESPs

Board Support Packages provide 'standard' support for the above operating systems, as defined by the operating system vendors. Radstone also provide Enhanced Support Packages for comprehensive hardware support in addition to that defined by the operating system vendors. This approach allows users to implement a verifiable BSP standard and yet not be locked out of using valuable extra features, which will adapt the BSP but shorten development times. ESP features may be added or removed as desired during development.

Typical features include VME DMA for VxWorks (not included in WindRiver's BSP definition) and VME enhancements like dynamic windowing and interrupt generation for LynxOS (not included in LynuxWorks' BSP definition. BCS is also part of the ESP.

Notes:

1) Although Radstone will make every effort to maintain functionality, due to the increasingly short lifetimes of system components, devices used to provide the I/O on the PPC4B are not guaranteed to remain fixed in the future.
2) For this reason, hardware should be accessed only through mechanisms provided by the Operating System's "Hardware Independence" mechanism (BSP, residual data, etc.), and not directly by application software.
3) If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimise direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.
4) Radstone supported Operating Systems guarantee compatibility at the application level through the Hardware Independence mechanisms mentioned above.

Build Styles

The PPC4B is available in Radstone's five electrically compatible build levels. These have two basic mechanical configurations:

- Air (convection)-cooled (build levels 1 to 3) in accordance with ANSI/VITA 1-1994 specification, designed to be used in standard industrial VME chassis
- Conduction-cooled (build levels 4 and 5) in accordance with IEEE Std 1101.2-1992, for use in Radstone or third party ATR style enclosures.

In addition to these COTS configurations, PPC4B may be supplied to meet the mechanical and thermal requirements of specific platforms with the addition of mission specific, to-type mechanics.

Radstone uses advanced thermal and mechanical design in the PCB, metal work and assembly process to build-in the required levels of ruggedness. Build level 2 and higher circuit card assemblies include conformal coating as standard.

All five styles fully support the power and versatility of the VMEbus, so no matter how large or diversified your project, absolute compatibility is assured at all stages of development.

A brief description of each build style follows:

Level 1

Intended for use in benign environments, level 1 also provides the ideal cost effective method of complete system development. The level 1 assembly comprises a double-Eurocard size printed wiring board with high quality commercial (plastic encapsulated) components.

As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to target style only in the final stages of system integration.

Level 2

As Level 1, but tested in manufacture to provide an extended operating range.

Level 3

Level 3 boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air-cooled, racking systems. These rugged boards comprise a double-Eurocard size printed wiring board fitted with wide temperature range, industrial grade components.

Level 4

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments, the level 4 board features wide temperature range, industrial grade devices, an integral thermal management layer. It also incorporates a central stiffening bar for additional strength.

Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack to which the boards are secured by screw driven wedgelocks. Level 4 boards are temperature characterised during manufacture.

Level 5

As Level 4, but tested in manufacture to provide an extended operating range.

See Appendix A for more details of the environmental specifications of each build style.

Objectives of this Manual

- To guide the reader through configuration, installation and power-up
- To provide the user with sufficient information to understand the operation of the PPC4B hardware

Note: Software support (e.g. drivers, BSPs, ESPs etc.) is described in separate manuals.

Documentation Audience

This manual is written to cover, as far as possible, the range of people who will handle or use the PPC4B including (but not limited to):

- Inspectors
- Installation technicians
- Hardware and software engineers
- System managers

While every effort has been made to keep the description of configuration, installation and power-up as simple and user-friendly as possible, a certain amount of background knowledge on these subjects is assumed.

In the Functional Description chapter, a higher degree of background knowledge is assumed on subjects including:

- Single board computer architecture
- Peripherals
- The VMEbus
- Communications

There is a glossary provided at the back of this manual that explains some of the terms used and expands abbreviations.

Scope of this Manual

This manual describes:

- All build standards of the PPC4B
- All variants of the PPC4B

This manual mentions, but does not describe in detail:

- PMCs, including the PMCPCI bridge product
- Carrier cards
- PPC4B on-board firmware
- Software support (drivers, BSPs, ESPs etc.)
- Application software

Structure of this Manual

This manual is structured in a way that will reflect the sequence of operations from receipt of the PPC4B up to getting it working in your system. Each topic is covered in a separate chapter and each chapter begins with a brief introduction that tells you what the chapter contains. In this way, you can skip any chapters that are not applicable or with which you are already familiar.

The chapters are:

Chapter 1 (this chapter) - gives a brief introduction, this manual's objectives, audience, scope, structure and conventions, safety notices, associated documentation and related web sites.

Chapter 2 - contains inspection instructions and describes product identification.

Chapter 3 - describes installation of the PPC4B in a system and power-up.

Chapter 4 - describes board configuration.

Chapter 5 - is a functional description.

Chapter 6 - describes the PPC4B's connectors and signals used.

Chapter 7 - describes the PPC4B's front panel.

Chapter 8 - outlines how to obtain technical assistance.

Appendix A - is a board specification.

There are also a glossary and an index provided.

Safety Notices

Safety Summary

Observe the following general safety precautions during operation, service and repair of this equipment. Failure to comply with these precautions or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Radstone Limited trading as Radstone Technology assumes no liability for the user's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Radstone is aware. Take note of these warnings and take all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Equipment

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

WARNING
Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components

WARNING
Power supply problems to be dealt with only by qualified personnel

All Radstone circuit boards are manufactured by UL-recognized manufacturers and have a flammability rating of 94V-0.

Caution
This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic inteference (EMI) if not installed and used in a cabinet with adequate EMI protection

European Notice: Board products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 (CISPR 22) Radio Frequency Interference.

EN50082-1 (IEC80-2, IEC801-3, IEC801-4) Electromagnetic Immunity.

The product also fulfils EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Caution
Only handle the board by the edges or front panel

Caution
Only use the PPC4B in backplanes that supply power on both the J1 and J2 connectors

Caution
Do not remove the heatsink.

There are ***no*** PROMs or other user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should ***not*** attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it (e.g. the main PowerPC processor). **Removal and re-attachment of the heatsink should only be carried out by Radstone.**



Conventions Used in this Manual

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'b' subscript. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

Note: When describing transfer rates, 'k' 'M' and 'G' mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$, $*2^{20}$ and $*2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follows the more familiar convention that bit 0 is the LSB and bit n is the MSB.

Signal names ending with a tilde (~) denote active low signals; all other signals are active high.

This manual uses three types of notice: notes, cautions and warnings.

1) Notes, which take the form '**Note:**', call attention to important features or instructions.

2) Cautions, which take the following form, alert you to system danger or loss of data.

Caution
This is the form a caution takes

3) Warnings, which take the following form, alert you to the risk of severe personal injury.

WARNING
This is the form a warning takes

Les avertissements vous préviennent qu'il existe un risque de blessure grave.

Warnhinweise sollen Sie auf mögliche schwere Körperverletzungen aufmerksam machen.

Associated Documents

Due to the complexity of some of the parts used on the PPC4B, it is not possible to include all the detailed data on all such devices in this manual. The following is a list of the specifications and data sheets that provide any additional information required:

VME64 Specification ANSI/VITA 1-1994 April 1995. *VMEbus International Trade Association AZ 85253 USA.*

VME64 Extensions Specification. Not Yet Published. *VMEbus International Trade Association AZ 85253 USA.*

PCI Local Bus Specification, Revision 2.1, June 1 1995. *PCI Special Interest Group OR 98214 USA.*

PCI System Design Guide.

IEEE P1386 Draft Standard for a Common Mezzanine Card Family.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards.

IEEE Std 802.3 Local Area Networks: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) - (ETHERNET) (1985) *The Institute of Electronic and Electrical Engineers Inc., NY 10017 USA.*

ANSI X3.131-1986 - Small Computer System Interface (SCSI), *American National Standards Institute NY10036, USA.*

ANSI X3.131-1994 : Information Systems - Small Computer Systems Interface-2 (SCSI-2) *American National Standards Institute NY10036, USA.*

ANSI/EIA/TIA-232-E - Interface Between Data Terminal Equipment and Data Communications Equipment Employing Serial Binary Data Interchange (December 1991) *Electronic Industries Association, DC20006 USA.*

ANSI/EIA/TIA-422-B, Electrical Characteristics of Balanced Voltage Digital Interface Circuits (December 1978). *Electronic Industries Association, DC20006 USA.*

PowerPC Microprocessor Common Hardware Reference Platform: A System Architecture, Version 1.0 (November 1995). *Morgan Kaufmann publishers Inc. San Francisco, California USA.*

PowerPC Microprocessor Family: The Programming Environments, 1994. *IBM VT 05452-4299 or Motorola AZ 85036 USA.*

The PowerPC Architecture: A Specification for a New Family of RISC Processors, Second Edition. *Morgan Kaufmann publishers Inc. San Francisco, California USA.*

PowerPC 740/750 RISC Microprocessor User's Manual. *Motorola AZ 85036 USA.*

MPC7400 RISC Microprocessor User's Manual. Motorola *MPC7400UM/D.*

MPC107 PCI Bridge/Memory Controller User's Guide. *Motorola AZ 85036 USA.*

NCR53C860 PCI-SCSI I/O Processor Data Manual. *NCR Microelectronic Products Division. CO 80916. USA.*

Digital Semiconductor 21143 PCI/CardBus 10/100-Mb/s Ethernet LAN Controller Hardware Reference Manual. *Advanced Micro Devices Inc. CA 94088-3453 USA.*

W83C553F System I/O Controller with PCI Arbiter Data Book. *Winbond Systems Laboratory.*

SMC37C93X Plug and Play Compatible Ultra I/O Controller. *Standard Microsystems Corporation.*

Universe II User Manual 1998. *Tundra Microsystems ON K2K 2M5 Canada.*

FLASH Memory, Volume 1 1995. *Intel corporation IL 60056-7641 USA.*

Datacom ICs. 1991. *Zilog Inc. CA 95008-6600.*

Z8036 Z-CIO/Z8536 CIO Counter/timer and Parallel I/O Unit Technical Manual. *Zilog Inc. CA 95008-6600.*

Atmel Non-volatile Memory Data Book, 1995-1996, *Atmel, San Jose, CA 95131*

Radstone I/O Modules Installation Guide, publication number RT5154.

Radstone SilverChip (PPC Boot Firmware) Manual, publication number RT5078.

Radstone PMCPCI Manual, publication number PMCPCI-0HH.

Radstone P0CC1 Manual, publication number P0CC1-0HH.

Radstone PMC Installation Note, publication number HN4/3-99.

Radstone BIT on PPCx User Guide, publication number RT5107.

Radstone PPC BIT Release Notes, publication number RT5111.

VxWorks PowerPC BSP for Radstone PPC4B and PPC6 V2.2 Beta Release Notes, publication number RT5135.

VxWorks ESP and ESPZ for Radstone PPCx Manual, publication number RT5106.

Radstone PowerX User Guide (VxWorks Edition), publication number RT5138.

LynxOS 3.1.0a BSP for Radstone PPCx Installation Manual, publication number RT5103.

LynxOS ESP for Radstone PPCx Manual, publication number RT5093.

World Wide Web Sites

Manufacturers of many of the devices used on the PPC4B maintain FTP or world-wide-web sites. Some useful sites for obtaining further relevant data are:

http://www.motorola.com
Motorola PowerPC data is available through this site.

http://www.chips.ibm.com
IBM PowerPC data is available through this site.

http://www.tundra.com
Universe chip information, including the user manual for the Universe II as an Adobe Acrobat .PDF file, is available through this site.

Radstone on the world-wide-web is available at:

http://www.radstone.co.uk

or

http://www.radstone.com

Chapter 2 - Inspection

This chapter gives guidelines on inspecting the PPC4B.

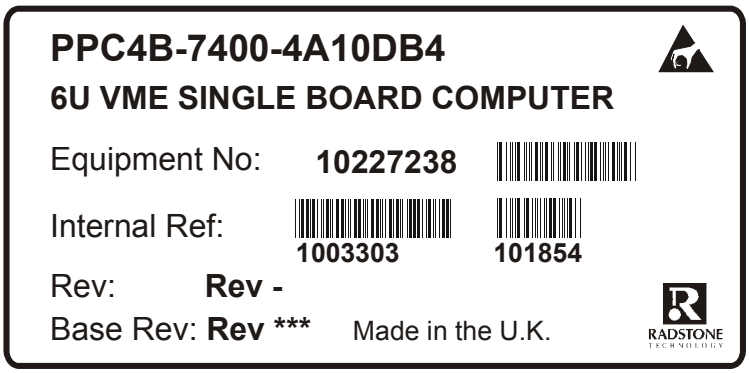
Observe antistatic precautions (wear an antistatic wrist-strap connected to an Earth point and work at an approved antistatic work station) when handling the board.

Caution
Only handle the board by the edges or front panel

Product Identification

Radstone boards are identified by labels at strategic positions. You can cross-check these against the Advice Note provided as a separate note with your delivery.

On the outside of the shipping box, and the antistatic bag, there is a label similar to the following form:



On the board within the antistatic bag, there are identifying labels similar to the following attached to the printed wiring board:

MADE IN UK	PPC4B-7400-4A10DB4	Base Rev
10227238	Rev -	Rev ***

A label giving the board's Ethernet number is also attached to the printed wiring board. The Ethernet number has the form XX-XX-XX-XX-XX-XX, for instance:

00-80-8E-
00-50-93

On conduction-cooled versions of the board, there are also labels similar to the following attached to the front panel:





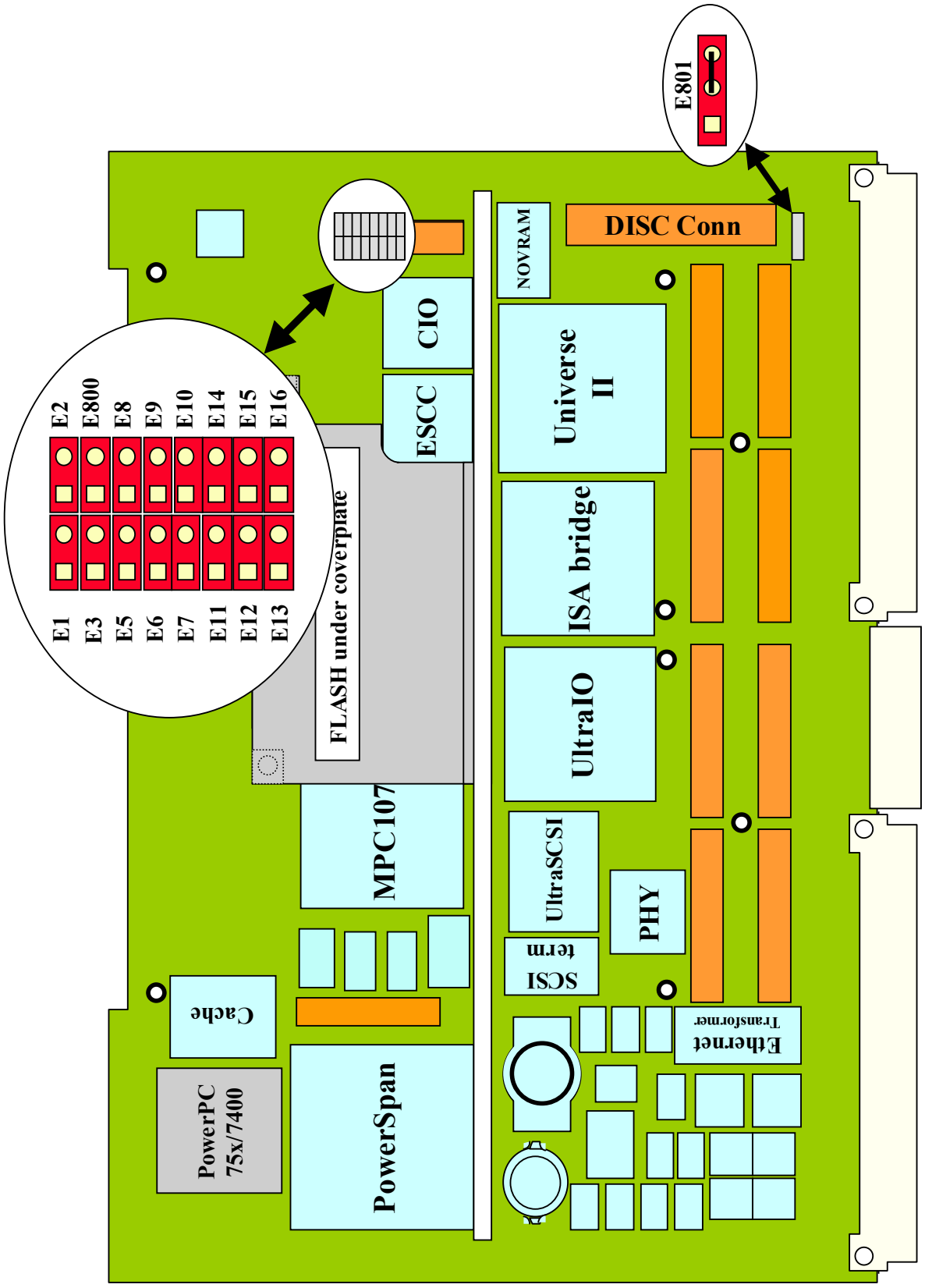
Inspection

1) Visually inspect the board for any damage and loose or dislodged components.
2) Report to Radstone any defects you detect.
3) Using the table below and Figure 2-1, visually inspect the board to ensure that the configuration is correct and that there are no loose or missing jumpers:

Link	Setting	Action
E1	Out	Front panel reset switch disabled
E2	Out	Boot from System FLASH
E3	Out	Machine Check exception enabled
E5	Out	Write protect FLASH bank 2
E6	Out	Write protect FLASH bank 1
E7	Out	Factory link
E8	Out	Write protect FLASH bank 4
E9	Out	Write protect FLASH bank 3
E10, E14, E15 and E16	Out	ID links (board ID = 15) (unless in a 5-row backplane)
E11	Out	On-board SCSI terminators disabled
E12	Out	Universe PCI slave image 0 enabled
E13	Out	Normal FLASH bank operation
E800	Out	32-bit signalling on PCI bus to PMC sites
E801	Pin 2 to pin 3	5V signalling on PCI bus to PMC sites

Caution
Only handle the board by the edges or front panel

Figure 2-1. Link Positions and Default Configuration



Pin 1 of link blocks is shown by a square pad in the above diagram.

Chapter 3 - Installation and Power-up

This chapter describes the installation of PMC cards and the installation of the PPC4B board in a system. It then describes power-up of the board.



Caution
Only handle the board by the edges or front panel

PMC Installation

Two single width (or one double-width) PMCs may be fitted to the PPC4B. There are no PMC keying pins, as the board can be user-configured for 5V or 3.3V signalling. Figure 3-1 overleaf shows the positions of these PMCs.

Each PMC is supplied with a full kit of parts for mounting it, full fitting instructions and a manual. For Radstone products, the PMC Installation Note, publication number HN4/3-99 contains the fitting instructions. PMCs ordered with a PPC4B can be supplied factory fitted by Radstone, if required.

It may be necessary to install driver software or implement other firmware configuration to achieve full functionality of a PMC (see the specific PMC manual for the exact procedure).

Note: You are recommended not to route analog signals through P0.

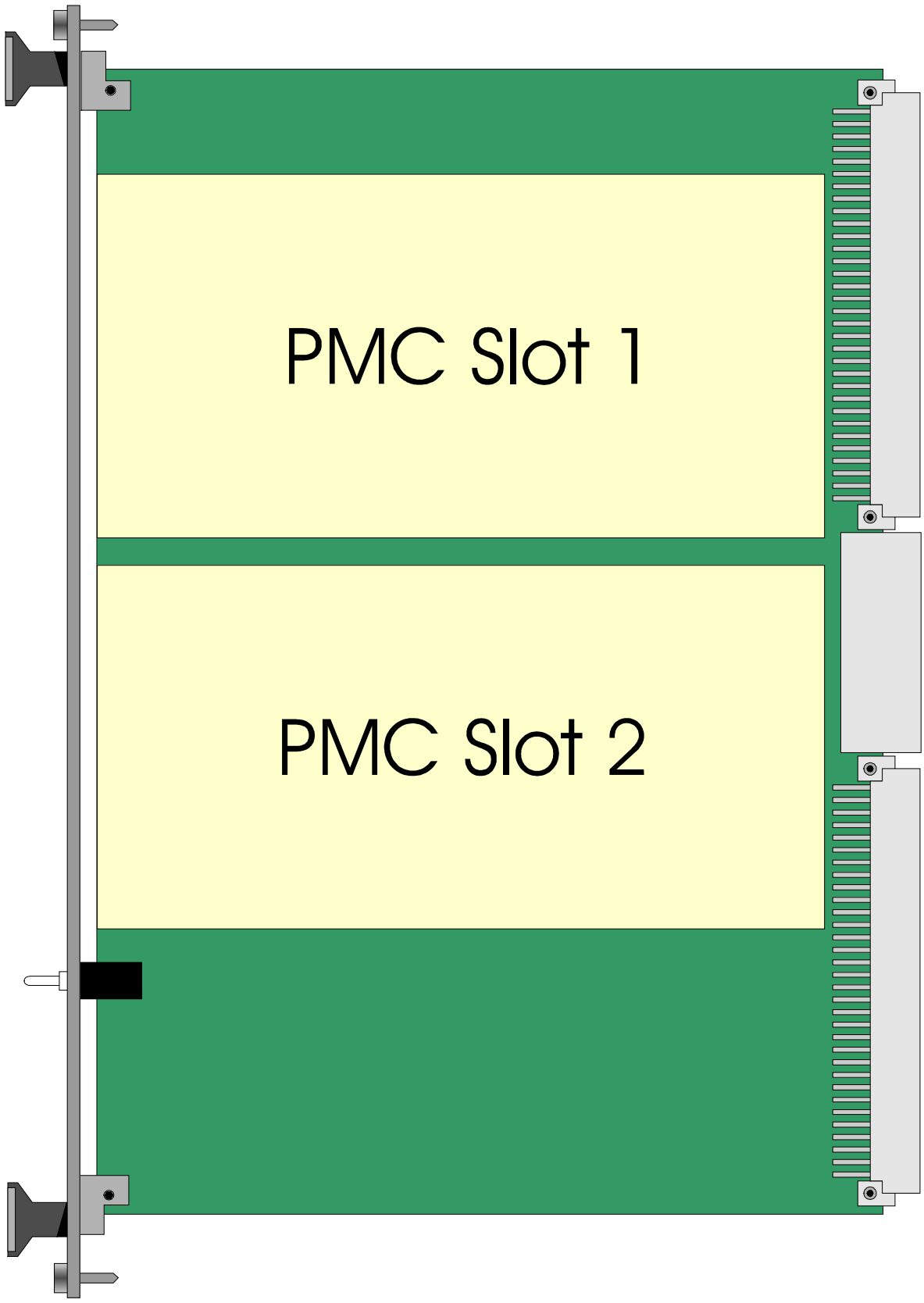
PMCPCI Expansion Card Installation

The PMCPCI PCI expansion card should only be installed in PMC slot 1, as this then takes out the full PCI bus through P0. The PMCPCI card occupies half of the PMC slot.

Caution
Current versions of the PMCPCI, PMCPCIM and PMCPCIS only work with 5V signalling. Under no circumstances should they be fitted to a PPC4B that is configured for 3.3V signalling (see Link E801). All three products are scheduled for update.

See Chapter 5 for more information on the PMCPCI.

Figure 3-1. PMC Positions



Board Installation

Before plugging the PPC4B into a development rack, you should first check the rack's backplane configuration links.

System Backplane Configuration Links

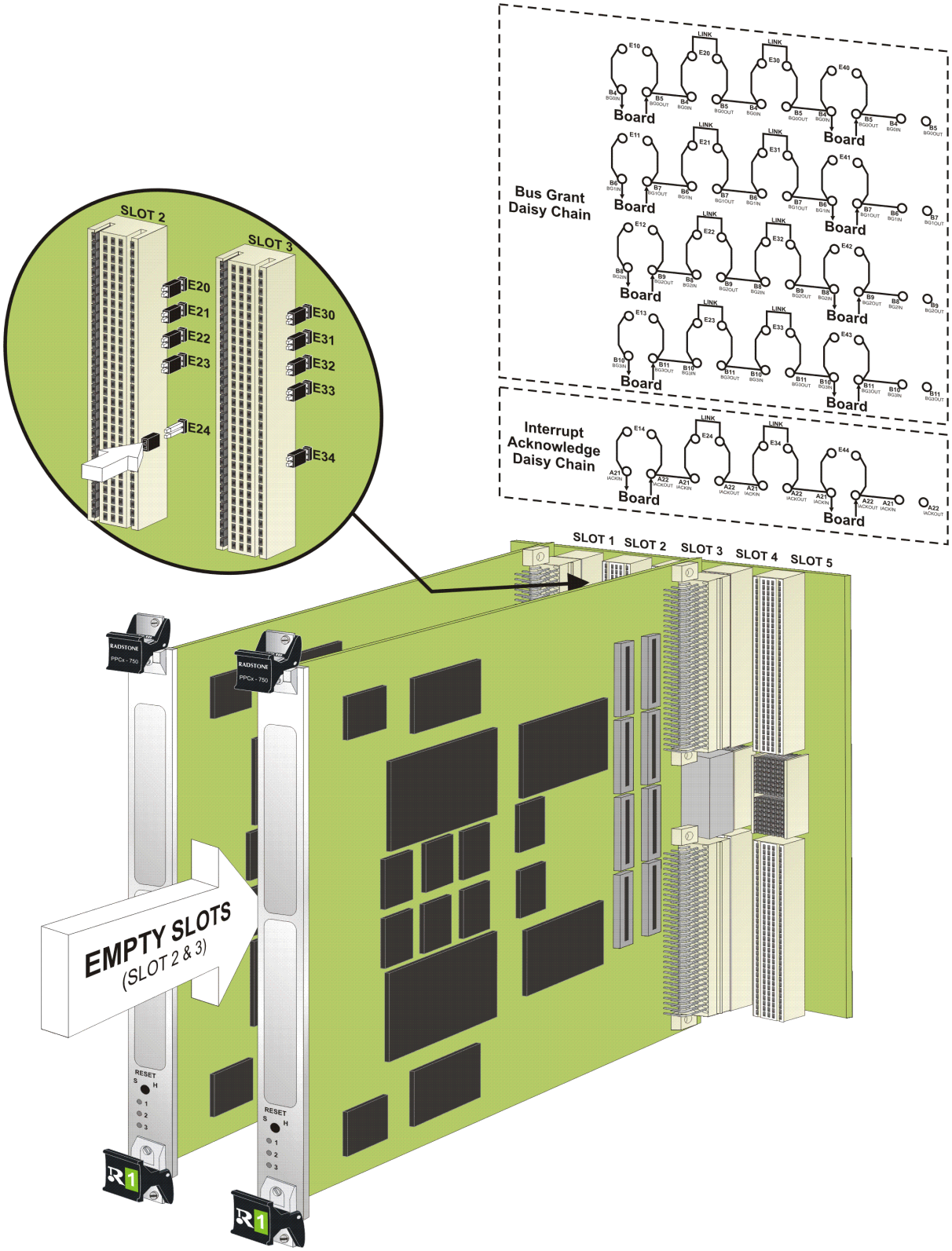
If a system slot is not occupied by a board, and there are boards to the right of the empty slot (e.g. your PPC4B), you need to ensure that the VME Bus Grant (BGx) and Interrupt Acknowledge (IACK) signals are linked across the empty slot.

These signals form a daisy chain, i.e. the 'Out' signal (BGxOUT~/IACKOUT~) from one slot becomes the 'In' signal (BGxIN~/IACKIN~) at the next slot (see Figure 3-2 overleaf). If the daisy chains are broken, the boards to the right of the break will never be able to become VMEbus Master or acknowledge VMEbus interrupts.

- In Radstone enclosures, the daisy chains are configured using two sets of links in the J1 (VMEbus) half of the backplane
  - The upper set of four links configures the VME Bus Grant (BGx) daisy chain
  - The lower link configures the VMEbus Interrupt Acknowledge (IACK) daisy chain
    - If a slot is empty and there are boards further down the daisy chain, connect the 'In' signal (BGxIN~/IACKIN~) at that slot to the corresponding 'Out' signal (BGxOUT~/IACKOUT~) at the same slot using these links
    - Some backplanes have daisy chains that automatically link the signals across empty slots (see the manual appropriate to your enclosure for further details)

Figure 3-2 shows the Bus Grant and Interrupt Acknowledge daisy chains, plus the associated links, on an example 5-slot backplane, including example empty slots (slots 2 and 3).

Figure 3-2. Daisy Chains



System Configuration Suggestions

Caution
Only handle the board by the edges or front panel

Use the PPC4B in a development rack on its own at first, before integrating it into a system with other cards. This way you can prove operation of the PPC4B in isolation before tackling any system configuration issues.

Link Configuration

- **Use the default link configuration (see Chapter 2) for the first power-up.** This way you can prove the board's operation before tackling any board configuration issues.
- When you need to alter your PPC4B's user configurable link settings, see Chapter 4 - Configuration to check that all the settings are correct for your application. You could start by trying the Suggested Configuration
- If you are using the SCSI bus, you are recommended to locate the PPC4B at one end and enable the terminator by fitting link E11. If you want to use the PPC4B somewhere other than at the end of the SCSI bus, ensure that E11 is not fitted. **Fitting E11 when the PPC4B is not located at the end of a SCSI bus may cause erroneous SCSI operation**

Air-cooled PPC4B

1) Insert the board into the required slot in the development rack.
2) Push the board **firmly** home to ensure the connectors mate properly with the backplane.
3) Tighten the captive screws at the top and bottom of the front panel to secure the board in position.

   Note: Pulling on any front panel cable connections could inadvertently disconnect the board if it is not secured.

4) Ensure that the board gets airflow of at least 300 feet/minute. If you need to operate your PPC4B on an extender card, fit an additional fan to supply the necessary air-flow.
5) To ensure optimum operation of the PPC4B with regard to EMC:
   - When taking I/O connections from the front panel connectors, or when the board is operating on a VME bus extender card, ensure a connection is made between the front panel and the chassis ground of the system
   - When taking I/O connections from P2 or P0, use the Radstone I/O Modules kit (or some equivalent system). See Appendix A for more details on the Radstone I/O Modules

Conduction Cooled PPC4B

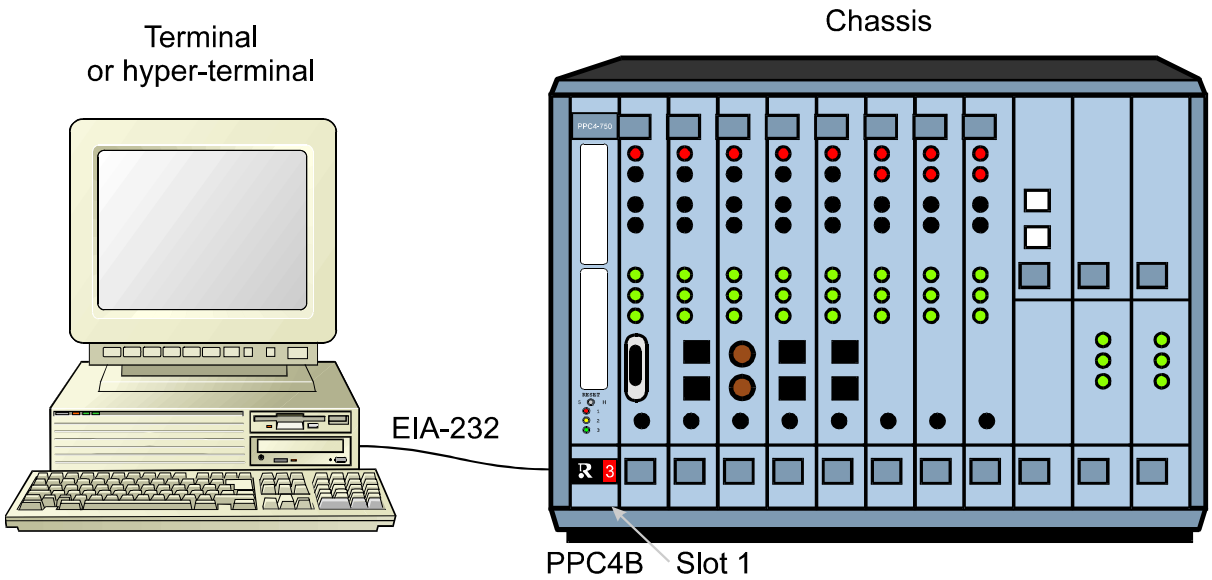
1) Insert the board into the required slot in the conduction-cooled enclosure.
2) Push the board **firmly** home to ensure the connectors mate properly with the backplane.
3) To ensure a correct mechanical/thermal interface, using a calibrated torque wrench, tighten the screw-driven wedgelocks at the top and bottom of the board to secure it in position. The recommended torque value is 0.6 to 0.8 Nm and the hexagon size is $^{3}/_{32}$".
4) If you need to operate a conduction-cooled PPC4B on an extender card, maintain an airflow of at least 300 feet/minute over it, by the use of a suitable fan.

Connecting a Terminal to Your PPC4B

To interact with on-board firmware (such as BIT, SilverChip or VxWorks), you need to attach a serial terminal or hyper-terminal to the PPC4B as shown in Figure 3-3.

The terminal should use the signals on your PPC4B's COM1 serial port. Details of how to connect to COM1 on the PPC4B are given below.

Figure 3-3. Example System



Data Format

COM1 is configured as DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled). Cables supplied by Radstone permit direct connection to a terminal without use of a null-modem.

Connecting the Terminal to COM1 on the PPC4B

There are two ways to connect to COM1 on the PPC4B: via connector P7 or via connector P2 (using I/O modules - described overleaf). P7 and P2 present the same serial signals, so use one method or the other, but not both. See Chapter 6 for more details of P7.

I/O Modules

Radstone's I/O modules can be used to connect to COM1 on the PPC4B. These bring the serial signals from the P2 backplane connector to a breakout panel. The procedure for using I/O modules is described below:

The following items are required:

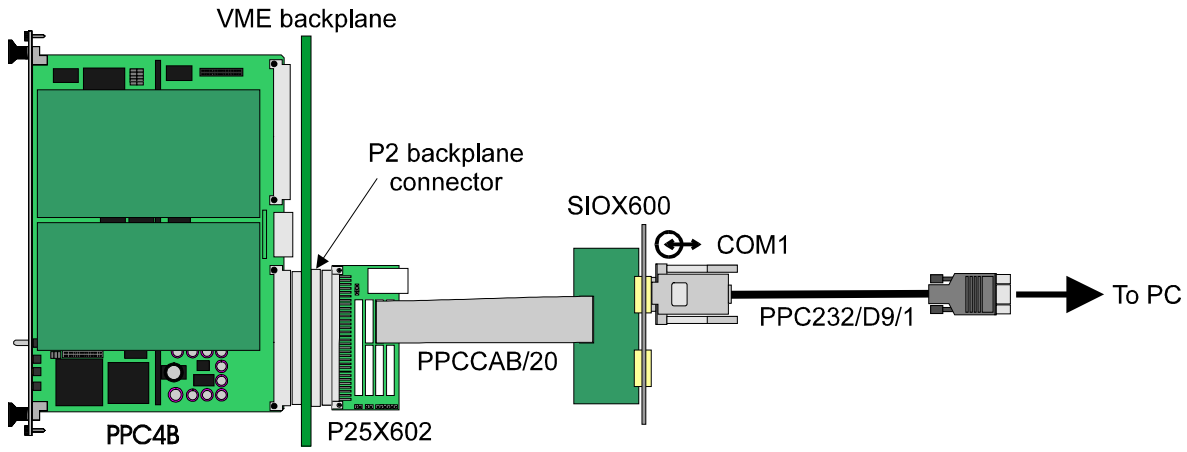
- The PPC4B
- A P25X602 transition module, which converts the non-conventional condensed pinout of the 5-row P2 connector to pinouts suitable for use by industry standard connectors
- An SIOX600, which is a 4HP wide, 3U high, dual fixed DTE RS232C interface adapter providing two serial I/O channels through two 9-way micro D-type sockets (with locking posts)

  Note: Two alternative modules, SIO2X600 and SIO3X600, are also available.

  - SIO2X600 is a 10HP wide, 3U high, dual RS232C interface adapter providing two serial I/O channels through two 25-way industry-standard D-type sockets (with locking posts), link configurable for DTE or DCE
  - The SIO3X600 is a 4HP wide, 3U high, fixed DTE interface adapter providing a single serial channel to EIA-530 through a 25-way industry-standard D-type socket (with locking posts)
- A cable for connecting the P25X602 to the SIOX600 (Radstone PPCCAB/20 recommended)
- A 9-way micro D-type to standard 9-way D-type cable for connecting the SIOX600 to a PC (for instance Radstone cable PPC232/D9/1, 1 meter long)

Figure 3-4 shows how the relevant parts connect:

Figure 3-4. Example I/O Module Set-up



For more details on these modules and information on fitting them, see the I/O Module Installation Guide, publication number RT5154.

Note: The COM1_DSR and COM1_RI signals are not available if the full PMC I/O through P2 option has been specified. This option has the following order numbers:

PPC4B-750-xxxxExx	PPC4B-750-xxxxFxx
PPC4B-7400-xxxxExx	PPC4B-750-xxxxFxx

Power-up

Your PPC4B is installed in a rack and connected to a terminal or hyper-terminal. You are almost ready to power-up, after a few checks.

Power-up Checklist

Before powering-up, check you have:

- Configured the backplane if necessary
- Followed the system configuration suggestions
- Ensured that the PPC4B is firmly secured in the rack/enclosure
- Checked the J1 and J2 connections of the slot to ensure that they both supply power

Caution
Only use the PPC4B in backplanes that supply power on both the J1 and J2 connectors. Use of backplanes that supply power on the J1 connector only may cause excessive current to be drawn through the power pins

- Ensured that the chassis power supply is within VMEbus Specification limits (5V +5% -2.5%) and sufficient for the PPC4B's requirements (up to 5.58A).

WARNING
Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components

Notes:

1) The PPC4B does not use the ±12V supply lines (VMEbus ±12V +5% -2.5%), but these lines do feed the PMC sites.

2) The +12V supply also feeds through a 1 Amp fuse to P2 pin C7 for the 10Base5 Ethernet transceiver. So although the PPC4B does not use +12V, users may take 12V power if a transceiver is connected.

3) The power supply to the Real Time Clock on the PPC4B is fed from the +5VSTDBY pin on the VMEbus. VMEbus compliance requires this voltage to be 5V + 5% -2.5%. There is no provision for 3V standby.

Power-up Routine

You can now power-up the board. The PPC4B's operation immediately following power-up depends on the firmware fitted, as shown in Figure 3-5. The firmware option is shown by the last digit in the product order code, as follows:

1 = SilverChip
2 = BIT + SilverChip
3 = VxWorks
4 = BIT + VxWorks

The product order code is shown on the label on the outside of the shipping box and antistatic bag:

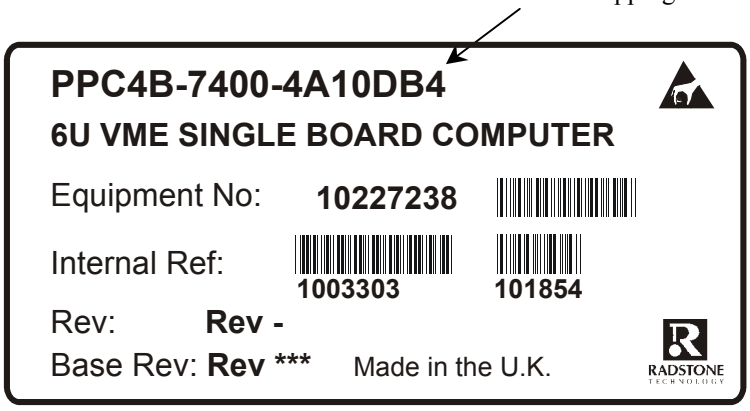
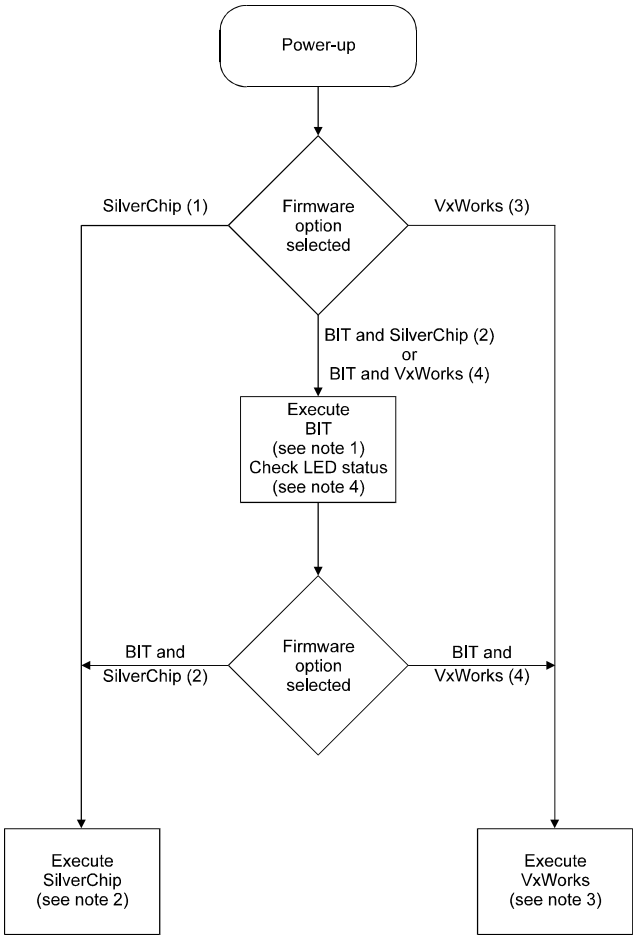


Figure 3-5. Firmware Flow on Power-up



Notes:

1) As BIT starts up, the first few lines you will see are similar to the following:

```
Using CCB at C0074000


Press any key to enter Options Menu after MPE


Radstone Technology Plc PPCBIT V3.2.3
====================================

Board Type : PPC4B 83 Mhz 750   Revision : 5A
Memory     : 128 Mb DRAM,
Cache      : 1024 Kb L2,
FLASH      : 16 Mb System Flash
```

For more details on BIT, see the BIT on PPCx User Guide, publication number RT5107.

2) As SilverChip starts up, the first few lines you will see are similar to the following:

```
Radstone Technology.
SilverChip PowerPC PReP Boot Firmware

Version: 3.50
Built (Jul 24 2000 14:05:48)

PPC4B-750 333MHz, 83MHz Bus Rev. 5A Ser. No. 9901243 ID No. 0x0
```

For more details on SilverChip, see the SilverChip (PPC Boot Firmware) Manual, publication number RT5078.

3) As VxWorks starts up, the first few lines you will see are similar to the following:

```
VxWorks System Boot


Copyright 1984-1996  Wind River Systems, Inc.



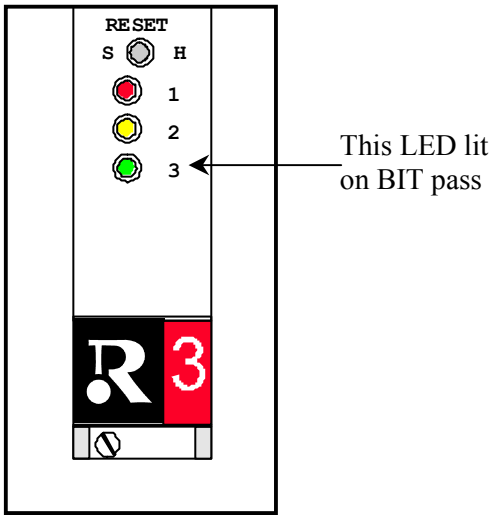

CPU: Radstone PPC4B-750
Version: 5.4
BSP version: 1.2/2
Creation date: May 21 2001, 17:39:32
```

For more details on VxWorks, see the VxWorks on PPCx User Guide, publication number RT5138.

4) If BIT is fitted (firmware option 2 or 4), as it runs through its power-up tests, it uses the LEDs on the PPC4B to show its progress and overall pass/fail. This is described in more detail in the BIT on PPCx User Guide (publication number RT5107), but briefly:

   - If BIT fails, the BIT Fail LED will be lit (see the BIT on PPCx User Guide for suggestions on what to do if this happens)
   - If BIT passes, the BIT Pass LED will be lit and the BIT Fail LED will be extinguished

   The red BIT Fail LED (LED0 in the Minimum Processing Environment tests) is LED '1' in the diagram below. The green BIT Pass LED (LED1 in the MPE tests) is LED '3' in the diagram below.



   After BIT has completed, the LEDs are user-programmable.

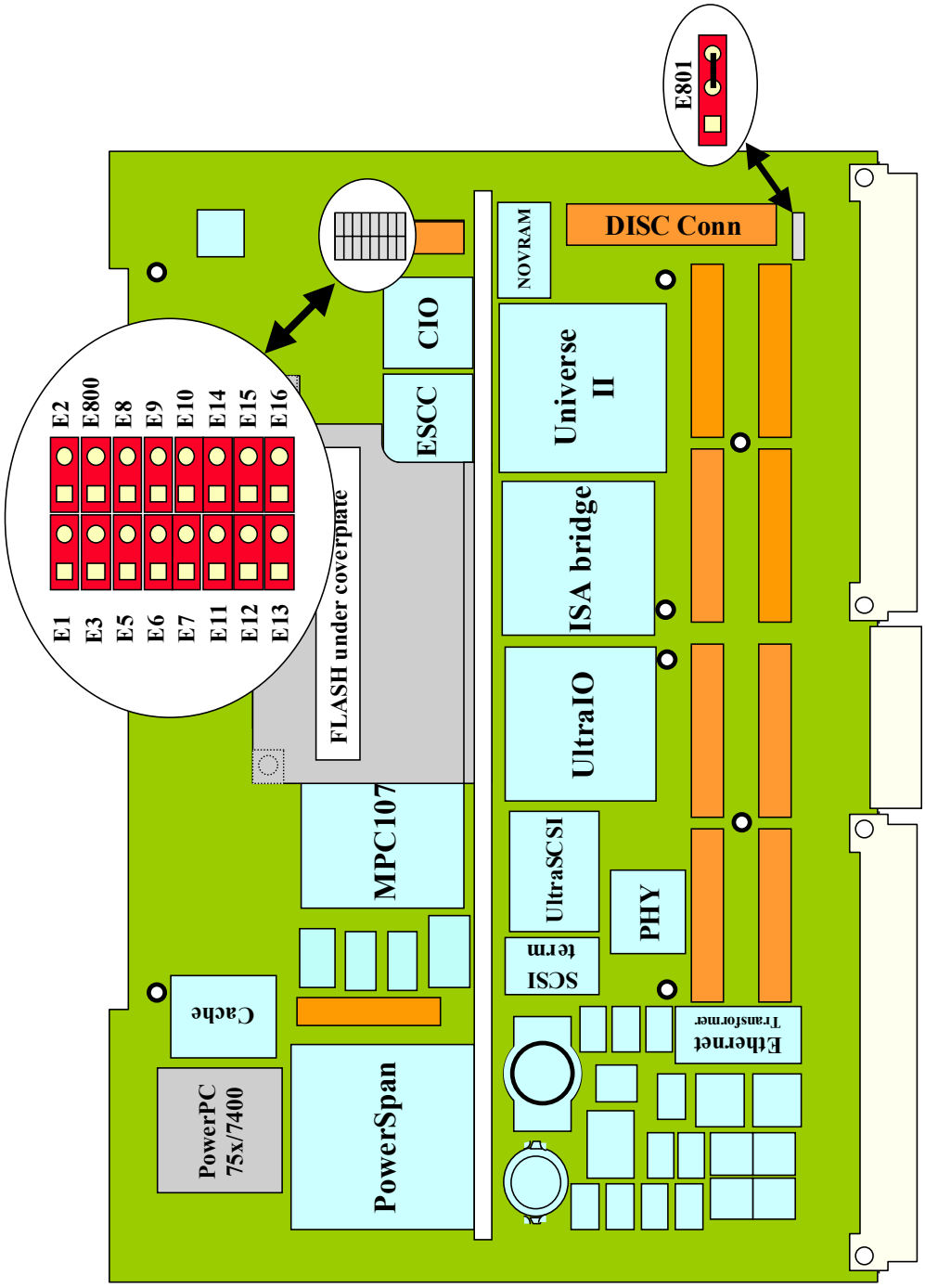
   If BIT is not fitted, the LEDs are user-programmable. LED '1' is ON by default after power-up.

5) See the Helpful Hints section in Chapter 8 for some suggestions to try if you experience problems (e.g. no display, BIT fails etc.)

Chapter 4 - Configuration

This chapter describes the configuration of links on the PPC4B. The board is delivered with push-on jumper links, but for rugged or Military applications, you are recommended to connect the posts using wire wraps.

Figure 4-1. Link Locations



Pin 1 of link blocks is shown by a square pad in the above and following diagrams.

Default Link Settings

Link	Setting	Action
E1	Out	Front panel reset switch disabled
E2	Out	Boot from System FLASH
E3	Out	Machine Check exception enabled
E5	Out	Write protect FLASH bank 2
E6	Out	Write protect FLASH bank 1
E7	Out	Factory link
E8	Out	Write protect FLASH bank 4
E9	Out	Write protect FLASH bank 3
E10, E14, E15 and E16	Out	ID links (board ID = 15) (unless in a 5-row backplane)
E11	Out	On-board SCSI terminators disabled
E12	Out	Universe PCI slave image 0 enabled
E13	Out	Normal FLASH bank operation
E800	Out	32-bit signalling on PCI bus to PMC sites
E801	Pin 2 to pin 3	5V signalling on PCI bus to PMC sites

If you wish to change any of these linkable options, refer to the appropriate section(s) in the following pages.

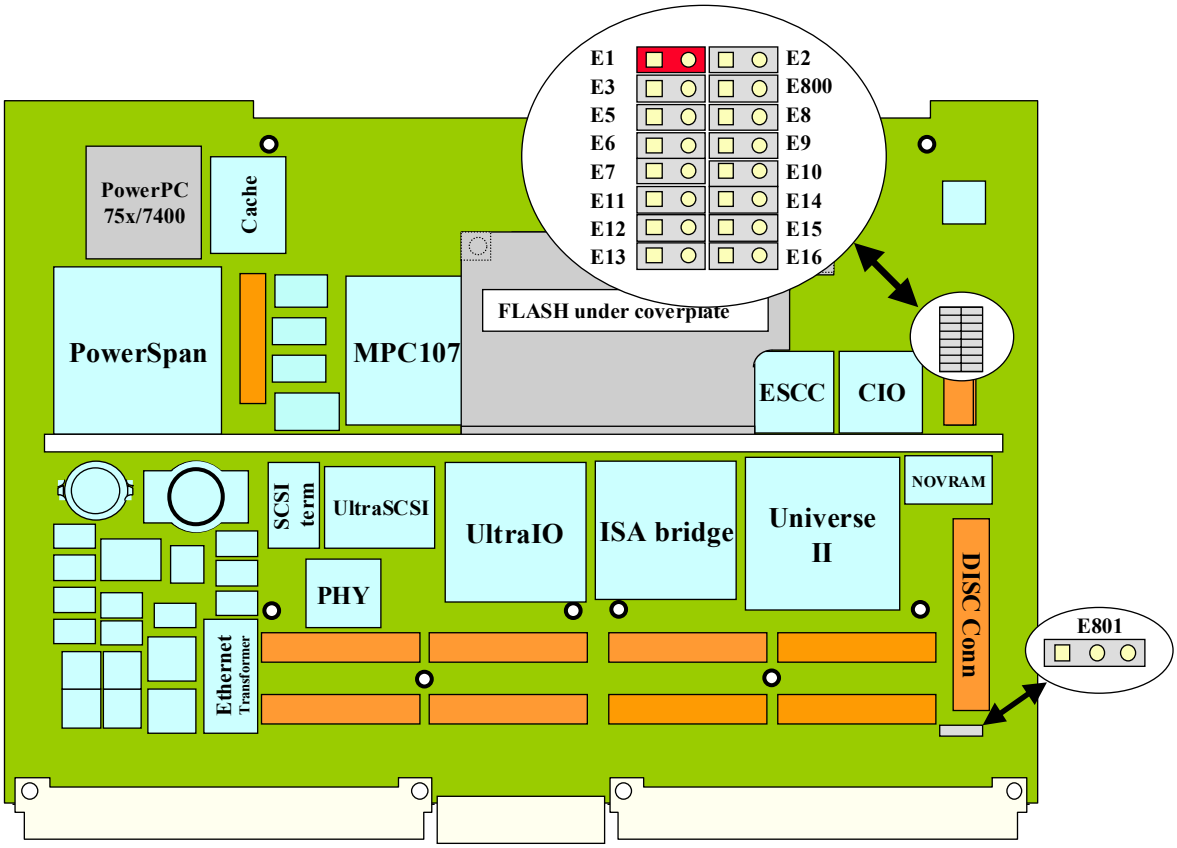
Caution
Only handle the board by the edges or front panel

Hint: If you are about to install your board and try a power-up for the first time, leaving your board with the above default configuration will enable you to prove operation before tackling any configuration issues.

Enable Front Panel Reset Switch Link (E1)

This link enables or disables the front panel reset switch, if the switch is fitted (not fitted on build levels 4 and 5):

Setting	Meaning
Out (default)	Disable reset switch
In	Enable reset switch



VME Boot Link (E2)

This link enables or disables booting of firmware over the VMEbus as follows:

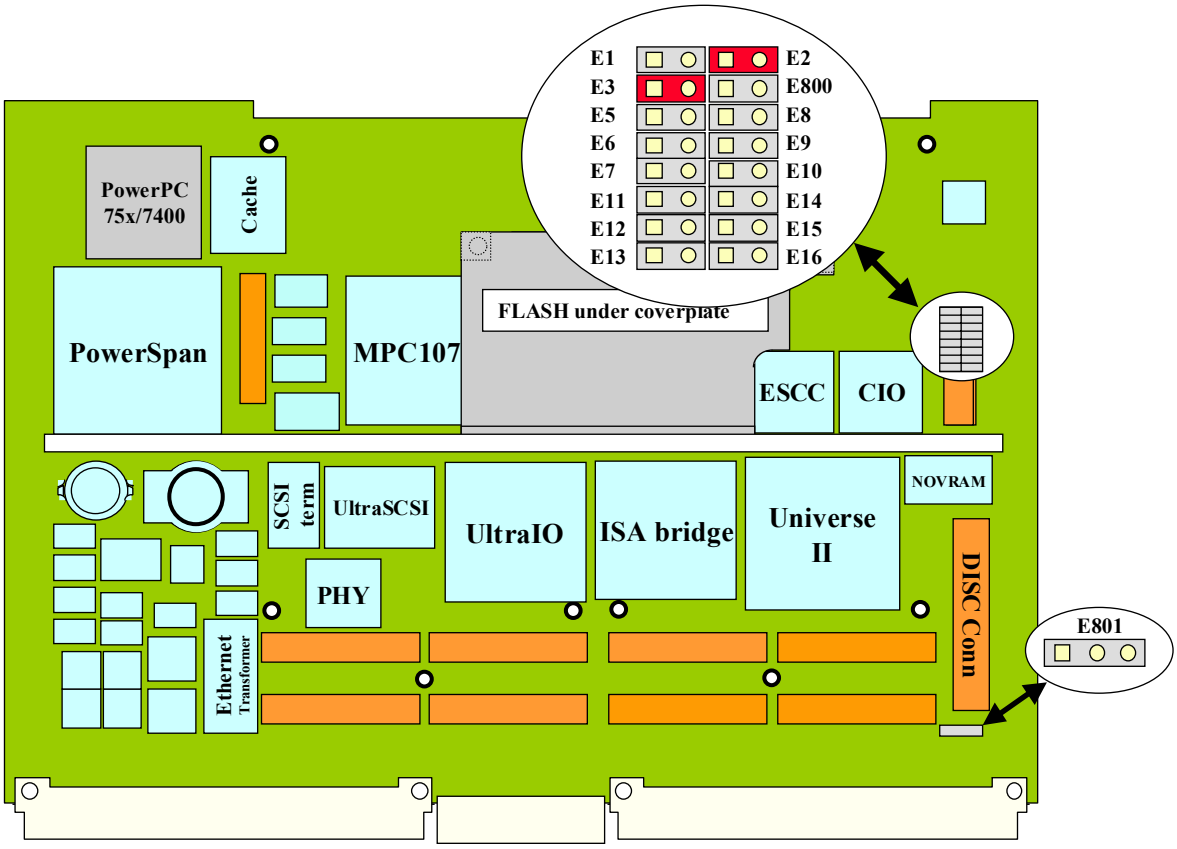
Setting	Meaning
In	Firmware boot over VME enabled
Out (default)	Firmware boot from System FLASH enabled

Use of this link relies on the default Universe configuration (see the VMEbus Interface Configuration section).

Machine Check Option Link (E3)

This link determines what action to take when the MPC107 PCI bridge signals a machine check due to a non-recoverable error. The options are to signal a machine check to the processor or to request an interrupt on IRQ13. For more details, see the Machine Check Exceptions section in Chapter 5.

Setting	Meaning
Out (default)	Machine Check exception enabled
In	Machine Check routed to IRQ13



FLASH Write Enable Links (E5, E6, E8 and E9)

These links enable or disable erasure/reprogramming of sections of the FLASH:

- E6 controls FLASH page 0
- E5 controls FLASH pages 1 to 3
- E9 controls the optional first unpaged 64 Mbyte extended section (MPC107 ROM bank 3)
- E8 controls the optional second unpaged 64 Mbyte extended section (MPC107 ROM bank 4)

See Chapter 5 for more details on FLASH operation.

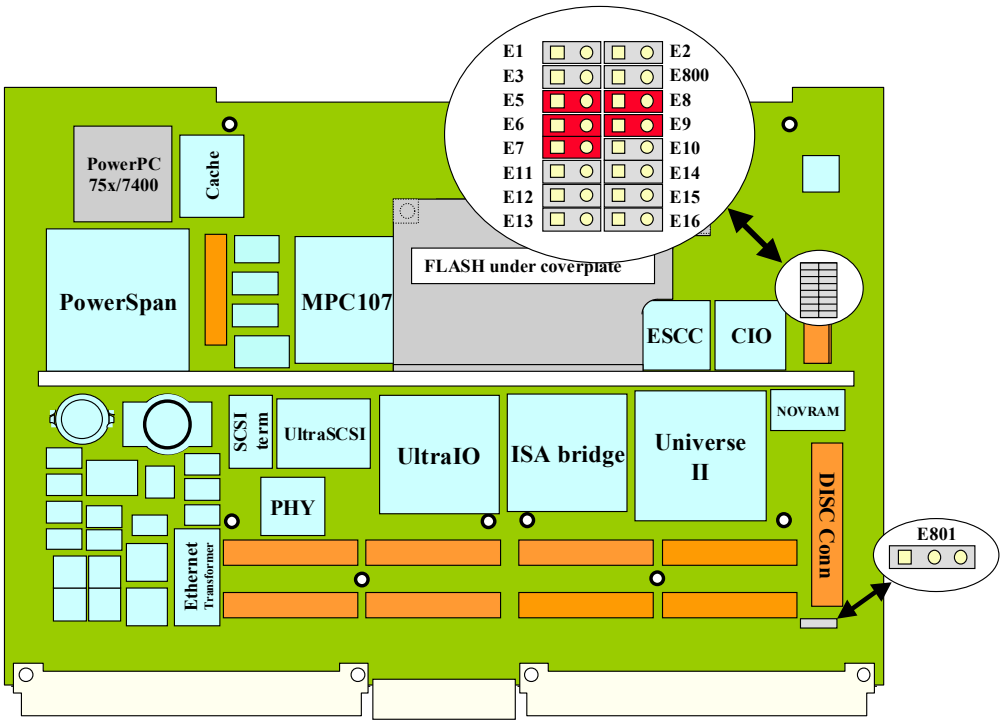
Setting	Meaning
In	Enable erasure/reprogramming of the section of FLASH
Out (default)	Disable erasure/reprogramming of the section of FLASH

Factory Link (E7)

This is a factory link, intended for initial debug purposes only, that overrides backplane write protection (FLASH_WREN~) and software control of the FLASH programming voltage. If this link is fitted, then the programming voltage to the FLASH is **only** controlled by links E5, E6, E8 and E9.

Note: **Do *not*** fit this link unless you only want E5, E6, E8 and E9 to turn on or off the FLASH programming voltage. If you fit the link for this purpose, remember to remove it after programming the FLASH.

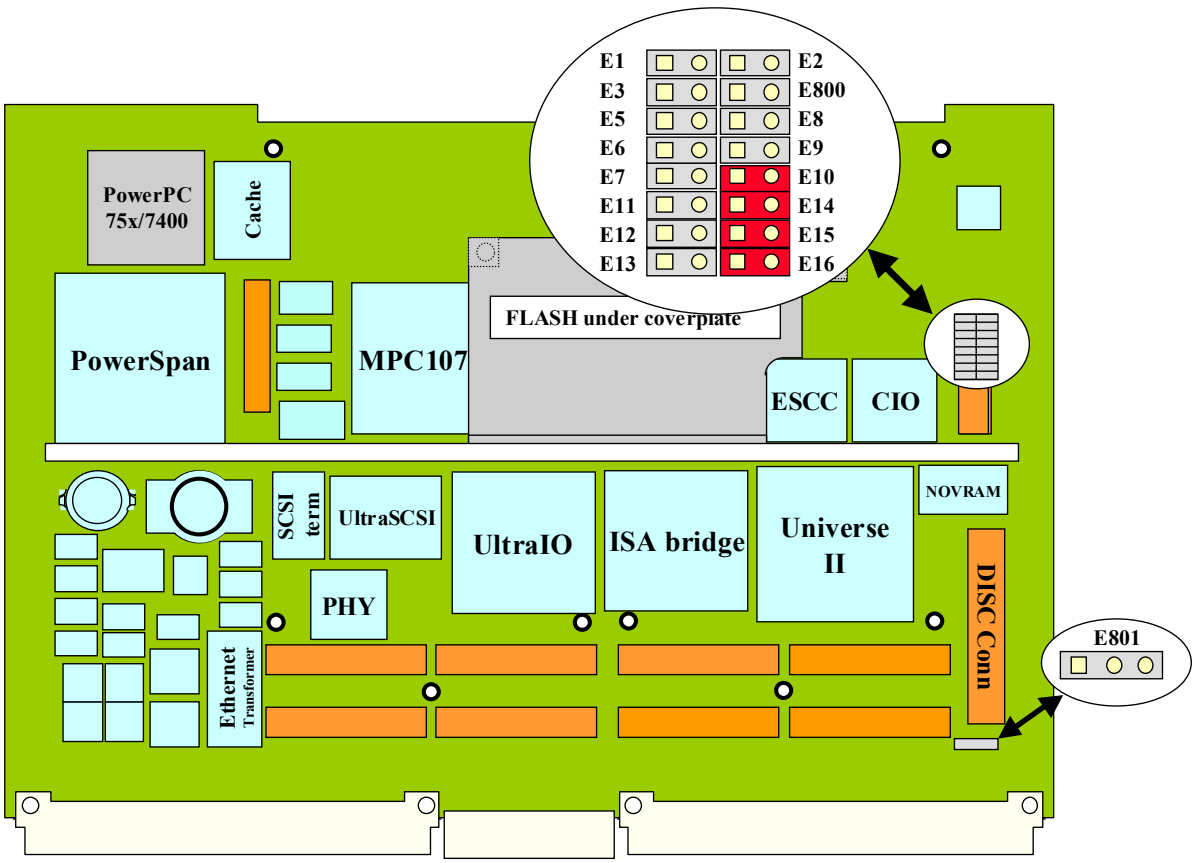
Setting	Meaning
Out (default)	Software controllable FLASH programming voltage
In	Software is not in control of the FLASH programming voltage



Geographical Addressing/Board ID Links (E10, E14, E15 and E16)

These links form a 4-bit board ID that may be read from the ID Link register (see Chapter 5). The links are decoded as follows:

Board ID	E10	E14	E15	E16
15 (default)	Out	Out	Out	Out
14	Out	Out	Out	In
13	Out	Out	In	Out
12	Out	Out	In	In
11	Out	In	Out	Out
10	Out	In	Out	In
9	Out	In	In	Out
8	Out	In	In	In
7	In	Out	Out	Out
6	In	Out	Out	In
5	In	Out	In	Out
4	In	Out	In	In
3	In	In	Out	Out
2	In	In	Out	In
1	In	In	In	Out
0	In	In	In	In



VME Slave Address Configuration

Chassis with VME64x-compliant backplanes provide Geographical Addressing facilities, i.e. the backplane slot position provides the board ID, as shown in the following table:

Slot	Slot 1 Functions	Board ID	A32 Address	A24 Address
1	Yes	0	0x00000000	0x000000
2	No	1	0x10000000	0x400000
3	No	2	0x20000000	0x800000
4	No	3	0x30000000	0xc00000
5	No	4	0x40000000	None
6	No	5	0x50000000	None
7	No	6	0x60000000	None
8	No	7	0x70000000	None
9	No	8	0x80000000	None
10	No	9	0x90000000	None
11	No	A	0xA0000000	None
12	No	B	0xB0000000	None
13	No	C	0xC0000000	None
14	No	D	0xD0000000	None
15	No	E	0xE0000000	None
16	No	F	0xF0000000	None

The Geographical Address signals GA0~ to GA3~ are brought onto the PPC4B through the P1 connector, where they are connected to links E16, E15, E14 and E10 respectively.

Caution

Do *not* fit the Board ID links if you wish to use Geographical Addressing, as the links override the Geographical Addressing signals where they are fitted.

The board ID also sets the board's VME slave addresses, as shown in the above table, so take care to avoid an address clash with other boards in the system.

Notes:

1) Any change to the Board ID links will require the hardware registers to be 'relearned' if BIT is not to fail.

2) BIT, if fitted, is set not to use Geographical Addressing by default. In this case, the Board ID must be set by the ID links.

On-board SCSI Terminator Enable Link (E11)

This link enables or disables the on-board SCSI terminators, as follows:

Disable On-board SCSI Terminators	Enable On-board SCSI Terminators
Out (default)	In

PCI Slave Image 0 Enable Link (E12)

This link determines whether the Universe PCI slave image 0 is enabled in PCI memory space at 0xF0000000 to 0xFFFFFFFF or disabled from power-up, as follows:

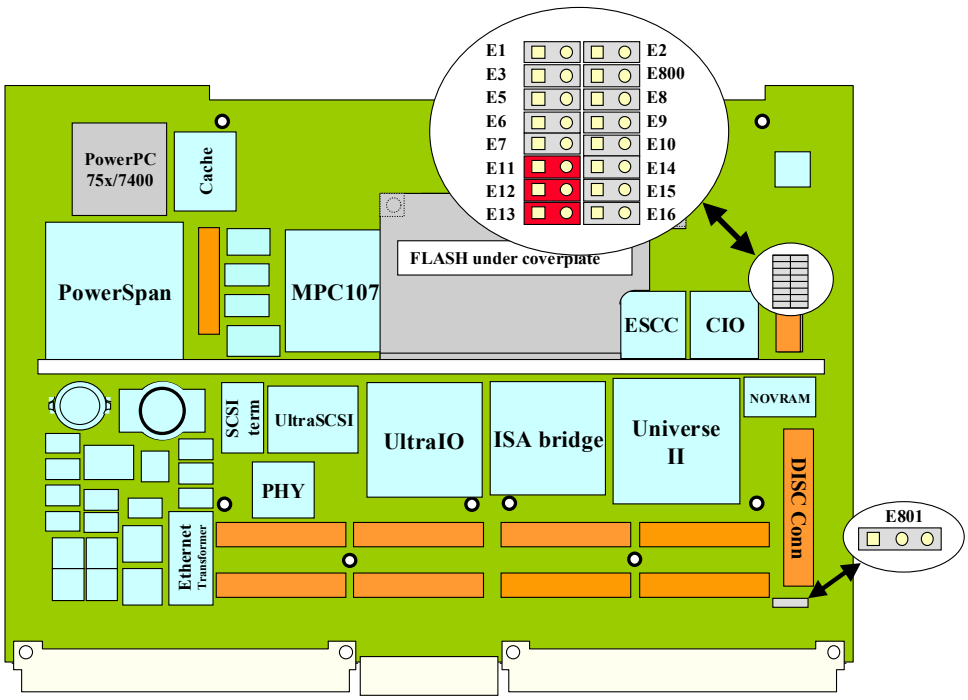
PCI Slave Image 0 Enabled	PCI Slave Image 0 Disabled
Out (default)	In

FLASH Bank Configuration Link (E13)

This link controls the bank configuration of the FLASH. Its state is reflected in the Memory Configuration Register (Port 0x0804) - see Chapter 5. Normally, this link is not fitted, and the FLASH banks operate as normal (see Chapter 5 for details of FLASH operation). When this link is fitted, the operation of the banks swaps over, that is when FLASH bank 1 is addressed, FLASH bank 2 is actually accessed, and vice-versa. This does not, however, affect the FLASH Write Enable links E5 and E6. They control the same FLASH bank regardless of the fitting of this link.

Normal FLASH Bank Operation	Swap FLASH Banks
Out (default)	In

Note: When this link is fitted and the PPC4B boots from FLASH, it boots from the swapped bank.



PMC Signalling Width Selection (E800)

This link controls whether 64-bit operation is enabled on the PCI bus that connects to the PMC sites, as follows:

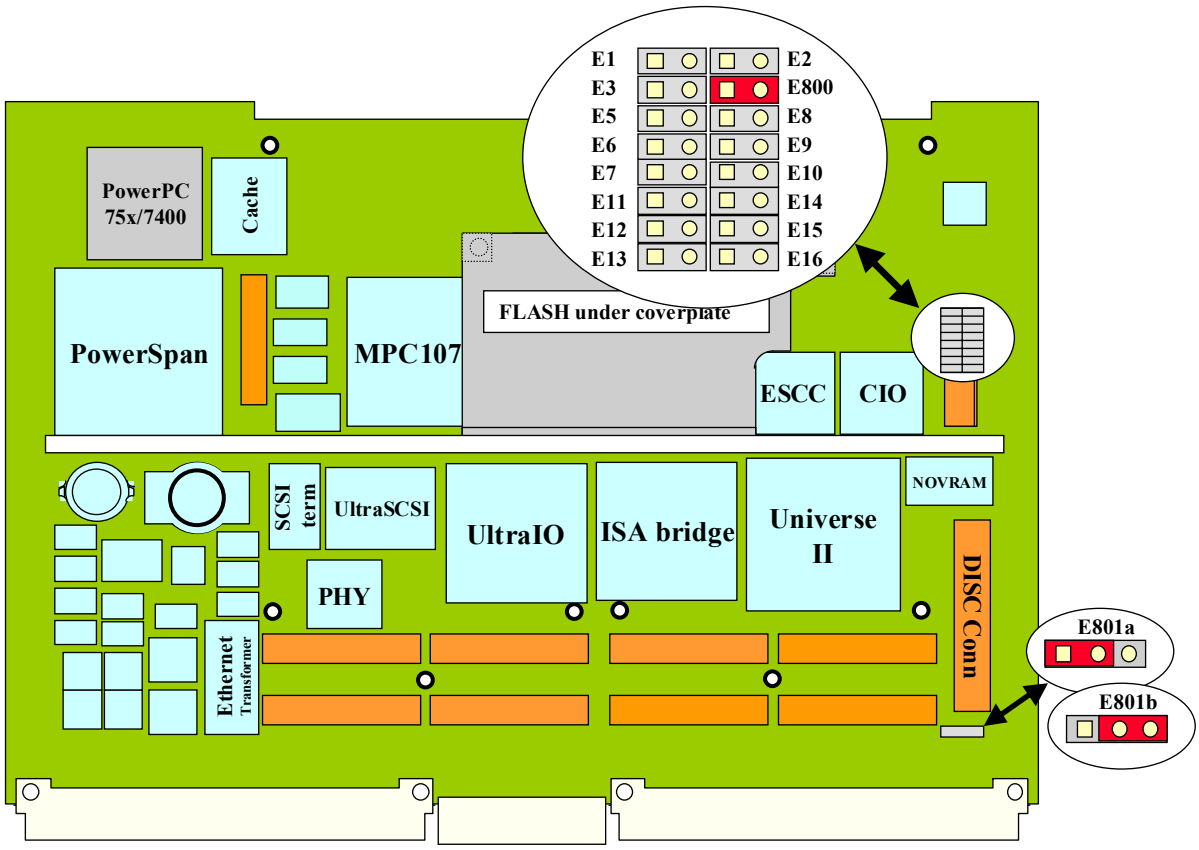
Setting	Meaning
Out (default)	64-bit signalling disabled (32-bit operation)
In	64-bit signalling enabled

PMC Signalling Voltage Selection Link (E801)

This is a two position link. It must be fitted in one of the two positions; no link fitted is not a valid setting.

The link selects the signalling voltage on the PCI bus to the PMC sites, as follows:

Setting	Meaning
Out	Not a valid setting
E801a	3.3V signalling
E801b (default)	5V signalling



Suggested Configuration

Although the default link configuration is for no links to be fitted, this may not suit your system, and you may need to fit links to configure your PPC4B before plugging it into your system. The following suggested link settings will be suitable in many cases:

Link	Setting	Action
E1	In	Front panel reset switch enabled
E2	Out	Boot from System FLASH
E3	In	Machine Check routed to IRQ13
E5	Out	Write protect FLASH bank 2
E6	Out	Write protect FLASH bank 1
E7	Out	Factory link
E8	Out	Write protect FLASH bank 4
E9	Out	Write protect FLASH bank 3
E10, E14, E15 and E16	Out	ID links (board ID = 15) (unless in a 5-row backplane)
E11	In	On-board SCSI terminators enabled
E12	Out	Universe PCI slave image 0 enabled
E13	Out	Normal FLASH bank operation
E800	Out	32-bit signalling on PCI bus to PMC sites
E801	Pin 2 to pin 3	5V signalling on PCI bus to PMC sites

If you are using the SCSI bus, you are recommended to locate the PPC4B at one end and enable the terminator by fitting link E11. If you want to use the PPC4B somewhere other than at the end of the SCSI bus, ensure that E11 is not fitted. **Fitting E11 when the PPC4B is not located at the end of a SCSI bus may cause erroneous SCSI operation.**

The power supply to the RTC on the PPC4B is fed from the VSTANDBY pin on the VMEbus. VMEbus compliance requires this voltage to be 5V ± 5%. There is no option for a 3.3V standby voltage.

VMEbus Interface Configuration

Several operating features of the Universe VME interface are set at power-up or reset by surface mount jumper links. All of these, except local register access, may be overridden by software. The default settings are:

Operating Feature	Setting
Register access slave image from VMEbus:	Enabled in A32 space at 0x80000000
VME CR/CSR slave image:	Disabled
PCI slave image 0:	Enabled in PCI memory space at 0xF0000000 to 0xFFFFFFFF †
Local register access:	PCI I/O space
Auto-ID scheme:	Disabled

Changing the default power-up options requires surface-mount rework tools and would normally only be done at the factory. Further details are available from technical support at Radstone.

† The PCI slave image 0 may be disabled from power-up by fitting link E12.

Chapter 5 - Functional Description

This chapter gives a functional description of the PPC4B.

Overview

The PPC4B is a highly integrated, CHRP-based VMEbus processor using the PowerPC 750 or 7400 RISC CPU with private L2 cache bus. The product offers an extensive range of standard functions including:

- Processors clocked at 333 MHz and above (350 MHz and above for the PowerPC 7400)
- 1 Mbyte of L2 cache on a private L2 cache bus (2 Mbytes for 7400 boards)
- User SDRAM up to 512 Mbytes on-board with ECC
- Up to 192 Mbytes of FLASH memory
- 512 Kbytes of EEPROM
- An Ultra-SCSI peripheral interface controller
- A 64-bit VMEbus interface using the Tundra Universe II VMEbus interface chip
- Direct connection for a keyboard and mouse
- Floppy disk controller
- Parallel/printer port
- On-board PCI Ethernet controller giving 10/100BaseT or 10Base 5 operation
- Two RS232 serial I/O channels up to 115.2 kbaud

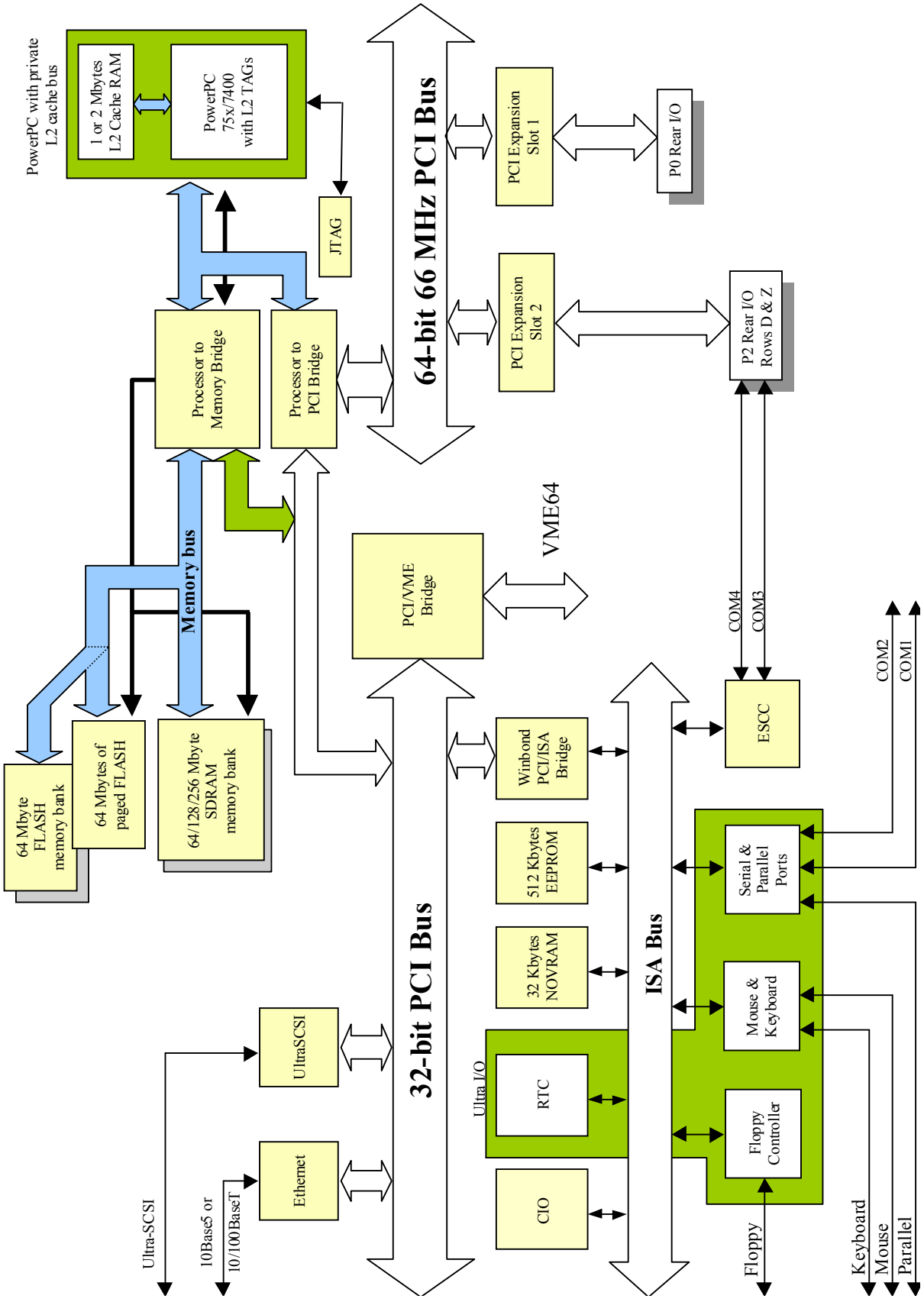
Expansion capabilities are provided by two PCI interface slots. PCI (PMC - IEEE P1386.1) provides an industry standard, high speed (up to 528 Mbytes/second) local expansion bus, designed for:

- Graphics
- High-speed communications (e.g. ATM, Fibre Channel, ISDN, etc.)
- Multi-media
- User-defined custom functions

PCI has established itself as the leading local interconnect standard, and the wide availability of compatible devices, coupled with its adoption on an array of platforms, ensures that PCI-based modules are both high-performance and low cost.

The highly integrated nature of the PPC4B makes it a true single board computer. In many ways, the PPC4B resembles a high performance PC motherboard, although in a more rugged, lower profile and more compact form factor.

Figure 5-1. PPC4B Block Diagram



Features

- Processor options of PowerPC 750 at 333 MHz and above or PowerPC 7400 at 350 MHz and above (**contact your nearest Sales office for details of speed grades**)
- Five build level options, three air-cooled and two conduction-cooled, gives maximum component reuse across multiple platforms
- Up to 512 Mbytes of on-board SDRAM with ECC for memory intensive applications
- Two 64-bit/66 MHz PCI/PMC expansion slots on-board give system expansion using IEEE P1386.1 standard single or double width PMCs
- Optional PCI expansion bridge (on a PMC card) and PMC carrier cards future proof your system design by enabling PCI sub-system expansion to add new, low cost interface capability as required
- Optional extra two fully featured RS232 or RS422/RS485 serial ports channels (in addition to two serial COM ports)
- Radstone COTS software support includes BIT, Boot firmware, BSPs and ESPs (with BCS) for LynxOS/LynxOS HA and VxWorks/Tornado,
- Wide range of shrink-wrapped application software available
- 64 Mbytes of paged FLASH ROM
- Up to 128 Mbytes of extended FLASH ROM
- 32 Kbytes of NOVRAM
- Real Time Clock (TOD/calendar)
- High-resolution graphics (via a PMC slot)
- Single slot 6U VME board form factor for reduced system cost and slot count
- Range of 3U rear-mounting I/O modules
- CHRP based design
- ANSI/VITA 1-1994 VME64 and VME64 extensions (5 row P1 and P2) compatible
- JTAG connections available via P0 connector
- Optional software maintenance giving automatic software revision updates and technical support
- Optional hardware and on-board firmware configuration management service giving a unique part number requiring customer authorisation for changes in product revision status

PowerPC Common Hardware Reference Platform

The PowerPC Common Hardware Reference Platform (CHRP) is an example implementation of a philosophy designed to allow software compatibility across different platforms based on the PowerPC processor. Aiming to achieve an open standard, the CHRP encourages the use of industry standard components and buses, and a wide range of operating systems.

As well as providing a detailed hardware design specification, the CHRP also embodies a software mechanism that allows the hardware to be isolated from the application by abstraction layers. It is these abstraction layers (in effect very low-level system drivers) that are the key to differentiation, scalability and future-proofing. The operating systems, applications and drivers can 'sit' on these layers without needing to be aware of the underlying hardware (other than general functionality). This is fundamentally different from PCs, which use a BIOS that ultimately constrains operating systems and applications alike.

The major purpose of the CHRP architecture "... is to give direction to system designers, while still enabling differentiation in areas where real value can be added, thus allowing the PowerPC microprocessor industry to build a reusable body of OS and application software...". The knowledge that both OS and application programs will run on any host that complies with the CHRP architecture, provides security for today's valuable software investments, as well as expansion capabilities for the future.

PowerPC Processor

The PPC4B is based around the MPC750 PowerPC chip. The PowerPC has become the most widely used of the new generation of RISC processors. Its pedigree is unequalled - jointly developed by world-leading computer companies and backed by long-term commitments from major OEMs.

The PowerPC 750 features:

- A 32-bit superscalar RISC processor implementing the PowerPC architecture
- A 32-bit physical address bus and a 64-bit external data bus
- On-chip 32 Kbyte 8-way set associative instruction and data caches
- MMU and integral FPU
- A large primary cache
- Enhanced branch prediction capabilities
- An on-chip L2 cache controller that connects to a private 64-bit wide, 2-way set associative L2 cache bus operating at up to 200 MHz

The PowerPC 750 implements a fully static architecture and offers sophisticated power management capabilities. As a result, its maximum power consumption is 6 Watts at 333 MHz.

As a build option, the PPC4B may be supplied with a PowerPC 7400 device, which adds Motorola's AltiVec 128-bit wide vector parallel processing unit to the 750 architecture.

The following table shows above the relative performance and power dissipation of the CPUs. These estimated values are supplied by PowerPC vendors. Radstone PowerPC SBCs use these processors in a standard CHRP architecture, providing a balanced general-purpose platform. The actual performance and power dissipation may vary depending on the application being run and resource usage of the configured system.

PowerPC CPU	CPU Frequency (MHz)	SPECint95	SPECfp95	CPU Power (Watts)
750	333	14.7	9.9	6.0
750	500	23.9	14.6	7.5
7400	450	21.4	19.5	11.5 (at 400 MHz)

The following table shows the frequency parameters for the chips:

Processor Type	Bus Frequency (MHz)	L2 Frequency (MHz)	Core Frequency (MHz)
MPC750	83.3	116.6 to 200	333 and above
MPC7400	83.3	116.6 to 200	350 and above

Memory

Level 2 Cache

The PPC4B provides L2 cache, connected to a separate L2 cache bus, as follows:

- 1 Mbyte on PowerPC 750 boards
- 2 Mbytes on PowerPC 7400 boards

By using a private cache bus, the cache traffic does not consume memory bus bandwidth.

The L2 cache is two-way set associative with a line size of 32 bytes, and is 64 bits wide. It is capable of operating in write-through or write-back modes, and can operate at speeds up to 133 MHz through a dedicated L2 cache bus interface. Having the L2 cache controller inside the MPC750 allows performance to be further enhanced by parallel compares on L1 and L2 tags, and filtering L2 cache traffic from the system bus. Memory accesses in the address range 0x00000000 to 0x30000000 (i.e. SDRAM) are cacheable by the L2 cache. Entries in write-through mode can be valid or invalid. Entries in write-back mode can be invalid, valid-unmodified or valid-modified. Full coherency on the system bus can be maintained.

L2 cache access times from the processor for a 32-byte burst are:

	133 MHz L2 Interface	Transfer Rate
Burst read hit non-pipelined	3,1,1,1	711 Mbytes/second
Burst read hit pipelined	1,1,1,1	1066 Mbytes/second

PCI Bridge and Memory Controller

The Motorola MPC107 and CA91L8200 PowerSpan form the Memory to PCI bridge. They interface the SDRAM and FLASH to the PowerPC processor and the two PCI buses.

The MPC107 provides a memory controller that supports a variety of DRAM, and FLASH or ROM configurations as main memory. The PPC4B is fitted with up to 512 Mbytes of SDRAM and up to 192 Mbytes of FLASH. The MPC107 can be configured for either ECC or parity generation data protection on the DRAM.

NOVRAM

There are 32 Kbytes of NOVRAM on the ISA Bus for maintenance of general system parameters, such as boot options, Ethernet addresses and VME configuration. See the ISA Bus Peripheral Components section for more details.

EEPROM

There are 512 Kbytes of EEPROM on the ISA Bus for large non-volatile storage with convenient byte update capability. See the ISA Bus Peripheral Components section for more details.

System RAM (SDRAM)

Between 64 and 512 Mbytes of SDRAM can be fitted directly to the PPC4B as shown in the following table:

SDRAM Size (Mbytes)	Banks	Organisation
64	1	8M x 72
128	1	32M x 72
256	2	32M x 72
512	2	64M x 72

All system memory runs contiguously and is dual-ported between the processor and PCI.

The MPC107 controls the memory. The MPC107 can be configured to provide either Error Correction Coding or parity data protection. The SDRAM has eight ECC or parity bits per 64 data bits. ECC is capable of detecting all single bit, double bit and nibble errors, and correcting single bit errors.

Following a hard reset, the MPC107 must be set up for the size and number of banks of SDRAM, and the appropriate number of wait states to match the SDRAM speed. This is done by the standard boot monitor firmware (SilverChip). The size of SDRAM may be checked by reading the Memory Configuration register (see the Control and Status Registers section). At least 100µs must have elapsed from the negation of reset before enabling the SDRAM. After being enabled, the SDRAM must not be accessed until at least 8 refreshes have occurred. If parity or ECC is to be enabled, then it is necessary to initialise the SDRAM to set-up valid parity bits.

The following table shows SDRAM access times from the processor, for a 83.3 MHz bus clock, for a 32 byte burst assuming RAS~ has been pre-charged and no pipelined page hit:

ECC Operation	Clocks Initial Access/Subsequent	Sustained Data Transfer Rate
With ECC	6-1-1-1	296.3 Mbytes/second
Without ECC	4-1-1-1	363 Mbytes/second

The following table shows SDRAM access times from the PCI, referenced to the 33 MHz PCI clock, for a 32-byte burst with no interference from L1 or L2 caches:

	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate (Mbytes/second)
Burst read	4-1-2-1-2-1-2-1	76
Burst write	2-1-1-1-1-1-1-1	118

Note: Integrity of SDRAM data cannot be guaranteed during a hard reset, as the memory controller is reset and SDRAM refresh disabled.

System/User FLASH ROM

64 Mbytes of paged FLASH provides the standard combined System and User ROM. The System ROM holds initialisation and operating system boot routines. A further 128 Mbytes of (non-paged) FLASH can also be fitted, providing a total of 192 Mbytes of 64-bit wide, directly accessible FLASH.

The FLASH pages are 16 Mbytes in length and reside at addresses 0xFF000000 to 0xFFFFFFFF in the processor memory map. They are controlled by the FLASH Paging Register (Port 0x080A). This register is cleared on reset, forcing page 0 to be the "boot page". The 16 Mbyte boot page can be considered as two individual 8 Mbyte sections: the "boot section" and the "alternate boot section". Normally processor accesses in the range 0xFF800000 to 0xFFFFFFFF go to the boot section, and processor accesses in the range 0xFF000000 to 0xFF7FFFFF go to the alternate boot section. However, fitting link E13 maps the alternate boot section into the boot section (and vice-versa). If the board is reset, it now boots from the alternate boot image. This link E13 swap-over only occurs when page 0 is selected, and works for both reads from and writes to page 0. The state of link E13 is reflected in the Memory Configuration Register (Port 0x0804).

Link E6 provides write protection for the boot page (page 0), when removed. Link E5 provides write protection for the rest of the paged FLASH, when removed.

The PPC4B can have a further two banks of FLASH, each of 64 Mbytes, fitted on-board. This FLASH is not paged. Link E9 provides write protection (when removed) for the first bank, and link E8 provides write protection (when removed) for the second. The Extended Memory Register (Port 0x806) shows which banks are fitted.

An overall write protection signal (FLASH_WREN~) is provided on P2 pin Z1 (and P0 pin A2, where fitted), which prevents erasure or reprogramming of all FLASH devices on the card when high. This is its default state if not connected to on the backplane.

Link E7, when fitted, overrides both the FLASH_WREN~ signal and all software control of the programming voltage (Vpp). Links E5, E6, E8 and E9 then control Vpp directly (see Chapter 4 for more details). Link E7 is intended for initial debug purposes only. After programming the FLASH, remember to remove link E7.

All of the FLASH may also be programmed by JTAG. See the JTAG section for more details.

The FLASH has a write capacity of 100,000 cycles per bank, and the software should write to the FLASH as 64-bits.

Note: Integrity of FLASH data cannot be guaranteed if a hard reset occurs during a FLASH write cycle.

If boot code is lost or corrupted, the VME boot option allows the boot section of the FLASH to be rewritten (see the VME Boot Option section overleaf).

The PPC4B has the same FLASH programming support as previous generation PPCx processors, so SCSI and Ethernet can be used for reprogramming the FLASH. Production/development at Radstone uses the SilverChip Boot Firmware to program the FLASH via the Ethernet, SCSI or VME. This feature is also available to the end-user using SilverChip.

VME Boot Option

Fitting link E2 and removing link E12 (see Chapter 4) allows the PPC4B to boot using code held in memory located on the VMEbus. This operation relies on the factory default power-up configuration for the VMEbus interface (see Chapter 4). The VME memory must be located in A32 space at address 0xFFF00000 and must be 32 bits wide (D32).

In this mode, accesses that would normally go to the FLASH now go to the PCI bus. The Universe converts these accesses to VME cycles. In this mode of operation, you can re-map the boot section of the FLASH (0xFF800000 to 0xFFFFFFFF) to address 0xFF000000 by setting the Configuration bit CF_FF0_LOCAL in MPC107 register 0xA8. You can now read from and write to the boot section of the FLASH using the address range 0xFF000000 to 0xFF7FFFFF. All writes should be 64-bit aligned accesses.

Note: In this mode, access to the original FLASH at 0xFF000000 to 0xFF7FFFF is not possible.

Once you have programmed the boot section of the FLASH, remove link E2 and carry out a hard reset. Normal booting now occurs from the FLASH and both sections are accessible again at their normal addresses.

Memory Maps

The PPC4B supports a CHRP memory map. It also supports both big and little endian byte addressing modes on the PCI.

In the following memory maps, no fixed addresses are given for PCI connected resources (SCSI, Ethernet, VME bridge and PMC slots), since the boot process configures these addresses.

Seen by the Processor

At power-up or after a hard reset, the PowerSpan PCI Bridge is not configured, so the MPC107 is used instead. In this case, the processor sees the following memory map:

Processor Address Range		PCI Address Range	Cycle Type
00000000	2FFFFFFF	No PCI cycle	System memory space
30000000	3000FFFF	No PCI cycle	PowerSpan
30010000	77FFFFFF	No PCI cycle	Reserved
78000000	7BFFFFFF	No PCI cycle	Extended User FLASH
7C000000	7FFFFFF	No PCI cycle	Extended User FLASH
80000000	FCFFFFFF	80000000 to FCFFFFFF	PCI memory space
FD000000	FDFFFFFF	00000000 to 00FFFFFF	PCI/ISA memory space
FE000000	FEBFFFFF	00000000 to 000BFFFF	PCI/ISA I/O space
FEC00000	FEDFFFFF	MPC107 CONFIG_ADDR	PCI configuration address register
FEE00000	FEEFFFFF	MPC107 CONFIG_DATA	PCI configuration data register
FEF00000	FEFFFFFF	FEF00000 to FEFFFFFF	PCI interrupt acknowledge
FF000000	FF7FFFFF	FF000000 to FF7FFFFF	User FLASH
FF800000	FFFFFFFF	FF800000 to FFFFFFFF	Boot FLASH

During normal operation, the MPC107 is disabled for PCI accesses, and the PowerSpan is used to access the PCI address range. The memory map the becomes programmable, with the following fixed addresses:

Processor Address Range		PCI Address Range	Cycle Type
00000000	2FFFFFFF	No PCI cycle	System memory space
30000000	3000FFFF	No PCI cycle	PowerSpan
30010000	77FFFFFF	No PCI cycle	Reserved
78000000	7BFFFFFF	No PCI cycle	Extended User FLASH
7C000000	7FFFFFF	No PCI cycle	Extended User FLASH
80000000	FEBFFFFF	User Programmable	PowerSpan address window
FEC00000	FEDFFFFF	MPC107 CONFIG_ADDR	PCI configuration address register
FEE00000	FEEFFFFF	MPC107 CONFIG_DATA	PCI configuration data register
FEF00000	FEFFFFFF	FEF00000 to FEFFFFFF	PCI interrupt acknowledge
FF000000	FF7FFFFF	FF000000 to FF7FFFFF	User FLASH
FF800000	FFFFFFFF	FF800000 to FFFFFFFF	Boot FLASH

PCI Memory Space Seen by the PCI Master

Approximately 1 Gbyte is available for PCI memory space as seen by the processor.

PCI Memory Address Range		Local Memory Cycle	Cycle Type
00000000	0007FFFF	No local memory cycle	EEPROM
00080000	007FFFFF	No local memory cycle	ISA/PCI memory space†
00800000	0087FFFF	No local memory cycle	NOVRAM
00880000	00FFFFFF	No local memory cycle	ISA/PCI memory space†
01000000	7EFFFFFF	No local memory cycle	PCI memory space
7F000000	7FFFFFFF	No local memory cycle	Reserved
80000000	FFFFFFFF	00000000 to 7FFFFFFF	System memory space

† Subtractively decoded by the ISA bridge if no PCI slave responds.

PCI I/O Space Seen by the PCI Master

Approximately 1 Gbyte is available for PCI I/O space as seen by the processor.

PCI I/O Address Range		Local Memory Cycle	Cycle Type
00000000	0000FFFF	No local memory cycle	ISA/PCI I/O space
00010000	007FFFFF	No local memory cycle	Reserved
00800000	3F7FFFFF	No local memory cycle	PCI I/O space
3F800000	3FFFFFFF	No local memory cycle	Reserved
40000000	FFFFFFFF	No local memory cycle	Reserved

PCI

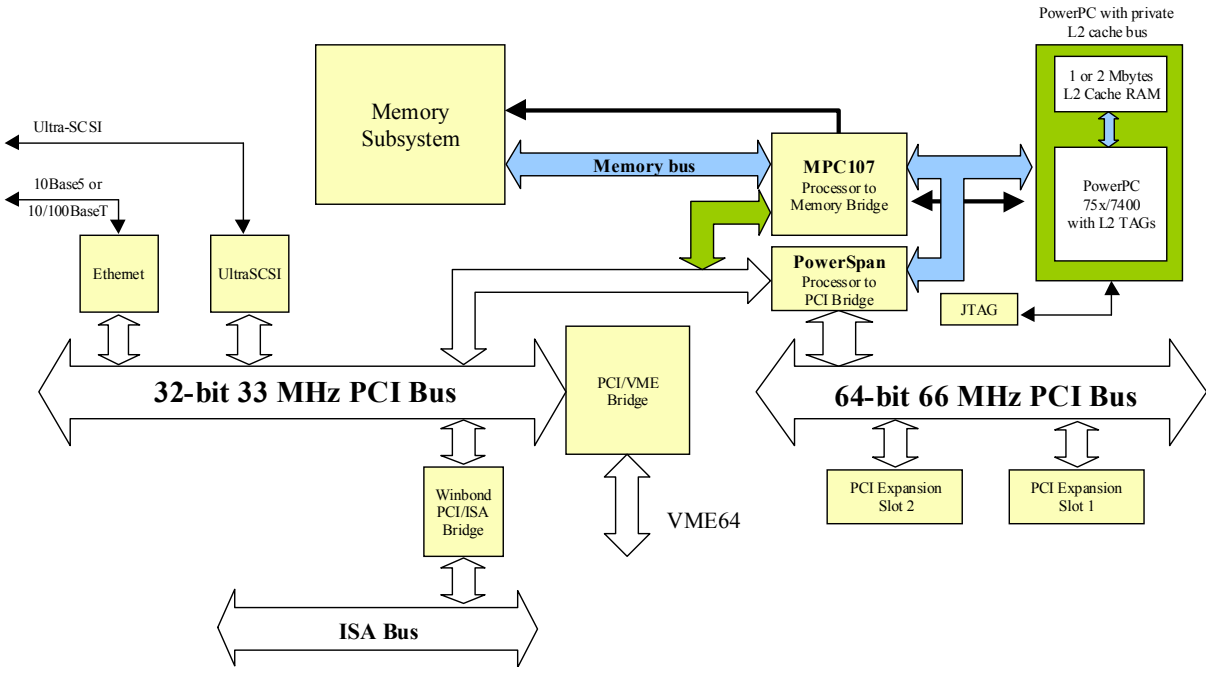
PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. It provides a synchronous 32- or 64-bit multiplexed address and data bus (at speeds of 33 or 66 MHz), allowing burst data transfers to 528 Mbytes/second.

The PPC4B has two PCI buses: one for internal PCI devices and one that allows communication with optional mezzanine expansion modules (PMCs). The internal PCI bus runs at 33 MHz and has a fixed data width of 32-bits. The PowerPC processor, Ethernet, Ultra-SCSI, VME interface controller and ISAbus Bridge (all of which have direct PCI connectivity) are attached to this bus, which provides a high-speed backbone for local interconnection of on-board devices. The Tundra Universe II chip provides full PCI to VME bridge capability.

Two PMC sites are provided as standard on the PPC4B. The PCI bus that connects to these PMC sites can run at 66 MHz and 64-bits wide (PCI64) or 33 MHz and 32-bits wide (PCI32), depending on the PMCs fitted. PCI64 gives a maximum burst transfer data rate of 528 Mbytes/second, compared with 132 Mbytes/second for PCI32. If a PMC is fitted that is not capable of running at 66 MHz, the PPC4B reduces the frequency to 33 MHz for *both* PCI slots. The PCI mezzanine format also provides 64 I/O pins for user definition.

The diagram below shows the main bus structure.

Figure 5-2. Main Bus Structure



The PowerSpan provides the processor access to both of the PCI buses, and also provides the PCI buses with a route to the processor bus resources. The MPC107 is connected to the internal PCI bus, but should not be considered as a PCI host bridge as, in normal operation, the MPC107 will neither source nor sink any PCI data. The exception to this is in generating PCI configuration cycles to the PowerSpan. The MPC107 interrupt response mechanism is also available. When the system boots from VME (link E2 fitted, link E12 not fitted), the MPC107 passes FLASH accesses to the PCI bus, so there is no need to set up a processor-to-PCI window in the PowerSpan for this operation.

Physical hardware on the PPC4B prevents the MPC107 becoming a bus master on the processor bus. This means that only the PowerSpan can provide PCI interfacing and DMA resources. The PowerSpan may be programmed to provide a PCI-to-PCI bridge function between the two PCI buses.

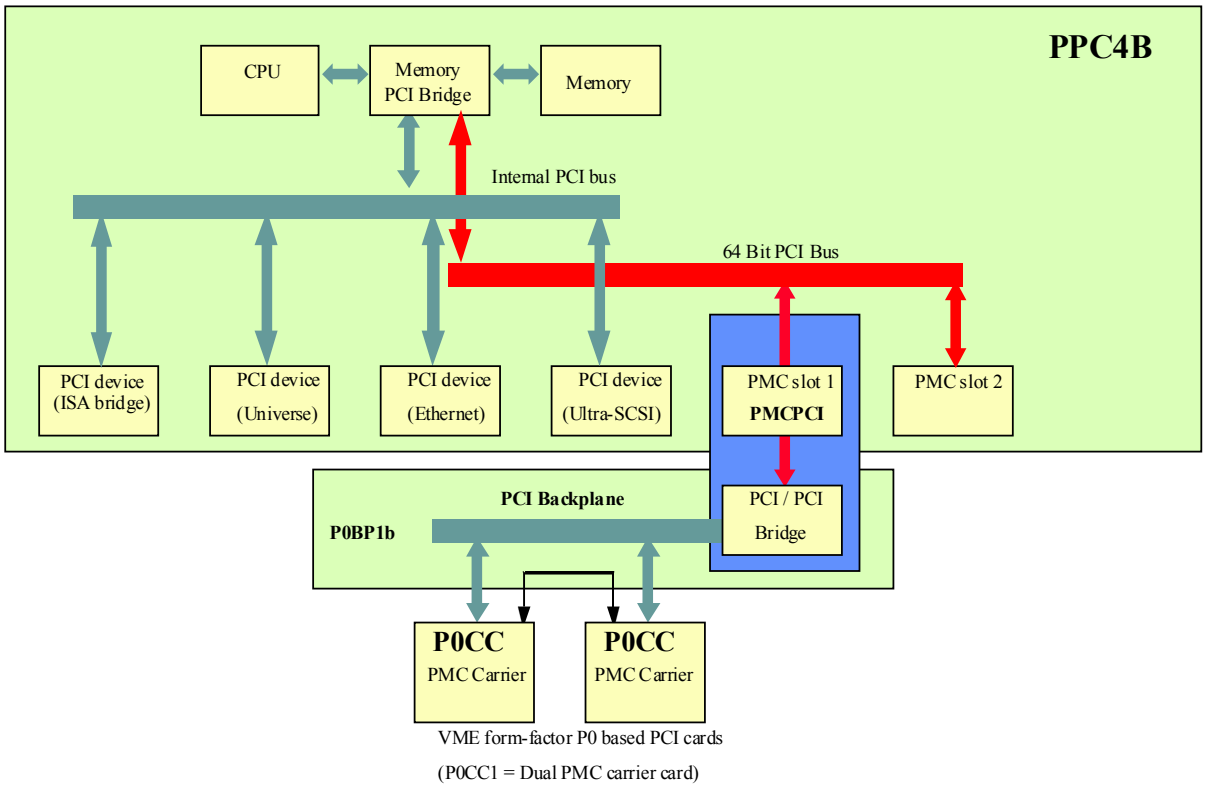
PCI Expansion Bus

In addition to the two on-board slots supporting air- or conduction-cooled PMCs, the PPC4B offers expansion of slots via a family of standard PMC Carrier Cards.

The PCI sub-system can support from 2 to 9 PMCs in a standard VME chassis. The P0CC1 6U PMC Carrier is a single-slot replacement unit supporting two single-width or one double-width PMCs, which can be linked to the PPC4B host via the P0/J0 interface on each card.

For those configurations requiring additional PCI functionality, Radstone's PMC PCI Bridge card (PMCPCI) bridges the on-board PCI bus out via the P0 connector, as shown below:

Figure 5-3. PCI Interconnectivity



Having done this, the user is free to:

- Use Radstone's range of P0 PMC carriers
- Interface the PPC4B directly to Radstone's range of SHARC-based DSP boards
- Use multiprocessing over PCI using Radstone's PPZero technology

In this way, the PPC4B can maintain concurrent bus operation, allows applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

To connect the PPC4B to P0-based carrier cards such as the P0CC1, a series of P0 add-on backplanes are available. These are PCBs for attaching to a system backplane that has J0 connectors fitted. The following variants are available:

Variant	PCI Backplane Slots	Master Slots	P0CC1 Slots
P0BP1-502	2	1	1
P0BP1-503	3	1	2
P0BP1-504	4	1	3
P0BP1-505	5	1	4

The P0BP1 backplane must be soldered onto the J0 system backplane, and can be used with either “type A” or “type B” J0 connectors. These backplanes are intended to have a host SBC with PMCPCI card plugged into the master slot, which is the left-most slot of the P0 PCI backplane. For further information about P0 backplanes, please contact Radstone directly or talk to your nearest Sales Office.

The following table shows the number of PCI slots available with and without the PCI expansion:

PCI Expansion	PMC Slots Available	VME Slots
Absent	2	1
Present	1 + 2n	1 + n

Where n is the number of P0 carrier cards fitted, up to a maximum of 4.

PMC Sites

The PPC4B has two sets of connectors ([J11, J12, J13 and J14] and [J21, J22, J23 and J24]) that allow standard PMCs to be connected to the PCI bus. The PMC I/O connector J14 is connected to P0 to allow backplane I/O on all styles. The PMC I/O connector J24 is a build option and, if fitted, is connected to P2 to allow backplane I/O on all styles.

The PCI bus that connects to the PMC sites can run at 66 MHz and 64-bits wide or 33 MHz and 32-bits wide, depending on the PMCs fitted. Running at 64-bit/66 MHz gives a maximum burst transfer data rate of 528 Mbytes/second, compared with 132 Mbytes/second for 32-bit/33 MHz. However, both PMCs must be 66 MHz capable for 66 MHz operation; if one of the PMCs is only 33 MHz capable, operation is downgraded to 33 MHz for *both* PMC sites. This PCI bus can have 5V or 3.3V signalling, user-selectable via link E801.

Front panel I/O is fully supported on levels 1 to 3 and, with reduced functionality, on levels 4 and 5 product. While a level 4 or 5 card can only accept conduction-cooled PMCs, levels 1, 2 and 3 boards can accept either air-cooled or conduction-cooled PMCs, as long as adequate cooling is provided. Air-cooled PMCs are defined in the IEEE 1386 Standard, and rugged conduction-cooled PMCs are defined in the Draft Standard for Conduction-cooled PMCs.

The range of PMCs available from Radstone at the time of writing are shown overleaf.

PMCs

A range of PMCs is available both from Radstone and third parties. PMCs available from Radstone, in various build standards including Radstone's state-of-the-art rugged conduction-cooled PMCs, include:

Name	Type	Build Levels	Description
PMCPCI	PCI expansion	1 to 5	Bridges PCI bus through P0 connector allowing PMC host to be connected to Radstone P0 PCI based products, e.g. P0CC1 carrier card, VANTEGRA SHARC DSP
PMC1553	MIL-STD-1553B interface	1 to 4	Front or rear I/O, single or dual channel, and RT-only or RT/BC/MT options
PMX1553	MIL-STD-1553B and serial interfaces	Level 4 preferred	Single MIL-STD-1553B channel and 4 channels of RS232/RS422 serial I/O
PMCEXT	Ethernet interface	1 and 2 only	100BaseTX Fast Ethernet interface
PMC-ATMF	ATM NIC interface	1 to 4	155 Mbps ATM adapter for OC-3 fiber networks
PMCF1	FLASH memory	1 to 5	High capacity FLASH. 32, 64, 96 or 128 Mbytes options
PMCF2	Compact FLASH	1 to 5	Solid state hard disk using 40 Mbyte Compact FLASH Card
PMCFA1	Fibre Channel interface	1 to 4	1 Gbit/second full duplex Fibre Channel single attach adapter
PMCGA1	Graphics	1 to 4	PCI graphics accelerator, composite video I/O
PMCGA2	Graphics	1 to 4	High performance PCI graphics accelerator, composite video I/O and digital video output
PMCHH1	DSP Gateway	1 to 5	High performance PCI/Link Port Bridge
PMC FA2	Fibre Channel interface	1 to 4	1 Gbit/second full duplex Fibre Channel dual attach adapter
PMC CAN	Vehicle comms interface	1 to 4	Dual CAN bus interfaces, MIC bus interface
PMX654	Asynchronous serial interface	1 to 4	4 RS232/422 serial ports, up to 1 Mbps
PMCPIO1	Parallel I/O	1 to 4	16 I/O channels, 16 output only
PMCQ1	Serial and MIL-STD-1553B interface	1 to 4	4 high-speed synch/asynch serial channels, single channel dual redundant MIL-STD-1553B interface
EPMCQ2	Serial and Ethernet interface	1 to 4	4 high-speed synch/asynch serial channels, single 10/100BaseT Ethernet

These products are supported by data sheets and manuals giving more information, and more details on the options. For more detail on any of these or forthcoming products, or for copies of the literature, please contact Radstone directly or your nearest Sales Office.

Note: Level 1 PMCs (both from Radstone and third parties) can be used on all air-cooled versions (Levels 1, 2 and 3) of the PPC4B, even if the PMC does not meet the extended temperature and environmental requirements of Levels 2 and 3. However, conduction-cooled variants of the PPC4B can only accept conduction-cooled PMCs.

VMEbus Interface

The Tundra Semiconductors CA91C142 Universe II PCI to VME bridge provides a full master/slave VMEbus interface. It includes the following features:

- Full slot 1 (system controller) functionality
- VME64 support
- Interrupt control (handler and generator)
- A DMA controller
- Interprocessor communications
- Support for block transfers between the VMEbus and local memory
- Software configurable VMEbus slave address decoding

Appendix A details the VMEbus compliance and basic VMEbus performance of the PPC4B.

The Universe II requests 4 Kbytes of PCI I/O space and 4 Kbytes of PCI memory space. You are advised to grant the memory space request, but not the I/O space request. This will avoid problems with legacy addressing.

Note: The Universe II does not self-address.

VMEbus Master Access

Four general-purpose, software-programmable PCI slave images are available for access to the VMEbus.

- All of these can be configured to access VMEbus A32, A24 or A16 address space
- An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address
- The start and end addresses of the A32, A24 and A16 PCI slave images may be set on any 64 Kbyte boundary in the approximately 1 Gbyte of PCI bus memory or I/O space addressable by the processor that is not allocated to other PCI attached devices
- One image may be set on 4 Kbyte boundaries to accommodate access to A16 space

One further, special purpose, PCI slave image allows mapping of A16 and A24 space.

- This slave image uses a 64 Mbyte window, aligned to any 64 Mbyte address in PCI memory space
- The window is divided into four 16 Mbyte quadrants
- The top 64 Kbytes of each quadrant maps to A16 space, while the rest of each quadrant maps to A24 space
- The Address Modifiers generated are software configurable for each quadrant

VMEbus master cycles may be coupled or write posted.

- Coupled cycles are retried on the PCI bus until the Universe II has ownership of the VMEbus and are not terminated on the PCI bus until all data has been transferred over the VMEbus
- Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred

VMEbus Slave Access

Four general-purpose, software-programmable VMEbus slave images are available.

- All of these may be defined in VMEbus A32, A24 or A16 space
- An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address
- The start and end addresses of the A32, A24 and A16 images may be set on any 64 Kbyte boundary

One further, special purpose, VMEbus slave image, the Register Access Slave Image, allows a VMEbus master to access the Universe's control and status registers.

VMEbus slave accesses to the PPC4B may be coupled, write posted or pre-fetched block read.

- Coupled slave transfers can only proceed once the slave posted write FIFO is empty
- Slave posted write cycles are queued in a FIFO until the PCI bus is available for the data to be transferred

Indivisible Cycles on VME

The Universe II may be programmed to generate RMW cycles on the VMEbus. Data from the read portion is compared with a 32-bit compare value, qualified with a 32-bit mask. If the comparison is true, then those bits enabled by the mask are swapped with a 32-bit swap field.

Alternatively, the Universe chip's VMEbus ownership bit may be set to cause it to acquire and hold ownership of the VMEbus. This method can be used in combination with VMEbus LOCK cycles to guarantee exclusive access to a VMEbus resource.

The Universe also supports VMEbus lock commands using ADOH cycles.

Slave RMW cycles on the VMEbus are handled by programming the Universe II to transform all incoming non-block read cycles into locked PCI cycles. However, the PowerSpan, which provides the PCI to memory interface, does not support incoming PCI lock cycles.

VMEbus Arbitration and Slot 1 Functions

The Universe II can be programmed to request the VME bus on any of the four bus request levels BR0 to BR3 in either fair or demand modes, and to release the bus in either ROR or RWD modes. The Universe II ignores any assertion of BCLR~ during its bus ownership.

When acting as System Controller, the Universe II provides the following VME bus arbitration functions:

- Fixed priority (PRI) arbitration with BCLR~ generation in priority mode
- Single level (SGL) arbitration
- Round robin (RR) arbitration
- Arbitration time-out (disabled, 16, 256μs)

Along with the following other miscellaneous functions:

- System Clock (SYSCLK) driver
- Interrupt Acknowledge (IACK) daisy chain driver
- Bus time-out (disabled, 16, 32, 64, 128, 256, 512, 1024μs)

VMEbus Master Block Transfers

The Universe's DMA controller may be used to transfer data between the PCI bus and the VMEbus using D32 or D64 transfers. DMA operations on the two buses are decoupled through a bi-directional FIFO. The DMA controller can:

- Transfer multiple blocks of data using entries in a linked-list
- Pack and unpack data to support differing data widths on the PCI bus and the VMEbus
- Generate an interrupt on completion or on encountering an error condition

VMEbus Slave Block Transfers

The VMEbus slave interface can respond to D32:BLT and D64:MBLT. For VMEbus slave block transfers, the Universe chip may be programmed to pre-fetch read data, which is queued in a FIFO.

Mailboxes

The Universe II contains four 32-bit mailboxes that can generate interrupts on the PCI bus or on the VMEbus when written to. Each mailbox has separate status, enable and interrupt mapping bits.

VMEbus Location Monitor

The Universe II contains a VMEbus location monitor that provides a VME interrupt broadcast mechanism. A user-specified address is programmed into the location monitor, which can then generate one of four PCI interrupts.

Semaphore Register

The Universe II provides a 32-bit register containing four semaphores, one in each byte.

- Each of the four semaphores is a 7-bit data field plus a 1-bit lock field
- Ownership of the semaphore is obtained by writing a unique value to the 7-bit field while setting the lock bit
- The write is only accepted if the lock bit is not already set
- Ownership can be confirmed by reading back the value in the 7-bit field after the write, and comparing it with the unique value written

The semaphores can be used to guarantee exclusivity of access to a resource shared between:

- Multiple processes
- Processes and bus masters (PCI or VME)
- Bus masters (PCI or VME)

VMEbus Interrupts

If programmed to do so, the Universe II responds to a VMEbus interrupt with a VMEbus interrupt acknowledge cycle. The Universe II captures the status/ID and then raises an interrupt on the PCI bus. No further VMEbus interrupts are handled on that level until the processor reads the status/ID and re-arms the interrupt handler.

The Universe II can be programmed to generate any level of VMEbus interrupt. It can raise an interrupt on the PCI bus when the VMEbus interrupt has been acknowledged.

Seven software interrupts in the Universe II allow an interrupt to be generated on any of the seven VMEbus IRQs.

VME Bus Errors

Assertion of VMEbus BERR~ during a coupled VMEbus master cycle causes a target-abort (bus error) on the PCI bus. A PCI target-abort during a coupled VMEbus slave cycle causes BERR~ on the VMEbus. See the Machine Check Exception section for further details of target abort.

A bus error during posted write transfers raises an interrupt (if enabled) to the processor. Several options are available, including stopping the operation and purging the offending transaction.

A bus error during a DMA operation raises an interrupt and stops the DMA operation on the bus where the error was detected.

VMEbus Retries

The Universe chip, as a PCI target, retries the PCI master under the following conditions:

- The PCI initiator requests a coupled cycle to the VMEbus whilst the Universe is not VMEbus master
- The PCI initiator requests a coupled cycle to the VMEbus whilst the posted write FIFO still contains data
- The PCI initiator requests a posted write cycle when the posted write FIFO can accept no more entries

The PPC4B does not support the VMEbus RETRY~ signal.

VMEbus Reset Options

Several Universe II operating features are set at power-up or reset by surface mount jumpers. See the VMEbus Interface Configuration section in Chapter 4 for the default options.

Ethernet Controller

The Digital 21143 Ethernet controller supports IEEE 802.3 and ANSI 8802-3 Ethernet standards. It incorporates:

- A direct PCI bus interface
- Independent receive and transmit DMA controllers
- Large independent FIFOs for receiving and transmitting

The DMA controllers access initialisation data, control descriptor rings and handle data transfers between SDRAM and on-chip memory with the Ethernet Controller arbitrating between DMA channels to minimise underflow or overflow.

Automatic packet deletion on receive (runt packets or after a collision) and packet re-transmission after a collision on transmission are supported. This minimises bus traffic by removing unnecessary accesses to shared memory. The network address (Ethernet number) is factory configured and held in a serial EEPROM.

Connection to the Ethernet controller is via the P2 connector (see Chapter 6). Three associated status LEDs (DS216 to DS218) are mounted on the back of the board near the Ethernet Controller chip (see the LEDs section). The default functions of these LEDs are receive status, link status and transmit status respectively. This may be overridden by the software.

The Ethernet controller requires 32 bytes of PCI I/O space. It cannot be accessed in PCI memory space.

As a build option, instead of 10Base5, the Ethernet port can be configured as a 10/100BaseT interface, provided by a National Semiconductor DP83843 MII PHY device. Chapter 6 gives the pinout.

The MII PHY device connects to five additional status LEDs (see the LEDs section for locations):

- **Collision LED (DS210)**. This indicates the presence of collision activity for 10 Mbytes/sec and 100 Mbytes/sec Half Duplex operation. This LED has no meaning for 10 Mbytes/sec or 100 Mbytes/sec full-duplex operation and remains deasserted. During 10 Mbytes/sec half-duplex mode, the LED drive pin is asserted after data transmission due to the heartbeat function
- **Transmit LED (DS211)**. This indicates the presence of transmit activity for 10 Mbytes/sec and 100 Mbytes/sec operation
- **Receive LED (DS212)**. This indicates the presence of any receive activity for 10 Mbytes/sec and 100 Mbytes/sec operation
- **Link LED (DS213)**. This indicates good link status for 10 Mbytes/sec and 100 Mbytes/sec operation
- **Full Duplex LED (DS214)**. This indicates Full Duplex mode status for 10 Mbytes/sec or 100 Mbytes/sec operation. The LED pin can be configured to indicate Polarity status for 10 Mbytes/sec operation

The MII PHY address is fixed at address 0x01 on the MII interface.

SCSI Scripts Processor

The NCR53C860 SIOP executes commands, in the form of SCSI scripts. It has a PCI interface and DMA controller, which are used to access the scripts and data held in system memory. The SIOP can transfer data at 7 Mbytes/second asynchronously and 20 Mbytes/second synchronously. Connection to the SCSI bus is made through the P2 connector. The pinout is given in Chapter 6.

The PPC4B has an on-board active SCSI terminator, which may be enabled or disabled with a jumper (see the E11 description in Chapter 4). The SCSI specification allows a maximum cable stub length of 10 cm. If the SCSI bus connections are taken directly from the backplane J2 connector, then the PPC4B may be located anywhere on the SCSI bus and the terminator should only be enabled if the PPC4B is at the end of the SCSI bus. Otherwise, the PPC4B must be at the end of the SCSI bus and the terminator must be enabled.

A software programmable SCSI Activity LED (DS208) is mounted on the back of the board. See the LEDs section and the SCSI Activity LED Register description for more details.

ISA Bus

To take full advantage of low-cost, industry standard components, general purpose I/O and auxiliary functions are implemented through an ISA bus interface. Facilities provided include:

- Parallel/printer port
- Two PC-compatible serial interfaces (COM1 and COM2)
- Floppy disk controller
- Real Time Clock
- Keyboard/mouse interface
- Non-volatile memory
- Two high speed RS232 or RS422 serial ports (COM3 and COM4)

ISA Bridge

A Winbond 83C553F provides the bridge between the PCI bus and the ISAbus for connection of native I/O devices. This device also provides the following functions:

Function	Equivalent to Function of
7 channel DMA between ISAbus and PCI bus	Two 83C37s
Timer block	One 82C54
Interrupt controller	Two 8259s
PCI bus arbiter	-

The ISA bridge positively decodes some I/O cycles on the PCI bus for internal resources. It subtractively decodes and claims all PCI memory and I/O cycles not claimed by other PCI targets, and forwards them to the ISAbus.

Apart from the ISA bridge, there are no other ISAbus masters in the PPC4B architecture.

The ISAbus may be reset under software control via the ISA Clock Divider register in the ISA bridge.

ISA Bus Peripheral Components

Ultra I/O

The SMC 37C935 Ultra I/O, connected to the ISAbus, contains a Floppy Disk Controller, Real-Time Clock, two serial ports, a parallel port and a keyboard/mouse controller. The IDE interface is not used on the PPC4B.

Floppy Disk Controller

Connection to the FDC is through an on-board header, P9. The pinout is given in Chapter 6. The FDC is software compatible with the DP8473, 765A and NS82077.

Real Time Clock

The clock/calendar provides the following information:

- Seconds
- Minutes
- Hours
- Days
- Months
- Years

Note: The power supply to the RTC on the PPC4B is fed from the +5VSTDBY pin. VMEbus compliance requires this voltage to be 5V ± 5%. There is no provision for 3V standby.

Serial I/O

The Ultra I/O provides two serial channels (COM1 and COM2) containing FIFOs, software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 115.2 kbaud, including the MIDI data rate. The Ultra I/O is clocked from a 14.31818 MHz source.

Connection to the serial ports is primarily through the P2 connector, although restricted access may be obtained through P7. Pinouts are given in Chapter 6.

Parallel I/O

The parallel port includes extended capabilities conforming to IEEE P1284. Connection to the parallel port is through the P2 connector. The pinout is given in Chapter 6.

Keyboard and Mouse Controller

A PS/2 compatible Keyboard and Mouse interface with Phoenix BIOS is integrated into the Ultra I/O. Connections to the mouse and keyboard are through the P2 connector. See Chapter 6 for the pinout.

ESCC

An 85230 ESCC provides two additional serial channels, COM3 and COM4. The 85230, which is software compatible with the AMD 8530, provides

- Synchronous or asynchronous operation
- Two baud rate generators covering a range of baud rates up to 230.4 kbaud for asynchronous operation and 3.6864 Mbaud for synchronous operation
- Two DPLLs to extract a clock from a serial data stream in typical low pin-count RS485 interfaces
- Receive and transmit FIFOs
- Four DMA channels to allow simultaneous reception and transmission on both interfaces
- Several facilities to enhance operation of frame based protocols such as HDLC, X-25 etc.

COM3 and COM4 can be configured by build options to be either RS232 or RS422/RS485.

- The RS232 option only provides a limited signal set [TXD, RXD, RTS, CTS, DCD, DTR and DSR]. As there are no clocking options, synchronous operation is not possible
- The RS422/485 option provides a RS530 compatible signal set with full clocking options, and is designed for synchronous operation. The signal set is [TXD, RXD, RTS, CTS, DCD, DTR, DSR, ST, RT and TT] or, in RS530 terminology, [BA, BB, CA, CB, CF, CD, CC, DB, DD and DA] respectively

Connection to COM3 and COM4 is via the P2 connector. See Chapter 6 for the pinout.

The ESCC transmission speeds depend on the clock (PCLK) fed in. The ESCC has a 14.7456 MHz oscillator feeding PCLK, so all the ESCC frequencies are based on 14.7456 MHz.

- When using an external clock source, the ESCC can transfer at a rate of ¼ PCLK, giving a maximum rate of 3.6864 Mbits/second
- When using clock extraction, the ESCC can extract at up to 1/8 PCLK, giving a maximum rate of 1.8432 Mbits/second
- When using NRZI, the ESCC can extract at up to 1/16 PCLK, giving a maximum rate of 0.9216 Mbits/second

Looking at the asynchronous operation, the baud rate is defined by:

$$\text{Baud Rate} = \frac{\text{Clock Frequency}}{2 \times (\text{Clock Mode}) \times (\text{Time Constant} + 2)}$$

where: Clock Frequency is in Hz,
Clock Mode is 16, 32 or 64
Time Constant is the value programmed into the ESCC's 16-bit register

This gives the maximum asynchronous baud rate of:

$$\text{Baud Rate} = \frac{14.7456 \times 10^6}{2 \times (16) \times (0 + 2)}$$

Baud Rate = 230400 bps

NOVRAM

A Simtek 11C88 provides 32 Kbytes of NOVRAM. This part provides read/write RAM shadowed by EEPROM with a capacity for 10,000 write cycles. The RAM is loaded from the EEPROM automatically at power up or under software control. The ISA bus master can also write to it as normal RAM. The RAM is stored to EEPROM under software control.

EEPROM

The PPC4B has 512 Kbytes of EEPROM fitted as standard, for convenient non-volatile data storage. The memory is provided by four Atmel AT28C010 128Kx8 bit EEPROMs and, as such, may be write-protected by use of the Atmel Software Protection Algorithm (see the Atmel datasheet for more information).

The EEPROM has the capacity for 10,000 write cycles, and may be chip-erased under software control (see the Atmel datasheet for more information).

Note: Integrity of EEPROM data cannot be guaranteed if a hard reset occurs during an EEPROM write cycle.

CIO

The 85C36 CIO provides three independent 16-bit counter/timers that each have a resolution of 333 ns. Two of the counter/timers may be linked to form a 32-bit counter/timer.

The functions of the I/O port bits are described in the Control and Status Registers section.

JTAG

There are three connectors on the PPC4B that carry JTAG-type signals: P6, P7 and the optional P0 (see Chapter 6 for more details on these connectors).

P7 JTAG

This is solely for the purpose of programming the MACH device, which contains various functions including the main PPC4B ISAbus registers. This device is programmed via JTAG, but does not have the necessary test cells within the device to make it a true JTAG test device.

P0 JTAG

The JTAG signals from P0 connect directly into the "MAIN" JTAG signals on P6. They have the following terminations:

TCK	⇒	+5V via a 4.7 kΩ pull-up resistor
TMS	⇒	+5V via a 6.8 kΩ pull-up resistor
TDI	⇒	+5V via a 6.8 kΩ pull-up resistor
TRST~	⇒	+5V via a 4.7 kΩ pull-up resistor

The PPC4B does not provide any buffering on the JTAG signals.

For P0 JTAG operation, P6 pin 38 (SEPARATE_CHAINS~) must **not** be connected to GND. This signal controls the splitting of the JTAG chains onto the P6 connector. The split takes place if P6 pin 38 is connected to GND, and is intended for use with an emulator connection where the emulator requires connection to the JTAG of the processor only.

P6 JTAG

P6 forms the main JTAG connection point and is composed of three separate JTAG chains:

1. JTAG chain “CPU” goes to the processor.
2. JTAG chain “107” goes to the MPC107, the L2 cache (if JTAGable) and the PowerSpan.
3. JTAG chain “MAIN” goes to two QS3J245 elements, the Ethernet, the Universe, PMC site 1 and PMC site 2.

Pin	Signal	Pin	Signal
1	-	2	TDI_MAIN
3	TCK	4	TRST~
5	TMS_CPU	6	TMS_107
7	TMS_MAIN	8	TDI_CPU
9	TDO_CPU	10	TDI_107
11	TDO_107	12	-
13	TDO_MAIN	14	-
33	-	34	TRST_CPU~
35	-	36	-
37	-	38	NAND_ON~
39	SEPARATE_CHAINS~	40	-

Notes:

1. Signals not involved with the JTAG operation have been removed from this table for clarity.
2. All the JTAG chains share a common TCK and TRST~ on pins 3 and 4 respectively.
3. By default, all the JTAG chains are connected together. The signal “SEPARATE_CHAINS~” may be used to separate them to allow, for instance, emulator access to the CPU chain.

JTAG Clock Frequencies

Different parts in the JTAG chain may have different maximum TCK frequencies. The main chain on the PPC4B has the following clock limitations:

21143	⇒ 10 MHz
Universe II	⇒ 20 MHz
QS3J254	⇒ 25 MHz
MPC107	⇒ 25 MHz
PowerPC 750/7400	⇒ 33 MHz
PowerSpan	⇒ TBA MHz

The JTAG clock should not exceed the maximum clock frequency of the slowest element in the JTAG chain. Using the data from the above components, the chain clock frequency should not exceed 10 MHz.

JTAG and PMC

The "MAIN" JTAG chain from P6 visits the PMC sites. These individually auto-bypass if a PMC is not fitted at the site. To achieve this, the PPC4B has BUSMODE2 to BUSMODE4 wired to 1, 0, 0 respectively. This effectively interrogates the PMC site as to whether it has a PCI compliant card fitted. The response from the PMC is returned on BUSMODE1. If the answer is yes (BUSMODE1 = 0), then the PMC site is included in the JTAG chain. If there is no PMC fitted, then a pull-up resistor on the PPC4B forces BUSMODE1 to 1 and the JTAG is bypassed.

Notes:

1. The PCI specification (section 2.2.10 on the optional JTAG pins) requires that if a PMC cannot/will not support JTAG, then it must have TDI connected to TDO. This means that the "MAIN" JTAG chain is complete even if there are PMC cards fitted that do not support JTAG.
2. The PMC sites cannot *source* the JTAG, as they are expected to receive the JTAG signals, being part of a chain.

Read-only Registers

The read-only registers of the PPC4B are **not** readable via the JTAG chain. This is due to the following reasons:

1. One of the read-only registers is a status register within the Winbond ISA bridge device (port 0x040A). This device is a non-JTAG part.
2. Similarly, the ID Link register is a read-only register that comes from the Ultra I/O device. This is also a non-JTAG part.
3. Most of the rest of the read-only registers are contained in the MACH device. This is not a JTAG device (although it potentially looks like it could be) and so is also not included in the JTAG chain.

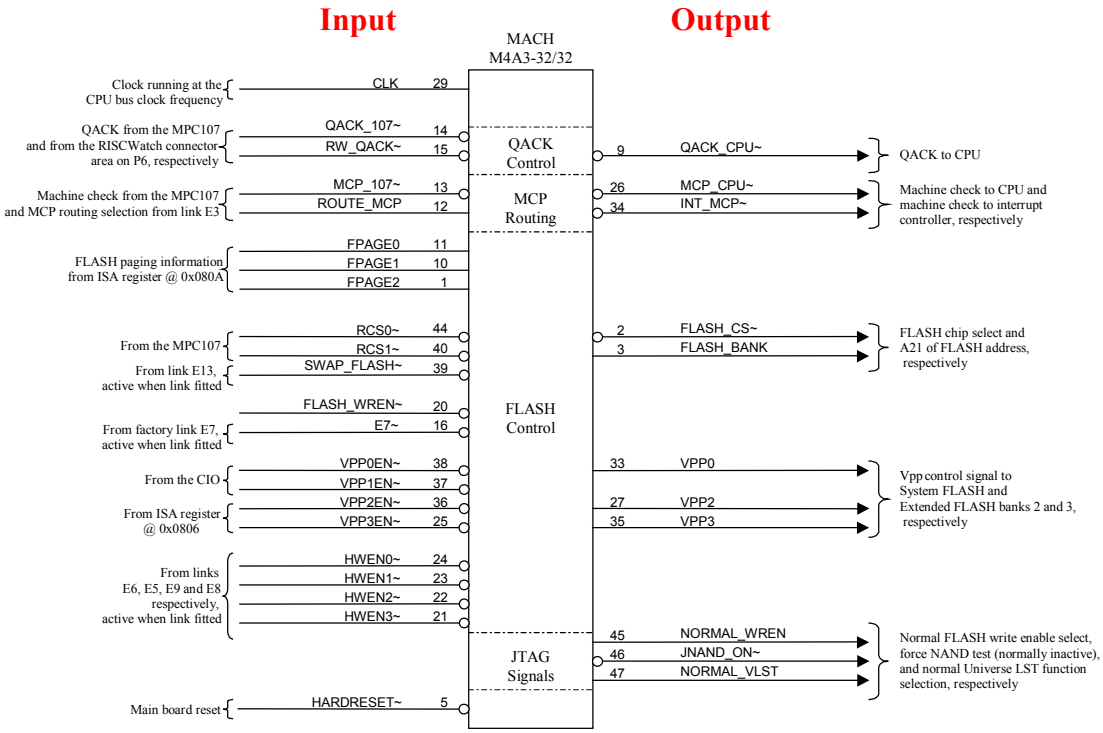
The final read-only register, the Vector register, is in the MPC107 which is in the "107" JTAG chain.

All of these registers are write protected from all users, including Radstone (although it could be argued that reprogramming the MACH device does, in fact, program some of the read-only registers).

JTAG Testing and JTAG FLASH Reprogramming

The NAND_ON~ signal is used to place the ISAbridge and SCSI controllers into test mode, which forces them off the PCIbus. If these two devices were not removed from the PCIbus, they might try and intercept any PCI signals that the JTAG generates and act on them. With both the ISAbridge and SCSI controllers in test mode, the PCIbus is now free to be exercised. The NAND_ON~ signal appears on P6 pin 38 and is, by default, inactive.

At the start of the "MAIN" JTAG chain (also the start of the P0 JTAG chain), there is a Lattice MACH M4A3-32/32 part. This is a functional element of the PPC4B that can be JTAG tested. Below is a diagram showing the connections to this MACH part:



When JTAG testing the board, take care not to drive the inputs to the device from this device, as this may lead to two devices driving the same lines.

The functionality of the relevant signals is described below.

JNAND_ON~ is an alternative NAND_ON~ signal to that on P6 pin 38. It is normally inactive.

FLASH_WREN~ is a wire-OR of P0 pin A2, P2 pin Z1 and a 4.7 kΩ pull-up resistor. When this is low (either P0 pin A2 or P2 pin Z1 is connected to GND), the FLASH chip enabling circuit allows writes, providing all the other conditions are correct.

VppEN0~ is an output from the CIO that requests the switching on of Vpp to FLASH page 0.

VppEN1~ is an output from the CIO that requests the switching on of Vpp to FLASH pages 1 to 3.

HWEN0~ is connected to +5V via a 4.7 kΩ pull-up resistor. This signal may be connected to GND by fitting link E6. This link, when fitted, indicates that the FLASH chip enabling circuit can allow writes to FLASH page 0, providing all the other conditions are correct.

HWEN1~ is connected to +5V via a 4.7 kΩ pull-up resistor. This signal may be connected to GND by fitting link E5. This link, when fitted, indicates that the FLASH chip enabling circuit can allow writes to FLASH pages 1 to 3, providing all the other conditions are correct.

Normal_WREN is always active; there is no external control of this signal. Normal_WREN indicates that the normal MPC107 write pulse is connected via a buffer to the FLASH device write lines.

VppEN2~ is an output from the ISA registers that requests the switching on of Vpp to FLASH bank 2.

VppEN3~ is an output from the ISA registers that requests the switching on of Vpp to FLASH bank 3.

HWEN2~ is connected to +5V via a 4.7 kΩ pull-up resistor. This signal may be connected to GND by fitting link E9. This link, when fitted, indicates that the FLASH chip enabling circuit can allow writes to FLASH bank 2, providing all the other conditions are correct.

HWEN3~ is connected to +5V via a 4.7 kΩ pull-up resistor. This signal may be connected to GND by fitting link E8. This link, when fitted, indicates that the FLASH chip enabling circuit can allow writes to FLASH bank 3, providing all the other conditions are correct.

In normal operation, the factory link (E7) is not fitted and so the FLASH Vpp generation circuit is in control of the Vpp lines to the FLASH devices. The logic is as follows:

- If FLASH_WREN~ is not connected to GND, then there will be ***no*** Vpp generation
- If FLASH_WREN~ is connected to GND, then VppEN0~ to VppEN3~ may request the generation of Vpp for their respective FLASH pages/banks. The requests are successful provided the respective HWENx~ is active (connected to GND via their links). If HWENx~ is not active, then the request for that page/bank does not generate Vpp and so programming can not take place
- If the factory link, E7, is fitted, then the state of FLASH_WREN~ and VppENx~ is ignored and the request to turn on Vpp is permanently active. Vpp is generated for a FLASH page/bank provided the respective HWENx~ is active (connected to GND via their links). If HWENx~ is not active then the request for that page/bank does not generate Vpp and so programming can not take place

In JTAG mode, the Normal_WREN signal can now be controlled by JTAG, and this signal controls the routing of the real FLASH write pulses. When Normal_WREN is high, the MPC107 write enable is connected to the FLASH write enables. When Normal_WREN is low, the redundant FLASH_WREN~ is connected to the FLASH write enables. This means that under JTAG conditions, the user can either JTAG the board in a way that uses the MPC107 write pulse to control the FLASH, or the user can pass in FLASH write enable directly from either the P0 or P2 connectors on the FLASH_WREN~ line.

LEDs

There are 21 LEDs on the PPC4B: three on the front of the PCB and 18 surface mounted on the back. On all product levels, the three LEDs on the front of the PCB are visible through the front panel. The LEDs on the back of the PCB are likely only to be visible in the inter-board separation gap.

On the front panel DS1 is red, DS2 is yellow and DS3 is green (Figure 7-1 shows their locations). These LEDs are software programmable and are controlled by Port C of the CIO (see the CIO Port C Data Register description for more details).

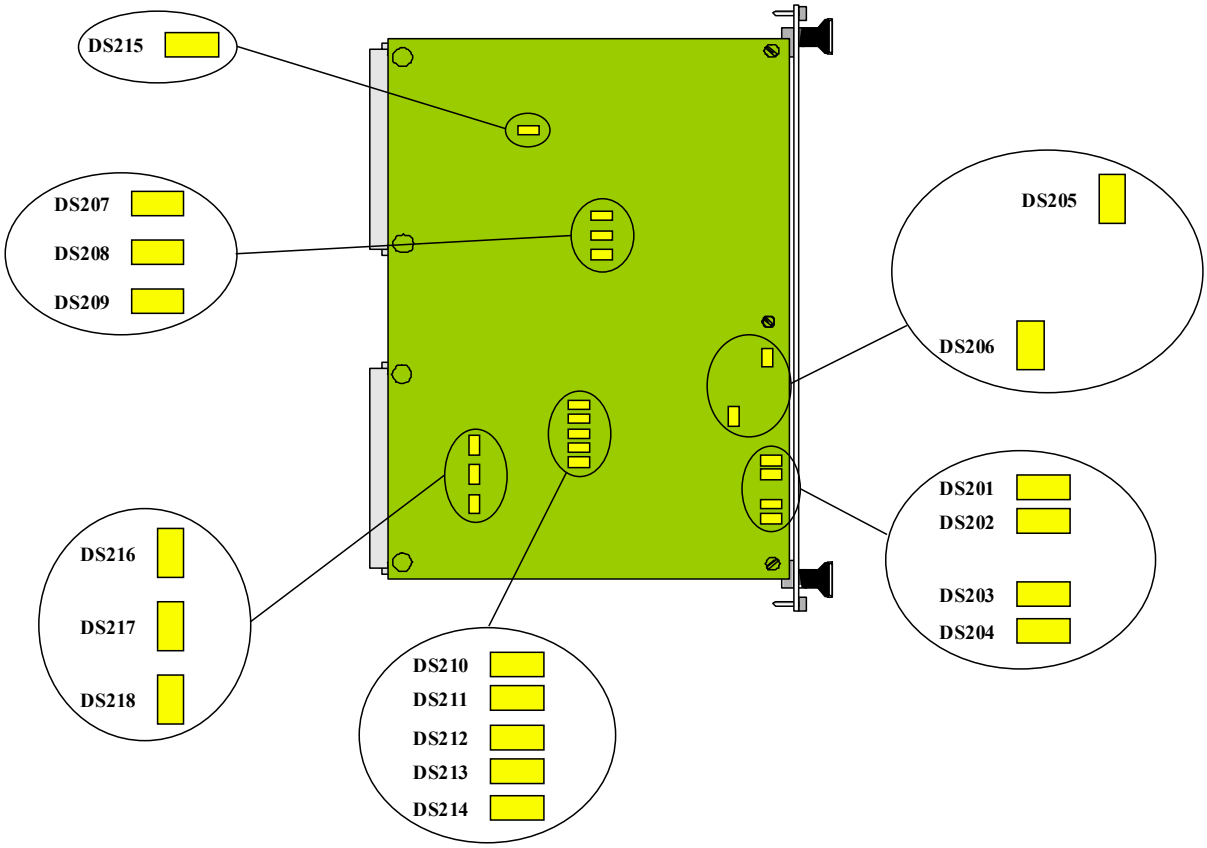
On the back of the PCB (see overleaf for a location diagram):

- DS201, DS202 and DS203 mirror DS1, DS2 and DS3 respectively
- DS204 is also software programmable and controlled by Port C of the CIO (see the CIO Port C Data Register description for more details). It is yellow
- DS205 is connected to the TRIG_OUT~ signal of the MPC107
- DS206 indicates whether the processor is in checkstop
- DS207 is controlled by register 0x086C on the ISA bus. This LED is reserved
- DS208 indicates SCSI activity (see the SCSI Activity LED Register, port 0x0808, for more details)
- DS209 on indicates that the hardware is configured for non-ECC operation. DS209 off indicates that ECC Mode Memory Timings are in use. See the Motherboard Type Register description for more details
- DS210 indicates the presence of collision activity for 10 Mbytes/sec and 100 Mbytes/sec Half Duplex Ethernet operation. This LED has no meaning for 10 Mbytes/sec or 100 Mbytes/sec full-duplex operation and remains deasserted. During 10 Mbytes/sec half-duplex mode, the LED drive pin is asserted after data transmission due to the heartbeat function
- DS211 indicates the presence of transmit activity for 10 Mbytes/sec and 100 Mbytes/sec Ethernet operation
- DS212 indicates the presence of any receive activity for 10 Mbytes/sec and 100 Mbytes/sec Ethernet operation
- DS213 indicates good link status for 10 Mbytes/sec and 100 Mbytes/sec Ethernet operation
- DS214 indicates Full Duplex mode status for 10 Mbytes/sec or 100 Mbytes/sec Ethernet operation. The LED pin can be configured to indicate Polarity status for 10 Mbytes/sec Ethernet operation
- DS215 indicates that addresses in the range 0x80000000 to 0xFEC00000 go to the PowerSpan and not the MPC107. The control for this functionality comes from register 0x086C on the ISA bus
- DS216 indicates the presence of any receive activity for 10Base5 Ethernet operation
- DS217 indicates good link status for 10Base5 Ethernet operation
- DS218 indicates the presence of transmit activity for 10Base5 Ethernet operation

DS210 to DS214 are only applicable if the PPC4B is configured for 10/100BaseT Ethernet operation. DS216 to DS218 are only applicable if the PPC4B is configured for 10Base5 Ethernet operation. The two sets of LEDs are mutually exclusive.

The default functions of LEDs DS216 to DS218 are given above, but these may be software-overridden.

Figure 5-4. LED Locations



Watchdog Timer

The PPC4B contains a Maxim 706 microprocessor supervisory circuit with a watchdog timer. This timer, once enabled, must be re-triggered every 1.6 seconds or a hard reset results. The CIO Port A Data Register (Port 0x862) contains the trigger bit.

Control and Status Registers

The control and status registers shown in Table 5-1 exist on the PPC4B for controlling or reading the status of the hardware.

In the table:

- The addresses are as seen by the processor
- R/W = Read/Write
  RO = Read Only
  WO = Write Only
- The registers in italics are described in detail in the pages following the table
- The others are registers in the ISA Bridge or other major devices, which are described in the detail in the appropriate device data sheet (which will also give the appropriate 'Type' column entry)

In the register descriptions, the bit significance is shown in big-endian mode (i.e. from the PowerPC 750/7400 programmer's viewpoint).

Table 5-1. Control and Status Registers

ISA I/O Port (Hex)	Contiguous I/O Mode Address	Description	Type
0000 to 000F	FE00 0000 to 000F	ISA Bridge DMA 1 Control	
0020 and 0021	FE00 0020 and 0021	ISA Bridge Interrupt 1 Control	
0040 to 0043	FE00 0040 to 0043	ISA Bridge Counter Control	
0060	FE00 0060	Keyboard	
0061	FE00 0061	ISA Bridge NMI Status and Ctrl	
0064	FE00 0064	Keyboard	
0071 and 0072	FE00 0071 and 0072	RTC	R/W
0078 to 007B	FE00 0078 to 007B	ISA Bridge BIOS Timer	
0080 to 0090	FE00 0080 to 0090	ISA Bridge DMA Pages	
0092	***FE00 0092***	***Port 92***	***R/W***
00A0 and 00A1	FE00 00A0 and 00A1	ISA Bridge Interrupt 2 Control	
00C0 to 00DE	FE00 00C0 to 00DE	ISA Bridge DMA 2 Control	
03F0 to 03F7	FE00 03F0 to 03F7	Ultra-I/O	
040A	FE00 040A	ISA Bridge DMA Scatter/Gather	RO
040B	FE00 040B	DMA 1 Extended Mode	WO
0410 to 043F	FE00 0410 to 043F	ISA Bridge DMA Scatter/Gather	
0481 to 048B	FE00 0481 to 048B	ISA Bridge DMA High Pages	
04D0 and 04D1	FE00 04D0 and 04D1	ISA Bridge Edge/Level Control	
04D6	FE00 04D6	DMA 2 Extended Mode	WO

(continued overleaf)

ISA I/O Port (Hex)	Contiguous I/O Mode Address	Description	Type
0804	*FE00 0804*	*Memory Configuration*	*RO*
0806	*FE00 0806*	*Extended Memory*	*R/W*
0808	*FE00 0808*	*SCSI Activity LED*	*WO*
080A	*FE00 080A*	*FLASH Paging*	*R/W*
080C	***FE00 080C***	***Equipment Present 1***	***RO***
0810	FE00 0810	RTC RAM Protect 1	WO
0812	FE00 0812	RTC RAM Protect 2	WO
0818	***FE00 0818***	***Key Lock***	***RO***
0840	*FE00 0840*	*COM4 Command/Status*	*R/W*
0841	*FE00 0841*	*COM4 Data*	*R/W*
0842	*FE00 0842*	*COM3 Command/Status*	*R/W*
0843	*FE00 0843*	*COM3 Data*	*R/W*
0854	*FE00 0854*	*Board Revision*	*RO*
0856	*FE00 0856*	*Extended Board Revision*	*RO*
0858	*FE00 0858*	*Extended Board ID*	*RO*
0860	*FE00 0860*	*CIO Port C Data*	*R/W*
0861	*FE00 0861*	*CIO Port B Data*	*R/W*
0862	*FE00 0862*	*CIO Port A Data*	*R/W*
0863	*FE00 0863*	*CIO Control*	*R/W*
0864	*FE00 0864*	*ID Link*	*RO*
0866	*FE00 0866*	*Motherboard Type*	*RO*
0868	*FE00 0868*	*ISA DMA Routing*	*R/W*
086C	*FE00 086C*	*PCI Routing*	*R/W*
	FEC0 0000	MPC107 PCI CONFIG_ADDR	R/W
	FEE0 0000	MPC107 PCI CONFIG_DATA	R/W
	FEF0 0000	Vector	RO

Port 92 (Port 0x0092)

This register provides an alternate soft reset.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D6: Reserved

D7: Setting this bit causes a soft reset to occur. It must be cleared before another soft reset can be issued.

Memory Configuration Register (Port 0x0804)

This register provides information on the PPC4B's memory.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: Memory type
0 = EDO DRAM
1 = SDRAM

D1: Extended information
0 = None available
1 = Port 0x0806 valid

D2 to D4: Reserved.

D5: FLASH boot section configuration
0 = FLASH boot sections are addressed normally
1 = FLASH boot sections are swapped

D6 and D7: Always = 00_b showing 64 Mbytes of paged FLASH always fitted on-board.

Extended Memory Register (Port 0x0806)

This register provides information about the physical SDRAM device size. It also provides information and control for any extended FLASH banks fitted.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 and D1: Physical SDRAM device size.

Bank Size (Mbytes)	D0	D1	Device Size
64 each bank	0	0	2Mx4x8 (64 Mbit)
128 each bank	0	1	4Mx4x8 (128 Mbit)
256 each bank	1	0	8Mx4x8 (256 Mbit)
Reserved	1	1	Reserved

D2: Extended FLASH Bank 3 Vpp status:
0 = Off
1 = On

D3: Extended FLASH Bank 2 Vpp status:
0 = Off
1 = On

D4: Extended FLASH Bank 3 Vpp control:
0 = Turn Vpp off
1 = Turn Vpp on

D5: Extended FLASH Bank 2 Vpp control:
0 = Turn Vpp off
1 = Turn Vpp on

Note: Although you may request that Vpp be turned on, the hardware links on the board may prevent Vpp from being generated. To check whether Vpp is actually on, you can read the status from bits D2 and D3.

D6: Extended FLASH bank 3 present
0 = Not fitted
1 = Fitted

D7: Extended FLASH bank 2 present
0 = Not fitted
1 = Fitted

SCSI Activity LED Register (Port 0x0808)

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This register allows control of the SCSI Activity LED, DS208.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D6: Reserved.

D7: SCSI Activity LED
0 = LED off
1 = LED on

FLASH Paging Register (Port 0x080A)

This register provides FLASH paging control for the main 64 Mbytes of System FLASH. The register also provides NVRAM write enable control.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: NOVRAM/Paging update control. This bit is only used for write operations to this register; read returns a zero (0).

When D0 is written as a 1, the NOVRAM Write Control bit is updated without updating the FLASH paging information.

When D0 is written as a 0, the FLASH paging information is updated without the NOVRAM control being updated.

D1: NOVRAM write-enable control. This read/write bit controls whether writes to the NOVRAM are actual writes or generate address-only cycles, as follows:
0 = Normal write operation
1 = Write produces address-only cycles

The address-only capability should be used when generating software NOVRAM commit or restore sequences. These require precise sequences of reads, however the PowerSpan always generates 8-byte reads on the PCI bus, which would disrupt the read sequence and so prevent the commit or restore from completing successfully. Obviously, if read sequences cannot be used, then writes must be used instead. By setting D1 to 1, writes to the NOVRAM are converted into address-only cycles. As the PowerSpan can carry out single-byte writes, this allows single byte address-only cycles to take place to the NOVRAM, which correctly responds to these cycles to allow the required commit or restore operation to take place. After carrying out the required software commit or restore cycle, return this bit to zero to allow normal write cycles to the NOVRAM to occur.

D2 to D4: Reserved. No function on write, read as zeros.

D5 to D7: System FLASH page. These three read/write bits provide the FLASH paging control. The FLASH page is selected directly by the binary value of these bits.

In a system that has 64 Mbytes of paged FLASH, D5 has no effect, otherwise it forms the MSB of the required FLASH page number, with D7 as the LSB.

Note: After updating this register, the user must ensure that the address range 0xFF000000 to 0xFFFFFFFF is purged from any instruction or data cache.

Equipment Present Register 1 (Port 0x080C)

This register provides information on hardware options and the state of the SCSI Terminator power fuse.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: Hardware ID0 (see the Motherboard Type Register for details)

D1: SCSI_FUSE_GOOD
0 = SCSI fuse bad
1 = SCSI fuse good

Note: This is a re-settable fuse that re-engages when the overcurrent condition is removed.

D2: PRSNT1_2~
0 = Slot 2 PMC present
1 = Slot 2 empty

D3: PRSNT1_1~
0 = Slot 1 PMC present
1 = Slot 1 empty

D4: Reserved

D5 and D6: L2 cache size

Size (Mbytes)	D5	D6
1	0	0
2	0	1
Reserved	1	0
Reserved	1	1

D7: L2_PRES~
0 = L2 cache present (D5 and D6 indicate cache size)
1 = L2 cache not present (D5 and D6 have no meaning)

Keylock Register (Port 0x0818)

This register provides information on the state of the keylock signal. See the Keylock section for more details.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D6: Reserved

D7: Keylock
0 = Keylock signal low
1 = Keylock signal high

COM4 Command/Status Register (Port 0x840)

A read of this register accesses the COM4 Status register (RR0), and a write accesses the COM4 Command register (WR0). On reset, the Status register is set to $x1xxx100_b$ and the Command register is set to 0x00.

The Command register (WR0) provides indirect access to all registers in the ESCC by a pointer-plus-value mechanism. To use this, first write the address of the register to access into the Control register, then carry out a second (read or write) access to the addressed register. This second access also clears the address bits, restoring default access to WR0/RR0. If you ever lose track of where you are in this sequence, you can safely read the Command Register, which clears the address bits without any unwanted side effects.

For a full description of the ESCC registers and how to program them, see the ESCC User's Manual from Zilog.

Note: There is only one set of address bits, which are shared between COM3 and COM4.

Command Register (WR0)

MSB LSB

D0	D1	D2	D3	D4	D5	D6	D7

D0 and D1: 00 = Null code
01 = Reset Rx CRC checker
10 = Reset Tx CRC generator
11 = Reset Tx underrun/EOM latch

D2 to D4: 000 = Null code
001 = Point high
010 = Reset external/status interrupts
011 = Send abort
100 = Enable interrupt on next Rx character
101 = Reset Tx interrupt pending
110 = Error reset
111 = Reset highest IUS

D5 to D7: Address of register to access (WR0 to WR7 for writes, RR0 to RR7 for reads). If D2 to D4 = 001 (point high), then D5 to D7 address the upper registers (WR8 to WR15 for writes, RR8 to RR15 for reads).

Status Register (RR0)

MSB LSB

D0	D1	D2	D3	D4	D5	D6	D7

D0: Break/abort
D1: Tx underrun/EOM
D2: CTS
D3: Synch/hunt
D4: DCD
D5: Tx buffer empty
D6: Zero count
D7: Rx character available

COM4 Data Register (Port 0x841)

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

This register provides direct access to the read and write FIFOs of COM4, bypassing the two-stage pointer-plus-value mechanism of the Command register. Any pointer value already set up in the Command register is unaffected by accesses to this register. A read of the register accesses the read FIFO (RR8), and a write accesses the write FIFO (WR8). A reset does not change the data bits of this register.

COM3 Command/Status Register (Port 0x842)

This register provides access to the COM3 Command and Status Registers. See the COM4 Command/Status Register (Port 0x840) for more details.

COM3 Data Register (Port 0x843)

This register provides direct access to the read and write FIFOs of COM3. See the COM4 Data Register (Port 0x841) for more details.

Board Revision Register (Port 0x0854)

This register provides information on the build state of the PPC4B.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D2: Number of artwork revision

Meaning	D0	D1	D2
Reserved	0	0	0
Revision 1	0	0	1
Revision 2	0	1	0
Revision 3	0	1	1
Revision 4	1	0	0
Revision 5	1	0	1
Revision 6	1	1	0
Use Extended Board Revision Register (port 0x0856)	1	1	1

D3 to D7: Letter of hardware build revision

Meaning	D3	D4	D5	D6	D7
Revision A	0	0	0	0	0
Revision B	0	0	0	0	1
:	:	:	:	:	:
Revision Y	1	1	0	0	0
Revision YA	1	1	0	0	1
:	:	:	:	:	:
Revision YG	1	1	1	1	1

Extended Board Revision Register (Port 0x0856)

If bits D0 to D2 of the Board Revision Register (Port 0x0854) hold the value 111_b, this register provides the major revision state of the board.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D7: Actual major artwork revision number.

Extended Board ID Register (Port 0x0858)

If the hardware ID bits ID2 to ID0 (bits D6 and D7 of the Motherboard Type Register, port 0x0866 and bit 0 of the Equipment Present Register 1, port 0x080C respectively) hold the value 000_b, this register provides the extended board ID value. The PPC4B falls into this category.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D7: Board ID:

Value	Board
0x07	PPC4B
0x08	PPC6
0x09	GPC4A
0x0A	EP1A

CIO Port C Data Register (Port 0x0860)

This register allows control of the three front-mounted and four of the rear-mounted software programmable LEDs.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D3: Write protect mask for D4 to 7 respectively:
0 = Write enabled
1 = Write protected

D4: DS3 and DS203, green
0 = LED on
1 = LED off

D5: DS204, yellow
0 = LED on
1 = LED off

D6: DS1 and DS201, red
0 = LED off
1 = LED on

D7: DS2 and DS202, yellow
0 = LED on
1 = LED off

See the LEDs section for the location of these LEDs.

Note: DS1 is on by default after power-up.

CIO Port B Data Register (Port 0x0861)

This register controls the DTR modem signals for the COM3 and COM4 serial ports and also the various transmit clocking options when RS422/485 transceivers are fitted.

For a description of how to set up this port for the operation described below, see the CIO Control Register section. Pull-up and pull-down resistors hold these bits to 10001000_b during reset of the CIO until the port is properly configured and enabled.

The data bits of this register are not changed by a reset.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: COM4_DTR (output)
0 = Assert DTR on COM4
1 = Negate DTR on COM4

D1 and D3: COM4_TX_CKSEL and COM4_TX_EN (output)
If RS422/485 transceivers are fitted, these bits configure the ESCC transmit clock options for the COM4 port, and assume that the ESCC has been programmed accordingly.

00 = Not a valid combination (ESCC transmit clock is neither transmitted on TT nor received on ST)
01 = ESCC supplies a transmit clock on TT
10 = ESCC transmit clock is received on ST
11 = ESCC transmit clock is received on ST and retransmitted on TT

If RS232 transceivers are fitted, D1 has no effect and D3 enables or disables the RS232 transceivers as follows:

0 = Disable all transceivers except the CTS receiver
1 = Enable all transceivers

D2: COM4_RX_EN (output)
0 = Disable receivers on RXD, CTS, DCD and DSR for COM4
1 = Enable receivers on RXD, CTS, DCD and DSR for COM4

Note: This bit has no effect if RS232 transceivers are fitted

D4: COM3_DTR (output)
0 = Assert DTR on COM3
1 = Negate DTR on COM3

D5 and D7: COM3_TX_CKSEL, COM3_TX_EN (output)
If RS422/485 transceivers are fitted, these bits configure the ESCC transmit clock options for the COM3 port, and assume that the ESCC has been programmed accordingly.

00 = Not a valid combination (ESCC transmit clock is neither transmitted on TT nor received on ST)
01 = ESCC supplies a transmit clock on TT
10 = ESCC transmit clock is received on ST
11 = ESCC transmit clock is received on ST and re-transmitted on TT

If RS232 transceivers are fitted, D5 has no effect and D7 enables or disables the RS232 transceivers, as follows:

0 = Disable all transceivers except the CTS receiver
1 = Enable all transceivers

D6: COM3_RX_EN (output)
0 = Disable receivers on RXD, CTS, DCD and DSR for COM3
1 = Enable receivers on RXD, CTS, DCD and DSR for COM3

Note: This bit has no effect if the RS232 transceivers are fitted.

CIO Port A Data Register (Port 0x0862)

This register controls certain hardware features of the PPC4B.

For a description of how to set up this port for the operation described below, see the CIO Control Register section. Pull-up and pull-down resistors hold these bits to $00111X11_b$ during reset of the CIO until the port is properly configured and enabled.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: COM4_RX_CKSEL (output)
0 = Disable the RT receiver on the COM4 port.
1 = Enable the RT receiver on the COM4 port.

Note: This bit has no effect if the RS232 transceivers are fitted.

D1: COM3_RX_CKSEL (output)
0 = Disable the RT receiver on the COM3 port.
1 = Enable the RT receiver on the COM3 port.

Note: This bit has no effect if the RS232 transceivers are fitted.

D2: RESET_SW_EN (output)
0 = Disable the front panel reset switch logic (if present).
1 = Enable the front panel reset switch logic (if present).

Note: This bit has no effect if the switch logic is not present or if link E1 is removed.

D3: Vpp_1_ENABLE (output)
0 = Enable Vpp on FLASH pages 1 to 3.
1 = Disable Vpp on FLASH pages 1 to 3.

Note: This bit has no effect unless P2 pin Z1 or P0 pin A2 is connected to GND and link E5 is fitted.

D4: Vpp_0_ENABLE (output)
0 = Enable Vpp on FLASH page 0.
1 = Disable Vpp on FLASH page 0.

Note: This bit has no effect unless P2 pin Z1 or P0 pin A2 is connected to GND and link E6 is fitted.

D5: WATCHDOG
If this bit is configured as an input, the watchdog is disabled.
If this bit is configured as an output, writing to it (the value is not significant) triggers the watchdog timer. Once triggered, the timer must be re-triggered at least once every 1.5 seconds, or a hard reset of the entire PPC4B occurs. Disabling the watchdog after triggering it clears the watchdog, and no reset is generated.

D6: COM4_DSR (input)
0 = DSR on the COM4 port is asserted.
1 = DSR on the COM4 port is negated.

D7: COM3_DSR (input)
0 = DSR on the COM3 port is asserted.
1 = DSR on the COM3 port is negated.

CIO Control Register (Port 0x0863)

This register is used to control the CIO ports. See the CIO datasheet for a full description of the control registers.

A reset of the CIO sets up ports A, B and C as follows:

- Disabled - external pins are tri-stated
- Non latching inputs
- Active high, TTL level outputs
- All bits configured as outputs
- No handshaking (simple parallel port)

Each port must be properly configured and set to its initial value before it can be enabled for use. The initial values are as follows:

Port A = 0x3B (non-latching inputs, active high TTL outputs, D0 to D7 outputs).

Port B = 0x88 (non-latching inputs, active high TTL outputs, D0 to D7 outputs).

Port C = 0x02 (non-latching inputs, active high TTL outputs, D4 to D7 outputs).

ID Link Register (Port 0x0864)

This register allows you to read the state of the Board ID links (E10, E14, E15 and E16), the FLASH programming voltages and the global FLASH write enable.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: FLASH Pages 1 to 3 Vpp state
0 = On
1 = Off

D1: Global FLASH Write Enable
0 = Enabled
1 = Disabled

D2: FLASH Page 0 Vpp state
0 = On
1 = Off

D3: GA4 (VME64 Geographical Address bit 4)

D4: E10/GA3
0 = Link fitted
1 = Link not fitted

D5: E14/GA2
0 = Link fitted
1 = Link not fitted

D6: E15/GA1
0 = Link fitted
1 = Link not fitted

D7: E16/GA0
0 = Link fitted
1 = Link not fitted

Note: Bits D4, D5, D6 and D7 are also connected to the VME64 Geographical Address bits GA3, GA2, GA1 and GA0 respectively. If you wish to read the status of the Geographical Address bits, do not fit the links, as they connect these bits to 0 Volts.

The Global FLASH Write Enable comes directly from a wire-OR connection of P0 pin A2 and P2 pin Z1. This signal has an on-board pull-up and so defaults to disabled. See the FLASH section for more details.

Motherboard Type Register (Port 0x0866)

This register provides information on the type of motherboard and DRAM ECC operation. The bits used in this register are compatible with the other members of the current Radstone PPC product range.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0: HW_ECC ENABLE
0 = Non-ECC
1 = ECC enabled

This read/write bit should only be changed when the MPC107 Memory Controller is inactive. This bit also controls LED DS209. When set for ECC Enabled, DS209 is off (see the LEDs section for more details).

D1: Reserved

D2: ECC_TYPE
0 = ECC
1 = Parity

D3: ECC
0 = ECC not fitted
1 = ECC fitted

D4 and 5: Bus Speed.

Bits	Speed (MHz)
11	83
10	66
01	100
00	Reserved

D6 and 7: Hardware ID2 and ID1 respectively. Used with Hardware ID0 (bit 0 of Equipment Present Register 1) to define the hardware type as follows:

ID2 to ID0	Hardware Type
111	PPC1/PPC3
110	PPC2
101	PPC1A
100	PPC2A
011	PPC4
010	PPC4A
001	Reserved
000	Use Extended ID Register (port 0x0858) for Hardware Type

The software inverts these bits, so (after inversion) values 0 to 6 are valid and 7 indicates that the Extended ID register should be used.

ISA DMA Routing Register (Port 0x0868)

This register provides DMA channel configuration for the ISA bridge. The Winbond ISA bridge has four 8-bit and three 16-bit DMA channels. DMA channels 0 to 3 are 8-bit channels, whilst channels 5 to 7 are 16-bit channels (there is no channel 4).

The ISA bridge has DMA channel 0 and 1 fixed as COM3_RX and COM4_RX respectively. DMA channels 2, 3, 5 and 6 can have their function altered by the value in this register, and DMA channel 7 is not used.

When the PPC4B is reset, this register is reset to zero. In this state, the DMAs for COM3_TX and COM4_TX are configured for 16-bit transfers and the floppy disc (FDC) and parallel port (LPT) are configured for 8-bit transfers.

This register can be used to reconfigure the DMAs so that you can get the desired DMA size:

Note: **Do *not*** alter this register during DMA operation.

MSB							**LSB**
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D5: Reserved

D6 and D7: DMA routing:

Register Bits		8-bit DMA		16-bit DMA	
D6	**D7**	**DMA2**	**DMA3**	**DMA5**	**DMA6**
0	**0**	FDC	LPT	COM3	COM4
0	**1**	*COM3*	LPT	*FDC*	COM4
1	**0**	FDC	*COM4*	COM3	*LPT*
1	**1**	*COM3*	*COM4*	*FDC*	*LPT*

Note: Italics show changes from the default.

PCI Routing Register (Port 0x086C)

This register controls the mapping of the PCI address range on the processor bus. This register is set to 0x02 on reset/power-up.

MSB							LSB
D0	D1	D2	D3	D4	D5	D6	D7

D0 to D5: Reserved

D6: Map to PowerSpan. This read/write bit controls whether accesses in the range 0x80000000 to 0xFEC00000 on the processor bus map to the MPC107 or the PowerSpan, as follows:
0 = 0x80000000 to 0xFEC00000 accesses map to the PowerSpan
1 = 0x80000000 to 0xFEC00000 accesses map to the MPC107 (default).

D7: Reserved. Write as 0.

When D6 is set (i.e. the MPC107 is being used), LED DS215 is on. When LED DS215 is off, D6 is 0 and the PowerSpan decodes the processor bus address range 0x80000000 to 0xFEC00000.

Interrupts and Error Reporting

The following table shows the various external interrupt sources to the processor and their relative priorities. The table also shows whether the previous state of the processor is recoverable.

Priority	Interrupt	Cause	Recoverability
0	System Reset	Power on, Hard reset	Non-recoverable
1	Machine Check	TEA~ input, Address or Data Parity error, Machine Check Input (MCP~), Non-maskable Interrupt (NMI~)	Non-recoverable in most cases
2	System Reset	Soft reset	Recoverable unless Machine Check occurs
3	System Management Interrupt	SMI~ input	Recoverable unless Machine Check or System Reset occurs
4	External Interrupt	INT~ input	Recoverable unless Machine Check or System Reset occurs

System Resets

There are two types of system reset that may be applied to the PPC4B: 'Hard' and 'Soft'.

Hard Reset

This causes the processor to begin executing code from address 0xFFF00100 in the System FLASH. By fitting a hardware jumper (E2), the System FLASH addresses may be passed to the VME instead of the FLASH. In this way, the processor can begin executing code from a VME source.

The following table summarises events that may cause a hard reset:

Source		Action	SYSRESET~ Generation
Hardware Events	Power-on	Hard reset all devices	Yes
	Received SYSRESET~		No
	Watchdog time-out		If System Controller
	Front-panel hard reset (build levels 1 to 3)		
Hardware Events	P0 (where fitted) hard reset signal (pin C1)	Hard reset all devices	If System Controller
	P2 hard reset signal (pin Z3)		
	P7 hard reset signal (pin B1)		
Software Events	SW_LRST bit VCSR bit	Hard reset excluding VMEbus interface	No
	SW_SYSRESET bit	Hard reset if System Controller	If System Controller

The SW_LRST, VCSR and SW_SYSRESET bits are located in the Universe II control registers. Another VME master may use these to reset the PPC4B

If triggered (via the CIO Port A Data Register), the watchdog will cause a reset unless re-triggered at least every 1.5 seconds.

The front panel hard reset may be disabled under software control or by removing hardware jumper E1.

Notes:

1) The front panel reset switch is not fitted on build levels 4 and 5.

2) Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled. Similarly, integrity of FLASH or EEPROM data cannot be guaranteed if a hard reset occurs during a FLASH or EEPROM write cycle, respectively.

See the System RAM section for SDRAM initialisation requirements following a hard reset.

Soft Reset

This causes the processor to reach a recoverable state and then branch to either 0x00000100 or 0xFFF00100, depending on the state of the IP bit in the processor's Machine State Register.

The following table summarises events that may cause a soft reset:

Source	
Hardware Events	Front-panel soft reset (build levels 1 to 3)
	P0 (where fitted) soft reset signal (pin C2)
	P2 soft reset signal (pin Z5)
	P7 (on-board connector) soft reset signal (pin B3)
Software Events	HOT_RESET bit in ISA-bridge

The front panel soft reset switch may be disabled under software control or by removing hardware jumper E1.

SilverChip does not support the use of soft reset.

Machine Check Exception

The PCI bridge may be configured to assert TEA~ to the processor for a FLASH write error or an unsupported local bus cycle. The processor may be configured to take a machine check exception or enter the checkstop state.

The processor address and data parity error inputs (APE~ and DPE~) are not used on the PPC4B. Address and data parity errors are reported via the machine check pin as described below.

The PCI bridge may be configured to assert the machine check input (MCP~) to the processor to signal a non-recoverable error. The processor may be configured to take a machine check exception or enter the checkstop state. Non-recoverable errors are:

- FLASH write error
- Unsupported local bus cycle
- PCI PERR or SERR
- Memory read ECC multi-bit error
- Memory select error (address out of range)
- PCI target abort (e.g. VMEbus BERR~) or master abort
- Refresh overflow error

In addition, the PCI bridge may be programmed to produce a machine check exception after a programmable number of correctable single bit errors.

Status bits in the PCI bridge allow the cause of the exception to be determined.

Link E3 allows the PPC4B hardware to be configured so that machine checks are signalled as an interrupt on IRQ13 rather than on the processor's MCP~ pin. This link is described in chapter 4.

If you know that a machine check may occur during a specific operation (e.g. a VMEbus BERR~ during a VMEbus memory sizing operation), it may be possible to ensure that the processor is in a recoverable state after the machine check exception. This can be done by using the SYNC instruction before and after the instruction that potentially causes machine check.

Non-Maskable Interrupt (NMI~)

The NMI~ output of the ISA bridge is connected to the NMI~ input of the PCI bridge. It is not generally required, as the PCI bridge can be configured to detect SERR on the PCI bus.

System Management Interrupt (SMI~)

The System Management Interrupt pin of the PCI bridge is connected to the SMI~ output from the ISA bridge to support the power management features of the ISA bridge.

External Interrupt (INT~)

The processor external interrupt pin (INT~) is asserted for a pending interrupt from the interrupt controller in the ISA bridge.

Interrupt priorities and modes are assigned as shown in the table below. The SilverChip Boot Firmware sets up these assignments. If you are using alternate boot firmware, it must duplicate these settings. Edge sensitive interrupts are sensitive to the rising edge (except for IRQ8, which is sensitive to the *falling* edge); level sensitive interrupts are active low.

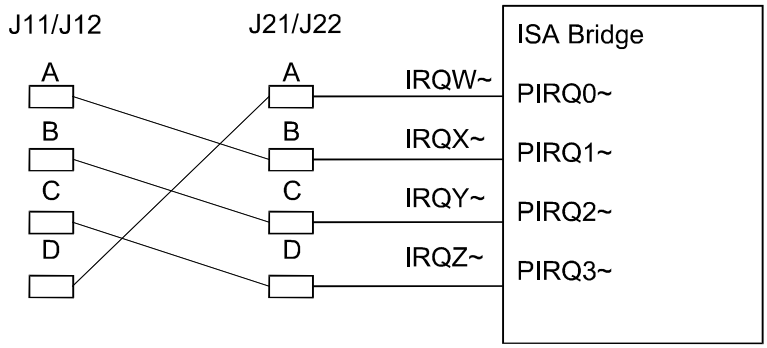
IRQ	Priority	Mode	Source
0	1	Edge	Timer 1 Counter 0 (internal to ISA bridge)
1	2	Edge	Ultra I/O IRQ1 (Keyboard)
2			Cascade for IRQ8 to IRQ15
3	11	Edge	Ultra I/O IRQ3 (COM2)
4	12	Edge	Ultra I/O IRQ4 (COM1)
5	13	Level	CIO
6	14	Edge	Ultra I/O IRQ6 (Floppy)
7	15	Edge	Ultra I/O IRQ7 (LPT1)
8	3	Edge	Ultra I/O IRQ8 (RTC)
9	4	Level	PCI and Ethernet
10	5	Level	COM3/COM4 Serial Ports
11	6	Level	PCI and VME
12	7	Edge	Mouse
13	8	Edge	Alternate Machine Check
14	9	Level	PCI and SCSI
15	10	Level	PCI

PCI Interrupts

There are 4 interrupt lines for the PMC expansion slots on the motherboard and the PMC carrier. These are connected to the PIRQ~ inputs of the interrupt controller. The PIRQ~ inputs may be routed to any IRQ that is set to level sensitive mode.

The interrupt routing follows the recommendations in the PCI specification and the PCI system design guide with a “rotation” between each slot.

The interrupt lines for the two on-board PMC slots are routed as shown below:



Two single function PMCs (which always use INTA~) are able to use unique IRQs with appropriate programming of the interrupt controller.

PCI Configuration

The boot process must configure the base address and space type (memory or I/O) of all the PCI attached peripherals.

Each PCI device also has several registers located in PCI configuration space, which is accessed by the processor through the MPC107 PCI bridge and memory controller using the CONFIG_ADDR and CONFIG_DATA registers. A full description of PCI configuration can be found in the PCI and MPC107 specifications.

The device number mapping for the PCI bus attached to the MPC107 follows:

Device Number	Function
0	MPC107 PCI bridge and memory controller
1 to 10	Not implemented
11	83C553 PCI to ISA bridge
12	53C860 SCSI controller
13	21143 Ethernet controller
14	Universe VME controller
15	PMC2
16	PMC1
17 to 30	Not implemented

Keylock

The keylock input signal allows the software to interrogate an external keyswitch. For example, SilverChip could request a password if the keyswitch is in the locked position and a password is set up in the NOVRAM.

The keylock signal defaults to high if no external connection is made.

Chapter 6 - Connectors

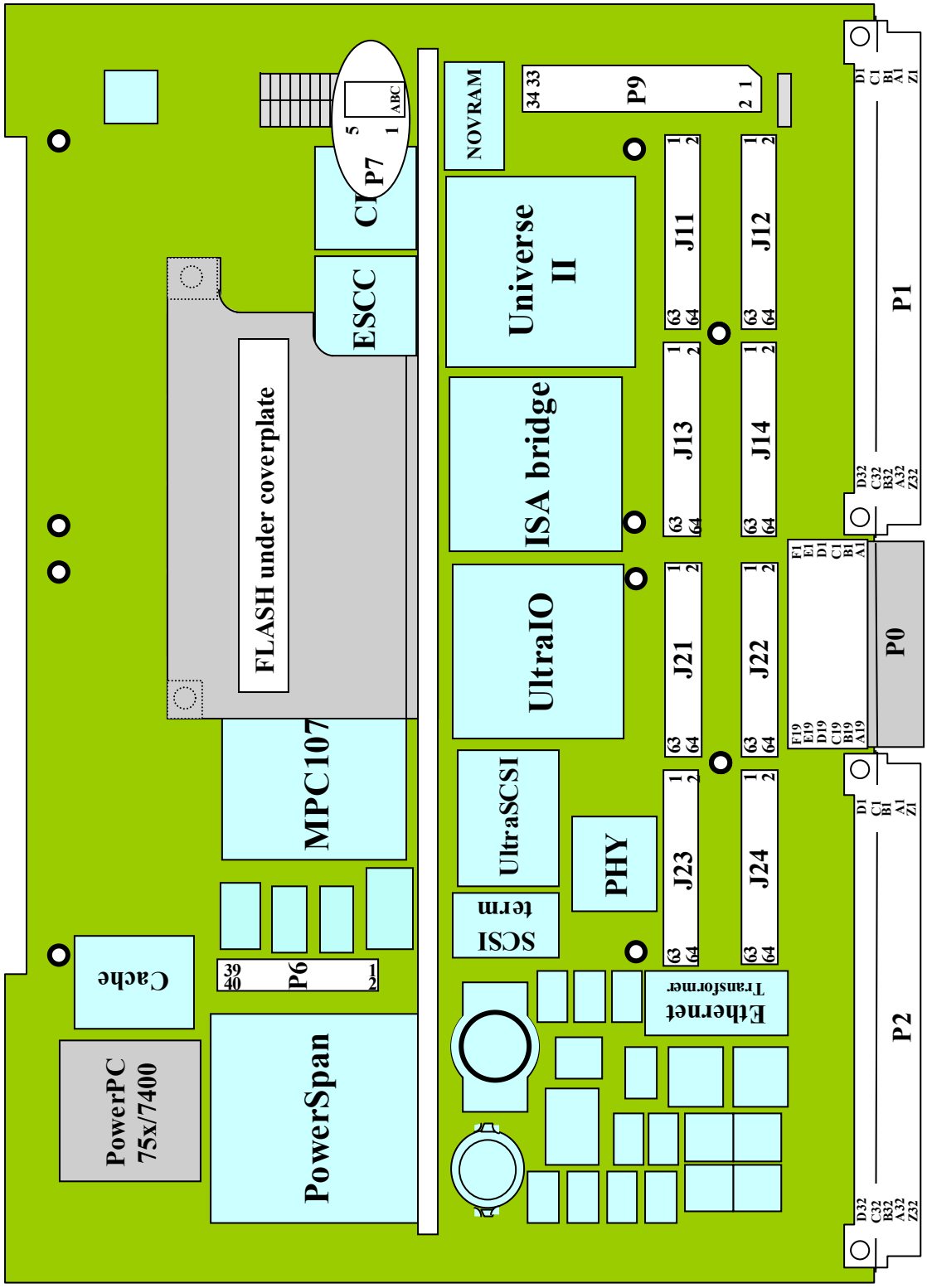
This chapter gives the pinouts and signal descriptions for the connectors on the PPC4B.

The following table shows the function of the connectors on the PPC4B:

Connector	Function
P1	VMEbus
P2	VMEbus
P0	PCI
J11, J12, J13, J14	PMC (site 1)
J21, J22, J23, J24	PMC (site 2)
P6	JTAG/Debug and RISCWatch (Factory use)
P7	Additional COM Ports/JTAG
P9	Floppy Disk Drive

The connector positions are shown in Figure 6-1 overleaf.

Figure 6-1. Connector Positions and Pin Numbering



P1 (VMEbus) Connector

Pin Number	Row z	Row a	Row b	Row c	Row d
1	NC	D00	BBSY~	D08	+5V
2	GND	D01	BCLR~	D09	GND
3	NC	D02	ACFAIL~	D10	NC
4	GND	D03	BG0IN~	D11	NC
5	NC	D04	BG0OUT~	D12	NC
6	GND	D05	BG1IN~	D13	NC
7	NC	D06	BG1OUT~	D14	NC
8	GND	D07	BG2IN~	D15	NC
9	NC	GND	BG2OUT~	GND	NC
10	GND	SYSCLK	BG3IN~	SYSFAIL~	GA0~
11	NC	GND	BG3OUT~	BERR~	GA1~
12	GND	DS1~	BR0~	SYSRESET~	3.3V
13	NC	DS0~	BR1~	LWORD~	GA2~
14	GND	WRITE~	BR2~	AM5	3.3V
15	NC	GND	BR3~	A23	GA3~
16	GND	DTACK~	AM0	A22	3.3V
17	NC	GND	AM1	A21	GA4~
18	GND	AS~	AM2	A20	3.3V
19	NC	GND	AM3	A19	NC
20	GND	IACK~	GND	A18	3.3V
21	NC	IACKIN~	SERA	A17	NC
22	GND	IACKOUT~	SERB	A16	3.3V
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7~	A14	3.3V
25	NC	A06	IRQ6~	A13	NC
26	GND	A05	IRQ5~	A12	3.3V
27	NC	A04	IRQ4~	A11	NC
28	GND	A03	IRQ3~	A10	3.3V
29	NC	A02	IRQ2~	A09	NC
30	GND	A01	IRQ1~	A08	3.3V
31	NC	-12V	+5VSTDBY	+12V	GND
32	GND	+5V	+5V	+5V	+5V

P2 Connector Standard Pinout

See the J24 connector description for an alternative P2 pinout.

Pin Number	Row z	Row a	Row b	Row c	Row d
1	FLASH_WREN~	DB0~ (SCSI)	+5V	Collision-/RX+	COM3_TXD_A
2	GND	DB1~ (SCSI)	GND	Collision+/RX-	COM3_TXD_B
3	EXRESET~	DB2~ (SCSI)	Reserved	Transmit-/TX+	COM3_RXD_A
4	GND	DB3~ (SCSI)	A24	Transmit+/TX-	COM3_RXD_B
5	EXABORT~	DB4~ (SCSI)	A25	Receive-	COM3_RTS_A
6	GND	DB5~ (SCSI)	A26	Receive+	COM3_RTS_B
7	SWAPFLASH~	DB6~ (SCSI)	A27	+12V Fused	COM3_CTS_A
8	GND	DB7~ (SCSI)	A28	nSTROBE	COM3_CTS_B
9	COM4_TXD_A	DBP~ (SCSI)	A29	D1	COM3_DSR_A
10	GND	ATN~ (SCSI)	A30	D2	COM3_DSR_B
11	COM4_TXD_B	BSY~ (SCSI)	A31	D3	COM3_DCD_A
12	GND	ACK~ (SCSI)	GND	D4	COM3_DCD_B
13	COM4_RXD_A	RST~ (SCSI)	+5V	D5	COM3_DTR_A
14	GND	MSG~ (SCSI)	D16	D6	COM3_DTR_B
15	COM4_RXD_B	SEL~ (SCSI)	D17	D7	COM3_TT_A
16	GND	C/D (SCSI)	D18	D8	COM3_TT_B
17	COM4_CTS_A	REQ~ (SCSI)	D19	nACK	COM3_ST_A
18	GND	I/O (SCSI)	D20	BUSY	COM3_ST_B
19	COM4_CTS_B	TERMPWR (SCSI)	D21	PERROR	COM3_RT_A
20	GND	MOUSE_CLK	D22	SELECT	COM3_RT_B
21	COM4_DCD_A	MOUSE_DATA	D23	nAUTOFD	COM4_RTS_A
22	GND	KBD_5V	GND	nFAULT	COM4_RTS_B
23	COM4_DCD_B	KBD_CLK	D24	nINIT	COM4_DSR_A
24	GND	KBD_DATA	D25	nSELECTIN	COM4_DSR_B
25	COM4_ST_A	COM2_TXD	D26	SPEAKER_OUT	COM4_DTR_A
26	GND	COM2_RXD	D27	KEYLOCK_IN	COM4_DTR_B
27	COM4_ST_B	COM2_RTS	D28	COM1_TXD	COM4_TT_A
28	GND	COM2_RI	D29	COM1_RXD	COM4_TT_B
29	COM4_RT_A	COM2_CTS	D30	COM1_RTS	COM1_DSR
30	GND	COM2_DTR	D31	COM1_CTS	COM1_RI
31	COM4_RT_B	COM2_DCD	GND	COM1_DTR	GND
32	GND	COM2_DSR	+5V	COM1_DCD	+5V

VMEbus Signal Descriptions

The VMEbus signals occupy rows z, a, b, c and d of the P1 connector and row b of the P2 connector.

Mnemonic	Signal Description
A01 to A15	**Address Bus (bits 1 to 15).** Address lines that are used to broadcast a short address
A16 to A23	**Address Bus (bits 16 to 23).** Address lines that are used with A01 to A15 and LWORD~ to broadcast a standard address
A24 to A31	**Address Bus (bits 24 to 31).** Address lines that are used with A01 to A23 and LWORD~ to broadcast an extended or 64-bit address
ACFAIL~	**AC Failure.** This shows that the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met
AM0 to AM5	**Address Modifier (bits 0 to 5).** These are used to broadcast information such as the address size, cycle type, master identification or any combination of these
AS~	**Address Strobe.** This shows when a valid address has been placed on the address bus
BBSY~	**Bus Busy.** This is driven low by the requester associated with the current bus master to show that the master is using the bus
BCLR~	**Bus Clear.** This is generated by an arbiter to show that there is a higher priority request for the bus than the one being processed. This requests the current master to release the bus
BERR~	**Bus Error.** This is generated by a slave or bus timer to tell the master that the data transfer did not complete
BG0IN~ to BG3IN~	**Bus Grant (0 to 3) In.** These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BgxIN~/BGxOUT~ signals form the bus grant daisy chain, i.e. the BGxOUT~ of one board forms the BgxIN~ of the next board in the daisy chain
BG0OUT~ to BG3OUT~	**Bus Grant (0 to 3) Out.** These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain
BR0~ to BR3~	**Bus Request (0 to 3).** A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D31	**Data Bus.** These are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers
DS0~, DS1~	**Data Strobe 0, 1.** These are used with LWORD~ and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus
DTACK~	**Data Transfer Acknowledge.** This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle
GND	The DC voltage reference for the system
IACK~	**Interrupt Acknowledge**. This is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN~ pin of slot 1, where it is monitored by the IACK daisy chain driver
IACKIN~	**Interrupt Acknowledge In.** This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN~/IACKOUT~ form the interrupt acknowledge daisy chain

Mnemonic	Signal Description
IACKOUT~	**Interrupt Acknowledge Out.** This is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress
IRQ1~ to IRQ7~	**Interrupt Request (1 to 7).** These are driven low by interrupters to request an interrupt on the corresponding level
LWORD~	**Longword.** This is used with DS0~, DS1~ and A01 to select which byte location(s) within the 4-byte group are accessed during the data transfer
Reserved	This signal is reserved for future enhancements of the VME specification
SERA	The serial clock used to synchronise the data transmission on the serial bus
SERB	This is used for serial data transmission
SYSCLK	**System Clock.** This provides a constant 16 MHz clock signal that is independent of any other bus timing
SYSFAIL~	**System Fail.** This shows that a failure has occurred in the system. This signal can be generated by any board in the system
SYSRESET~	**System Reset.** When this is low, it causes the system to be reset
WRITE~	**Write.** This is generated by a master to show whether the data transfer cycle is a read or a write
+5VSTDBY	**+5 Volts DC Standby.** This supplies +5V DC to devices requiring battery back-up. **Note:** The power supply to the RTC on the PPC4B is fed from this pin. VMEbus compliance requires this voltage to be 5V ± 5%. There is no provision for 3V standby
+5V	+5 Volts DC power
+12V	+12 Volts DC power
-12V	-12 Volts DC power
GA0~ to GA4~	**Geographic Address**. These are used to set the slave VME address of the board. GA0~ to GA3~ may be set to zero by fitting links E1 to E4 respectively. When GA4~ is not connected, a pull-up resistor on the PPC4B pulls the signal high
3.3V	These pins are not connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on P0 and the PMC sites, and capacitively decoupled to ground

P2 I/O Signal Descriptions

Mnemonic	Description
DB0~ to DB7~	SCSI bus data
DBP~	SCSI bus data parity
ATN~	SCSI bus Attention
BSY~	SCSI bus Busy
ACK~	SCSI bus Acknowledge
RST~	SCSI bus Reset
MSG~	SCSI bus Message phase
SEL~	SCSI bus Select
C/D	SCSI bus Command/Data phase
REQ~	SCSI bus Request
I/O	SCSI bus I/O phase
TERMPWR	**SCSI bus terminator power.** Supplies power for external SCSI bus terminators. Rated at 1 Amp†
MOUSE_CLK	**Mouse Clock.** Clock drive for mouse
MOUSE_DATA	**Mouse Data.** Mouse data line
KBD_5V	**Keyboard 5V.** Supplies power for the keyboard and mouse. Rated at 300 mA†
KBD_CLK	**Keyboard Clock.** Clock drive for the keyboard
KBD_DATA	**Keyboard Data.** Keyboard data line
COM1/2_TXD	COM1/2 Transmit Data
COM1/2_RXD	COM1/2 Receive Data
COM1/2_RTS	COM1/2 Request-To-Send
COM1/2_RI	COM1/2 Ring Indicator
COM1/2_CTS	COM1/2 Clear-To-Send
COM1/2_DTR	COM1/2 Data Terminal Ready
COM1/2_DCD	COM1/2 Data Carrier Detect
COM1/2_DSR	COM1/2 Data Set Ready
KEYLOCK_IN	**Keylock input.** Used to detect the state of an external keyswitch. May be used to implement system password protection
SPEAKER_OUT	**Loudspeaker Output.** Outputs Timer2 Audio. May be used to drive 4 or 8Ω loudspeaker
nSELECTIN	Parallel port Select In
nINIT	Parallel port INIT
nFAULT	Parallel port FAULT
nAUTOFD	Parallel port AUTOFD
SELECT	Parallel port SELECT

† These are resettable fuses. The fuse rating is the current rating that the fuse can carry. In 20°C still air, the fuse trips at twice the rated current.

Mnemonic	Description
PERROR	Parallel port PERROR
BUSY	Parallel port BUSY
nACK	Parallel port ACK
D1 to D8	Parallel port data bits
nSTROBE	Parallel port STROBE
+12V	**12 Volts.** Rated at 1 Amp to power external Ethernet transceiver. Also used by P2 adapter†
Receive+/-	10Base5 receive data
Transmit+/-	10Base5 transmit data
Collision+/-	10Base5 collision
TX+/-	10/100BaseT transmit data
RX+/-	10/100BaseT receive data
FLASH_WREN~	Global FLASH write enable
EXRESET~	External Reset (Hard Reset)
EXABORT~	External Abort (Soft Reset)
COM3/4_TXD_A	RS422 or RS232 Transmit Data
COM3/4_TXD_B	RS422 Transmit Data
COM3/4_RXD_A	RS422 or RS232 Receive Data
COM3/4_RXD_B	RS422 Receive Data
COM3/4_CTS_A	RS422 or RS232 Clear To Send
COM3/4_CTS_B	RS422 Clear To Send
COM3/4_DCD_A	RS422 or RS232 Data Carrier Detect
COM3/4_DCD_B	RS422 Data Carrier Detect
COM3/4_RTS_A	RS422 or RS232 Ready To Send
COM3/4_RTS_B	RS422 Ready To Send
COM3/4_DSR_A	RS422 or RS232 Data Set Ready
COM3/4_DSR_B	RS422 Data Set Ready
COM3/4_DTR_A	RS422 or RS232 Data Terminal Ready
COM3/4_DTR_B	RS422 Data Terminal Ready
COM3/4_ST_A/B	RS422 Send Timing
COM3/4_RT_A/B	RS422 Receive Timing
COM3/4_TT_A/B	RS422 Terminal Timing
SWAPFLASH~	Wire-Ored to link E13 to provide same functionality (swap boot images in FLASH page 1)

† This is a resettable fuse. The fuse rating is the current rating that the fuse can carry. In 20°C still air, the fuse trips at twice the rated current.

PMC Connector Pinouts

J11 and J21

Pin	Signal	Pin	Signal
1	TCK	2	-12V
3	GND	4	INTA~
5	INTB~	6	INTC~
7	BUSMODE1~	8	+5V
9	INTD~	10	No connection
11	GND	12	No connection
13	CLK	14	GND
15	GND	16	GNT~
17	REQ~	18	+5V
19	VIO	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3~
27	AD22	28	AD21
29	AD19	30	+5V
31	VIO	32	AD17
33	FRAME~	34	GND
35	GND	36	IRDY~
37	DEVSEL~	38	+5V
39	GND	40	LOCK~
41	No connection	42	No connection
43	PAR	44	GND
45	VIO	46	AD15
47	AD12	48	AD11
49	AD09	50	+5V
51	GND	52	C/BE0~
53	AD06	54	AD05
55	AD04	56	GND
57	VIO	58	AD03
59	AD02	60	AD01
61	AD00	62	+5V
63	GND	64	REQ64~

J12 and J22

Pin	Signal	Pin	Signal
1	+12V	2	TRST~
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	No connection
9	No connection	10	No connection
11	BUSMODE2~	12	3.3V
13	RST~	14	BUSMODE3~
15	3.3V	16	BUSMODE4~
17	No connection	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V
25	IDSEL	26	AD23
27	3.3V	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2~
33	GND	34	No connection
35	TRDY~	36	3.3V
37	GND	38	STOP~
39	PERR~	40	GND
41	3.3V	42	SERR~
43	C/BE1~	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD08	50	3.3V
51	AD07	52	No connection
53	3.3V	54	No connection
55	No connection	56	GND
57	No connection	58	No connection
59	GND	60	No connection
61	ACK64~	62	3.3V
63	GND	64	No connection

J13 and J23

Pin	Signal	Pin	Signal
1	Reserved (PCI)	2	GND
3	GND	4	C/BE7~
5	C/BE6~	6	C/BE5~
7	C/BE4~	8	GND
9	VIO	10	PAR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	VIO	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	VIO	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	VIO	58	AD32
59	Reserved (PCI)	60	Reserved (PMC)
61	Reserved (PCI)	62	GND
63	GND	64	Reserved (PMC)

PMC Signal Descriptions

Mnemonic	Description
AD0 to AD63	**Address/Data bits.** Multiplexed address and data bus
C_BE0 to C_BE7	**Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
FRAME~	**FRAME.** Driven low by the current master to signal the start and duration of an access
DEVSEL~	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE3
IRDY~	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	**LOCK.** Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE1~	**Bus Mode 1.** Driven low by a PMC if it supports the current bus mode
BUSMODE2~ to BUSMODE4~	**Bus mode.** Driven by the host to indicate the bus mode. On the PPC4B this is always PCI. BUSMODE2~ is only connected to a 4.7 kΩ pull-up. BUSMODE3~ and BUSMODE4~ are only connected to 1kΩ pull-downs
RST~	**Reset.** Driven low to reset the PCI bus
TRDY~	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
PERR~	**Parity Error.** Driven low by a PCI agent to signal a parity error
SERR~	**System Error.** Driven low by a PCI agent to signal a system error
STOP~	**STOP.** Driven low by a PCI target to signal a disconnect or target-abort
INTA~ to INTD~	**Interrupt lines.** Level-sensitive, active-low interrupt requests
CLK	**Clock.** All PCI bus signals except RST~ are synchronous to this clock
REQ~	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
GNT~	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles
NC	**No connection**
REQ64~	**Request 64 Bit**. Driven low by a PCI master to request 64-bit transfer. Only connected to a 4.7 kΩ pull-up on the PPC4B
ACK64~	**Acknowledge 64 Bit**. Driven low by PCI agent in response to REQ64. Only connected to a 4.7 kΩ pull-up on the PPC4B
PAR64	**Parity.** Parity protection bit for AD32 to AD63 and BE4 to BE7
M66EN	**66 MHz Operation.** Connected to GND for 33 MHz operation or left unconnected for 66 MHz
TCK	**Test Clock.** Clock for the PMC JTAG
TMS	**Test Mode Select.** Select Test Mode for PMC JTAG
TRST~	**Test Reset.** Reset any PMC JTAG devices
TDI	**Test Data In.** Input data for PMC JTAG chain
TDO	**Test Data Out.** Data from a PMC JTAG chain
3.3V	These pins are not connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on P0 and P1, and capacitively decoupled to ground
VIO	The supply rail for the I/O voltage for the PCI bus. For I/O signalling only, ***not*** main supply

J14 I/O Connector

J14 is routed to P0.

Pin	Signal	Pin	Signal
1	PMC1_IO_1	2	PMC1_IO_2
3	PMC1_IO_3	4	PMC1_IO_4
5	PMC1_IO_5	6	PMC1_IO_6
7	PMC1_IO_7	8	PMC1_IO_8
9	PMC1_IO_9	10	PMC1_IO_10
11	PMC1_IO_11	12	PMC1_IO_12
13	PMC1_IO_13	14	PMC1_IO_14
15	PMC1_IO_15	16	PMC1_IO_16
17	PMC1_IO_17	18	PMC1_IO_18
19	PMC1_IO_19	20	PMC1_IO_20
21	PMC1_IO_21	22	PMC1_IO_22
23	PMC1_IO_23	24	PMC1_IO_24
25	PMC1_IO_25	26	PMC1_IO_26
27	PMC1_IO_27	28	PMC1_IO_28
29	PMC1_IO_29	30	PMC1_IO_30
31	PMC1_IO_31	32	PMC1_IO_32
33	PMC1_IO_33	34	PMC1_IO_34
35	PMC1_IO_35	36	PMC1_IO_36
37	PMC1_IO_37	38	PMC1_IO_38
39	PMC1_IO_39	40	PMC1_IO_40
41	PMC1_IO_41	42	PMC1_IO_42
43	PMC1_IO_43	44	PMC1_IO_44
45	PMC1_IO_45	46	PMC1_IO_46
47	PMC1_IO_47	48	PMC1_IO_48
49	PMC1_IO_49	50	PMC1_IO_50
51	PMC1_IO_51	52	PMC1_IO_52
53	PMC1_IO_53	54	PMC1_IO_54
55	PMC1_IO_55	56	PMC1_IO_56
57	PMC1_IO_57	58	PMC1_IO_58
59	PMC1_IO_59	60	PMC1_IO_60
61	PMC1_IO_61	62	PMC1_IO_62
63	PMC1_IO_63	64	PMC1_IO_64

J24 PMC I/O and Full P2 Option Pinout

J24 may be fully routed to the P2 connector, depending on the build option (see the Ordering Information section in Appendix A). If used, then COM3 and COM4 are no longer routed to P2. P2 now looks like:

J24 Pin Number	PMC Signal	P2 Connection	Original Signal	J24 Pin Number	PMC Signal	P2 Connection	Original Signal
1	PMC2_IO_1	D1	COM3_TXD_A	2	PMC2_IO_2	Z1	FLASH_WREN~
3	PMC2_IO_3	D2	COM3_TXD_B	4	PMC2_IO_4	D3	COM3_RXD_A
5	PMC2_IO_5	Z3	EXRESET~	6	PMC2_IO_6	D4	COM3_RXD_B
7	PMC2_IO_7	D5	COM3_RTS_A	8	PMC2_IO_8	Z5	EXABORT~
9	PMC2_IO_9	D6	COM3_RTS_B	10	PMC2_IO_10	D7	COM3_CTS_A
11	PMC2_IO_11	Z7	SWAPFLASH~	12	PMC2_IO_12	D8	COM3_CTS_B
13	PMC2_IO_13	D9	COM3_DSR_A	14	PMC2_IO_14	Z9	COM4_TXD_A
15	PMC2_IO_15	D10	COM3_DSR_B	16	PMC2_IO_16	D11	COM3_DCD_A
17	PMC2_IO_17	Z11	COM4_TXD_B	18	PMC2_IO_18	D12	COM3_DCD_B
19	PMC2_IO_19	D13	COM3_DTR_A	20	PMC2_IO_20	Z13	COM4_RXD_A
21	PMC2_IO_21	D14	COM3_DTR_B	22	PMC2_IO_22	D15	COM3_TT_A
23	PMC2_IO_23	Z15	COM4_RXD_B	24	PMC2_IO_24	D16	COM3_TT_B
25	PMC2_IO_25	D17	COM3_ST_A	26	PMC2_IO_26	Z17	COM4_CTS_A
27	PMC2_IO_27	D18	COM3_ST_B	28	PMC2_IO_28	D19	COM3_RT_A
29	PMC2_IO_29	Z19	COM4_CTS_B	30	PMC2_IO_30	D20	COM3_RT_B
31	PMC2_IO_31	D21	COM4_RTS_A	32	PMC2_IO_32	Z21	COM4_DCD_A
33	PMC2_IO_33	D22	COM4_RTS_B	34	PMC2_IO_34	D23	COM4_DSR_A
35	PMC2_IO_35	Z23	COM4_DCD_B	36	PMC2_IO_36	D24	COM4_DSR_B
37	PMC2_IO_37	D25	COM4_DTR_A	38	PMC2_IO_38	Z25	COM4_ST_A
39	PMC2_IO_39	D26	COM4_DTR_B	40	PMC2_IO_40	D27	COM4_TT_A
41	PMC2_IO_41	Z27	COM4_ST_B	42	PMC2_IO_42	D28	COM4_TT_B
43	PMC2_IO_43	D29	COM1_DSR	44	PMC2_IO_44	Z29	COM4_RT_A
45	PMC2_IO_45	D30	COM1_RI	46	PMC2_IO_46	Z31	COM4_RT_B
47	PMC2_IO_47	NC		48	PMC2_IO_48	NC	
49	PMC2_IO_49	NC		50	PMC2_IO_50	NC	
51	PMC2_IO_51	NC		52	PMC2_IO_52	NC	
53	PMC2_IO_53	NC		54	PMC2_IO_54	NC	
55	PMC2_IO_55	NC		56	PMC2_IO_56	NC	
57	PMC2_IO_57	NC		58	PMC2_IO_58	NC	
59	PMC2_IO_59	NC		60	PMC2_IO_60	NC	
61	PMC2_IO_61	NC		62	PMC2_IO_62	NC	
63	PMC2_IO_63	NC		64	PMC2_IO_64	NC	

P0 Connector Pinout

P0 is routed to J14.

Note: Due to the large amount of I/O required to be handled by the PPC4B, the Type B (95-way) connector shown below is preferred to the Type A (80-pin), and is fitted by default if no particular type is specified. Type A (80-way) connectors use rows 9, 10 and 11 for keying.

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	TCK	REDLED~	EXTRESET~	TDO	TRST~	GND
2	FLASH_WREN~	GREENLED~	EXTABORT~	TMS	TDI	GND
3	3.3V†	3.3V†	3.3V†	+5V	+5V	GND
4	PMC1_IO_5	PMC1_IO_4	PMC1_IO_3	PMC1_IO_2	PMC1_IO_1	GND
5	PMC1_IO_10	PMC1_IO_9	PMC1_IO_8	PMC1_IO_7	PMC1_IO_6	GND
6	PMC1_IO_15	PMC1_IO_14	PMC1_IO_13	PMC1_IO_12	PMC1_IO_11	GND
7	PMC1_IO_20	PMC1_IO_19	PMC1_IO_18	PMC1_IO_17	PMC1_IO_16	GND
8	PMC1_IO_25	PMC1_IO_24	PMC1_IO_23	PMC1_IO_22	PMC1_IO_21	GND
9						GND
10						GND
11						GND
12	PMC1_IO_30	PMC1_IO_29	PMC1_IO_28	PMC1_IO_27	PMC1_IO_26	GND
13	PMC1_IO_35	PMC1_IO_34	PMC1_IO_33	PMC1_IO_32	PMC1_IO_31	GND
14	PMC1_IO_40	PMC1_IO_39	PMC1_IO_38	PMC1_IO_37	PMC1_IO_36	GND
15	PMC1_IO_45	PMC1_IO_44	PMC1_IO_43	PMC1_IO_42	PMC1_IO_41	GND
16	PMC1_IO_50	PMC1_IO_49	PMC1_IO_48	PMC1_IO_47	PMC1_IO_46	GND
17	PMC1_IO_55	PMC1_IO_54	PMC1_IO_53	PMC1_IO_52	PMC1_IO_51	GND
18	PMC1_IO_60	PMC1_IO_59	PMC1_IO_58	PMC1_IO_57	PMC1_IO_56	GND
19	+5V	PMC1_IO_64	PMC1_IO_63	PMC1_IO_62	PMC1_IO_61	GND

† The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on P1 and the PMC connectors, and capacitively decoupled to ground.

EXTRESET~ generates a Hard Reset and EXTABORT~ generates a Soft Reset. See the System Resets section in Chapter 5 for more details.

REDLED~ and GREENLED~ are driven identically to their respective LEDs except that they each have separate buffers with 220Ω series resistors.

Note: You are recommended not to route analog signals through P0.

P6 JTAG/Debug and RISCWatch Connector Pinout

P6 combines a JTAG connector section (for factory test purposes only) and a RISCWatch connector section. The RISCWatch section allows the connection of software debugging tools that use the processor's JTAG port to control the operation of the processor. P6 has the following pinout:

Pin	Signal	Pin	Signal
1	HRESET~	2	TDI_MAIN
3	TCK	4	TRST~
5	TMS_CPU	6	TMS_107
7	TMS_MAIN	8	TDI_CPU
9	TDO_CPU	10	TDI_107
11	TDO_107	12	BGCPU~
13	TDO_MAIN	14	BRCPU~
15	GND	16	GND
17	TT(1)	18	TT(0)
19	TT(3)	20	TT(2)
21	TBRST~	22	TT(4)
23	GND	24	GND
25	TA~	26	AACK~
27	ARTRY~	28	TEA~
29	TS~	30	DBG~
31	GND	32	EMU~
33	CHECKSTOP~	34	TRST_CPU~
35	HRESET_CPU~	36	SRESET_CPU~
37	HALTED	38	NAND_ON~
39	SEPARATE_CHAINS~	40	+3.3V pull-up

For more information on JTAG, see Chapter 5.

RISCWatch Section Signal Descriptions

Signal	Pin	Description
GND	31	Signal ground
EMU~	32	When connected to GND, creates QACK~ to the processor. This connection should be made with an emulator
CHECKSTOP~	33	Processor Checkstop output
HRESET_CPU~	35	Processor Hard Reset
SRESET_CPU~	36	Processor Soft Reset
TMS_CPU	5	Processor JTAG Test Mode Select
TCK	3	Processor JTAG Test Clock
+3.3V pull-up	40	Power-on status signal to RISCWatch hardware
TRST_CPU~	34	Processor JTAG Test Reset
TDI_CPU	8	Processor JTAG Test Data In
TDO_CPU	9	Processor JTAG Test Data Out
SEPARATE_CHAINS~	39	Allows access to the separate JTAG chains

For more information on JTAG, see Chapter 5.

EST Emulator Connection

An optional interposer board (PPC4EST) for EST Emulator connection is available from Radstone. This interposer board makes connection to an EST emulator easier.

If the interposer board is *not* being used, the following connections between the PPC4B (using the P6 connector) and the EST header need to be made:

EST Pin	P6 Pin	Signal	EST Pin	P6 Pin	Signal
1	9	TDO	2	-	QACK~
3	8	TDI	4	34	TRST~
5	37	QREQ~	6	40	VDD
7	3	TCK	8	-	
9	5	TMS	10	-	
11	36	SRESET~	12	15	GND
13	35	HRESET~	14	-	
15	33	CHECKSTOP~	16	15	GND

The following additional connections also need to be made on P6:

P6 Pin	Signal	Connect To
32	EMU~	GND
39	SPLIT_CHAINS~	GND

Note: The EST does not currently use QACK~. When it does, EMU~ may need to be connected to QACK~ instead of GND.

P7 Additional COM Port Connector Pinout

P7 combines a JTAG connector section, which is for factory purposes only, and a section that contains additional COM1, COM2, external reset and abort connections. For more information on JTAG, see Chapter 5. P7 has the following pinout:

Pin	A	B	C
1	GND	EXTRESET~	COM1_RTS
2	MACH_TMS	GND	COM1_CTS
3	MACH_TCK	EXTABORT~	COM1_RXD
4	MACH_TDI	KBD_5V	COM1_TXD
5	MACH_TDO	COM2_TXD	COM2_RXD

Signal Descriptions

Mnemonic	Description
KBD_5V	Keyboard 5V. Supplies power for the keyboard and mouse. Rated at 300mA†
COM1/2_TXD	COM1/2 Transmit Data
COM1/2_RXD	COM1/2 Receive Data
COM1_RTS	COM1Request-To-Send
COM1_RI	COM1 Ring Indicator
COM1_CTS	COM1 Clear-To-Send
COM1_DTR	COM1 Data Terminal Ready
COM1_DCD	COM1 Data Carrier Detect
COM1_DSR	COM1 Data Set Ready
EXTRESET~	Generates a Hard Reset. See the System Resets section in Chapter 5 for more details
EXTABORT~	Generates a Soft Reset. See the System Resets section in Chapter 5 for more details

Note: These are the same signals as presented at the P2 connector. It is therefore not advisable to connect both the P2 and P7 connection points at the same time.

† This is a resettable fuse. The fuse rating is the current rating that the fuse can carry. At 20°C still air, the fuse trips at twice the rated current.

P9 Floppy Disk Drive Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	Density Select 0
3	GND	4	NC
5	GND	6	Density Select 1
7	GND	8	Index~
9	GND	10	Motor Select 0~
11	GND	12	Drive Select 1~
13	GND	14	Drive Select 0~
15	GND	16	Motor Select 1~
17	GND	18	Direction~
19	GND	20	Step~
21	GND	22	Write Data~
23	GND	24	Write Gate~
25	GND	26	Track 0~
27	GND	28	Write Protect~
29	GND	30	Read Data~
31	GND	32	Head Select~
33	NC	34	Disk Change~

Chapter 7 - Front Panel

This chapter describes the features found on the PPC4B front panel.

Air-cooled Versions

PMC Slots

There are two PMC slots in the front panel. However, if you have not ordered PMCs for the sites, then Radstone will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-Radstone PMC, it must comply with the P1386.1 standard for air-cooled PMCs to ensure that it mates correctly with the PPC4B mechanics. Radstone PMCs comply with the standard.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel should fill the slot and may provide front panel connection to the module. Radstone PMCs are delivered with a full kit of parts for mounting them plus fitting instructions.

LEDs

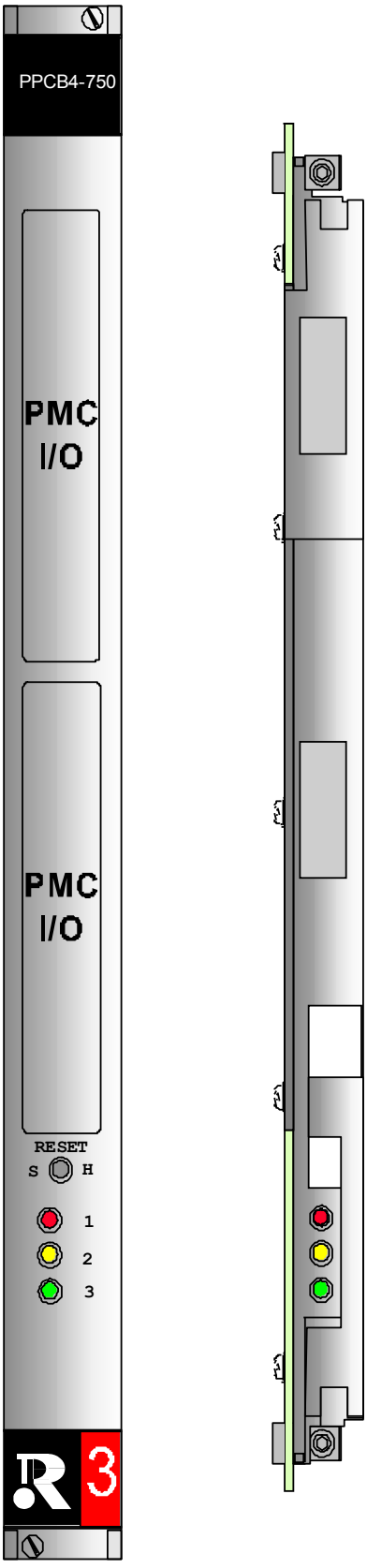
Three software programmable LEDs (DS1 to DS3) are mounted on the front panel. DS1 is red, DS2 is yellow and DS3 is green. See the LEDs section in Chapter 5 for more details.

Switches

A momentary action toggle switch is fitted to allow generation of a hard reset or abort. With the board in the orientation as shown in Figure 7-1, moving the switch to the left causes an abort, and moving the switch to the right causes a hard reset.

The switch may be disabled under hardware or software control. Software control is enabled following power-up. See Chapter 5 for more details.

Figure 7-1. PPC4B Front Panels



Air-cooled
Build levels 1, 2 and 3

Conduction-cooled
Build levels 4 and 5

Conduction-cooled Versions

PMC Slots

There are two conduction-cooled PMC slots in the front panel, allowing limited access to PCI signals.

If you are fitting a non-Radstone PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPC4B mechanics. Radstone PMCs comply with the standard.

LEDs

Three software programmable LEDs (DS1 to DS3) are mounted on the front panel. DS1 is red, DS2 is yellow, and DS3 is green. See the LEDs section in Chapter 5 for more details.

Switches

There are no switches on the conduction-cooled front panel.

Chapter 8 - Technical Assistance

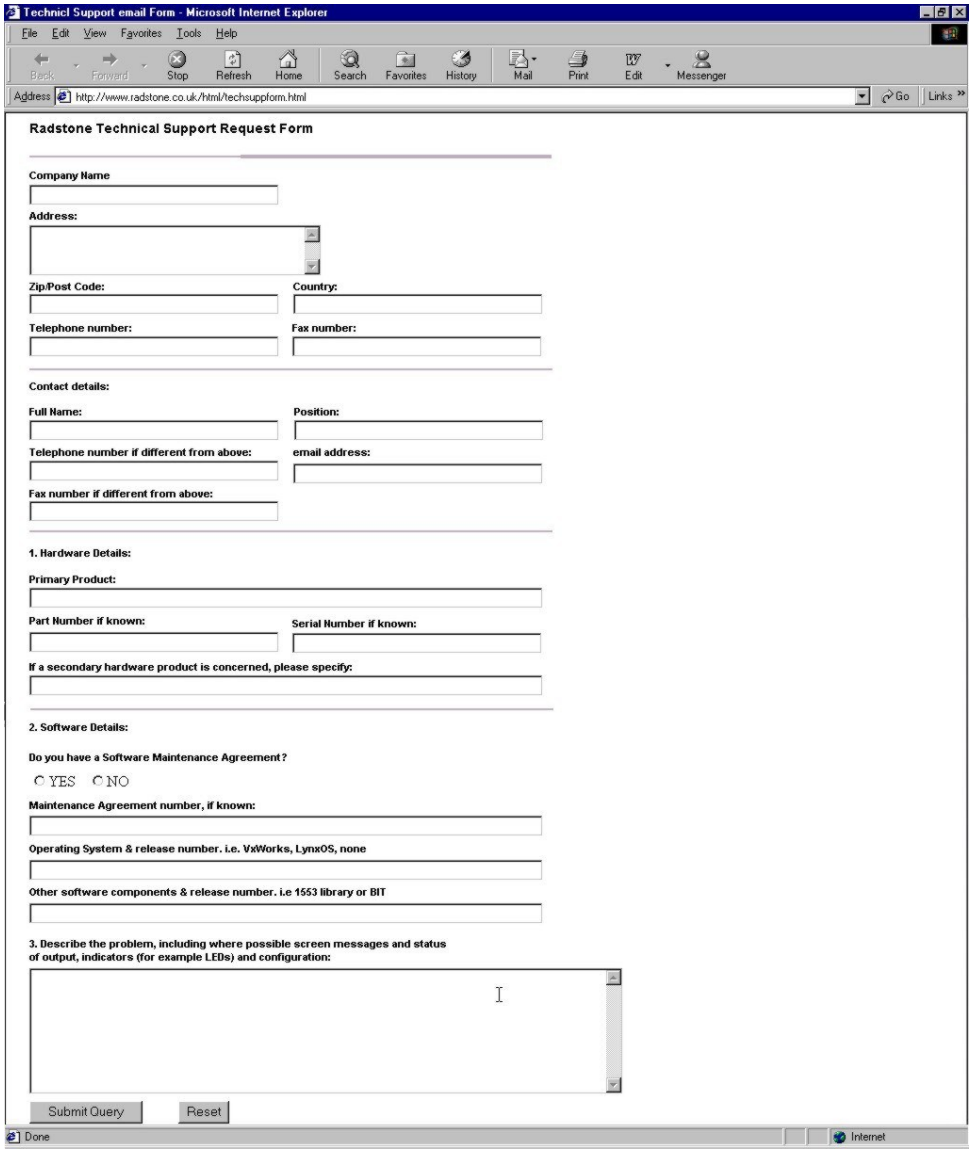
This chapter provides Radstone contact information (including details of information to have available when you call to report a problem) and some helpful hints for troubleshooting your PPC4B.

Radstone Contact Information

Radstone does not anticipate that you will experience problems with your PPC4B. However, in the unlikely event that you do have problems, for assistance please contact Radstone's Technical Help Line on::

+44 1327 359804 outside the UK
01327 359804 in the UK

Alternatively, you may register support requests using the Technical Support Request Form available through the Radstone web site at http://www.radstone.co.uk. This form looks like:



If you telephone for technical support, please be prepared to provide the same information as required above.

Your query will be logged on Radstone's Technical Support database and allocated a unique Call Reference Number (CRN) for use in future correspondence.

Helpful Hints

If you are experiencing a problem with your PPC4B, there follow some general suggestions of actions you may take, which may resolve the problem without the need to contact Radstone's technical support.

- Check that there are no vacant slots in the rack without jumpers (or that an automatic daisy chaining backplane is being used)
- Check that there is only one board configured as system controller in a system and that this is in slot 1 of the rack
- Check that the VME rack has its VMEbus backplane terminators fitted (the manual for your rack should tell you whether the terminators are built in)
- Check that the power supply is within VME limits on the power rails (+5V +5% -2.5%, +12V +5% -2.5%, -12V +5% -2.5%) with a digital volt meter

WARNING
Any problems with the power supply should only be dealt with by qualified personnel.

- Check the board's configuration links. If you are unsure of which link configuration to use, try the configuration suggested in Chapter 4 initially
- If you are using the SCSI bus, then check that the cable stub length is less than 10 cm. You are also recommended to locate the PPC4B at one end and enable the bus terminator by fitting link E11. If you want to use the PPC4B somewhere other than at the end of the SCSI bus, ensure that E11 is not fitted. **Fitting E11 when the PPC4B is not located at the end of a SCSI bus may cause erroneous SCSI operation.**
- Ensure that the board is firmly seated and secured in the rack and that all male/female connectors mate together correctly
- Prove the PPC4B's operation in isolation before adding it into a multi-board system
- If you have made your own cable for connection between P7 and a terminal, check that the pinout is correct
- Check that the terminal/hyperterminal is receiving power, switched on and set up for DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled)
- If your PPC4B is in its default configuration (all links out) when BIT runs, BIT will fail with the following message displayed:

```
PPC60x  (00000000        SELF TEST  ) failed
This card is not a BIT Master. Polling BIT Enable Word
```

This is no cause for alarm. It is due to BIT expecting your PPC4B to be configured as BIT Master. To cure the problem, insert all the Processor ID links (E10, E14, E15, E16) to give a processor ID of 0 (and BIT Mastership) and fit your PPC4B in system slot 1

- Ensure that air-cooled PPC4Bs receive air-flow of at least 300 feet/minute. If you need to operate your PPC4B on an extender card, this requires an additional fan to supply the necessary air flow
- Ensure that conduction cooled PPC4Bs are fully installed in the conduction cooled box and that the wedgelocks are correctly tightened. If, for any reason, you need to operate a conduction cooled PPC4B on an extender card, you must maintain an airflow of at least 300 feet/minute over it

- If you are having problems programming the FLASH, then check that the appropriate write enable link (E5, E6, E8 or E9) is fitted, and that the backplane signal, FLASH_WREN~ (P2 pin Z1 or P0 pin A2) is connected to GND. If FLASH_WREN~ is not connected, then you may try fitting the factory link (E7) as a temporary fix. This link overrides all the normal protection and makes E5/E6/E8/E9 switch the FLASH programming voltage, Vpp, directly. See the FLASH section in Chapter 5 and the E5, E6, E7, E8 and E9 descriptions in Chapter 4 for more details.
- If you are having difficulty booting over the VMEbus, ensure that link E2 is not fitted. See Chapter 4 for more details.

Appendix A - Specifications

This appendix provides the detailed technical specification for the PPC4B. It covers the following items:

- VMEbus compliance
- Local resources
- Power requirements
- EMC regulatory compliance and safety
- Reliability/Mean Time Between Failures
- Environmental specifications for all build levels of both convection- and conduction-cooled boards
- General dimensions
- Weight
- Ordering Information and options

VMEbus Compliance

The PPC4B conforms to the ANSI/VITA 1-1994 standard for VME64.

Master:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Slave:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Interrupt Handler:	D08(O), IH(1-7)
Interrupter:	I(1-7)
VMEbus Arbiter:	SGL, RRS, PRI, BCLR~ generation
VMEbus Requester:	ROR, RWD Early BBSY~ release Bus capture and hold
Bus Time-out Module:	16, 32, 64, 128, 256, 512, 1024 μS, disabled
Other Slot 1 Functions:	Slot 1 detector, IACK~ daisy chain driver, SYSCLK driver
Auto Slot ID:	VME64 specified and SCV64 compatible modes or geographical addressing via 5-row P1 connector

Local Resources

Processor	PowerPC 750 at 266 MHz and above or PowerPC 7400 at 350 MHz and above.
SDRAM	Up to 512 Mbytes with ECC or parity on-board.
L2 Cache	1 Mbyte on PowerPC 750 boards, 2 Mbytes on PowerPC 7400 boards. Private L2 cache bus.
FLASH	64 Mbytes of paged on-board programmable FLASH, 64 bits wide.
Extended FLASH	2 optional banks, each of 64 Mbytes, 64-bits wide.
RTC	Built into Ultra I/O device. RTC backed up by connection to VMEbus 5VSTDBY pin.
NOVRAM	32 Kbyte SRAM device with shadow 32 Kbyte EEPROM providing automatic recall on power-up and software controlled store and recall cycles.
EEPROM	512 Kbytes.
PCI	32-bit, 33 MHz internal bus; 64-bit, 66 MHz PMC bus.
SCSI	8-bit fast Ultra-SCSI via the P2 connector.
Ethernet	Ethernet or IEEE 802.3 (10Base5 or 10/100BaseT) via the P2 connector.
PMC Slots	Air-cooled: Two 5V, 64-bit, 66 MHz IEEE P1386.1 compliant slots with front panel and P0 I/O, and restricted P2 I/O. Conduction-cooled: Two 5V, 64-bit, 66 MHz rugged PMC compliant slots with P0 I/O, restricted P2 I/O and limited front panel I/O.
Serial I/O	Two PC-style COM ports via the P2 connector and restricted access via the P7 connector. Two further COM ports via the P2 connector, configurable at build time as RS232 asynchronous or RS422 synchronous or asynchronous interfaces.
Keyboard and Mouse	PS/2 compatible Keyboard and Mouse interface via the P2 connector.
Parallel I/O	Centronics style port via the P2 connector.
Floppy Disk Interface	MFM 1.44/2.88 Mbyte. On-board 34-way header.
Counter/Timers	Three independent 16-bit counter/timers with a resolution of 333ns. Two timers may be linked to form a 32-bit counter/timer.
Front Panel I/O	PMC I/O for Levels 1 to 3. Levels 4 and 5 have limited front panel I/O for PMCs with the appropriate layout, and connector size and location.
Status LEDs	3 software programmable LEDs (DS1 is red, DS2 is yellow and DS3 is green) front panel mounted on all levels. 5 10/100BaseT Ethernet status LEDs (DS210 to DS214) on the back of the board. 3 10Base5 Ethernet status LEDs (DS216 to DS218) on the back of the board. 1 SCSI Activity LED (DS208) on the back of the board.
Reset switch	Front panel mounted on levels 1 to 3. Not present on levels 4 or 5.
Operating Systems	LynxOS VxWorks/Tornado
PCI Expansion	PCI through P0 using Radstone PPZero technology.

Power Requirements

Main Power

The PPC4B-7400 with 512 Mbytes of SDRAM, 192 Mbytes of FLASH and 2 Mbytes of L2 cache requires 27.9W from the +5V +5%, -2.5% supply.

These figures are based on a 400 MHz MPC7400 running at 375 MHz with an 83 MHz processor bus and a 187 MHz cache bus. The card was running comprehensive tests and gave measured values for +5V supply current of 4.41 A.

The CPU core power, at 1.8V, was measured to be 6.0W. Since the present CPU specification states a maximum of 11.3W, the extra 5.3W has been added to the overall power consumption figure by assuming a 90% conversion efficiency, giving an extra 5.9W on the 5V power. As the current trend for processors is for the core voltage and power consumption to drop with successive generations, the overall PPC4B power consumption will change as the CPU power consumption changes.

The PPC4B does not use the ±12V supply lines, but they do feed the PMC sites.

Although the +12V supply is not used on the board, it does feed through a 1 Amp fuse to P2 pin C7 for the 10Base5 Ethernet transceiver. So although the board does not use +12V, users could take 12V power when a transceiver is connected.

Note: When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded, especially from the +5V supply. The VME specification allows a maximum of 1 Amp to be drawn from each +5V supply pin (9 pins in total) in a single slot over the PPC4B's specified operating temperature range. It may not be possible to support all combinations of SDRAM and PMCs within this limit.

The PPC4B uses the undefined pins (rows a, c, d and z) of the VMEbus P2 connector for I/O and power/ground connections.

WARNING
Do not exceed the maximum rated input voltages or apply reversed bias to the assembly.
If such conditions occur, toxic fumes may be produced due to the destruction of components

Caution
Only use the PPC4B in backplanes that supply power on both the J1 and J2 connectors

Real Time Clock Backup

The RTC backup supply is provided by the VME standby voltage VSTANDBY (5V +5%, -2.5%). Under these conditions, the RTC circuit should draw a maximum of 7µA.

EMC Regulatory Compliance and Safety

Air-cooled versions of PPC4B are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction-cooled versions are designed for integration into EMC hardened cabinets/boxes.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

Mean Time Between Failures

The following table shows some calculated MTBFs for the PPC4B-7400-1A10B:

Environment	Fail Rate (Failures per million hours)	MTBF (Hours)
Ground Benign 30°C	12.24423	81,671
Ground Fixed 40°C	34.75957	28,769
Ground Mobile 45°C	62.7744	15,930
Naval Sheltered 40°C	53.87006	18,563
Naval Unsheltered 45°C	94.6015	10,571
Airborne Inhabited Cargo 55°C	80.80347	12,376
Airborne Inhabited Fighter 55°C	116.5227	8,582
Airborne Uninhabited Cargo 70°C	143.23	6,982
Airborne Uninhabited Fighter 70°C	212.6638	4,702
Airborne Rotary Wing 55°C	139.269	7,179
Space Flight 30°C	11.23655	88,995
Missile Flight 45°C	77.9733	12,825
Missile Launch 55°C	184.8995	5,408

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMCs.

The failure rates used in this calculation are based on MIL-HDBK-217F Notice 1 with commercial or non-military quality level. Where a component did not comply with the MIL-HDBK, the closest equivalent, compliant component was used.

See the Ordering Information section for more details on the meaning of the order code.

Environmental Specifications

Convection-cooled Boards

Build Style	Temperature (°C)	Low Pressure (Feet)	Vibration	Shock	Humidity/ Salt Fog	Comments
Standard (Level 1)	**Operating:** 0 to +55 with airflow of 300 feet/minute. **Storage:** -40 to +85 **Shock**: 10°C/minute over range	**Operating:** 15,000 **Storage:** 50,000	**Random:** 0.002g^2/Hz from 10 to 2000 Hz **Sine:** 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating
Extended Temp (Level 2)	**Operating:** -20 to +65 with airflow of 300 feet/minute **Storage:** -40 to +85 **Shock**: 10°C/minute over range	**Operating:** 15,000 **Storage:** 50,000	**Random:** 0.002g^2/Hz from 10 to 2000 Hz **Sine:** 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterised.
Rugged Air-cooled (Level 3)	**Operating:** -40 to +75 with airflow of 600 feet/minute **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 15,000 **Storage:** 50,000 **Rapid Decompression:** 0 to 50,000	**Random:** 0.04g^2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine:** 5g from 5 to 2000 Hz	20g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.

Conduction-cooled Boards

Build Style	Temperature (°C)	Low Pressure (Feet)	Vibration	Shock	Humidity/ Salt Fog	Comments
Rugged Conduction-cooled (Level 4)	**Operating:** -40 to +75 at the thermal interface **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 70,000 **Storage:** 70,000 **Rapid Decompression:** 0 to 70,000	**Random:** 0.1g^2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine:** 5g from 5 to 2000 Hz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.
Rugged Conduction -cooled (Level 5)	**Operating:** -40 to +85 at the thermal interface **Storage:** -50 to +100 **Shock**: 10°C/minute over range	**Operating:** 70,000 **Storage:** 70,000 **Rapid Decompression:** 0 to 70,000	**Random**: 0.1g^2/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine:** 5g from 5 to 2000 Hz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

Mechanical Construction

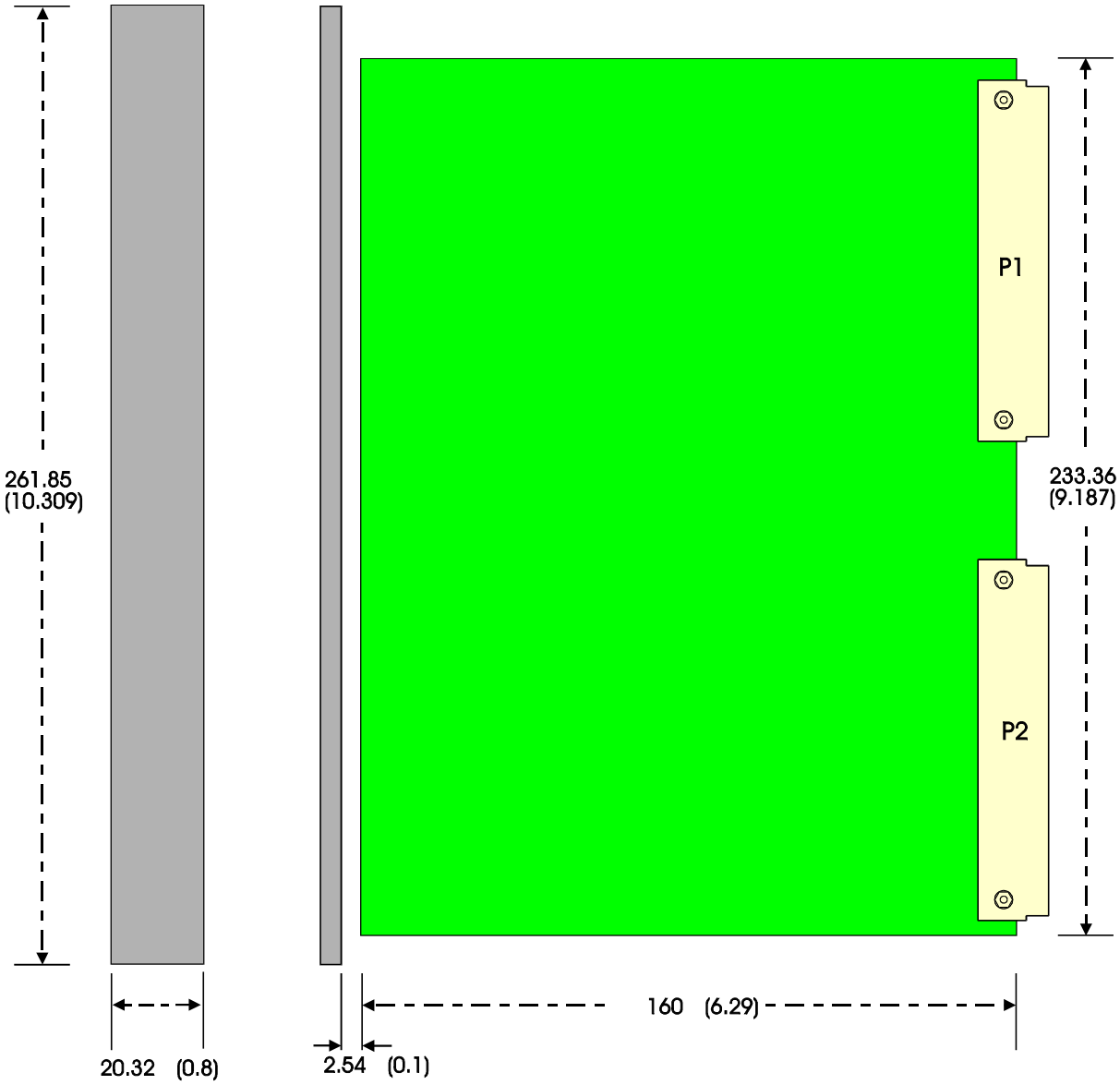
Weight

The approximate weight of the PPC4B is 520g for levels 1 to 3 and 550g for level 4.

Dimensions

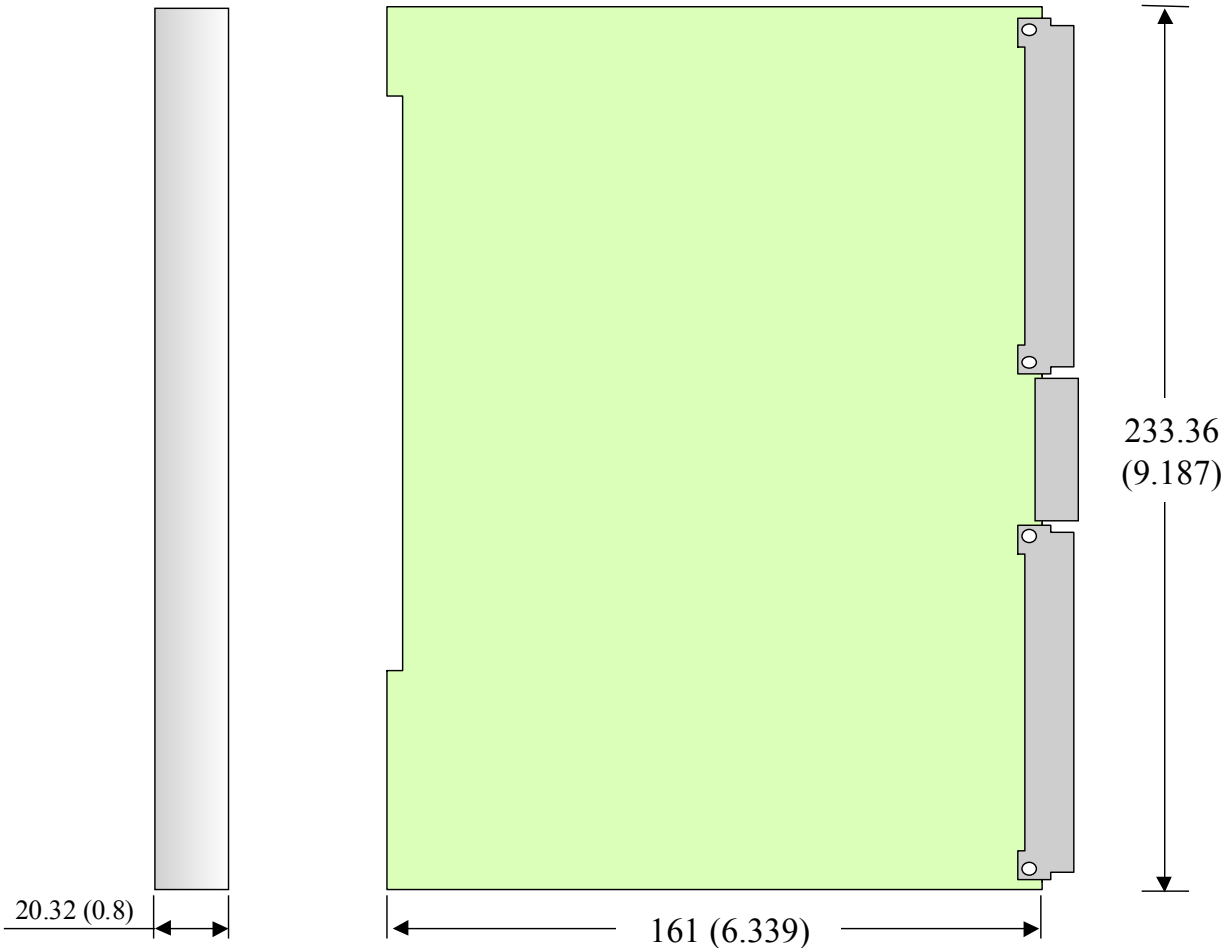
Air-cooled Board

The air-cooled PPC4B is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.



Conduction-cooled Boards

The Conduction-cooled PPC4B is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. The dimensions shown below are in millimetres, with inches (in parentheses) for general guidance only.



Ordering Information

The order code is specified as **PPC4B-750-abcdefg** or **PPC4B-7400-abcdefg**, where 750 and 7400 refer to the corresponding PowerPC processor, and **abcdefg** are explained in the following table:

a (Build Level)	b (Processor, Frequency)	c (SDRAM)	d (Extended FLASH)	e (Ethernet, COM3/COM4 and PMC I/O Configuration)	f (P0)	g (Software)
1, 2, 3, 4 or 5	4 = 750 @ 500 MHz	1 = 128 Mbytes	0 = None	A = 10Base5/RS422/None	0 = No P0	1 = SilverChip
	A = 7400 @ 400 MHz	2 = 256 Mbytes	1 = 64 Mbytes	B = 10/100BaseT/RS422/None	A = Type A	2 = BIT + SilverChip
		3 = 512 Mbytes	2 = 128 Mbytes	C = 10Base5/RS232/None	B = Type B	3 = VxWorks
				D = 10/100BaseT/RS232/None		4 = BIT + VxWorks
				E = 10Base5/None/Full		
				F = 10/100BaseT/None/Full		

All other items, such as 64 Mbytes of paged FLASH, 512 Kbytes of EEPROM, Ultra-SCSI interface, Mouse/Keyboard interface, Floppy interface, Parallel interface, 2 x RS232 ports, 2 PMC slots, 5-row P1 and P2 connectors, are standard. 1 Mbyte of L2 cache is fitted as standard on PowerPC 750 boards, and 2 Mbytes is fitted on PowerPC 7400 boards.

Operating Systems

Standard availability includes:

- VxWorks/Tornado BSP and ESP
- LynxOS BSP and ESP

Please contact Radstone for more details of these or availability of other operating systems.

I/O Modules (3U)

For use with chassis, Radstone offers backplane transition modules to convert the condensed P2 and P0 pinouts to industry-standard formats, plus 3U breakout panels offering a variety of industry standard connectors such as SCSI, Serial I/O, parallel, mouse, keyboard, 10Base2, 10Base5, Ethernet and 10/100BaseT. Internal cables and a basic set of external cables are available. These transition and I/O modules are intended for development use in a benign environment, and so are only available in level 1 or 2 build standards.

For more details see the I/O Module Installation Guide, publication number RT5154.

Glossary

Notes

1) The VMEbus signals are explained in chapter 6.

2) This glossary only features terms special to this manual. Explanations of more general terms can be found in the Radstone Glossary, publication number RT5116.

CR/CSR

Configuration ROM/Control and Status Register.

PPC4B

Radstone's single board computer that can be based on the PowerPC 750 or PowerPC 7400 processor, both with integral L2 cache controller. The PPC4B can provide up to 512 Mbytes of SDRAM and up to 192 Mbytes of FLASH on-board.

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