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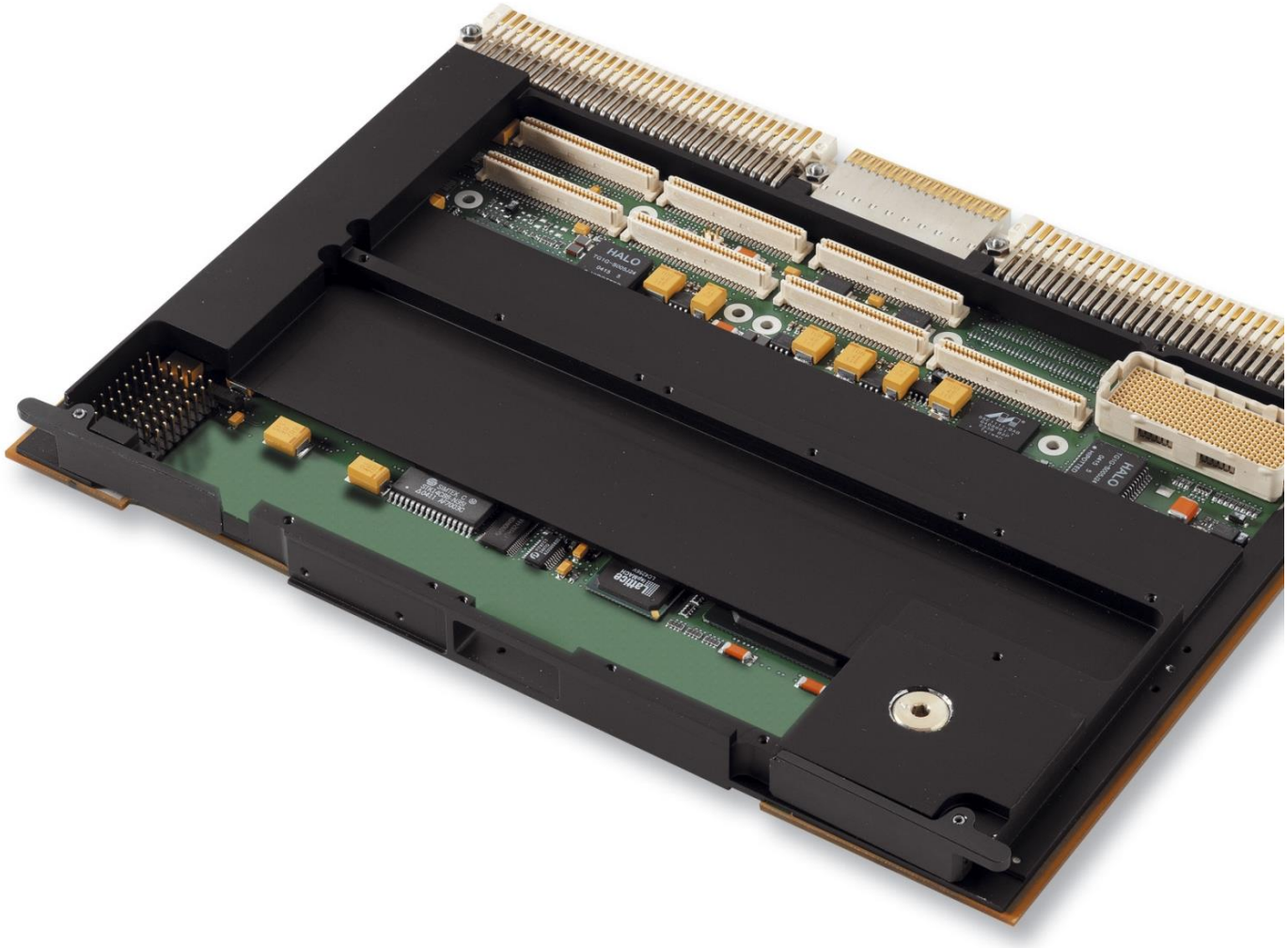
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Hardware Reference Manual

PPC7D 6U VME Single Board Computer

Publication No. PPC7D-0HH Rev. A



abaco SYSTEMS

Document History

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Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems Ltd. is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

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Preface

This manual contains hardware details for PPC7D single board computers. The information contained in this document must be used in conjunction with PowerX Quick Start, PowerX User Guides and/or the PowerX product Manual.



LINK

PowerX Quick Start Guide, publication number RT5142

PowerX Range Hardware Reference Manual, publication PPC-0HH

PowerX User Guide (VxWorks Edition), publication number RT5138

PowerX User Guide (Tornado/Platforms/VxWorks Edition), publication number PXBSP-PTR-0HU

PowerX User Guide (Workbench/Platforms/VxWorks Edition), publication number PXBSP-WBV-0HU

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1 • Link Settings

This section describes the configuration of links on the PPC7D. The board is delivered with push-on jumper links, but for more rugged or military applications, link pins must be connected using wire wraps.

NOTE

Some Link functions change between different artwork versions. Read 'Board Revision Register' register offset 0x854 to find artwork version

Figure 1-1 Link Locations

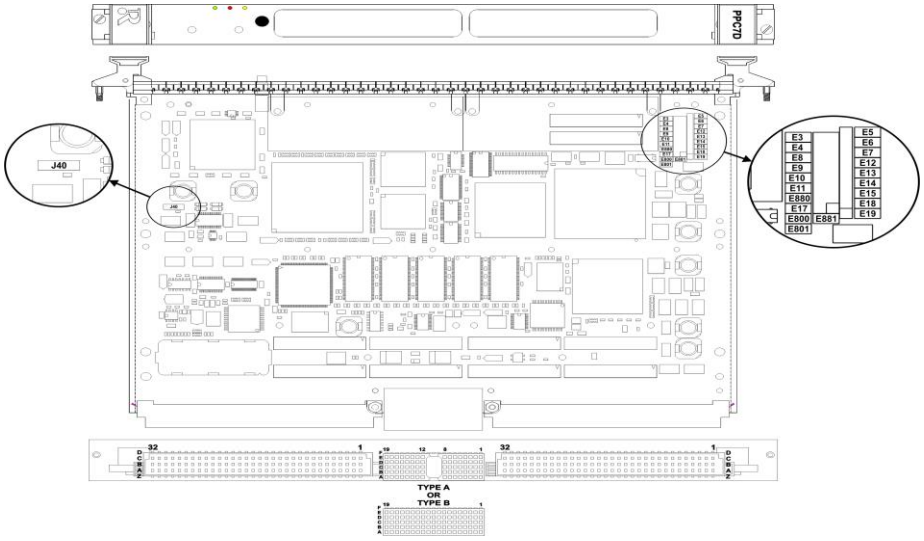


Table 1-1 Factory Default Link Settings

Link	Setting	Function	Link	Setting	Function
E3	Out	Select main Boot Image	E17	Out	ECC Disabled
E4	Out	Select main Boot Image	E18	Out	PMC 1 VIO is 3.3V/Auto
E5	Out	Standby supply voltage is 5V	E19	Out	PMC 2 VIO is 3.3V/Auto
E8	Out	Boot from System Flash	E6, E7, E12,E13	Out	ID links (board ID = 15)
E9	Out	Flash Write Protected or Password disabled	E800	Out	See AFIX manual
E10	Out	System Flash Write Protected	E801	Out	See AFIX manual
E11	Out	User Flash Write Protected	E880‡	Out	Non-Volatile Memory Protection – artwork 4 onwards
E14	Out	Contiguous JTAG chain	E881	Out	Geographical links disabled – artwork 4 onwards
E15	Out	Reset Switch enable	J40	Out	Normal Flash operation – artwork 4 onwards
E16	Out	Flash lock-down blocks cannot be unlocked by software – prior to artwork 4			

TIP

Before changing any of these link options, refer to the following sections.

If you are about to install your board and power up for the first time, leaving your board in the default configuration (as above), will enable board operation to be proved prior to tackling any configuration issues.

NOTE

‡ Prior to artwork 4, Link E880 is called E16.

1.1 PMC VIO Voltage Select links (E18 & E19)

This link selects the voltage of the VIO supply for the PMC site (each site is independent); E18 for PMC1 & E19 for PMC2.

Normal operation is no link fitted, which selects 3.3V operation; however, if a PMC card is fitted that connects the +5V rail to the VIO supply, the PPC7D will detect this and inhibit the supply of 3.3V to the VIO rail. This protects both PPC7D and the PMC card from damage.

If a PMC is fitted that requires VIO at +5V, and if the PMC tracking doesn't link the VIO supply to +5V, then the links need to be fitted to force the VIO to +5V.



NOTE

When the VIO is at +5V (either auto mode or forced mode) the PMC clock will be limited to 33 MHz.

Table 1-2 PMC VIO Voltage Select links

Setting	Function
In	+5V VIO
Out (default)	+3.3V / Auto

1.2 RTC Standby Supply Voltage Link (E5)

This link selects the voltage of the standby supply to the I²C RTC (DS1337). As the normal VME standby voltage is 5V, the link should not normally be fitted. However, the PPC7D can be linked to use a backup supply of 3.3V.



NOTE

If the link is fitted the Backup supply should never be allowed to go above 3.5V or damage to the DS1337 device may result.

Table 1-3 RTC Standby Supply Voltage Link

Setting	Function
In	3.3V standby
Out (default)	5V standby

1.3 Overall Flash Write Enable Link (E9) – Prior to artwork 4

This link enables or disables erasure/reprogramming of a both sections of the Flash.

Table 1-4 Overall Flash Write Enable Link

Setting	Function
In	Enable erase/program Flash
Out	Disable erase/program Flash

NOTE

To give more system flexibility, the Flash can also be write enabled by linking pin A2 of the P0 connector to Ground or Z1 of the P2 connector.

1.4 Password Enable Link (E9) – artwork 4 and above

This link enables the Flash protection password to be read from the Flash Password String Register on CS0. This password is used to lock the Flash sector locking (see the Flash section for more information about use of passwords).

Table 1-5 Password Enable Link

Setting	Function
In	Enable password
Out (default)	Password inhibited

NOTE

To give more system flexibility, the Flash password can also be enabled by linking pin A2 of the P0 connector to Ground or Z1 of the P2 connector.

1.5 Flash Lock-down Link (E16) – prior to artwork 4

This link enables or disables the lock-down function of the Flash devices. Flash blocks can be locked in software; this stops any erasing or reprogramming of the data. Once a block is locked it can only be unlocked if this link is fitted.

Table 1-6 Flash Lock-down Link

Setting	Function
In	Overrides the lock-down function enabling blocks to be erased or programmed through software
Out (default)	Flash blocks that are lock-down can't be unlocked with the unlock command.

1.6 Flash Write Enable Links (E10 and E11)

Each link enables or disables erasure/reprogramming of a section of the Flash. E11 controls the User Flash and E10 controls the System Flash.

Table 1-7 Flash Write Enable Links

Setting	Function
In	Enables erasure/reprogramming of the section of Flash
Out (default)	Disables erasure/reprogramming of the section of Flash

NOTE

Regardless of any link settings for the Flash write protection the Boot Recovery can't be write enabled and also the Boot data area can't be write-protected. See the Functional Description for more details of these Flash areas.

1.7 VME Boot Link (E8)

This link holds the CPU in reset to allow a VME master to program boot code to the Flash devices. To program the boot code into the Flash devices the VME master will need to program up both the Universe II and also the MV64360/64460 to allow a window from VME into the Flash devices.

Table 1-8 VME Boot Link

Setting	Function
In	VME programming mode
Out (default)	Normal boot mode

Use of this link relies on the default Universe II configuration (see the VMEbus Interface Configuration section).

1.8 Flash Boot Image Select Links (E3 & E4)

The System Flash is divided into four sections, with all sections accessible all the time. Using these links, the four sections can be swapped around in the memory map. This allows for two (three if the data area is not required) boot images to be blown into the Flash, a Factory blown Boot recovery image, with the links selecting which image is used at boot time. The state of the links is reflected in the Flash Control Register (Port 0x086E). Normally, these links are not fitted and the PPC7D boots from the default boot area from Flash. However, when either of the links is fitted, the PPC7D boots from another boot image. After boot time, the link setting can be software-overridden to select the different images.

Table 1-9 Flash Boot Image Select Links

E3	E4	Function
Out (default)	Out (default)	Normal Flash boot image operation
Out	In	Alternate Flash boot image
In	Out	Recovery Boot image
In	In	2nd Alternate Flash boot image (Data area)

1.9 Split JTAG chain Link (E14)

This link controls the configuration of the JTAG chain, as follows:

Table 1-10 Split JTAG chain Link

Setting	Function
In	Splits JTAG chain
Out (default)	Contiguous JTAG chain

When the link is removed the JTAG is routed from the VME P1 connector (pins Z1, Z3, Z5, Z7, Z11) to the complete JTAG chain.

When the link is fitted the JTAG chain is split into 3 chains as follows:

- CPLD programming chain routed to the P10 connector
- CPU (RISCWATCH) routed to the P8 connector
- All other JTAG devices to the VME P1 connector

1.10 Enable Front Panel Reset Switch Link (E15)

This link enables or disables the front panel reset/abort switch, as follows:

Table 1-11 Enable Front Panel Reset Switch Link

Setting	Function
In	Disable reset switch
Out (default)	Enable reset switch

1.11 ECC Enable Link (E17)

This link enables or disables ECC on the SDRAM, as follows:

Table 1-12 ECC Enable Link

Setting	Function
In	Enables ECC
Out (default)	Disables ECC

1.12 Geographical Link Enable (E881) – artwork 4 and above

This link enables or disables the geographical address links (E6, E7, E12 and E13). This link determines from which source the geographical address is taken from.

Table 1-13 Geographical Link Enable

Setting	Function
In	Use geographical address set by links
Out (default)	Use geographical address supplied from VME interface

1.13 Geographical Addressing/Board ID Links (E6, E7, E12 and E13)

These links form a 4-bit board ID that may be read from the ID Link register (see the Functional Description section). The links are decoded as follows:

Table 1-14 Geographical Addressing/Board ID Links

Board ID	E13	E12	E7	E6
15 (default)	Out	Out	Out	Out
14	Out	Out	Out	In
13	Out	Out	In	Out
12	Out	Out	In	In
11	Out	In	Out	Out
10	Out	In	Out	In
9	Out	In	In	Out
8	Out	In	In	In
7	In	Out	Out	Out
6	In	Out	Out	In
5	In	Out	In	Out
4	In	Out	In	In
3	In	In	Out	Out
2	In	In	Out	In
1	In	In	In	Out
0	In	In	In	In

Links E6, E7, E12 and E13 are also connected to the VME64 GA0~ to GA3~ signals respectively on P1 row D (see the P1 connector description in the Connectors Section). If you wish to read the status of the Geographical Address signals, do not fit these links, as they connect the signals to 0V.

1.14 VME Slave Address Configuration

The board ID should be set up according to the system slot into which the board is inserted, as shown in the following table. The board ID also sets the board's VME slave addresses, as shown, so take care to avoid an address clash with other boards in the system.

Table 1-15 VME Slave Address Configuration

Slot	Slot 1 Functions	Board ID	A32 Address	A24 Address	
1	Yes	0	0x0000 0000	0x00 0000	
2	No	1	0x1000 0000	0x40 0000	
3	No	2	0x2000 0000	0x80 0000	
4	No	3	0x3000 0000	0xC0 0000	
5	No	4	0x4000 0000	None	
6	No	5	0x5000 0000	None	
7	No	6	0x6000 0000	None	
8	No	7	0x7000 0000	None	
9	No	8	0x8000 0000	None	
10	No	9	0x9000 0000	None	
11	No	A	0xA000 0000	None	
12	No	B	0xB000 0000	None	
13	No	C	0xC000 0000	None	
14	No	D	0xD000 0000	None	
15	No	E	0xE000 0000	None	
16	No	F	0xF000 0000	None	



NOTE

Any change to the Board ID links will require the hardware registers to be 'relearned' if BIT is not to fail.

1.15 VMEbus Interface Configuration

Several operating features of the Universe II VME interface are set at powerup or reset by surface mount jumper links. All of these, except local register access, may be overridden by software. The default settings are:

Table 1-16 VMEbus Interface Configuration (default settings)

Operating Feature	Setting
Register access slave image from vmebus	Enabled in A32 space at 0x8000 0000
VME cr/csr slave image	Disabled
PCI slave image 0	Enabled in PCI memory space at 0xF000 0000 to 0xFFFF FFFF
Local register access	PCI I/O space
Auto-id scheme	Disabled

Changing the default power-up options requires surface-mount rework tools and would normally only be done at the factory. Further details are available from technical support at Abaco.

1.16 AFIXSG SCSI Termination Links (E800 & E801)

These links provide SCSI termination for the AFIXSG module. See the AFIXSG manual for more information on these links.

1.17 Non-Volatile Memory Protect Link (E880) – Artwork REV4 & Above

This link enables or disables writing to the NVRAM and Flash areas.

Table 1-17 Non-Volatile Memory Protect Link

Setting	Function
In	Disables writes
Out (default)	Enables writes

1.18 Flash BANC Write Enable Link (J40) – Artwork REV4 and Above

This link enables erasure/reprogramming of the BANC area of Flash. This link is for factory use and is not intended for customer usage.

Table 1-18 Flash BANC Write Enable Link

Setting	Function
Out (default)	Disables erasure/reprogramming of the section of BANC
Other	Contact factory

2 • Functional Description

2.1 Introduction

The PPC7D is a highly integrated, VMEbus processor using the PowerPC RISC CPU with integrated L2 cache. The product offers an extensive range of standard functions including processors clocked at 1000 MHz and above, DDR SDRAM up to 1024 MB onboard with ECC, onboard serial, parallel, and two channels of 10/100/1000 base Ethernet, up to 256 MB (512 MB artwork 4 and above) of Flash memory, 5 x USB2 interfaces, a 64-bit VMEbus interface, and direct connection for a keyboard and mouse.

Expansion capabilities are provided by two 64-bit at up to 133 MHz PCI-X interface slots. PCI-X is backward compatible with standard PCI (IEEE P1386.1) and provides an industry-standard, high-speed (1024 MB/s) local expansion bus, designed for graphics, high-speed communications (e.g., ATM, FDDI, ISDN, etc.), multi-media and user-defined custom functions. PCI-X has established itself as the leading local interconnect standard, and the wide availability of compatible devices, coupled with its adoption on an array of platforms, ensures that PCI-based modules are both high-performance and low cost.

Expansion capabilities are further extended with the addition of an AFIX module connector. This interface is connected to a 32 bit 33 MHz PCI bus. This interface is designed to allow PCI interfaces to be added without taking up a PMC site.

The highly integrated nature of the PPC7D makes it a true single board computer. In many ways, the PPC7D resembles a high performance PC motherboard, although in a more rugged, lower profile and more compact form factor.

The PPC7D has been designed to be a plug in upgrade/replacement of the PPC range of PowerX boards. To enhance the connection capabilities, the PPC7D uses 5-row P1 and P2 connectors, but still retains the PPC basic pinout.

Figure 2-1 PPC7D General View

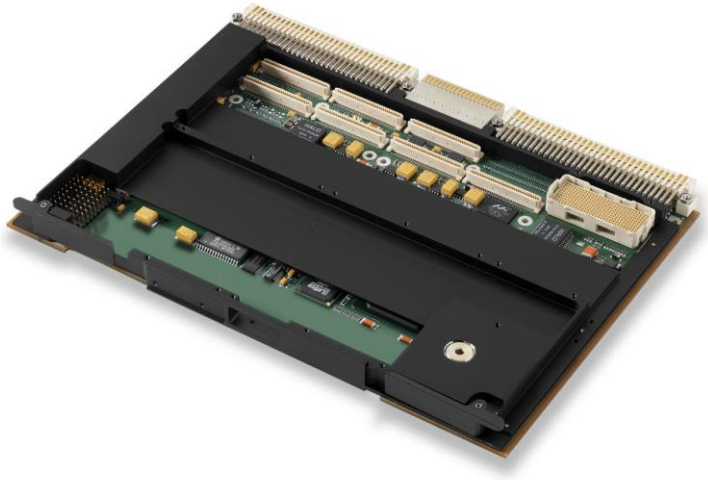
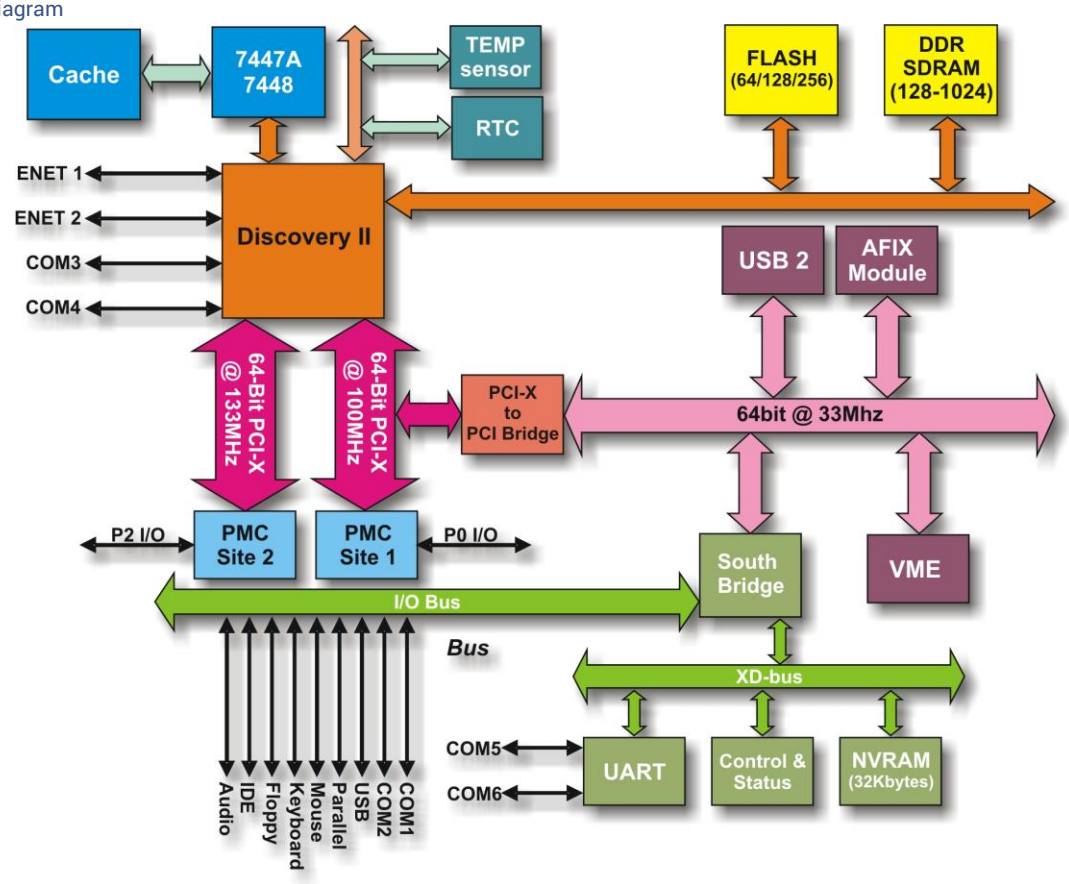


Figure 2-2 PPC7D Block Diagram



NOTES

Due to the increasingly short lifetimes of system components, the I/O devices used on the PPC7D are not guaranteed to remain fixed in the future.

Hardware should be accessed only through mechanisms provided by the Operating System's "Hardware Independence" mechanism (BSP, HAL, residual data, etc.), and not directly by application software.

If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

Abaco supported Operating Systems guarantee compatibility at the application level through the Hardware Independence mechanisms mentioned above.

2.2 PPC7D artwork revision history (major changes)

Artwork rev 1: Prototype only

Artwork rev 2: Changed ALMA 2 VME interface to Universe 2 VME (1st production artwork)

Artwork rev 3: Updated DISCO II (MV64360) to DISCO III (MV64460)

Artwork rev 4: Changed Flash to Spansion, added ETI, 7448 support, Geographical links enabled via ID_LINK enable

NOTE

Read 'Board Revision Register' register offset 0x854 to find artwork version.

2.3 Features

- Various PowerPC processor options including the PowerPC 7447A CPU at 1000 MHz, 7448 CPU at 1400 MHz and above (**contact your nearest Sales office for details of speed grades**) gives low power, low cost, high performance PowerPC RISC CPU and system interfaces all on one device as main system resource
- Marvell DISCO II/III host bridge - MV64360 (MV64460 on artwork 3 and above)
- Up to 1024 MB of DDR SDRAM with optional ECC for memory intensive applications running at 266 MHz and above
- Two 64-bit PMC PCI-X sites (PMC1 at up to 100 MHz & PMC2 at up to 133 MHz) expansion slots onboard give system expansion using IEEE P1386.1 standard single or double width PMCs
- AFIX module expansion with 3.3V/5V 32 bit @ 33 MHz PCI bus
- Optional PCI expansion bridge (on a short PMC card) and PMC carrier cards future proof your system design by enabling PCI sub-system expansion to add new, low cost interface capability as required
- Two onboard Ethernet controllers giving 10/100/1000BaseT
- Abaco COTS software support includes BIT, Boot firmware, BSPs and ESPs (with BCS) for LynxOS/LynxOS HA, VxWorks/Tornado and RTEMS
- Wide range of shrink-wrapped application software available
- 512 MB of Flash ROM (limited to 256 MB prior to artwork 4)
- 32 KB of NOVRAM
- Real Time Clock (TOD/calendar) with battery backup using VME standby supply
- Temperature Sensor (Board and CPU)
- Elapsed time indicator (only on artwork 4 and above)
- 2 off RS232 serial I/O channels up to 150 kbaud (COM1 & COM2)
- 2 off RS485/422/232 software selectable multi-protocol serial I/O channels supporting HDLC, BISYNC, UART & Transparent protocols up to 10 Mbaud in RS485/422 or 150kbaud in RS232 (COM3 & COM4)
- 2 off RS485/RS232 serial I/O channels up to 1.5 Mbaud in RS485/422 or150 kbaud in RS232 (COM5 & COM6)
- 5 off USB 2.0 ports
- Parallel printer port
- 16 bit wide IO interface
- Keyboard/mouse interface
- Floppy disk controller
- VME64 interface using TUNDRA Universe II VMEbus interface chip

- Single slot 6U VME form factor for reduced system cost and slot count
- Range of 3U rear-mounting I/O modules
- ANSI/VITA 1-1994 VME64 and VME64 extensions (5 row P1 and P2) compatible
- Five build standards
- Optional software maintenance giving automatic software revision updates and technical support
- Optional hardware and onboard firmware configuration management service giving a unique part number requiring customer authorisation for changes in product revision status

2.4 PowerPC Platform

The PowerPC Platform is an example implementation of a philosophy designed to allow software compatibility across different platforms based on the PowerPC processor. Aiming to achieve an open standard, the PowerPC Platform encourages the use of industry standard components and buses, and a wide range of operating systems.

As well as providing a detailed hardware design specification, the PowerPC Platform also embodies a software mechanism that allows the hardware to be isolated from the application by abstraction layers. It is these abstraction layers (in effect very low-level system drivers) that are the key to differentiation, scalability and future-proofing. Operating systems, applications and drivers can 'sit' on these layers without needing to be aware of the underlying hardware (other than general functionality). This is fundamentally different from PCs, which use a BIOS that ultimately constrains operating systems and applications alike.

The major purpose of the PowerPC Platform architecture "... is to give direction to system designers, while still enabling differentiation in areas where real value can be added, thus allowing the PowerPC microprocessor industry to build a reusable body of OS and application software...". The knowledge that both OS and application programs will run on any host that complies with the PowerPC Platform architecture provides security for today's valuable software investments, as well as expansion capabilities for the future.

2.4.1 Processor

The PowerPC has become the most widely used of the new generation of RISC processors. Its pedigree is unequalled - jointly developed by world-leading computer companies and backed by long-term commitments from major OEMs.

2.4.2 PowerPC Processor

The PowerPC is a 32-bit superscalar RISC processor, clocked at 1400 MHz and above, with the following features:

- 64-bit external data bus
- On-chip 32 KB instruction and data caches
- On-chip 512 KB of L2 Cache with 7447 or 1 MB with 7448
- Enhanced branch prediction capabilities
- MMU and integral FPU

The PowerPC implements a fully static architecture and offers sophisticated power management capabilities. As a result, its typical power consumption is 9.3 Watts at 1167 MHz.

Table 2-1 PPC Processor Speed

PowerPC CPU	CPU Frequency (MHz)	Dhrystone	MIPS
7447A	1000	2310	2.1
7448	1400	2773	3.2



NOTE

The above estimated values are supplied by Motorola Semiconductor, and illustrate the performance and power dissipation of the CPU. Abaco PowerX SBCs are designed to take the processor, providing a balanced general-purpose platform. The actual performance and power dissipation may vary depending on the application being run and resource usage of the configured system.

2.4.3 MPC7447A

The PPC7D is based around the MPC7447A PowerPC chip. This device contains:

- A 32-bit implementation of the PowerX architecture
- 32 KB, 8-way set associative instruction and data caches
- On chip 512 KB of L2 cache
- The processor has a 36-bit physical address bus and a 64-bit data bus.

Table 2-2 MPC7447A PowerPC

Processor Type	Bus Frequency (MHz)	Core Frequency (MHz)
MPC7447A	133	1000 and above

2.4.4 MPC7448

The PPC7D can alternatively be fitted with the MPC7448 PowerPC chip. This device contains:

- A 32-bit implementation of the PowerX architecture
- 32 KB, 8-way set associative instruction and data caches
- On chip 1 MB of L2 cache

The processor has a 36-bit physical address bus and a 64-bit data bus.

Table 2-3 MPC7448 PowerPC

Processor Type	Bus Frequency (MHz)	Core Frequency (MHz)
MPC7448	133	1400 and above

2.5 Memory

2.5.1 System RAM

Between 128 and 1024 MB of DDR system memory is available. The SDRAM is configured as two banks, with the MV64360/64460 directly controlling both. The MV64360/64460 data protection is by two methods:

- Error Correction Coding - capable of detecting all single bit, double bit and nibble errors, and correcting single bit errors
- Parity - aids the detection of errors, but offers no correction

2.5.2 System Flash

Up to 8 MB of System Flash is provided. This holds initialisation and operating system boot routines. The System Flash is configured as a 32-bit wide device.

2.5.3 User Flash

Between 24 and 504 MB of User Flash may be fitted. The data width is configured as a 32-bit wide device.

2.5.4 NOVRAM

For maintenance of general system parameters, such as boot options, Ethernet addresses and VME configuration, 32 KB of onboard NOVRAM provides a convenient non-volatile storage area.

2.5.5 Controller

The Marvell MV64360/64460 device provides a DDR SDRAM memory controller and a Flash interface.

2.5.6 Maps

The PPC7D supports programmable memory maps. No memory maps are provided in this manual as no memory locations are fixed in hardware. Please refer to the manuals for the software that is installed on the PPC7D for more information.

2.5.7 DDR SDRAM

The following table shows the options available for SDRAM onboard the PPC7D:

Table 2-4 SDRAM Options

SDRAM Size (MB)	Banks	SDRAM Organization
128	1	16M x 16
256	2	16M x 16
256	1	32M x 16
512	2	32M x 16
512	1	64M x 16
1024	2	64M x 16

The SDRAM is protected by eight ECC bits per 64 data bits. All single bit, double bit and nibble errors can be detected, and single bit errors can be corrected.

Following a hard reset, the Marvell MV64360/64460 PCI Bridge/Memory Controller must be set up for the size and number of banks of SDRAM and the appropriate number of wait states to match the SDRAM speed. This is done by the standard Boot firmware. The size of the SDRAM may be checked by reading the Memory Configuration register (see the Control and Status Registers section).

At least 100µs must have elapsed from the negation of reset before enabling the SDRAM. After being enabled, the SDRAM must not be accessed until at least 8 refreshes have occurred. If ECC is to be enabled, then it is necessary to initialize the SDRAM to set up valid ECC bits.

SDRAM access times from the processor, for a 32-byte burst are shown in the table:

Table 2-5 SDRAM Processor Access Speeds

Bus Speed	Clocks Access	Data Transfer Rate
133 MHz (no page hit)	19:1:1:1	193 MB/s
133 MHz (pipelined)	19:1:1:1:12:1:1:1	230 MB/s
133 MHz (pipelined & page hit)	19:1:1:1:2:1:1:1	316 MB/s

SDRAM access times from the PCI, referenced to the 100 MHz PCI clock, for a 512-byte burst with no interference from L1 or L2 caches, are shown in the table:

Table 2-6 SDRAM PCI Access Speeds

Action	Clock Cycles Initial Access/Subsequent	Equivalent Transfer Rate (MB/Second)
Burst Read	88:1.....1	332 MB/s
Burst Write	2:1.....1	711 MB/s

2.5.8 Flash

At artwork 4 the Flash array devices were changed from Intel to Spansion Flash devices. This has made a few changes to the function of the array. This update of devices should become almost in-visible when using the correct software drivers.

The Flash array is divided into two sections; one bank is termed the BOOT Flash and the other is referred to as USER Flash. Both Flash sections are configured as 32 wide and the MV64360/64460 bus burst is supported to allow for maximum bus bandwidth.

Boot Flash

This section is a total of 8 MB in size. The area is broken down into 4 areas, each area being 2 MB in size: Main BOOT, Alternate BOOT, Recovery BOOT and extended BOOT. All areas can be seen (depending on memory map setup) at any time but the areas may be swapped around depending on the boot link configuration and/or Flash control register setup.

The Flash has a write capacity of 100,000 cycles per block (128 KB block size) and the software should write to the Flash as 32-bits.

NOTES

Integrity of Flash data cannot be guaranteed if a hard reset occurs during a Flash write cycle.

Instead of fitting the link E5 (Overall Flash Write Enable), the signal (Flash_WREN~) is available on P0 pin A2 (if fitted and NO dual 10/100/1000 Ethernet) or P2 pin Z1 (if J24 option is not fitted). Pulling this signal low is the same as fitting the link.

Main BOOT

This area is used as the main default boot area of the PPC7D. This area would be the area that the user would put the default boot firmware. This area is selected for booting by not fitting E4 (BOOT_ALTERNATE) and E3 (BOOT_RECOVERY) links.

To write to this area, Links E9 (Overall Flash Write Enable) and E10 (System Flash Write Protected) need to be fitted.

Alternate BOOT

This area would normally contain a backup or alternate boot image. This is useful when developing boot code to be able to switch between two images to check operation. If an alternate boot image is not required, this area can be used to hold User data or for extended boot code. This area is selected for booting from when the link E4 (BOOT_ALTERNATE) is fitted and E3 (BOOT_RECOVERY) not fitted.

To write to this area, Links E9 (Overall Flash Write Enable) and E10 (System Flash Write Protected) need to be fitted.

Recovery BOOT

This area contains a boot image that is designed to recover the boot areas when the main and alternate boot areas have been made so that the PPC7D will not boot from them. This area is selected for booting from by fitting the link E3 (BOOT_RECOVERY~) and E8 (BOOT_ALTERNATE) not fitted.

The recovery image is programmed in the factory. As this area is designed to be able to recover the boot code it has been made so that the user can NOT modify this area. There are no link settings that make this area writeable by the user.

Prior to artwork 4, the recovery image only uses 1 Mbyte of the 2 MB of space, the 1 MB of space that is left over is an area of Flash that is NEVER write protected whatever the write protection links are set to.

Artwork 4 and above, the recovery image is 256 KB and is aliased 8 times in the 2 Mbyte space.

Extended BOOT

This area would normally contain data or extended boot code for the boot firmware. If required, a second alternate boot image can be programmed into this area. This boot image is selected by fitting links E8 (BOOT_ALTERNATE) & E3 (BOOT_RECOVERY).

To write to this area, Links E9 (Overall Flash Write Enable) and E10 (System Flash Write Protected) need to be fitted.

User Flash

This Flash array is for the user to place application code or data. It is a contiguous array of 56, 120, 248 or 504 MB (depends on Flash array size).

To write to this area, links E9 (Overall Flash Write Enable) and E11 (WRITE_ENABLE_USER) need to be fitted.

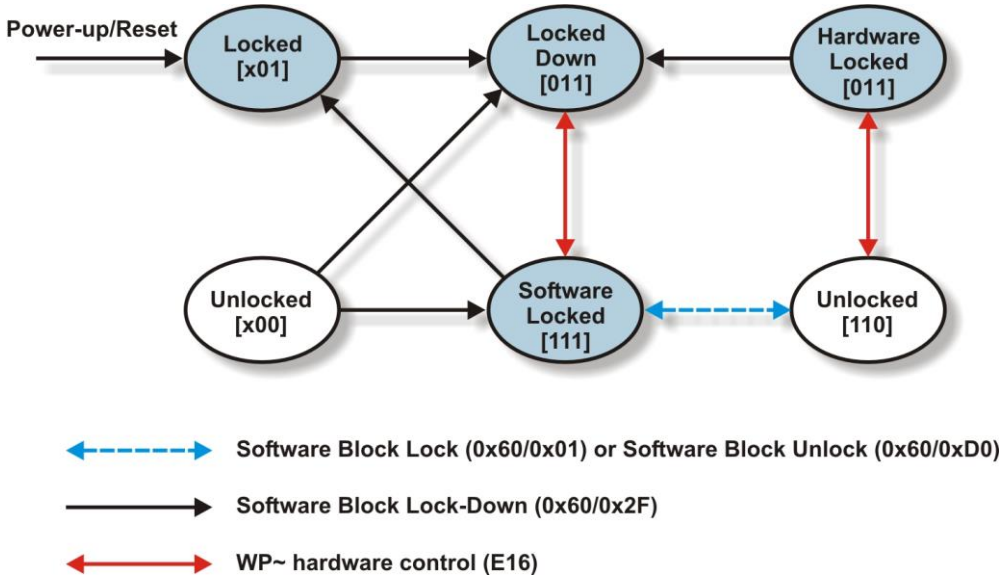
Flash Lockdown – Prior to Artwork 4

In addition to the hardware links provided on the PPC7D to provide write protection of the flash devices, there is a software-controlled block locking provided in the Flash devices.

Individual block locking is used to protect user code and/or data within the flash memory array. All blocks power up locked to protect array data from being altered during power transitions. Locked blocks cannot be programmed or erased; they can only be read.

Software-controlled security is implemented with the Block Lock and Block Unlock commands of the flash devices. (For full information see Intel Flash data sheet)

Figure 2-3 Flash Block Lock/Unlock Operation



NOTES

Binary positions [a,b,c] represent [WP~, D1, D0], x = either '1' or '0'.

D1 indicates block Lock-down status. D1='0', Lock-down has not been issued to this block. D1='1', Lock-down has been issued to this block.

D0 indicates block lock status. D0='0', block is unlocked. D0='1', block is locked.

Locked-down = Hardware + Software locked.

[011] states should be tracked by system software to determine difference between Hardware locked and Locked-Down states.

Fit Link E16 to make WP~ inactive, remove link E16 to make WP~ active

Block Lock

All blocks default to the locked state after initial powerup or reset. An unlocked block can be locked by issuing the Block Lock command sequence. This sets the block lock status bit and fully protects the block from program or erase. Attempted program or erase operations to a locked block will return an error in SR1.

Block Unlock

A locked block can be unlocked by issuing the Block Unlock command. All unlocked blocks return to the locked state when the device is reset or powered down. Unlocked blocks may be programmed or erased.

Block Lock-Down

The Lock-Down Block command adds an additional level of security to the device. Issuing the Lock-Down Block command sets the lock-down status bit and locks the block. The Lock-Down Block command can be used if the block's current state is either locked or unlocked. Once this bit is set, WP~ is enabled (E16 removed) as a hardware lock control for that particular block. If a block is locked-down and WP~ is de-asserted (E16 fitted), the user may issue the Unlock Block command to allow program or erase operations on that block.


NOTE

Only device reset or power down can clear the lock-down status bit.

Flash Lockdown – Artwork 4 and Above

As well as the hardware link Flash write protection, the Flash devices themselves provide a software-controlled block locking mechanism. Individual block locking can be used to protect user code and/or data in the Flash memory array. Locked blocks cannot be programmed or erased; they can only be read.

Certain block locking and unlocking commands need a password to be entered into the Flash devices. This password is contained in logic on the PPC7EP. The Password Enable link (E9) allows software access to the password. The intention behind the password inhibit is to disallow a crashed board access to block unlocking commands. This then inhibits the ability to erase protected Flash data.

Software-controlled security is implemented with the Block Lock and Block Unlock commands of the Flash devices. For full information see the S29GL512N 512 Mb page-mode Flash data sheet at:


LINK

http://www.spansion.com/support/technical_documents/flash_datasheets.html

2.6 PCI Buses

There are three PCI buses on the PPC7D.

PCI-2 is connected to all of the onboard PCI devices and the AFIX module. This bus is implemented as a 64-bit PCI bus running at 33 MHz (64-bit to Universe II device only). This gives a burst rate up to 264 MB/s between PCI agents.

PCI1 is the PCI-X/PCI bus that is routed to the PMC2 site, the CPU Host bridge interface. This bus is implemented as a 64-bit PCI-X/PCI bus running at up to 133 MHz. This gives a burst rate up to 1064 MB/s between PCI agents.

PCI2 is the PCI-X/PCI bus that is routed to the PMC1 site, the PCU Host bridge interface & the HB8 PCI-X to PCI bridge. This bus is implemented as a 64-bit PCI-X/PCI bus running at up to 100 MHz. This gives a burst rate up to 800 MB/s between PCI agents.

The PCI bus structure of the PPC7D is shown in the Block Diagram at the beginning of this section:

2.6.1 Memory/PCI Bridge

The Memory/PCI Bridge on the PPC7D is provided by a Marvell MV64360/64460 Discovery device:

This device provides:

- Host Bridge between the processor bus and the two PCI-X buses
- PCI arbiters
- DDR SDRAM memory controller and Flash interface (see the Memory section)
- 2 off Ethernet 10/100/1000 MACs
- 2 off Serial channels (COMs 3 & 4)

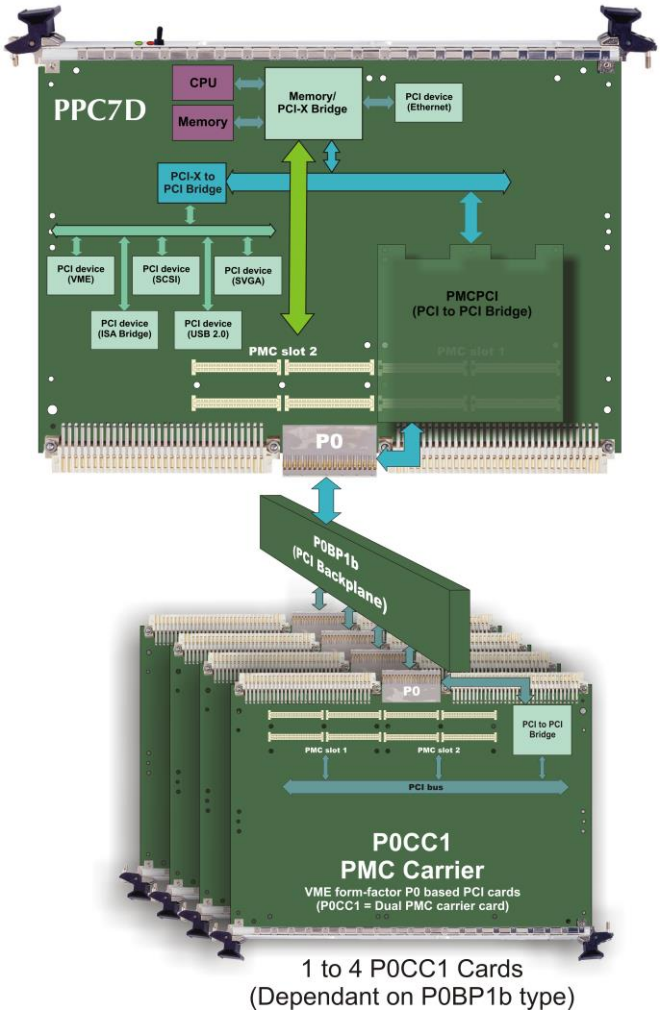
2.7 PCI-X

PCI has become a highly desirable local interface bus, due to its high bandwidth, glueless interface and low cost. PCI provides a synchronous 32 or 64-bit multiplexed address and data bus at speeds of 33 or 66 MHz, allowing burst data transfers to 528 MB/s. PCI-X is an enhanced PCI expansion bus that is backward compatible with the standard PCI bus by provides higher clocking speeds of up to 133 MHz and signalling techniques to provide a higher transfer rates, burst data transfers to 1024 MB/s. The PPC7D uses PCI to provide a high-speed backbone for local interconnection of onboard devices (processor, USB, South bridge and VME64, all of which have direct PCI connectivity). The Universe II chip provides full PCI to VME bridge capability.

As well as local interconnection of onboard devices, PCI-X also allows communication with optional mezzanine expansion modules (PMCs). The PCI-X mezzanine format also provides 64 I/O pins for user definition. A range of PMCs are available from Abaco, including high-performance graphics, MIL-STD-1553, asynchronous serial, Fast Ethernet, Flash memory, Fibre Channel and ATM, all fully compliant with the IEEE P1386.1 standard.

Using the PCI to PCI bridge device on the PMCPCI bridge card (see overleaf), the PPC7D can maintain concurrent bus operation. This allows applications using PMCs for routing and communications to operate efficiently and in parallel without being blocked.

Figure 2-4 PCI Interconnections



To connect the PPC7D to P0-based carrier cards such as the P0CC1, a series of P0 add-on backplanes are available. These are PCBs for attaching to a system backplane that has J0 connectors fitted. The following variants are available:

Table 2-7 P0 Backplane Options

Variant	PCI Backplane Slots	Master Slots	P0cc1 Slots
P0BP1-502	2	1	1
P0BP1-503	3	1	2
P0BP1-504	4	1	3
P0BP1-505	5	1	4

The P0BP1 backplane must be soldered onto the J0 system backplane, and can be used with either type A or type B J0. These backplanes are intended to have a host SBC with PMCPCI card plugged into the master slot, which is the left-most slot of the P0 PCI backplane. For further information about P0 backplanes, please contact Abaco directly or talk to your nearest Sales Office.

2.7.1 PCI Bridge and Memory Controller

The Marvell MV64360/64460 Discovery provides the CPU to Memory-PCI bridge. This interfaces the processor to the SDRAM, Flash and the two PCI-X buses.

2.7.2 PCI Expansion Bus

Two PMC slots are provided as standard on the PPC7D. These PCI-X slots are 64 bits wide and run at up to 133 MHz. During reset the PPC7D performs a negotiation to determine the capabilities of the PMC card fitted. The bus speed (33/66/100 or 133 MHz) and bus format (PCI-X or PCI) is then set to reflect the capabilities of the PMC.

For those configurations requiring additional PCI functionality, the PMC to PCI Bridge card (PMCPCI) bridges the onboard PCI bus out via the P0 connector, allowing use of a range of P0 PMC carriers, or interfacing the PPC7D directly to Abaco's range of SHARC-based DSP boards.

2.7.3 PCI Configuration

The boot process must configure the base address and space type (memory or I/O) of all the PCI attached peripherals. The memory requirements of each PCI device are given in the appropriate device descriptions in this section.

Each PCI device also has several registers located in PCI configuration space, which is accessed by the processor through the MV64360/64460 PCI bridge and memory controller using the CONFIG_ADDR and CONFIG_DATA registers. A full description of PCI configuration can be found in the MV64360/64460 specifications.

The device number mapping for the PCI bus 2 attached to the HB8 is as follows:

Table 2-8 PCI Bus Device Mapping

Device No.	Function
0 to 15	Not implemented
16	AFIX ID1
17	Not implemented
18	South bridge
19	Not implemented
20	Universe II VME controller
21	AFIX ID2
22	AFIX ID3
23	AFIX ID4
24 to 27	Not implemented
29	USB 2
30	Not implemented

The device number mapping for the PCI-X0 bus is as follows:

Table 2-9 PCI-X0 Bus Device Mapping

Device Number	Function
0 TO 23	Not implemented
24	PMC1A
25	Not implemented
26	PMC1B
27	HB8 Bridge
28 TO 30	Not implemented

The device number mapping for the PCI-X1 bus is as follows:

Table 2-10 PCI-X1 Bus Device Mapping

Device Number	Function
0 TO 22	Not implemented
23	PMC2A
24	Not implemented
25	PMC2B
26 TO 30	Not implemented

2.8 Utility I/O and Auxiliary Function Bus

To take full advantage of low-cost, industry standard components, general purpose I/O and auxiliary functions are implemented through a South bridge bus interface. Facilities provided include:

- Parallel/printer port
- Four PC-compatible serial interfaces
- Floppy disk controller
- Real-time clock
- Keyboard/mouse interface
- USB

2.9 Input/Output

The PPC7D has a wide variety of possible I/O connectivity, including the following ports:

- Ethernet
- Serial
- Mouse/keyboard
- Parallel/printer
- USB

To maximise the flexibility of connecting to these ports, a range of I/O modules are available, attached by a VME P2 transition module. Using rear I/O minimises the effort needed to remove boards from a rack, so improving maintainability and reliability.

2.10 Software Support

Abaco's software strategy for PPC boards allows fully integrated system-level solutions to be realised easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high-level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of the PPCx family, so providing a common look, feel and interface for technology inserts.

Abaco has invested more than 50 man-years of engineering talent into the PowerX architecture so that customers can develop market-leading products using the O/S and development environment best suited to their long-term program requirements.

2.11 Boot Firmware

Developed as an integral part of the Abaco PowerX strategy, the Boot firmware provides a foundation layer to interface between the raw Abaco board hardware, with its highly programmable device setups and flexibility, and the supported Operating Systems, which require a straight-forward booting and device interface model.

The PPC Boot Firmware includes comprehensive configuration facilities, interactive or auto-boot sequencing from a range of device types, automatic PCI resource allocation at initialisation, PCI display/interrogation utilities and other valuable features for system integrators.

Memory or other speed and feature enhancements are seamlessly absorbed by the Boot firmware, giving the same look and feel to the O/S and the user application as the Abaco hardware models advance. This allows the constant use of latest technology in required areas without system impact. Where particular operating systems define the use of alternate boot methods (e.g., VxWorks bootroms), the Boot firmware technology is absorbed into such boot methodology.

2.12 Built-In Test

PPC BIT probes from the lowest level of discrete onboard hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialisation tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

2.13 Background Condition Screening

BCS supplements the BIT initialisation test coverage with further health screening that can co-exist with a standard COTS Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic check-summing, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in Flash in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.

2.14 Resetting the PPC7D

There are two types of reset that may be applied to the PPC7D: 'Hard' and 'Soft'.

2.14.1 Hard Reset

This causes the processor to begin executing code from address 0xFFF0 0100 in the System Flash. By fitting a hardware jumper (E2), the System Flash addresses may be passed to the VME instead of the Flash. In this way, the processor can begin executing code from a VME source.

Table 2-11 Events that May Cause a Hard Reset

Source		Action	Sysreset~ Generation
Hardware Events	Poweron	Hard reset all devices	Yes
	Received SYSRESET~		No
	Watchdog time-out		If System Controller
	Front-panel hard reset		
	P0 (where fitted and NO dual 10/100/1000 Ethernet) hard reset signal (pin C1)		
Software Events	SW_LRST bit	Hard reset excluding VMEbus Interface	No
	VCSR bit		
	SW_SYSRESET bit	Hard reset if System Controller	If System Controller

The SW_LRST, VCSR and SW_SYSRESET bits are located in the Universe II PCI-VME bridge.

The front panel hard reset may be disabled under software control or by fitting hardware jumper E14.



NOTE

Integrity of SDRAM data cannot be guaranteed during hard reset, since the memory controller is reset and SDRAM refresh disabled. Similarly, integrity of Flash or EEPROM data cannot be guaranteed if a hard reset occurs during a Flash or EEPROM write cycle, respectively.

See the SDRAM section for SDRAM initialization requirements following a hard reset.

2.14.2 Soft Reset

This causes the processor to reach a recoverable state and then branch to either 0x0000 0100 or 0xFFF0 0100, depending on the state of the IP bit in the processor's Machine State Register.

Table 2-12 Events that May Cause t Soft Reset

Source	
Hardware Events	Front-panel Soft Reset
	P0 (where fitted and NO dual 10/100/1000 Ethernet) soft reset signal (pin C2)
	P8 (onboard connector) soft reset signal (pin 11)
Software Events	HOT_RESET bit in ISA-bridge

The front panel soft reset switch may be disabled under software control or by fitting hardware jumper E14. The standard boot firmware does not support the use of soft reset.

2.14.3 VMEbus Remote Reset

Another VME master may reset the PPC7D via the Universe II control registers. This causes a hard reset.

2.14.4 Watchdog Reset

If enabled and triggered (via the Watchdog control register), the watchdog will cause a hard reset unless re-triggered (via the Watchdog Trigger Register) every 1.6 seconds.

2.15 JTAG

All of the JTAG chain connections are routed to connector P1 (see the Connectors section for more details).

There are three chains on the PPC7D. One chain is solely for the purpose of programming the CPLD device, which contains various functions, including the main PPC7D ISAbus registers. This device is programmed via JTAG. The second chain is for the CPU to allow debug tools to be used. The third chain is for all the other JTAG devices on the PPC7D, which can include any PMC JTAG devices.

The JTAG signals from P10 connect into the "CPLD" JTAG signals. They have the following terminations:

TCK ⇒ +3.3V via a 4.7 kΩ pull-down resistor

TMS ⇒ +3.3V via a 4.7 kΩ pull-up resistor

TDI ⇒ +3.3V via a 4.7 kΩ pull-down resistor

The JTAG signals from P8 connect into the “CPU” JTAG signals. They have the following terminations:

TCK ⇒ +3.3V via a 1 kΩ pull-down resistor

TMS ⇒ +3.3V via a 10 kΩ pull-up resistor

TDI ⇒ +3.3V via a 1 kΩ pull-down resistor

TRST~ ⇒ +3.3V via a 1 kΩ pull-up resistor

The JTAG signals from P1 connect into the “MAIN” JTAG signals on the PPC7D. They have the following terminations:

TCK ⇒ +5V via a 470Ω pull-down resistor

TMS ⇒ +5V via a 4.7 kΩ pull-up resistor

TDI ⇒ +5V via a 4.7 kΩ pull-up resistor

TRST~ ⇒ +5V via a 1 kΩ pull-up resistor

The chain consists of the following in the order listed (with split JTAG link E14 fitted):

- Universe II
- PMC1
- PMC2
- HB8
- MV64360/64460
- Ethernet PHYs

The chain consists of the following in the order listed (with split JTAG link E14 removed):

- Universe II
- PMC1
- PMC2
- HB8
- MV64360/64460
- CPLDs
- CPU
- Ethernet PHYs

2.15.1 JTAG Clock Frequencies

Different parts in the JTAG chain may have different maximum TCK frequencies. The main chain on the PPC7D has the following clock limitations:

Universe II ⇒ 10 MHz

HB8 ⇒ 10 MHz

MV64360/64460 ⇒ 1 MHz

CPLDs ⇒ 25 MHz

PowerPC 744X ⇒ 33 MHz

Ethernet PHYs ⇒ 25 MHz

The JTAG clock should not exceed the maximum clock frequency of the slowest element in the JTAG chain. Using the data from the above components, the chain clock frequency should not exceed 1 MHz.

2.15.2 JTAG and PMC

The "MAIN" JTAG chain from P1 visits both of the PMC sites. These individually auto-bypass if a PMC is not fitted at the site. To achieve this, the PPC7D has BUSMODE2 to BUSMODE4 wired to 1, 0, 0 respectively. This effectively interrogates the PMC site as to whether it has a PCI compliant card fitted. The response from the PMC is returned on BUSMODE1. If the answer is yes (BUSMODE1 = 0), then the PMC site is included in the JTAG chain. If there is no PMC fitted, then a pull-up resistor on the PPC7D forces BUSMODE1 to 1 and the JTAG is bypassed.



NOTES

The PCI specification (section 2.2.10 on the optional JTAG pins) requires that if a PMC cannot support JTAG, then it must have TDI connected to TDO. This means that the "MAIN" JTAG chain is complete even if there are PMC cards fitted that do *not* support JTAG.

The PMC sites cannot *source* the JTAG since, being part of a chain, they are expected to *receive* the JTAG signals.

2.16 Ethernet Controller

The MV64360/64460 device provides two Ethernet MACs that are capable of 10/100/1000 Base Ethernet. To interface these to the physical interface two Marvell 88E1111 PHY's are used.

The DMA controllers handle data transfers between CPU memory and on-chip memory with the Ethernet Controller arbitrating between DMA channels to minimise underflow or overflow.

Automatic packet deletion on receive (runt packets or after a collision) and packet re-transmission after a collision on transmission are supported. This minimises bus traffic by removing unnecessary accesses to shared memory. The network addresses (Ethernet number) are factory configured.

Connection to the Ethernet controller is via the P2 connector & P0 (see the Connectors section). Twelve associated status LEDs (DS207 to DS218) are mounted on the rear of the board near the Ethernet PHY chips (see the Software Programmable LEDs section). The default functions of these LEDs are TX activity, RX activity status, Duplex, Link 10, Link 100 and Link 1000, but they may be overridden by the software.

2.17 Universe II

This provides the VMEbus Interface. See later.

2.18 Temperature sensing

The PPC7D has a LM92 to measure the board temperature. This can be set up to cause Interrupts on either high or low ranges. It also has an independent output to cause a Machine check on a more extreme temperature.

The PPC7D has a ADT7461 to measure the CPU temperature. This can be set up to cause Interrupts on either high or low ranges. It also has an independent output to cause a Machine check on a more extreme temperature.

Both of these devices are accessed on the I^2C interface from the MV64360/64460. The LM92 is address 0x90, the ADT7461 is address 0x4C.

2.19 I²C interface

There are 3 devices on the I²C interface from the MV64360/64460 and are accessed with the following addresses:

LM92 0x90 (Board temperature sensor)

ADT7461 0x4C (CPU temperature sensor)

DS1337 0xD0 (RTC)

DS1682 0xD6 (ETI) – only on artwork 4 and above

2.20 South Bridge

An ALI-M1535 provides a bridge from the PCI bus to the ISAbus for connection of native I/O devices. This device also provides the following functions:

Table 2-13 South Bridge Functions

Function	Equivalent to Function of
7 channel DMA between ISAbus and PCI bus	Two 83C37s
Timer block	One 82C54
Interrupt controller	Two 8259s
PCI bus arbiter	-

The south bridge positively decodes some I/O cycles on the PCI bus for internal resources. It subtractively decodes and claims all PCI memory and I/O cycles not claimed by other PCI targets, and forwards them to the ISAbus.

Apart from the south bridge, there are no other ISAbus masters in the PPC7D architecture.

2.21 PMC Sites

The PPC7D has two sets of connectors ({J11, J12, J13, J14} and {J21, J22, J23, J24}) that allow standard PMCs to be connected to the PCI bus. The PPC7D can accept either air-cooled or conduction cooled PMCs, as long as adequate cooling is provided. Air-cooled PMCs are defined in the IEEE 1386 Standard. Front panel I/O is fully supported.

The PMC I/O connector are connected to the backplane connectors to allow backplane I/O. J14 (PMC site 1) is connected to P0 and J24 is partially connected to P2.

Fitting a PMCPCI allows the PCI bus to come out to the backplane via P0 (must be fitted in PMC slot 1).

2.22 South Bridge Peripheral Components

The South Bridge, connected to the PCIbus, contains a floppy disk controller, 16-bit digital IO, two serial ports, a parallel port and a keyboard/mouse controller. The IDE interface is not used on the PPC7D.

2.22.1 Floppy Disk Controller

Connection to the FDC is through P2. This interface is only available with the digital IO build option and requires software to direct the FDC to the interface pins. The pinout is given in the Connectors section. The FDC is software compatible with the DP8473, 765A and NS82077.

2.22.2 Serial I/O

The Ultra I/O provides two serial channels (COM1 and COM2) containing FIFOs, software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 500 kbaud (using the 8 MHz clock input), including the MIDI data rate but this is limited to 150 kbaud by the RS232 interface drivers.

Connection to the serial ports is primarily through the P2 connector, although access may be obtained through front panel connectors (depending on options fitted).

2.22.3 Parallel I/O

The parallel port includes extended capabilities conforming to IEEE P1284. Connection to the parallel port is through the P2 connector. This interface is only available on the Parallel port build option.

2.22.4 Keyboard and Mouse Controller

A PS/2 compatible Keyboard and Mouse interface with Phoenix BIOS is integrated into the Ultra I/O. Connections to the mouse and keyboard are through the P2 connector. This interface is not available if the USB build option is fitted.

2.23 VMEbus Interface

The TUNDRA Universe II PCI to VME bridge provides the VMEbus interface. This complies with the VME64 specification and provides:

- All slot 1 (system controller) functions
- Interrupt control
- A DMA controller
- Interprocessor communications
- Block transfer support

The Specifications section details the VMEbus compliance and basic VMEbus performance of the PPC7D.



NOTE

The Universe II does not self-address.

2.23.1 VMEbus Master Access

Five general-purpose, software-programmable PCI slave images are available for access to the VMEbus. All of these can be configured to access VMEbus A32, A24 or A16 address space. An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address. The VME window size can be set to 16/32/64/128/256/512/1024/2048 MB in size.

VMEbus master cycles may be coupled or write posted. Coupled cycles are retried on the PCI bus until the Universe II has ownership of the VMEbus and are not terminated on the PCI bus until all data has been transferred over the VMEbus. Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred

2.23.2 VMEbus Slave Access

Eight general-purpose, software-programmable VMEbus slave images are available. All of these may be defined in VMEbus A32, A24 or A16 space. An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any onboard address. The start address and size of window are programmable.

VMEbus slave accesses to the PPC7D may be coupled, write posted or pre-fetched block read. Coupled slave transfers can only proceed once the slave posted write FIFO is empty. Slave posted write cycles are queued in a FIFO until the PCI bus is available for the data to be transferred

2.23.3 Indivisible Cycles on VME

The Universe II chip may be programmed to generate RMW cycles on the VMEbus. The Universe II chip's VMEbus ownership-bit may be set (VME Request control register) to cause it to acquire and hold ownership of the VMEbus.

2.23.4 VMEbus Arbitration

The Universe II chip's VMEbus arbiter supports PRI and RRS arbitration with BCLR~ generation in priority mode. The VMEbus requester may operate in fair or demand mode and may be configured as RWD or ROR.

2.23.5 VMEbus Master Block Transfers

The Universe II chip's DMA controller may be used to transfer data between the PCI bus and the VMEbus. DMA operations on the two buses are decoupled through a bi-directional FIFO. The DMA controller can generate an interrupt on completion or on encountering an error condition.

2.23.6 VMEbus Slave Block Transfers

The VMEbus slave interface can respond to D32:BLT and D64:MBLT. For VMEbus slave block transfers, the Universe II chip may be programmed to pre-fetch read data, which is queued in a FIFO.

2.23.7 VMEbus Interrupts

If programmed to do so, the Universe II responds to a VMEbus interrupt with a VMEbus interrupt acknowledge cycle. The Universe II captures the status/ID and then raises an interrupt on the PCI bus. No further VMEbus interrupts are handled on that level until the processor reads the status/ID and re-arms the interrupt handler.

The Universe II can be programmed to generate any level of VMEbus interrupt. It can raise an interrupt on the PCI bus when the VMEbus interrupt has been acknowledged.

Seven software interrupts in the Universe II allow an interrupt to be generated on any of the seven VMEbus IRQs.

2.23.8 VME Bus Errors

Assertion of BERR~ during a coupled VMEbus master cycle causes a target-abort (bus error) on the PCI bus. A PCI bus target-abort during a coupled VMEbus slave cycle causes BERR~ on the VMEbus. See the Machine Check Exception section for further details of target abort.

A bus error during posted write transfers raises an interrupt (if enabled) to the processor. Several options are available, including stopping the operation and purging the offending transaction.

A bus error during a DMA operation raises an interrupt and stops the DMA operation on the bus where the error was detected.

2.23.9 VMEbus Retries

The Universe II chip, as a PCI target, retries the PCI master under the following conditions:

- The PCI initiator requests a coupled cycle to the VMEbus whilst the Universe II is not VMEbus master
- The PCI initiator requests a coupled cycle to the VMEbus whilst the posted write FIFO still contains data
- The PCI initiator requests a posted write cycle when the posted write FIFO can accept no more entries

The PPC7D does not support the VMEbus RETRY~ signal.

2.23.10 VME Programming Option – prior to artwork 4

Fitting link E8 allows the PPC7D to have new boot firmware programmed via the VMEbus as a VME bus slave.

This link is intended for factory use only. Normally, if the Boot firmware gets corrupted the Recovery boot option should be used to restore the Boot firmware.

This link holds the onboard processor in reset. This is required when the onboard Flash contents are unknown and new boot firmware is required to be loaded into the Flash from VME.

To load new firmware from VME, the VME master relies on the reset configuration of the Universe II. The register set of the Universe II appears at address 0x8000 0000 on VME in A32 Space, by default. The VME master will use these registers to set up windows onto the PCI bus from VME.

The PCI-X to PCI bridge (HB8) when in VME boot mode is placed into Non-transparent mode, also the PCI-X bus is restricted to PCI mode only. This device needs to be programmed up to allow access from the PCI bus that the Universe II is located on to the PCI-X bus that the MV64360/64460 is located.

The MV64360/64460 will have its register set available at address 0x1400 0000. The PowerPC's boot Flash can be accessed at address 0xFFF0 0000 on PCI. These areas will need mapping onto VME to allow access of the Flash memory

For correct operation of the Flash memory, 0x84AA 613E should be written to the MV64360/64460 registers at offset 0x468 & 0x46C. The Flash memory can now be read or written to. Writes to the Flash memory should always be done as a 32 bit write.

The boot area that can be accessed at 0xFFF0 0000 will depend on the Boot link settings (E3 & E4). Also, the write protection of the boot areas is also controlled by the link settings (E9 & E10).

NOTE

The Recovery boot area cannot be written to by configuration of either the Boot links (E3 & E4) or the write protection links (E9 & E10). The Recovery boot area has been designed to only be programmed in the factory.

Once you have programmed the boot section of the Flash, remove link E8 and carry out a hard reset. Normal booting now occurs from the Flash and both User and Boot sections are accessible again at their normal addresses.

2.23.11 VME Programming Option – artwork 4 and above

VME programming is not supported.

2.23.12 VMEbus Reset Options

Several Universe II chip operating features are set at powerup or reset by surface mount jumpers. See VMEbus Interface Configuration in the Link Settings section for the default options.

2.24 COM3 & COM4

The Marvell disco used on this card supports to two multi-protocol serial controllers (MPSC). Each channel supports HDLC, BISYNC, UART and Transparent protocols. The MPSCs are implemented in hardware which allows for superior performance over a microcoded implementation.

In HDLC mode, the MPSCs perform all framing operations, such as; bit stuffing/stripping, flag generation and part of the data link operations (e.g., address recognition functions). The MPSCs directly support common HDLC protocols including those used by ISDN and frame relay.

The MPSCs operation is based on link list of descriptors in memory. They have dedicated SDMAs that handles the descriptors and transmit/receive data transfer.

The baud rate generators can be programmed up to 55 Mbaud, however the interface devices used limit this down to 10 Mbaud in RS485/422 mode and 150 kbaud in RS232.

The serial channels are clocked at 133⅓ MHz. This gives the following available baud rates:

Table 2-14 133⅓ MHz Serial Channel Speeds

Band Required	Divisor (Decimal)	Divisor (Hex)	Output Baud	Tolerance
300	27778	0x6c82	300	0%
600	13889	0x3641	600	0%
1200	6944	0x1b20	1200	0%
2000	4167	0x1047	2000	0%
2400	3472	0xd90	2400	0%
3600	2314	0x90a	3601	0.03%
4800	1736	0x6c8	4800	0%
7200	1157	0x485	7202	0.03%
9600	868	0x364	9600	0%
14400	579	0x243	14392	0.05%
19200	434	0x1b2	19201	0.005%
38400	217	0xd9	38402	0.005%
57600	147	0x93	56689	1.6%
111000	75	0x4b	111111	0.1%
115200	72	0x48	115740	0.47%
128000	65	0x41	128205	0.16%
150000	56	0x38	148809	0.8%

2.25 COM5 & COM6

An ST16C2550 UART provides two serial channels (COM5 and COM6) containing FIFOs, software compatible with the INS8250N-B, PC16550A and PC16450. The baud rates are programmable from 50 baud up to 1500 kbaud using the 24 MHz clock input (see port 0x870 bit 4) or 750 kbaud using the standard 12 MHz clock.

In RS232 output mode the baud rate is limited to 150 kbaud by the interface buffers.

When the serial channels are clocked at 12 MHz, the following baud rates are available:

Table 2-15 12 MHz Serial Baud Rates

Band Required	Divisor (Decimal)	Divisor (Hex)	Output Baud	Tolerance
300	2500	0x9c4	300	0%
600	1250	0x4e2	600	0%
1200	625	0x271	1200	0%
2000	375	0x177	2000	0%
2400	312	0x138	2403	0.13%
3600	208	0xd0	3605	0.13%
4800	156	0x9c	4807	0.14%
7200	104	0x68	7211	0.15%
9600	78	0x4e	9615	0.15%
14400	52	0x34	14423	0.15%
19200	39	0x27	19230	0.16%
38400	20	0x14	37500	2.4%
57600	13	0xd	57692	0.16%
111000	7	0x7	107142	3.5%
115200	7	0x7	107142	7%
128000	6	0x6	125000	2.3%
150000	5	0x5	150000	0%

Connection to the serial ports is primarily through the P2 connector, although access may be obtained through front panel connectors (depending on options fitted).

2.26 Watchdog Timers

The PPC7D contains a Maxim 706 microprocessor supervisory circuit with a watchdog timer. Once enabled, this timer must be re-triggered every 1.6 seconds or a hard reset results. The trigger control registers is 0x82C and is enabled via Control register 0x828.



NOTE

Once this bit is enabled as an output, software needs to write to the trigger register to keep the board from resetting. Disabling this pin once it has been enabled does not disable the Watchdog.

The MV64360/64460 also contains a watchdog timer. This timer has a programmable timeout interval. The watchdog output pin needs to be enabled in the MV64360/64460 as MPP bit 9 before the watchdog can reset the PPC7D.

2.27 Front Panel Switches and Indicators

2.27.1 Air-cooled Versions

PMC Slots

There are two PMC slots in the front panel. However, if you have not ordered PMCs for the sites then Abaco will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-Abaco PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPC7D mechanics. This will be the case for Abaco PMCs.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel will fill the slot and will usually provide connection to the module. PMCs are delivered with a full kit of parts for mounting them, and the manual for the module normally contains instructions on how to fit the module.

LEDs

Three software programmable LEDs (DS219 to DS221) are mounted such that they can be viewed through the front panel. DS219 is yellow, DS220 is red and DS221 is green. See the Software Programmable LEDs section below for more details.

Switches

A momentary action toggle switch is fitted to allow generation of a hard reset or abort. With the board in the orientation as shown in Figure E.6, moving the switch to the left causes an abort, and moving the switch to the right causes a hard reset.

2.27.2 Conduction-cooled Versions

PMC Slots

There are two conduction-cooled PMC slots in the front panel, allowing limited access for front panel connections. If you are fitting a non-Abaco PMC, it must comply with the standard for rugged, conduction-cooled PMCs to ensure that it mates correctly with the PPC7D mechanics. This will be the case for Abaco PMCs.

LEDs

Three software programmable LEDs (DS219 to DS221) are mounted such that they can be viewed from the front of the card. DS219 is yellow, DS220 is red and DS221 is green. See the Software Programmable LEDs section below for more details.

Switches

There are no switches on the conduction-cooled front panel.

2.28 Software Programmable LEDs

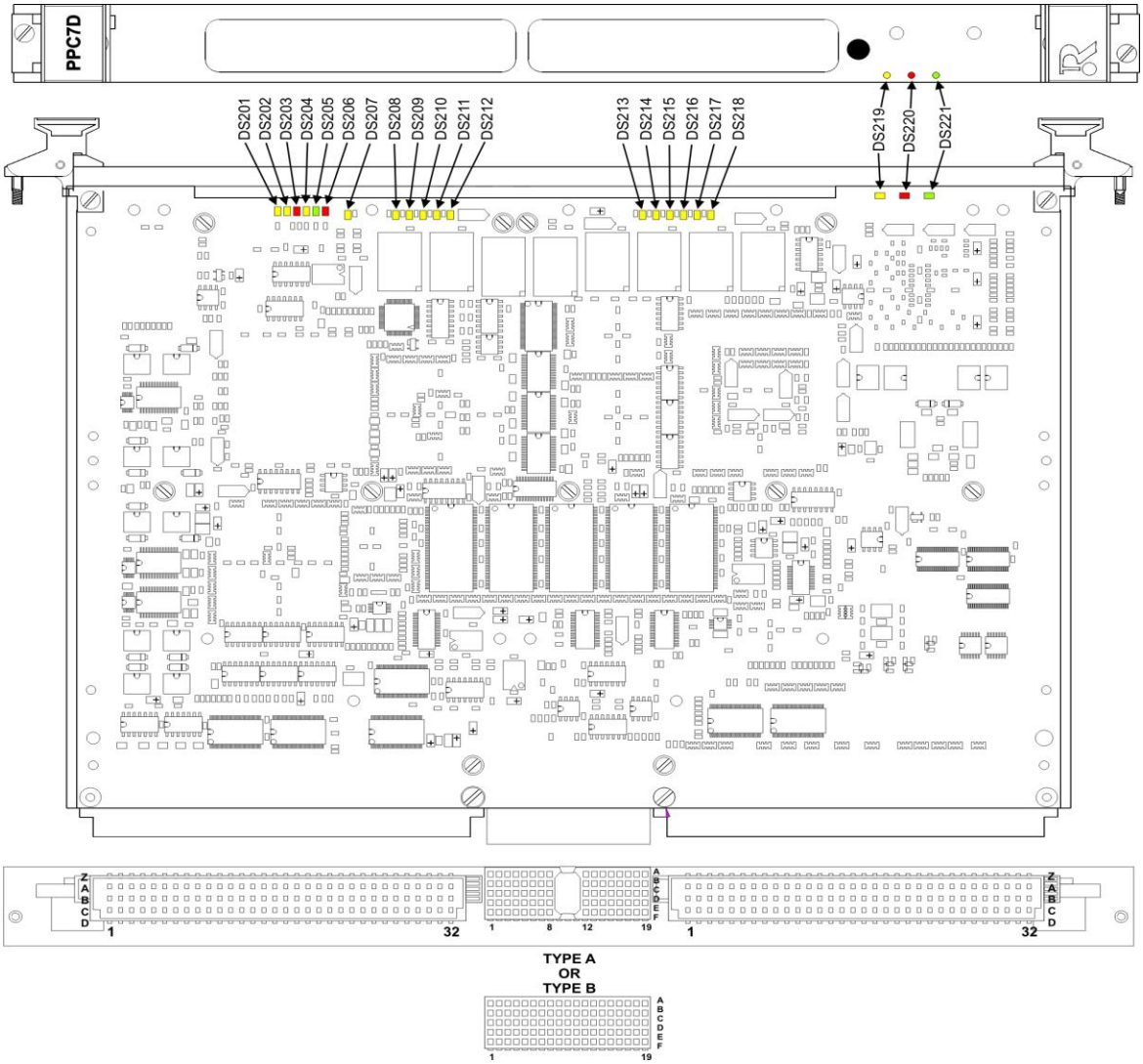
The PPC7D has the following software programmable LEDs:

Control register 0x820 provides four signals, which are connected to four of the LEDs. There is a separate control bit for each LED. Three are visible in the front panel (DS219/220/221) and also on the back of the board as DS203/204/205, together with DS202.

The other LEDs are all surface mounted on the back of the PCB.

DS213, DS214, DS215, DS216, DS217 and DS218 are Ethernet status LEDs for channel 0, and DS207, DS208, DS209, DS210, DS211 and DS212 are for channel 1. The default functions of these LEDs are link, TX activity, RX activity status, Duplex, 1000BaseT, 100BaseT and 10BaseT respectively, but these may be overridden by the software.

Figure 2-5 Position of LEDs



2.29 Control and Status Registers

Table 2-16 Control and Status Registers

ISA I/O Port (Hex)	Description	Row A
0000 to 000F	South Bridge DMA 1 Control	
0020 and 0021	South Bridge Interrupt 1 Control	
0040 to 0043	South Bridge Counter Control	
0060	Keyboard	
0061	South Bridge NMI Status and Control	
0064	Keyboard	
0071 and 0072	RTC	R/W
0078 to 007B	South Bridge BIOS Timer	
0080 to 0090	South Bridge DMA Pages	
00A0 and 00A1	South Bridge Interrupt 2 Control	
00C0 to 00DE	South Bridge DMA 2 Control	
02E8 to 02EF	COM6	R/W
02F8 to 02FF	South Bridge COM2	R/W
03E8 to 03EF	COM5	R/W
03F8 to 03FF	South Bridge COM1	R/W
040A	South Bridge DMA Scatter/Gather	RO
040B	DMA 1 Extended Mode	WO
0410 to 043F	South Bridge DMA Scatter/Gather	
0481 to 048B	South Bridge DMA High Pages	
04D0 and 04D1	South Bridge Edge/Level Control	
04D6	DMA 2 Extended Mode	WO
0804	Memory Configuration	RO
0806	Memory Configuration Extend	RO
0808	SCSI Activity LED	R/W
080C	Equipment Present 1	RO
080E	Equipment Present 2	RO
0810	Equipment Present 3	RO
0812	Equipment Present 4	RO
0818	Key Lock	RO
0820	LEDS	R/W
0824	COMs	R/W
0826	RTS	R/W
0828	Reset	R/W
082C	Watchdog Trig	R/W
082E	Interrupt	R/W
0830	Interrupt Status	RO
0832	PCI configuration	RO
0854	Board Revision	RO
0858	Extended ID	RO
0864	ID Link	RO
0866	Motherboard Type	RO
0868	Flash Write control	RO
086A	Software Flash write protect	R/W
086E	Flash Control	R/W
0870	IO control	R/W
0880	Link geographical	RO

Where: R/W = Read/Write RO = Read Only WO = Write Only

The control and status registers exist on the PPC7D for controlling or reading the status of the hardware. The addresses are as seen by the processor.

Certain registers are described in detail in the following pages. The others are registers in the ISA Bridge or other major devices, which are described in the detail in the appropriate device data sheet (which will also give the appropriate 'Type' column entry).

In the following register descriptions, the bit significance is shown in big-endian mode (i.e., from the viewpoint of the PowerPC 750 programmer).



NOTE

Some register functions change between different artwork versions. Read 'Board Revision Register' register offset 0x854 to find artwork version

2.29.1 Memory Configuration Register (Port 0x0804)

This register provides information on the SDRAM fitted.

MSB = D0, LSB = D7

D0: Memory type

1 = SDRAM

D1: NVRAM type

0 = FRAM
1 = NVSRAM

D2 & D3: CAS latency

Table 2-17 Port 0x0804 (D2 & D3)

D2	D3	Latency
0	0	Reserved
0	1	Reserved
1	0	2.5
1	1	Reserved

D4 & D5: Reserved always read as '0'

D6: SDRAM Bank 1 Fitted

0 = Fitted
1 = Not fitted

D7: SDRAM Bank 0 Fitted, always read as '0'

2.29.2 Memory Configuration Extend Register (Port 0x0806)

This register provides size information for the SDRAM and Flash memory banks.

MSB = D0, LSB = D7

D0 and D1: SDRAM Bank size

0 = 128 MB
1 = 256 MB
2 = 512 MB
3 = 1024 MB

D2 : Reserved

D3: Flash type

1 = K3 Flash fitted (prior to artwork 4)
0 = Spansion Flash fitted (artwork 4 and above)

D4 to D7: Flash banks and size configuration for K3 Flash

Table 2-18 Port 0x0806 K3 Flash (D4 to D7)

D4	D5	D6	D7	Device Size	No. Of Banks	MB
1	1	1	1	64 M bit	1	16
1	0	1	1	64 M bit	2	32
0	1	1	1	64 M bit	3	48
0	0	1	1	64 M bit	4	64
1	1	0	1	128 M bit	1	32
1	0	0	1	128 M bit	2	64
0	1	0	1	128 M bit	3	96
0	0	0	1	128 M bit	4	128
1	1	0	0	256 M bit	1	64
1	0	0	0	256 M bit	2	128
0	1	0	0	256 M bit	3	192
0	0	0	0	256 M bit	4	256
1	1	1	0	Reserved	1	Reserved
1	0	1	0	Reserved	2	Reserved
0	1	1	0	Reserved	3	Reserved
0	0	1	0	Reserved	4	Reserved

D4 to D7: Flash banks and size configuration for Spansion Flash

Table 2-19 Port 0x0806 Spansion Flash (D4 to D7)

D4	D5	D6	D7	Device Size	No. Of Banks	MB
1	1	1	1	Reserved	1	Reserved
1	0	1	1	Reserved	2	Reserved
0	1	1	1	Reserved	3	Reserved
0	0	1	1	Reserved	4	Reserved
1	1	0	1	512 M bit	1	128
1	0	0	1	512 M bit	2	256
0	1	0	1	512 M bit	3	384
0	0	0	1	512 M bit	4	512
1	1	0	0	256 M bit	1	64
1	0	0	0	256 M bit	2	128
0	1	0	0	256 M bit	3	192
0	0	0	0	256 M bit	4	256
1	1	1	0	1 G bit	1	256
1	0	1	0	1 G bit	2	512
0	1	1	0	1 G bit	3	768
0	0	1	0	1 G bit	4	1024

2.29.3 SCSI Activity LED Register (Port 0x0808)

This register allows control of the SCSI activity LED.

MSB = D0, LSB = D7

D0 to D6: Reserved.

D7: SCSI activity LED

0 = LED off
1 = LED on

2.29.4 Equipment Present Register 1 (Port 0x080C)

This register provides information on hardware options and the state of the SCSI Terminator power fuse.

MSB = D0, LSB = D7

D0: Hardware ID0 (see the Motherboard Type Register for details)

D1: Reserved Reads '0'


NOTE

This is a re-settable fuse that re-engages when the overcurrent condition is removed.

D2: PRSNT1_2~

0 = Slot 2 PMC present
1 = Slot 2 empty

D3: PRSNT1_1~

0 = Slot 1 PMC present
1 = Slot 1 empty

D4: AFIX

1 = AFIX module fitted
0 = No AFIX module fitted

D5 to D7: Reserved, always reads '0'

2.29.5 Equipment Present Register 2 (Port 0x080E)

This register provides information on hardware options fitted to the PPC7D.

MSB = D0, LSB = D7

D0: Universe II Fitted

0 = Not fitted
1 = Fitted

D1: Reserved, always reads '0'

D2: COMs 3 to 6 Fitted

0 = Not fitted
1 = Fitted

D3: Gigabit Ethernet Fitted

0 = Not fitted
1 = Fitted

D4: Dual Gigabit Ethernet Fitted

0 = Not fitted
1 = Fitted

Table 2-20 Port 0x080E (D3 & D4)

D3	D4	Ethernet Interfaces Decode
0	0	Dual 10/100 Ethernet from P2
1	0	Single 10/100/1000 Ethernet from P2
0	1	Reserved
1	1	One 10/100/1000 Ethernet from P2 One 10/100/1000 Ethernet from P0

D5 to D7: Reserved, always reads '0'

2.29.6 Equipment Present Register 3 (Port 0x0810)

This register provides information on hardware options fitted to the PPC7D.

MSB = D0, LSB = D7

D0 to D2: Reserved. Always reads '0'

D3: PMC2 IO voltage

0 = 5V
1 = 3.3V

D4: PMC1 IO voltage

0 = 5V
1 = 3.3V

D5: 3.3V PMC power

0 = Powered by onboard power supply
1 = Power from taken from 3.3V pins on VME connectors

D6 & D7: Reserved, always reads '0'

2.29.7 Equipment Present Register 4 (Port 0x0812)

This register provides pinout information on hardware options fitted to the PPC7D.

MSB = D0, LSB = D7

D0: STATUS E801

0 = Link Fitted
1 = Link not Fitted

D1: STATUS E800

0 = Link Fitted
1 = Link not Fitted

D2 to D4: Reserved

D5: ISA IO Fitted

0 = P2 AFIX IO is routed from motherboard resources (NO AFIX option)
1 = No connection to P2 AFIX IO from motherboard resources

D6: PS2 Fitted on P2 muxed USB/PS2 pins

0 = PS2 not routed to P2
1 = PS2 Mouse on P2/A20 & P2/A21 & PS2 Keyboard on P2/A23 & P2/A24

D7: USB2 on P2 muxed USB/PS2 pins

0 = USB2 not routed to P2
1 = USB2 port 1 on P2/A20 & P2/A21, port 2 on P2/A23 & P2/A24

2.29.8 Key Lock Register (Port 0x0818)

This register provides information on the state of the keylock signal. See the Keylock section for more details.

MSB = D0, LSB = D7

D0 to D6: Reserved

D7: Keylock

0 = Keylock signal low
1 = Keylock signal high

2.29.9 LED Register (Port 0x0820)

This register provides control for the 4 user LEDs fitted to the PPC7.

MSB = D0, LSB = D7

D0 & D1: Always reads '0'

D2 & D3: Selects the NVRAM page (each page is 8 KB)

D4: DS201, yellow

0 = LED off, OFFLINE~ High
1 = LED on, OFFLINE~ Low

D5: DS219 and DS204, Yellow

0 = LED on, SYSFAIL~ Low
1 = LED off, SYSFAIL~ High

D6: DS220 and DS203, Red and SYSFAIL~ (P0 B1) signal

0 = LED off
1 = LED on

D7: DS221 and DS205, Green and SYSFAIL~ (P0 B2) signal

0 = LED off
1 = LED on

See the Software Programmable LEDs section for the location of these LEDs.



NOTE

DS12 and DS2 are on by default after powerup.

2.29.10 COMs Register (Port 0x0824)

This register provides control for COMs 3 & 4, for the Clocks and interface configuration.

MSB = D0, LSB = D7

D0: COM3_CLK_EN, this bit enables the TSCLK3 signal out on to COM3_TT (transmit clock)

0 = Disabled
1 = Enabled

D1: TSCLK3_EN, enabled COM3_RT (receive transmit clock) is linked to TSCLK3

0 = Disabled
1 = Enabled

D2: COM3_RS232, selects which interface is used for COM3

0 = RS232
1 = RS422

D3: COM3_TX_EN, when enabled allows all of the COM3 interface buffers.

0 = Disabled
1 = Enabled

D4: COM4_CLK_EN, this bit enables the TSCLK4 signal out on to COM4_TT (transmit clock)

0 = Disabled
1 = Enabled

D5: TSCLK4_EN, enabled COM4_RT (receive transmit clock) is linked to TSCLK4

0 = Disabled
1 = Enabled

D6: COM4_RS232, selects which interface is used for COM4

0 = RS232
1 = RS422

D7: COM4_TX_EN, when enabled allows all of the COM4 interface buffers.

0 = Disabled
1 = Enabled

2.29.11 RTS Register (Port 0x0826)

This register provides options for when the COMs channel data transmitters are enabled. This selection logic only works in RS422 interface mode.

MSB = D0, LSB = D7

D0: Loopback

0 = No loopback
1 = Loopback COMs channels 3,4,5 & 6

D1: COM4_CLK defines MV64360/64460 GPP bit 9 function

0 = Use as PMC site 2 second PCI Bus Request
1 = Use as COM4 SCLK

D2 and D3: COM3 transmitter function select

Table 2-21 Port 0x0826 (D2 & D3)

D3	D2	Transmit Function Selected
0	0	Not enabled
0	1	Enabled
1	0	Enabled by RTS3
1	1	Enabled by RTS3 & stretched

D4: COM5 & 6 RS232, selects which interface is used for COM5 & 6

0 = RS232
1 = RS422

D5: COM5 & 6 Enable

0 = Disabled
1 = Enabled

D6 and D7: COM4 transmitter function select

Table 2-22 Port 0x0826 (D6 & D7)

D7	D6	Transmit Function Selected
0	0	Not enabled
0	1	Enabled
1	0	Enabled by RTS4
1	1	Enabled by RTS4 & stretched

2.29.12 Watchdog Register (Port 0x0828)

This register controls the watchdog resets features of the PPC7D.

MSB = D0, LSB = D7

D0: Last reset was a watchdog

0 = Normal reset
1 = Last board reset was caused by a watchdog timeout

D1 to D5: Reserved – Reads '0'

D6: Watchdog enable

0 = Trig output disabled
1 = Trig output enabled

Once the trig output is enabled the Watchdog trig register (0x082C) needs to be accessed every 1.5 seconds, or a hard reset of the entire PPC7D occurs.

D7: RESET_SW_EN (output)

0 = Disable the front panel reset switch logic.
1 = Enable the front panel reset switch logic.


NOTE

This bit has no effect if the switch logic is not present or if link E14 is fitted.

2.29.13 Watchdog Trig (Port 0x082C)

This is a dummy register that is written to trigger the watchdog.

MSB = D0, LSB = D7

D0 to D7: Don't care for writes, undefined for reads


NOTE

Data written is not used and Reads don't trigger the watchdog.

2.29.14 Interrupt Enable Register (Port 0x082E)

This register controls the enables of the various interrupts.

MSB = D0, LSB = D7

D0: Temperature Interrupt

0 = Disabled
1 = Enabled to INTF of ISA bridge

D1: HB8 Bridge Interrupt

0 = Disabled
1 = Enabled to INTF of ISA bridge

D2: PHY 1 Interrupt

0 = Disabled
1 = Enabled to INTF of ISA bridge

D3: PHY 0 Interrupt

0 = Disabled
1 = Enabled to INTF of ISA bridge

D4: ETI Interrupt (prior to artwork 4 bit reads '0' and writes are don't care)

0 = Disabled
1 = Enabled to INTF of ISA bridge

D5: Reserved – Reads '0'

D6: Temperature Critical interrupt

0 = Disabled
1 = Enabled to MCP input of CPU

D7: Reserved – Reads '0'

2.29.15 Interrupt Status Register (Port 0x0830)

This register shows the interrupt status of the interrupts controlled by the Interrupt enable register.

MSB = D0, LSB = D7

D0: Temperature Interrupt

0 = Not active
1 = Active

D1: HB8 Bridge Interrupt

0 = Not active
1 = Active

D2: PHY 1 Interrupt

0 = Not active
1 = Active

D3: PHY 0 Interrupt

0 = Not active
1 = Active

D4: ETI Interrupt (prior to artwork 4 bit reads '0')

0 = Not active
1 = Active

D5: ISA NMI

0 = Not active
1 = Active

D6: Temperature Critical interrupt

0 = Not active
1 = Active

D7: Reserved – Reads '0'

2.29.16 PCI-X/PCI configuration Status Register (Port 0x0832)

This register shows the status of the PCI-X/PCI busses.

MSB = D0, LSB = D7

D0: Reserved – Reads '0'
D1 to D3: PCI0 Configuration

Table 2-23 Port 0x0832 PCI0 (D1 to D3)

D1	D2	D3	Configuration
0	0	0	PCI @ 33 MHz
0	0	1	PCI @ 66 MHz
0	1	0	Reserved
0	1	1	Reserved
1	0	0	PCI-X @ 33 MHz
1	0	1	PCI-X @ 66 MHz
1	1	0	PCI-X @ 100 MHz
1	1	1	PCI-X @ 133 MHz

D4: Reserved – Reads '0'
D5 to D7: PCI1 Configuration

Table 2-24 Port 0x0832 PCI1 (D1 to D3)

D1	D2	D3	Configuration
0	0	0	PCI @ 33 MHz
0	0	1	PCI @ 66 MHz
0	1	0	Reserved
0	1	1	Reserved
1	0	0	PCI-X @ 33 MHz
1	0	1	PCI-X @ 66 MHz
1	1	0	PCI-X @ 100 MHz
1	1	1	PCI-X @ 133 MHz

2.29.17 Board Revision Register (Port 0x0854)

This register provides information on the build state of the PPC7.

MSB = D0, LSB = D7
D0 to D2: Number revision of hardware build state

1 = Revision 1
2 = Revision 2
3 = Revision 3
4 = Revision 4 – indicates artwork 4
All other values are Reserved.

D3 to D7: Letter revision of hardware build state

0x0 = Revision A
0x1 = Revision B
...
0x18 = Revision Y
0x19 = Revision YA
...
0x1F = Revision YG

2.29.18 Extended ID Register (Port 0x0858)

This register provides Board hardware type.

MSB = D0, LSB = D7

D0 to D7: Board ID register

0x0E = PPC7A10 - 7410/755
0x0F = PPC7A5X – 745x
0x10 = PPC7FW (MPC7410 with Firewire)
0x16 = PPC7C
0x17 = PPC8A
0x18 = PPC7D
0x21 = PP7EP

For other ID patterns contact Abaco

2.29.19 ID Link Register (Port 0x0864) – prior to artwork 4

This register allows you to read the Board ID links (E6, E7, E12 and E13) or the VME Geographical address pins.

MSB = D0, LSB = D7

D0: Reserved

D1: Reserved

D2: GAP (VME64 Geographical Parity bit)

D3: GA4 (VME64 Geographical Address bit 4)

D4: E13/GA3

0 = Link fitted
1 = Link not fitted

D5: E12/GA2

0 = Link fitted
1 = Link not fitted

D6: E7/GA1

0 = Link fitted
1 = Link not fitted

D7: E6/GA0

0 = Link fitted
1 = Link not fitted



NOTE

Bits D4, D5, D6 and D7 are also connected to the VME64 Geographical Address bits GA3, GA2, GA1 and GA0 respectively. Do not fit the links if you wish to read the status of the Geographical Address bits, as the links connect these bits to 0V.

2.29.20 ID Link Register (Port 0x0864) – artwork 4 onwards

This register allows you to read the Board ID links (E6, E7, E12 and E13) or the VME Geographical address pins.

MSB = D0, LSB = D7

D0: LINK_IDEN

0 = Link not fitted
1 = Link E881fitted

D1: Reserved

D2: GAP (VME64 Geographical Parity bit)

0 = when E881 fitted or GAP low when E881 is not fitted
1 =GAP high when E881 is not fitted

D3: GA4 (VME64 Geographical Address bit 4)

0 = when E881 fitted or GA4 low when E881 is not fitted
1 = GA4 high when E881 is not fitted

D4: E13/GA3

0 = Link E13 fitted when E881 fitted or GA3 low when E881 is not fitted
1 = Link E13 not fitted when E881 fitted or GA3 high when E881 is not fitted

D5: E12/GA2

0 = Link E12 fitted when E881 fitted or GA2 low when E881 is not fitted
1 = Link E12 not fitted when E881 fitted or GA2 high when E881 is not fitted

D6: E7/GA1

0 = Link E7 fitted when E881 fitted or GA1 low when E881 is not fitted
1 = Link E7 not fitted when E881 fitted or GA1 high when E881 is not fitted

D7: E6/GA0

0 = Link E6 fitted when E881 fitted or GA0 low when E881 is not fitted
1 = Link E6 not fitted when E881 fitted or GA0 high when E881 is not fitted

2.29.21 ID Link Register (Port 0x0880) – artwork 4 onwards

This register allows you to read the Board ID links (E6, E7, E12 and E13) or the VME Geographical address pins.

MSB = D0, LSB = D7

D0: LINK_IDEN

0 = Link not fitted
1 = Link E881fitted

D1: Reserved

D2: GAP (VME64 Geographical Parity bit)

0 = when E881 is not fitted or GAP low when E881 fitted
1 =GAP high when E881 fitted

D3: GA4 (VME64 Geographical Address bit 4)

0 = when E881 is not fitted or GA4 low when E881 fitted
1 = GA4 high when E881 fitted

D4: E13/GA3

0 = Link E13 fitted when E881 is not fitted or GA3 low when E881 fitted
1 = Link E13 not fitted when E881 is not fitted or GA3 high when E881 fitted

D5: E12/GA2

0 = Link E12 fitted when E881 is not fitted or GA2 low when E881 fitted
1 = Link E12 not fitted when E881 is not fitted or GA2 high when E881 fitted

D6: E7/GA1

0 = Link E7 fitted when E881 is not fitted or GA1 low when E881 fitted
1 = Link E7 not fitted when E881 is not fitted or GA1 high when E881 fitted

D7: E6/GA0

0 = Link E6 fitted when E881 is not fitted or GA0 low when E881 fitted
1 = Link E6 not fitted when E881 is not fitted or GA0 high when E881 fitted

2.29.22 Motherboard Type Register (Port 0x0866)

This register provides information on the type of motherboard and SDRAM ECC operation. The bits used in this register are compatible with the other members of the current Abaco PPC product range.

MSB = D0, LSB = D7

D0: HW_ECC ENABLE

0 = Non-ECC
1 = ECC enabled

D1: PLL2 (see table below)

D2: ECC_TYPE

0 = Reserved
1 = ECC

D3: ECC

0 = ECC not fitted
1 = ECC fitted

D4: PLL1 (see table below)
D5: PLL0 (see table below)

Table 2-25 Port 0x0866 (D4 & D5)

PLL2	PLL1	PLL0	Bus Speed (MHz)
1	1	1	Reserved
1	1	0	Reserved
1	0	1	Reserved
1	0	0	133
0	1	1	Reserved
0	1	0	100
0	0	1	66
0	0	0	Reserved

D6 and D7: Hardware ID2 and ID1 respectively. Used with Hardware ID0 (bit 0 of Equipment Present Register 1) to define the hardware type as follows:

Table 2-26 Port 0x0866 (D6 & D7)

ID2 To ID0	Hardware Type
111	PPC1/PPC3
110	PPC2
101	PPC1A
100	PPC2A
011	PPC4
010	PPC4A
000	Use Extended ID

2.29.23 Flash Write Protection (Port 0x0868)

This register provides information on the Flash write protection.

MSB = D0, LSB = D7

D0: Flash write enable link – prior to artwork 4

0 = link not fitted
1 = link fitted

D0: PASSWORD enable link – artwork 4 onwards

0 = link not fitted
1 = link fitted

D1: Status of the P2 or P0 Flash_WREN~ signal

0 = Signal not active (Pin high)
1 = Signal active (Pin low)

D2: Flash BOOT write enable link

0 = link not fitted
1 = link fitted

D3: Flash USER write enable link

0 = link not fitted
1 = link fitted

D4: Always reads '0'

D5: Writes to Flash recovery section

0 = Disabled
1 = Enabled

D6: Writes to Flash BOOT section

0 = Disabled
1 = Enabled

D7: Writes to Flash USER section

0 = Disabled
1 = Enabled

2.29.24 Software Flash write protect (Port 0x086A) – prior to artwork 4 only

This register provides information on the Flash write protection.

MSB = D0, LSB = D7

D0 to D5: Always reads '0'

D6: Software write enable System/Boot area

0 = Disabled
1 = Enabled

D7: Software write enable User area

0 = Disabled
1 = Enabled

2.29.25 Flash Control Register (Port 0x086E)

This register provides status and control signals for the Boot sections of the Flash devices.

When the PPC7D is reset, this register is reset to reflect the status of the BOOT links (E8, E3 & E4), after boot software can then override these link settings by writing to bits D5 & D7 in this register.

Status signals BOOT_ALTERNATE, BOOT_FROM_VME & BOOT_RECOVERY show the real link settings. Signals SELECT_ALTERNATE & SELECT_RECOVERY show what image is really selected.

MSB = D0, LSB = D7

D0: NVRAM Write Protect

0 = NVRAM is write protected
1 = Writes to NVRAM are enabled

D1: BOOT_ALTERNATE (reflects the status of user link E4). This bit is read-only.

0 = Link not fitted
1 = Link fitted

D2: VME_BOOT_MODE (reflects the status of user link E8). This bit is read-only.

0 = Link not fitted
1 = Link fitted

D3: BOOT_RECOVERY (reflects the status of user link E3). This bit is read-only.

0 = Link not fitted
1 = Link fitted

D4: Reserved reads '0'

D5: SELECT_ALTERNATE (see SELECT_RECOVERY)

D6: Flash_CONTROL_WRITTEN

0 = Register not written
1 = Register written

D7: SELECT_RECOVERY

Table 2-27 Port 0x086E (D5 & D7)

SELECT_ALTERNATE	SELECT_RECOVERY	Area Selected
0	0	Main
0	1	Recovery
1	0	Alternate
1	1	Extended

2.29.26 IO Control Register (Port 0x0870)

This register allows selection of onboard IO options.

MSB = D0, LSB = D7

D0: USB_SUPPLY_STATUS

0 = USB supply off
1 = USB supply on

D1, D2, D3: Reserved reads '0'

D4: UART_CLK_HIGH

0 = Standard Com5 & 6 UART clock 12 MHz
1 = High speed Com5 & 6 UART clock 24 MHz

D5: USB_POWER_ON_CONTROL

0 = USB supply off
1 = USB supply on

D6 & D7: Reserved

2.30 Control and Status Registers on CS0

These registers are accessed via the MV64360/64460 CS0 address window (see MV64360/64460 for more information for setting up this address window).

Table 2-28 Registers on CS0

CS0 I/O Port (Hex)	Description	Type
0000	Board ID	RO
0002	Last Reset source	RO
0003	Reset register	R/W
0004 to 0007	Board ID string	RO
0010 & 0011	PCI configuration	RO
0014 to 0017	Flash password	RO

Where: R/W = Read/Write RO = Read Only

2.30.1 Board ID (Port 0x0)

This register provides Board hardware type.

MSB = D0, LSB = D7

D0 to D7: Board ID register

0x0E = PPC7A10 - 7410/755
0x0F = PPC7A5X – 745x
0x10 = PPC7FW (MPC7410 with Firewire)
0x16 = PPC7C
0x17 = PPC8A
0x18 = PPC7D

For other ID patterns contact Abaco

2.30.2 Last Reset Source (Port 0x2)

This register provides information about what caused the last reset.

MSB = D0, LSB = D7

D0 to D2: Reserved

D3: MV64360/64460 watchdog timed out

0 = Did not cause the last reset
1 = Caused the last reset

D4: MAX706 Watchdog Timed out

0 = Did not cause the last reset
1 = Caused the last reset

D5: Reset switch

0 = Did not cause the last reset
1 = Caused the last reset

D6: Universe II

0 = Did not cause the last reset
1 = Caused the last reset

D7: RiscWatch connector reset driven

0 = Did not cause the last reset
1 = Caused the last reset

2.30.3 Reset Register (Port 0x3)

This register provides a 4bit register that is not cleared or changed on any reset apart from a power up when it is cleared to '0'.

MSB = D0, LSB = D7

D0 to D3: Reserved Reads '0'

D4 to D7: 4 bit register

2.30.4 Board ID String (Port 0x4 to 0x7)

This register provides a board ID string, which shows 'PPC7' when read as a 32 bit value.

Port 0x4

MSB = D0, LSB = D7

D0 to D7: Reads 0x50 ('P')

Port 0x5

MSB = D0, LSB = D7

D0 to D7: Reads 0x50 ('P')

Port 0x6

MSB = D0, LSB = D7

D0 to D7: Reads 0x43 ('C')

Port 0x7

MSB = D0, LSB = D7

D0 to D7: Reads 0x37 ('7')

2.30.5 PCI Configuration (Port 0x10 to 0x11)

This register is a PCI-X/PCI & Flash configuration status register.

Port 0x10 - PMC1 Configuration

MSB = D0, LSB = D7

D0: PMC VIO

0 = 3.3V
1 = 5V

D1 & D2: Reserved Reads '0'

D3 to D7: PCI Configuration

Table 2-29 Port 0x10 (D3 to D7)

D3	D4	D5	D6	D7	PCI Configuration
0	0	0	0	1	PCI-X @ 133 MHz
0	0	0	1	0	PCI-X @ 100 MHz
0	0	1	0	0	PCI-X @ 66 MHz
0	1	0	0	0	PCI @ 66 MHz
1	0	0	0	0	PCI @ 33 MHz

All other patterns Reserved

Port 0x11 – PMC2 Configuration

Same as PMC1 Configuration above.

2.30.6 Flash Password String (Port 0x14) – Artwork 4 Onwards

This register provides the Flash password string, which shows "Data" when read as a 32-bit value if the Password Enable Link (E9) is fitted, otherwise "****" is read back.

2.30.7 Flash Password String (Port 0x18) – Artwork 4 Onwards

This register provides the Flash password string, which shows "Safe" when read as a 32-bit value if the Password Enable Link (E9) is fitted otherwise "****" is read back.

2.31 Status Registers on CS1

These registers are accessed via the MV64360/64460 CS1 address window (see MV64360/64460 for more information for setting up this address window).

Table 2-30 Registers on CS1

CS0 I/O Port (Hex)	Description	Type
0000 to 0003	Checker board 1	RO
0004 to 0007	Checker board 2	RO

Where: RO = Read Only

2.31.1 Checker Board 1 (Port 0x0 to 0x3)

This register provides a checker board value of 0x5555 5555 when read as a 32 bit value.

2.31.2 Checker Board 2 (Port 0x4 to 0x7)

This register provides a checker board value of 0xAAAA AAAA when read as a 32 bit value.

2.32 Registers on CS2

These registers are accessed via the MV64360/64460 CS2 address window (see MV64360/64460 for more information for setting up this address window).

These registers are used to access the AFIX IO bus.

Table 2-31 Registers on CS2

CS0 I/O Port (Hex)	Description	Type
0003	AFIX IO	RW
0002	Not used	N/A
0001	AFIX address	RW
0000	AFIX ID	RO

Where: R/W = Read/Write RO = Read Only

2.32.1 AFIX IO (Port 0x3)

This register is used to access the AFIX data register that is pointed to be AFIX address. Writes to this register must be 8-bit wide.

2.32.2 AFIX address (Port 0x1)

Address of the AFIX IO register that is to be accessed by the AFIX IO port. Writes to this register must be 8-bit wide.

2.32.3 AFIX ID (Port 0x0)

This register provides the ID of the AFIX module that is fitted.

2.33 Interrupts and Error Reporting

The following table shows the various external interrupt sources to the processor and their relative priorities. It also shows whether the previous state of the processor is recoverable.

Table 2-32 External Interrupts

Priority	Interrupt	Cause	Recoverability
0	System Reset	Power on, Hard reset	Non-recoverable
1	Machine Check	Address or Data Parity error, Machine Check Input (MCP~), Non-maskable Interrupt (NMI~)	Non-recoverable in most cases
2	System Reset	Soft reset	Recoverable unless Machine Check occurs
3	System Management Interrupt	SMI~ input	Recoverable unless Machine Check or System Reset occurs
4	External Interrupt	INT~ input	Recoverable unless Machine Check or System Reset occurs

2.33.1 System Resets

See the Resetting the PPC7D section at the start of this section.

2.33.2 Machine Check Exception

The South Bridge can be configured the signal NMI on certain conditions. The hardware on the PPC7D routes this signal to the CPU as the MCP~ (Machine Check) interrupt.

The South Bridge can drive this signal due to the following conditions:

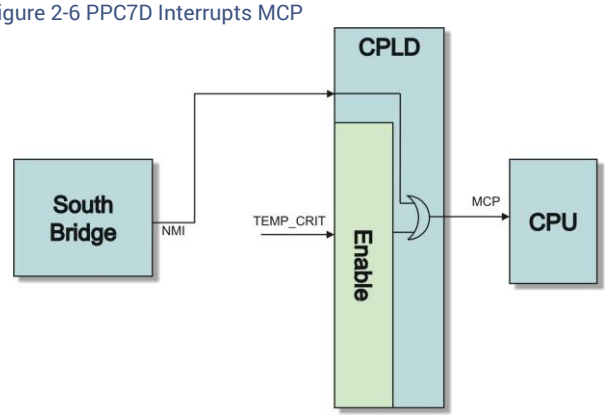
- PCI bus error
- PCI SERR~ signal driven active

The PCI SERR~ signal can be driven low by other PCI devices to report a error condition.

The processor may be configured to take a machine check exception or enter the checkstop state.

The CPLD can also generate a Machine check on the temperature becoming critical (see register 0x82e & 0x830). The temperature alarm can be from either the board temperature sensor (LM92) or/and the CPU core temperature sensor (ADT7461).

Figure 2-6 PPC7D Interrupts MCP

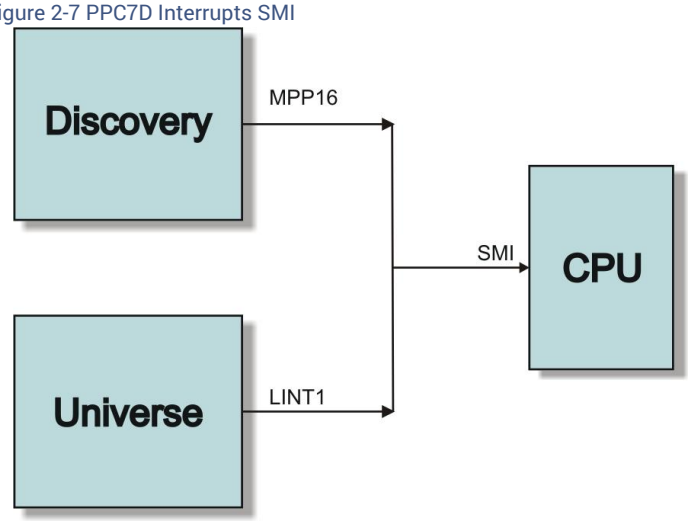


2.33.3 System Management Interrupt (SMI~)

A SMI~ interrupt to the CPU can be generated using the MPP[16] pin. This pin would normally be set to WDNMI (watchdog non-maskable).

It is also possible for the Universe II to generate a SMI~ interrupt to the CPU via it's INT1 pin.

Figure 2-7 PPC7D Interrupts SMI

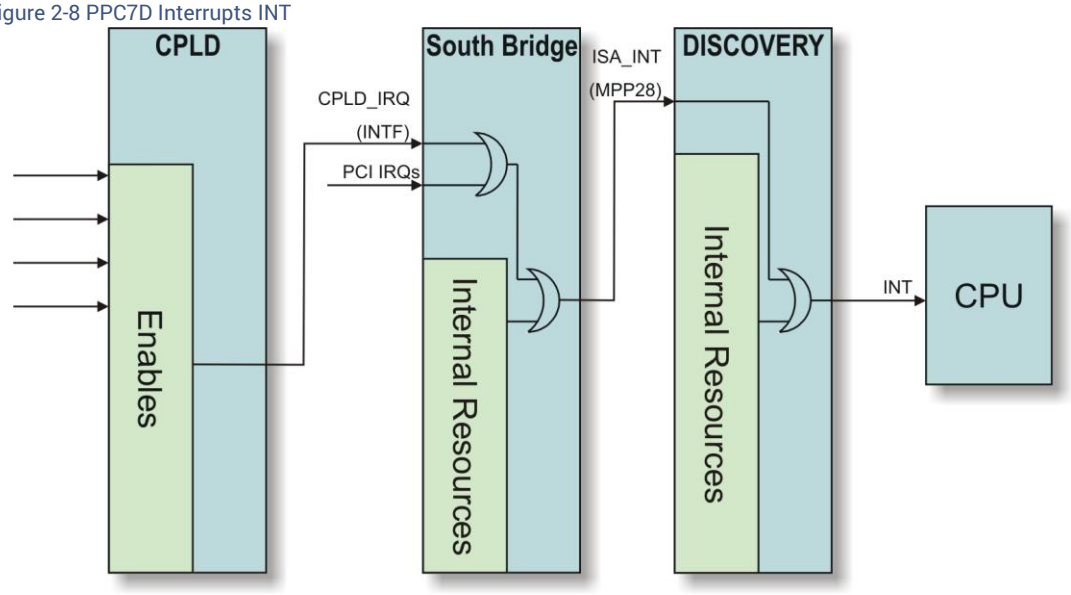


2.33.4 External Interrupt (INT~)

The processor external interrupt pin (INT~) is asserted for a pending interrupt from the interrupt controller in the South Bridge.

Interrupt priorities and modes are assigned as the firmware running on the PPC7.

Figure 2-8 PPC7D Interrupts INT



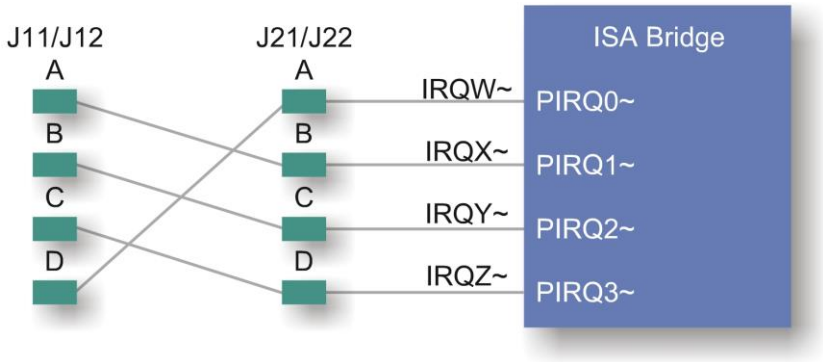
2.33.5 PCI Interrupts

There are 4 interrupt lines for the PMC expansion slots on the motherboard and the PMC carrier. These are connected to the PIRQ~ inputs of the interrupt controller. The PIRQ~ inputs may be routed to any IRQ that is set to level sensitive mode.

The interrupt routing follows the recommendations in the PCI specification and the PCI system design guide with a “rotation” between each slot.

The interrupt lines for the two onboard PMC slots are routed as shown below:

Figure 2-9 Interrupt Routing



Two single function PMCs (which always use INTA~) are able to use unique IRQs with appropriate programming of the interrupt controller.

2.34 Keylock

The keylock input signal allows the software to interrogate an external keyswitch. For example, the boot firmware could request a password if the keyswitch is in the locked position and a password is set up in the NVRAM.

The keylock signal defaults to high if no external connection is made.

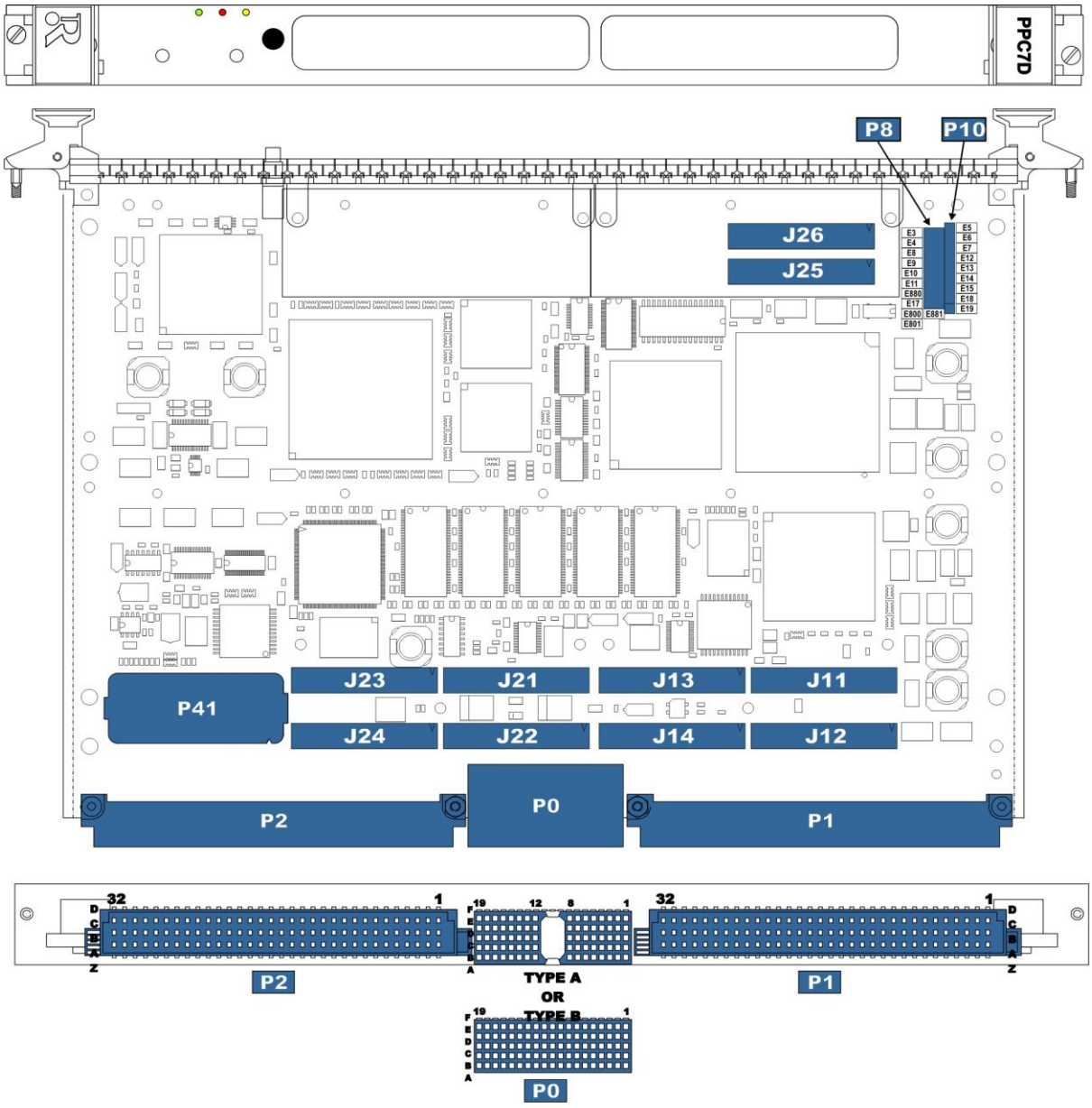
3 • Connectors

This section gives the pin assignments and signal descriptions for the connectors on the PPC7D.

Table 3-1 Connector Functions

Connector	Function		Connector	Function
P1	VMEbus		P41	AFIX connector
P2	VMEbus/Rear I/O		J11, J12, J14	PMC (site 1)
P0	PMC site 1 I/O		J21, J22, J24	PMC (site 2)
P8	RISCWatch		J25, J26	I/O expansion
P10	JTAG (Factory use)			

Figure 3-1 Connector Positions



3.1 Backplane Connectors

3.1.1 P1 (VMEbus) Pin Assignments

The PPC7D P1 connector conforms to the VME64x standard. For pin assignments and signal descriptions, refer to the Standard Interfaces section. Additional signals, indicated in the table shown right, replace those given in the Standard table.

Table 3-2 P1 Pin Assignments

Pin No.	Row Z
1	JTAG_RST~
2	GND
3	JTAG_TCK
4	GND
5	JTAG_TDO
6	GND
7	JTAG_TDI
8	GND
9	JTAG_TMS

3.1.2 P2 Connector Standard Pin Assignments

Table 3-3 P2 Pin Assignments – with J24 not fitted

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	Flash_WREN~	P41_B1	+5V	RX0+	COM3_TXD_A
2	GND	P41_A2	GND	RX0-	COM3_TXD_B
3	EXT_RESET~	P41_B2	Reserved	TX0+	COM3_RXD_A
4	GND	P41_C2	A24	TX0-	COM3_RXD_B
5	EXT_ABORT~	P41_A3	A25	RX1+	COM3_RTS_A
6	GND	P41_C3	A26	RX1-	COM3_RTS_B
7	N/C	P41_B4	A27	P41_A5	COM3_CTS_A
8	GND	P41_C5	A28	GPIO0 or P41_B5	COM3_CTS_B
9	COM4_TXD_A	P41_C6	A29	GPIO1 or P41_A6	COM5_TXD
10	GND	P41_B7	A30	GPIO2 or P41_A8	COM5_RTS
11	COM4_TXD_B	P41_B8	A31	GPIO3 or P41_A9	COM6_TXD
12	GND	P41_C8	GND	GPIO4 or P41_B12	COM6_RTS
13	COM4_RXD_A	P41_C9	+5V	GPIO5 or P41_A13	COM5_RXD
14	GND	P41_C13	D16	GPIO6 or P41_B13	COM5_CTS
15	COM4_RXD_B	P41_C14	D17	GPIO7 or P41_A14	COM3_TT_A
16	GND	P41_B15	D18	GPIO8 or P41_A16	COM3_TT_B
17	COM4_CTS_A	P41_C16	D19	GPIO9 or P41_B16	COM3_ST_A
18	GND	P41_C17	D20	GPIO10 or P41_A17	COM3_ST_B
19	COM4_CTS_B	P41_B18	D21	GPIO11 or P41_A21	COM3_RT_A
20	GND	USBP1 or MOUSE_CLK	D22	GPIO12 or P41_B21	COM3_RT_B
21	N/C	USBP1~ or MOUSE_DATA	D23	GPIO13 or P41_A22	COM4_RTS_A
22	GND	KBD_5V	GND	GPIO14 or P41_A24	COM4_RTS_B
23	N/C	USBP2 or KBD_CLK	D24	GPIO16 or P41_B24	COM6_RXD
24	GND	USBP2~ or KBD_DATA	D25	GPIO17 or P41_A25	COM6_CTS
25	COM4_ST_A	COM2_TXD or P41_C25	D26	SPEAKER_OUT or P41_B25	N/C
26	GND	COM2_RXD or P41_A27	D27	KEYLOCK_IN or P41_A28	N/C
27	COM4_ST_B	COM2_RTS or P41_B27	D28	COM1_TXD	COM4_TT_A
28	GND	P41_C27	D29	COM1_RXD	COM4_TT_B
29	COM4_RT_A	COM2_CTS or P41_C28	D30	COM1_RTS	N/C
30	GND	P41_B29	D31	COM1_CTS	N/C
31	COM4_RT_B	P41_A30	GND	TX1+	GND
32	GND	P41_C30	+5V	TX1-	+5V

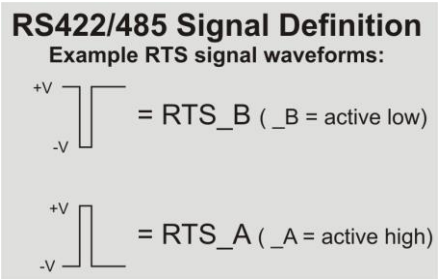
For more details See the Alternate P2 Pin Assignments for AFIX Pins section.

NOTE

When RS422 mode is selected for COM5 & 6 the pinout is as follows:

Table 3-4 P2 Pin Assignment for COM5 & 6 in RS422 Mode

Pin No.	Row D
9	COM5_TXD_A
10	COM5_TXD_B
11	COM6_TXD_A
12	COM6_TXD_B
13	COM5_RXD_A
14	COM5_RXD_B
23	COM6_RXD_A
24	COM6_RXD_B



3.1.3 P2 Connector Pinout (when J24 is fitted)

Table 3-5 P2 Pin Assignments – with J24 fitted

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	PMC2_IO_2	P41_B1	+5V	RX0+	PMC2_IO_1
2	GND	P41_A2	GND	RX0-	PMC2_IO_3
3	PMC2_IO_5	P41_B2	Reserved	TX0+	PMC2_IO_4
4	GND	P41_C2	A24	TX0-	PMC2_IO_6
5	PMC2_IO_8	P41_A3	A25	RX1+	PMC2_IO_7
6	GND	P41_C3	A26	RX1-	PMC2_IO_9
7	PMC2_IO_11	P41_B4	A27	P41_A5	PMC2_IO_10
8	GND	P41_C5	A28	GPIO0 or P41_B5	PMC2_IO_12
9	PMC2_IO_14	P41_C6	A29	GPIO1 or P41_A6	PMC2_IO_13
10	GND	P41_B7	A30	GPIO2 or P41_A8	PMC2_IO_15
11	PMC2_IO_17	P41_B8	A31	GPIO3 or P41_A9	PMC2_IO_16
12	GND	P41_C8	GND	GPIO4 or P41_B12	PMC2_IO_18
13	PMC2_IO_20	P41_C9	+5V	GPIO5 or P41_A13	PMC2_IO_19
14	GND	P41_C13	D16	GPIO6 or P41_B13	PMC2_IO_21
15	PMC2_IO_23	P41_C14	D17	GPIO7 or P41_A14	PMC2_IO_22
16	GND	P41_B15	D18	GPIO8 or P41_A16	PMC2_IO_24
17	PMC2_IO_26	P41_C16	D19	GPIO9 or P41_B16	PMC2_IO_25
18	GND	P41_C17	D20	GPIO10 or P41_A17	PMC2_IO_27
19	PMC2_IO_29	P41_B18	D21	GPIO11 or P41_A21	PMC2_IO_28
20	GND	USBP1 or MOUSE_CLK	D22	GPIO12 or P41_B21	PMC2_IO_30
21	PMC2_IO_32	USBP1~ or MOUSE_DATA	D23	GPIO13 or P41_A22	PMC2_IO_31
22	GND	KBD_5V	GND	GPIO14 or P41_A24	PMC2_IO_33
23	PMC2_IO_35	USBP2 or KBD_CLK	D24	GPIO16 or P41_B24	PMC2_IO_34
24	GND	USBP2~ or KBD_DATA	D25	GPIO17 or P41_A25	PMC2_IO_36
25	PMC2_IO_38	COM2_TXD or P41_C25	D26	SPEAKER_OUT or P41_B25	PMC2_IO_37
26	GND	COM2_RXD or P41_A27	D27	KEYLOCK_IN or P41_A28	PMC2_IO_39
27	PMC2_IO_41	COM2_RTS or P41_B27	D28	COM1_TXD	PMC2_IO_40
28	GND	P41_C27	D29	COM1_RXD	PMC2_IO_42
29	PMC2_IO_44	COM2_CTS or P41_C28	D30	COM1_RTS	PMC2_IO_43
30	GND	P41_B29	D31	COM1_CTS	PMC2_IO_45
31	PMC2_IO_46	P41_A30	GND	TX1+	GND
32	GND	P41_C30	+5V	TX1-	+5V

For more details see the Alternate P2 Pin Assignments for AFIX Pins section.

3.1.4 Alternate P2 Pin Assignments for AFIX Pins

Table 3-6 P2 Pin Assignments – No AFIX Fitted

Pin No.	GPIO	Floppy	LPT	HB8_IO
C8	GPIO0	RDATA~	STROBE~	HB8/IO0
C9	GPIO1	WGATE~	LPTD0	HB8/IO1
C10	GPIO2	WDATA~	LPTD1	HB8/IO2
C11	GPIO3	HDSEL~	LPTD2	HB8/IO3
C12	GPIO4	FD_DIR~	LPTD3	HB8/IO4
C13	GPIO5	STEP~	LPTD4	HB8/IO5
C14	GPIO6	DSKCHG~	LPTD5	HB8/IO6
C15	GPIO7	DRV2~	LPTD6	HB8/IO7
C16	GPIO8	DRV1~	LPTD7	HB8/IO8
C17	GPIO9	MOT0~	ACK~	HB8/IO9
C18	GPIO10	MOT1~	BUSY	HB8/IO10
C19	GPIO11	WPROT~	PERROR	HB8/IO11
C20	GPIO12	TRK0~	SELECT	HB8/IO12
C21	GPIO13	INDEX~	AUTOFD~	HB8/IO13
C22	GPIO14	DENSEL	ERR~	HB8/IO14
C23	GPIO16	GPIO16 (ACGAME3)	INIT~	HB8/IO15
C24	GPIO17	GPIO17 (ACGAME4)	SLCTIN~	Not used
C25	SPEAKER	SPEAKER	SPEAKER	SPEAKER
C26	KEYLOCK	KEYLOCK	KEYLOCK	KEYLOCK
A25	TXD2~	TXD2~	TXD2~	TXD2~
A26	RXD2~	RXD2~	RXD2~	RXD2~
A27	RTS2~	RTS2~	RTS2~	RTS2~
A28	CTS2~	CTS2~	CTS2~	CTS2~



NOTES

When there is an AFIX module fitted, these pins are connected only to the AFIX, see the appropriate AFIX module documentation for signal connections.

There is no south bridge connection to GPIO15 on the P2 connector.

HB8 I/O, GPIO, Floppy or LPT section is via software control of the south bridge.

3.1.5 P2 I/O Signal Descriptions

Table 3-7 P2 I/O Signal Descriptions

Mnemonic	Signal Description
P41/XXX	IO routed to AFIX module connector, for signal descriptions see AFIX manual
MOUSE_CLK	Mouse Clock. Clock drive for mouse
MOUSE_DATA	Mouse Data. Mouse data line
KBD_5V	Keyboard 5V. Supplies power for the keyboard and mouse or USB supply when USB is fitted. Rated at 1A†
KBD_CLK	Keyboard Clock. Clock drive for the keyboard
KBD_DATA	Keyboard Data. Keyboard data line
COM1/2/3/4/5/6_TXD	COM1/2/3/4/5/6 Transmit Data
COM1/2/3/4/5/6_RXD	COM1/2/3/4/5/6 Receive Data
COM1/2/3/4/5/6_RTS	COM1/2/3/4/5/6 Request-To-Send
COM1/2/3/4/5/6_CTS	COM1/2/3/4/5/6 Clear-To-Send
COM3/4_TT	COM3/4 Terminal timing
COM3/4_RT	COM3/4 Receive timing
COM3/4_ST	COM3/4 Send timing
KEYLOCK_IN	Keylock input. Used to detect the state of an external keyswitch. May be used to implement system password protection
SPEAKER_OUT	Loudspeaker Output. Outputs Timer2 Audio. May be used to drive 4Ω or 8Ω loudspeaker
NSELECTIN	Parallel port Select In
nINIT	Parallel port INIT
nFAULT	Parallel port FAULT
nAUTOFD	Parallel port AUTOFD
SELECT	Parallel port SELECT
PERROR	Parallel port PERROR
BUSY	Parallel port BUSY
nACK	Parallel port ACK
D1 to D8	Parallel port data bits
nSTROBE	Parallel port STROBE
TX0±/TX1±	10/100BaseT transmit data
RX0±/RX±	10/100BaseT receive data
Flash_WREN~	Global Flash write enable
EXT_RESET~	External Reset (Hard Reset)
EXT_ABORT~	External Abort (Soft Reset)
USBP1/USBP1~	USB interface Port 1
USBP2/USBP2~	USB interface Port 2
PMC2_IO_1 to PMC2_IO_46	I/O signals from PMC site 2

† This is a resettable fuse. The fuse rating is the current rating that the fuse can carry. In 20°C still air, the fuse trips at twice the rated current.

3.1.6 P1 JTAG Signal Descriptions

Table 3-8 P1 JTAG Signal Descriptions

Mnemonic	Signal Description
JTAG_TRST~	Reset JTAG chain
JTAG_TCK	JTAG clock
JTAG_TMS	JTAG test mode select
JTAG_TDI	JTAG data in
JTAG_TDO	JTAG data out

NOTE

When the JTAG split link (E14) is removed the JTAG chain is:

Universe II, PMC1, PMC2, HB8, MV64360/64460, Cache Rams, PHY's.

When the VME boot link is fitted the JTAG chain is:

Universe II, PMC1, PMC2, HB8, MV64360/64460, PLD's, Cache Rams, PHY's.

3.1.7 10/100/1000 Base-T Signal Connections

To remain backward compatible with the existing PPC range the PPC7D can be ordered with two channels of 10/100 Base-T network (these connections are shown in the P2 pinout).

NOTE

The hardware on the PPC7D will advertise 1000 Base-T even when the hardware is configured for dual 10/100. This may cause the Auto-Negotiation of the PHY not to complete if the PPC7D is connected to another network device that advertises 1000 Base-T. Software drivers should be written to inhibit 1000 Base-T in the PHY configuration if the software detects 10/100 base network configuration.

Table 3-9 Backplane Ethernet Options

Connector_Pin	Dual 10/100	Single 10/100/1000	Dual 10/100/1000
P2_C3	TX0+	ETH0_0+ (Pair 0 Channel 0 Pair)	ETH0_0+ (Pair 0 Channel 0 Pair)
P2_C4	TX0-	ETH0_0- (Pair 0 Channel 0 Pair)	ETH0_0- (Pair 0 Channel 0 Pair)
P2_C1	RX0+	ETH0_1+ (Pair 1 Channel 0 Pair)	ETH0_1+ (Pair 1 Channel 0 Pair)
P2_C2	RX0-	ETH0_1- (Pair 1 Channel 0 Pair)	ETH0_1- (Pair 1 Channel 0 Pair)
P2_C31	TX1+	ETH0_2+ (Pair 2 Channel 0 Pair)	ETH0_2+ (Pair 2 Channel 0 Pair)
P2_C32	TX1-	ETH0_2- (Pair 2 Channel 0 Pair)	ETH0_2- (Pair 2 Channel 0 Pair)
P2_C5	RX1+	ETH0_3+ (Pair 3 Channel 0 Pair)	ETH0_3+ (Pair 3 Channel 0 Pair)
P2_C6	RX1-	ETH0_3- (Pair 3 Channel 0 Pair)	ETH0_3- (Pair 3 Channel 0 Pair)
P0_A1	N/C	N/C	ETH1_0+ (Pair 0 Channel 1 Pair)
P0_A2	Flash_WREN~	Flash_WREN~	ETH1_0- (Pair 0 Channel 1 Pair)
P0_B1	REDLED~	REDLED~	ETH1_1+ (Pair 1 Channel 1 Pair)
P0_B2	GREENLED~	GREENLED~	ETH1_1- (Pair 1 Channel 1 Pair)
P0_C1	EXTRESET~	EXTRESET~	ETH1_2+ (Pair 2 Channel 1 Pair)
P0_C2	EXTABORT~	EXTABORT~	ETH1_2- (Pair 2 Channel 1 Pair)
P0_D1	TCE1~	TCE1~	ETH1_3+ (Pair 3 Channel 1 Pair)
P0_D2	TCT1~	TCT1~	ETH1_3- (Pair 3 Channel 1 Pair)

NOTE

There are 8 signals per1000 Base-T connection.

3.1.8 P0 Connector Pin Assignments - Type B (95-way)

P0 is routed to J14 and partially to J24.

NOTE

Due to the large amount of I/O required to be handled by the PPC7, Type B connectors are preferred to the Type A (80-pin) shown overleaf and are fitted by default no particular type is specified.

Table 3-10 P0 Connector Pin Assignments - Type B

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
1	N/C / ENET1_0+	REDLED~ / ENET1_1+	EXTRESET~ / ENET1_2+	TCE1 / ENET1_3+	TCE0	GND
2	Flash_WREN~ / ENET1_0-	GREENLED~ / ENET1_1-	EXTABORT~ / ENET1_2-	TCT1 / ENET1_3-	TCT0	GND
3	3.3V†	3.3V†	3.3V†	+5V	+5V	GND
4	PMC1_IO_5	PMC1_IO_4	PMC1_IO_3	PMC1_IO_2	PMC1_IO_1	GND
5	PMC1_IO_10	PMC1_IO_9	PMC1_IO_8	PMC1_IO_7	PMC1_IO_6	GND
6	PMC1_IO_15	PMC1_IO_14	PMC1_IO_13	PMC1_IO_12	PMC1_IO_11	GND
7	PMC1_IO_20	PMC1_IO_19	PMC1_IO_18	PMC1_IO_17	PMC1_IO_16	GND
8	PMC1_IO_25	PMC1_IO_24	PMC1_IO_23	PMC1_IO_22	PMC1_IO_21	GND
9	PMC2_IO_50	PMC2_IO_49	PMC2_IO_62	PMC2_IO_56	PMC2_IO_55	GND
10	PMC2_IO_48	PMC2_IO_47	GND	PMC2_IO_64	PMC2_IO_63	GND
11	PMC2_IO_52	PMC2_IO_51	PMC2_IO_61	PMC2_IO_58	PMC2_IO_57	GND
12	PMC1_IO_30	PMC1_IO_29	PMC1_IO_28	PMC1_IO_27	PMC1_IO_26	GND
13	PMC1_IO_35	PMC1_IO_34	PMC1_IO_33	PMC1_IO_32	PMC1_IO_31	GND
14	PMC1_IO_40	PMC1_IO_39	PMC1_IO_38	PMC1_IO_37	PMC1_IO_36	GND
15	PMC1_IO_45	PMC1_IO_44	PMC1_IO_43	PMC1_IO_42	PMC1_IO_41	GND
16	PMC1_IO_50	PMC1_IO_49	PMC1_IO_48	PMC1_IO_47	PMC1_IO_46	GND
17	PMC1_IO_55	PMC1_IO_54	PMC1_IO_53	PMC1_IO_52	PMC1_IO_51	GND
18	PMC1_IO_60	PMC1_IO_59	PMC1_IO_58	PMC1_IO_57	PMC1_IO_56	GND
19	+5V	PMC1_IO_64	PMC1_IO_63	PMC1_IO_62	PMC1_IO_61	GND

† The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on the VME P1 connector, the external PMC option is fitted then this is routed to the PMC connectors J12/J22, and capacitively decoupled to ground.

EXTRESET~ generates a Hard Reset and EXTABORT~ generates a Soft Reset. See the Resetting the PPC7D section for more details.

NOTE

Analogue signals should not be routed through P0.

3.1.9 P0 Connector Pin Assignments - Type A (80-way)

P0 is routed to J14.

NOTE

Due to the large amount of I/O required to be handled by the PPC7D, Type B (95-way) connectors are preferred to Type A and are fitted by default no particular type is specified.

Table 3-11 P0 Connector Pin Assignments - Type A

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
1	N/C / ENET1_0+	REDLED~ / ENET1_1+	EXTRESET~ / ENET1_2+	TCE71/ ENET1_3+	TCE0	GND
2	Flash_WREN~ / ENET1_0-	GREENLED~ / ENET1_1-	EXTABORT~ / ENET1_2-	TCT71/ ENET1_3-	TCT0	GND
3	3.3V†	3.3V†	3.3V†	+5V	+5V	GND
4	PMC1_IO_5	PMC1_IO_4	PMC1_IO_3	PMC1_IO_2	PMC1_IO_1	GND
5	PMC1_IO_10	PMC1_IO_9	PMC1_IO_8	PMC1_IO_7	PMC1_IO_6	GND
6	PMC1_IO_15	PMC1_IO_14	PMC1_IO_13	PMC1_IO_12	PMC1_IO_11	GND
7	PMC1_IO_20	PMC1_IO_19	PMC1_IO_18	PMC1_IO_17	PMC1_IO_16	GND
8	PMC1_IO_25	PMC1_IO_24	PMC1_IO_23	PMC1_IO_22	PMC1_IO_21	GND
9	PMC1_IO_30	PMC1_IO_29	PMC1_IO_28	PMC1_IO_27	PMC1_IO_26	GND
10	PMC1_IO_35	PMC1_IO_34	PMC1_IO_33	PMC1_IO_32	PMC1_IO_31	GND
11	PMC1_IO_40	PMC1_IO_39	PMC1_IO_38	PMC1_IO_37	PMC1_IO_36	GND
12	PMC1_IO_45	PMC1_IO_44	PMC1_IO_43	PMC1_IO_42	PMC1_IO_41	GND
13	PMC1_IO_50	PMC1_IO_49	PMC1_IO_48	PMC1_IO_47	PMC1_IO_46	GND
14	PMC1_IO_55	PMC1_IO_54	PMC1_IO_53	PMC1_IO_52	PMC1_IO_51	GND
15	PMC1_IO_60	PMC1_IO_59	PMC1_IO_58	PMC1_IO_57	PMC1_IO_56	GND
16	+5V	PMC1_IO_64	PMC1_IO_63	PMC1_IO_62	PMC1_IO_61	GND

† The 3.3V pins are *not* connected to a 3.3V supply. They are merely bussed together with the 3.3V pins on the VME P1 connector, the external PMC option is fitted then this is routed to the PMC connectors J12/J22, and capacitively decoupled to ground.

EXTRESET~ generates a Hard Reset and EXTABORT~ generates a Soft Reset. See the Resetting the PPC7D section for more details.

NOTE

Analogue signals should not be routed through P0.

3.1.10 P0 I/O Signal Descriptions

Table 3-12 P0 I/O Signal Descriptions

Mnemonic	Signal Description
REDLED~	Driven identically to the corresponding LED except that this signal has a separate buffer with a 180Ω series resistor
GREENLED~	Driven identically to the corresponding LED except that this signal has a separate buffer with a 180Ω series resistor
Flash_WP~	Flash Write Protect signal
EXTRESET~	Generates a Hard Reset. See the Resetting the PPC7D section for more details
EXTABORT~	Generates a Soft Reset. See the Resetting the PPC7D section for more details
N/C	No connection
TCE0 & TCE1	MV64260 Timer counter enable
TCT0 & TCT1	MV64260 Timer counter terminal count
3.3V†	These pins are not connected to a 3.3V supply
+5V	+5V DC power
PMC1_IO_1 to PMC1_IO_64	I/O signals from PMC site 1
PMC2_IO_47 to PMC_IO_52, PMC2_IO_55 to PMC_IO_58 and PMC2_IO_61 to PMC_IO_64	I/O signals from PMC site 2. PMC2_IO_48, PMC2_IO_50, PMC_IO_52, PMC2_IO_56, PMC2_IO_58, PMC2_IO_62 and PMC2_IO_64 are not available when a Fibre Channel PMC with rear I/O is fitted
GND	The DC voltage reference for the system
ENET1_0+ / ENET1_0-	Pair 0 Channel 1 Pair
ENET1_1+ / ENET1_1-	Pair 1 Channel 1 Pair
ENET1_2+ / ENET1_2-	Pair 2 Channel 1 Pair
ENET1_3+ / ENET1_3-	Pair 3 Channel 1 Pair

3.2 PMC Connector Pin Assignments

J11/J21 and J12/J22 give the signals for 32-bit PCI. J13/J23 give the signals for 64-bit PCI and J14/J24 give the user I/O signals.

3.2.1 J11 and J21

Table 3-13 PMC Connector Pin Assignments - J11 and J21

Pin No.	Signal	Pin No.	Signal
1	TCK	2	-12V
3	GND	4	INTA~
5	INTB~	6	INTC~
7	BUSMODE1~	8	+5V
9	INTD~	10	N/C
11	GND	12	N/C
13	CLK	14	GND
15	GND	16	GNTA~
17	REQA~	18	+5V
19	VIO	20	AD31
21	AD28	22	AD27
23	AD25	24	GND
25	GND	26	C/BE3~
27	AD22	28	AD21
29	AD19	30	+5V
31	VIO	32	AD17
33	FRAME~	34	GND
35	GND	36	IRDY~
37	DEVSEL~	38	+5V
39	GND	40	LOCK~
41	N/C	42	N/C
43	PAR	44	GND
45	VIO	46	AD15
47	AD12	48	AD11
49	AD09	50	+5V
51	GND	52	C/BE0~
53	AD06	54	AD05
55	AD04	56	GND
57	VIO	58	AD03
59	AD02	60	AD01
61	AD00	62	+5V
63	GND	64	REQ64~

3.2.2 J12 and J22

Table 3-14 PMC Connector Pin Assignments - J12 and J22

Pin No.	Signal	Pin No.	Signal
1	+12V	2	TRST~
3	TMS	4	TDO
5	TDI	6	GND
7	GND	8	N/C
9	N/C	10	N/C
11	BUSMODE2~	12	3.3V†
13	RST~	14	BUSMODE3~
15	3.3V†	16	BUSMODE4~
17	N/C	18	GND
19	AD30	20	AD29
21	GND	22	AD26
23	AD24	24	3.3V†
25	IDSELA	26	AD23
27	3.3V†	28	AD20
29	AD18	30	GND
31	AD16	32	C/BE2~
33	GND	34	IDSELB
35	TRDY~	36	3.3V†
37	GND	38	STOP~
39	PERR~	40	GND
41	3.3V†	42	SERR~
43	C/BE1~	44	GND
45	AD14	46	AD13
47	M66EN	48	AD10
49	AD08	50	3.3V†
51	AD07	52	REQB~
53	3.3V†	54	GNTB~
55	N/C	56	GND
57	N/C	58	N/C
59	GND	60	N/C
61	ACK64~	62	3.3V†
63	GND	64	N/C

† The 3.3V pins are connected to the PPC7D main 3.3V supply.



CAUTION

Do not fit a PMC that requires more than 8 watts from the 3.3V supply.

3.2.3 J13 and J23

Table 3-15 PMC Connector Pin Assignments - J13 and J23

Pin No.	Signal	Pin No.	Signal
1	Reserved (PCI)	2	GND
3	GND	4	CBE7~
5	CBE6~	6	CBE5~
7	CBE4~	8	GND
9	V (I/O)	10	PARR64
11	AD63	12	AD62
13	AD61	14	GND
15	GND	16	AD60
17	AD59	18	AD58
19	AD57	20	GND
21	V (I/O)	22	AD56
23	AD55	24	AD54
25	AD53	26	GND
27	GND	28	AD52
29	AD51	30	AD50
31	AD49	32	GND
33	GND	34	AD48
35	AD47	36	AD46
37	AD45	38	GND
39	V (I/0)	40	AD44
41	AD43	42	AD42
43	AD41	44	GND
45	GND	46	AD40
47	AD39	48	AD38
49	AD37	50	GND
51	GND	52	AD36
53	AD35	54	AD34
55	AD33	56	GND
57	V (I/O)	58	AD32
59	Reserved (PCI)	60	Reserved (PMC)
61	Reserved (PCI)	62	GND
63	GND	64	Reserved (PMC)

3.2.4 J14 PMC I/O

J14 is routed to P0.

Table 3-16 PMC Connector Pin Assignments - J14

Pin No.	Signal	Pin No.	Signal
1	PMC1_IO_1	2	PMC1_IO_2
3	PMC1_IO_3	4	PMC1_IO_4
5	PMC1_IO_5	6	PMC1_IO_6
7	PMC1_IO_7	8	PMC1_IO_8
9	PMC1_IO_9	10	PMC1_IO_10
11	PMC1_IO_11	12	PMC1_IO_12
13	PMC1_IO_13	14	PMC1_IO_14
15	PMC1_IO_15	16	PMC1_IO_16
17	PMC1_IO_17	18	PMC1_IO_18
19	PMC1_IO_19	20	PMC1_IO_20
21	PMC1_IO_21	22	PMC1_IO_22
23	PMC1_IO_23	24	PMC1_IO_24
25	PMC1_IO_25	26	PMC1_IO_26
27	PMC1_IO_27	28	PMC1_IO_28
29	PMC1_IO_29	30	PMC1_IO_30
31	PMC1_IO_31	32	PMC1_IO_32
33	PMC1_IO_33	34	PMC1_IO_34
35	PMC1_IO_35	36	PMC1_IO_36
37	PMC1_IO_37	38	PMC1_IO_38
39	PMC1_IO_39	40	PMC1_IO_40
41	PMC1_IO_41	42	PMC1_IO_42
43	PMC1_IO_43	44	PMC1_IO_44
45	PMC1_IO_45	46	PMC1_IO_46
47	PMC1_IO_47	48	PMC1_IO_48
49	PMC1_IO_49	50	PMC1_IO_50
51	PMC1_IO_51	52	PMC1_IO_52
53	PMC1_IO_53	54	PMC1_IO_54
55	PMC1_IO_55	56	PMC1_IO_56
57	PMC1_IO_57	58	PMC1_IO_58
59	PMC1_IO_59	60	PMC1_IO_60
61	PMC1_IO_61	62	PMC1_IO_62
63	PMC1_IO_63	64	PMC1_IO_64

3.2.5 J24 PMC I/O and Partial P2 Option

J24 may be partially routed to the P2 connector, depending on the build option. If used, then COM3 and COM4 are no longer routed to P2. P2 now has the connections shown in the following table:

Table 3-17 PMC Connector Pin Assignments – J24

J24 Pin No.	PMC Signal	Connections		J24 Pin No.	PMC Signal	Connections	
		P2	P0			P2	P0
1	PMC2_IO_1	D1		2	PMC2_IO_2	Z1	
3	PMC2_IO_3	D2		4	PMC2_IO_4	D3	
5	PMC2_IO_5	Z3		6	PMC2_IO_6	D4	
7	PMC2_IO_7	D5		8	PMC2_IO_8	Z5	
9	PMC2_IO_9	D6		10	PMC2_IO_10	D7	
11	PMC2_IO_11	Z7		12	PMC2_IO_12	D8	
13	PMC2_IO_13	D9		14	PMC2_IO_14	Z9	
15	PMC2_IO_15	D10		16	PMC2_IO_16	D11	
17	PMC2_IO_17	Z11		18	PMC2_IO_18	D12	
19	PMC2_IO_19	D13		20	PMC2_IO_20	Z13	
21	PMC2_IO_21	D14		22	PMC2_IO_22	D15	
23	PMC2_IO_23	Z15		24	PMC2_IO_24	D16	
25	PMC2_IO_25	D17		26	PMC2_IO_26	Z17	
27	PMC2_IO_27	D18		28	PMC2_IO_28	D19	
29	PMC2_IO_29	Z19		30	PMC2_IO_30	D20	
31	PMC2_IO_31	D21		32	PMC2_IO_32	Z21	
33	PMC2_IO_33	D22		34	PMC2_IO_34	D23	
35	PMC2_IO_35	Z23		36	PMC2_IO_36	D24	
37	PMC2_IO_37	D25		38	PMC2_IO_38	Z25	
39	PMC2_IO_39	D26		40	PMC2_IO_40	D27	
41	PMC2_IO_41	Z27		42	PMC2_IO_42	D28	
43	PMC2_IO_43	D29		44	PMC2_IO_44	Z29	
45	PMC2_IO_45	D30		46	PMC2_IO_46	Z31	
47	PMC2_IO_47		B10	48	PMC2_IO_48		A10
49	PMC2_IO_49		B9	50	PMC2_IO_50		A9
51	PMC2_IO_51		B11	52	PMC2_IO_52		A11
53	PMC2_IO_53			54	PMC2_IO_54		
55	PMC2_IO_55		E9	56	PMC2_IO_56		D9
57	PMC2_IO_57		E11	58	PMC2_IO_58		D11
59	PMC2_IO_59			60	PMC2_IO_60		
61	PMC2_IO_61		C11	62	PMC2_IO_62		C9
63	PMC2_IO_63		E10	64	PMC2_IO_64		D10



NOTE

P0 pins A9, A10, A11, C9, D9, D10 and D11 are not available if a Fibre Channel PMC with rear I/O is fitted.

3.3 PMC Signal Descriptions

Table 3-18 PMC Signal Descriptions

Mnemonic	Signal Description
AD0 to AD63	Address/Data bits. Multiplexed address and data bus
C_BE0 to C_BE7	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
FRAME~	FRAME. Driven low by the current master to signal the start and duration of an access
DEVSEL~	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	Parity. Parity protection bit for AD0 to AD31 and BE0 to BE3
PARR64	Parity. Parity protection bit for AD32 to AD63
IRDY~	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE1~	Bus Mode 1. Driven low by a PMC if it supports the current bus mode
BUSMODE2~, BUSMODE3~ and BUSMODE4~	Bus mode. Driven by the host to indicate the bus mode. On the PPC7D this is always PCI. BUSMODE2~ is only connected to a 4.7 kΩ pull-up. BUSMODE3~ and BUSMODE4~ are connected to GND.
RST~	Reset. Driven low to reset the PCI bus
TRDY~	Target Ready. Driven low by the current target to signal its ability to complete the current data phase
PERR~	Parity Error. Driven low by a PCI agent to signal a parity error
SERR~	System Error. Driven low by a PCI agent to signal a system error
STOP~	STOP. Driven low by a PCI target to signal a disconnect or target-abort
INTA~ to INTD~	Interrupt lines. Level-sensitive, active-low interrupt requests
CLK	Clock. All PCI bus signals except RST~ are synchronous to this clock.
REQA/B~	Request. Driven low by a PCI agent to request ownership of the PCI bus
GNTA/B~	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSELA/B	Initialization Device Select. Device chip select during configuration cycles
N/C	No connection
REQ64~	Request 64 Bit. Driven low by PCI master to request 64 bit transfer
ACK64~	Acknowledge 64 Bit. Driven low by PCI agent in response to REQ64
TCK	Test Clock. Clock for the PMC JTAG
TMS	Test Mode Select. Select Test Mode for PMC JTAG
TRST~	Test Reset. Reset any PMC JTAG devices
TDI	Test Data In. Input data for PMC JTAG chain
TDO	Test Data Out. Data from a PMC JTAG chain



NOTE

The PPC7D supports PMC clocking at speeds up to 133 MHz. However, if a PMC is fitted to the PPC7D that does not support the 133 MHz clocking speed, then the PPC7D will slow the clock speed down to the level that the PMC supports. Both sites are controlled separately.

3.4 P10 PLD Connector Pin Assignments

P10 is the programming JTAG chain this is normally for factory use.

Table 3-19 PLD Connector Pin Assignments

Pin No.	Description
1	VCC
2	PLD_TDO
3	PLD_TDI
4	N/C
5	KEYWAY
6	PLD_TMS
7	GND
8	PLD_TCK

NOTE

This interface will only work if the JTAG chain split link is fitted (E14) is fitted. For more information on JTAG, see JTAG Functional Description Section.

3.5 P8 RISCWatch Connector Pin Assignments

P8 is the RISCWatch connector allowing the connection of software debugging tools that use the processor's JTAG port to control the operation of the processor.

Table 3-20 P8 RISCWatch Connector Pin Assignments

Pin No.	Signal	Pin No.	Signal
1	TDO_CPU	2	EMU~/QACK_IN~
3	TDI_CPU	4	TRST~
5	QREQ~	6	+3.3V pull-up
7	TCK	8	N/C
9	TMS	10	N/C
11	SRESET_CPU~	12	GND
13	HRESET_CPU~	14	N/C
15	CHECKSTOP~	16	GND

NOTE

This interface will only work if the JTAG chain split link is fitted (E14) is fitted. For more information on JTAG, see the Functional Description Section.

3.5.1 P8 Signal Descriptions

Table 3-21 P8 Signal Descriptions

Signal	Description
TDO_CPU	Processor JTAG Test Data Out
EMU~	When connected to GND, creates QACK~ to the processor. This connection should be made with an emulator
TDI_CPU	Processor JTAG Test Data In
TRST~	Processor JTAG Test Reset
+3.3V PULL-UP	Power-on status signal to RISCWatch hardware
TCK	Processor JTAG Test Clock
TMS	Processor JTAG Test Mode Select
SRESET_CPU~	Processor Soft Reset
GND	Signal ground
HRESET_CPU~	Processor Hard Reset
CHECKKSTOP~	Processor Checkstop output
GND	Signal ground

For more information on JTAG, see the Functional Description Section

3.6 EST Emulator Connection

Table 3-22 EST Emulator Connection

Pin No.	Signal	Description
1	TDO_CPU	Processor JTAG Test Data Out
2	QACK_IN~	Quiescent grant to Processor
3	TDI_CPU	Processor JTAG Test Data In
4	TRST~	Processor JTAG Test Reset
5	QREQ~	Processor Quiescent request
6	+3.3V pull-up	Power-on status signal to EST hardware
7	TCK	Processor JTAG Test Clock
9	TMS	Processor JTAG Test Mode Select
11	SRESET_CPU~	Processor Soft Reset
12	GND	Signal ground
13	HRESET_CPU~	Processor Hard Reset
15	CHECKKSTOP~	Processor Checkstop output
16	GND	Signal ground

3.7 P41 AFIX Connector Pin Assignments

Table 3-23 P41 AFIX Connector Pin Assignments

Pin No.	Row K	Row J	Row H	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	PCI2(18)	GND	MOUSE_CLK~	GND	TCK	GND	GND	P41_B1	GND
2	PCI2(0)	PCI2(19)	RDATA~	MOUSE_DATA~	CLK1	TRST~	PLD0	P41_C2	P41_B2	P41_A2
3	PCI2(1)	VCC	WGATE~	VCC	CLK2	VCC	PLD1	P41_C3	GND	P41_A3
4	P3V3	PCI2(20)	P3V3	KBD_CLK~	P3V3	TDI	VCC	GND	P41_B4	GND
5	PCI2(2)	PCI2(21)	WDATA~	KBD_DATA~	CLK3	TMS	PLD2	P41_C5	P41_B5	P41_A5
6	PCI2(3)	GND	HDSEL~	GND	CLK4	GND	PLD3	P41_C6	GND	P41_A6
7	GND	PCI2(22)	GND	USB3P	GND	TDO	GND	GND	P41_B7	GND
8	PCI2(4)	PCI2(23)	FD_DIR~	USB3N	POWER_OK	66EN	EREADY	P41_C8	P41_B8	P41_A8
9	PCI2(5)	P3V3	STEP~	P3V3	HARDRESET~	P3V3	N/C	P41_C9	GND	P41_A9
10	P3V3	PCI2(24)	P3V3	USB4P	P3V3	I2C_CLK	P3V3	GND	+5V	GND
11	PCI2(6)	PCI2(25)	DSKCHG~	USB4N	IDSEL1	I2C_DATA	N/C	+12V	GND	+12V
12	PCI2(7)	GND	DRV0~	GND	IDESEL2	GND	N/C	GND	P41_B12	GND
13	GND	PCI2(26)	GND	PCI2_CBE0	GND	PCI2_ACK64~	GND	P41_C13	P41_B13	P41_A13
14	PCI2(8)	PCI2(27)	DRV1~	PCI2_CBE1	IDSEL3	PCI2_REQ64~	AFIX_FITTED~	P41_C14	GND	P41_A14
15	PCI2(9)	P2V5	MOT0~	P2V5	IDSEL4	P2V5	ALEN	GND	P41_B15	GND
16	P2V5	PCI2(28)	P2V5	PCI2_CBE2	P2V5	PCI2_PAR	P2V5	P41_C16	P41_B16	P41_A16
17	P3V3	PCI2(29)	P3V3	PCI2_CBE3	P3V3	PCI2_PAR64	IOR~	P41_C17	GND	P41_A17
18	P3V3	GND	P3V3	GND	P3V3	GND	IOW~	GND	P41_B18	GND
19	GND	PCI2(30)	GND	USB5P	GND	IRQW~	GND	+12V	P41_B19	-12V
20	PCI2(10)	PCI2(31)	MOT1~	USB5N	PCI2_FRAME~	IRQX~	ID(0)	GND	GND	GND
21	PCI2(11)	VCC	WPROT~	VCC	PCI2_TRDY~	VCC	ID(1)	P41_C21	P41_B21	P41_A21
22	P3V3	TXD2~	P3V3	PS2_FITTED~	P3V3	IRQY~	P3V3	P41_C22	P41_B22	P41_A22
23	PCI2(12)	RXD2~	TRK0~	N/C	PCI2_IRDY~	IRQZ~	ID(2)	GND	GND	GND
24	PCI2(13)	GND	INDEX~	GND	PCI2_STOP~	GND	ID(3)	P41_C24	P41_B24	P41_A24
25	GND	RTS2~	GND	PCI2_PERR~	GND	GNT0~	GND	P41_C25	P41_B25	P41_A25
26	PCI2(14)	CTS2~	DENSEL	PCI2_SERR~	REQ0~	GNT1~	ID(4)	GND	GND	GND
27	PCI2(15)	P2V5	ACGAME2	P3V3	REQ1~	P3V3	ID(5)	P41_C27	P41_B27	P41_A27
28	P2V5	ISA_IO_FITTED	P2V5	PCI2_DEVSEL~	P3V3	GNT2~	P2V5	P41_C28	GND	P41_A28
29	PCI2(16)	KEYLOCK	ACGAME3	PCI2_LOCK~	REQ2~	GNT3~	ID(6)	GND	P41_B29	GND
30	PCI2(17)	GND	SPEAKER	GND	REQ3~	GND	ID(7)	P41_C30	GND	P41_A30

3.7.1 P41 I/O Signal Descriptions

NOTE

Some signals descriptions are described in previous connectors

Table 3-24 P41 I/O Signal Descriptions

Mnemonic	Signal Description
VCC	Main +5V from VME
P3V3	3.3V supply
P2V5	2.5V Supply
P41/XXX	IO routed from AFIX module connector to P2 connector, for signal descriptions see AFIX manual
PCI2(0:31)	PCI Address/Data bus
PCI2_XXXX	PCI Control signals
CLK1 -> 4	PCI Clock inputs
REQ0 -> 3	PCI Requests from AFIX
GNT0 -> 3	PCI Grants to AFIX
IDSEL1 -> 3	IDSELs to AFIX PCI devices
EREADY	FPGA is ready
HARDRESET~	Reset AFIX
ISA_IO_FITTED~	Shows ISA IO is linked to P2 connector
AFIX_FITTED~	Shows AFIX fitted
POWER_OK	PPC7D board power OK
KEYLOCK	Keylock input. Used to detect the state of an external keyswitch. May be used to implement system password protection
SPEAKER	Loudspeaker Output. Outputs Timer2 Audio. May be used to drive 4Ω or 8Ω loudspeaker
66EN	High for 66 MHz PCI (not supported on PPC7D)
ALE	Latch AFIX address
IOR~	Read AFIX IO register
IOW~	Write AFIX IO register
ID0 -> 7	AFIX IO data bus

4 • Specifications

4.1 Mechanical Construction

Table 4-1 Mechanical Construction

Feature	Details
Weight	PPC7D Level 4 (no PMCs or AFIX fitted) 620g PPC7D Level 3 (no PMCs or AFIX fitted) 590g Most of the overall weight is due to the heatsink.
Dimensions	The air-cooled PPC7D is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. The Conduction-cooled PPC7D is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. For layout drawings, refer to the Standard Interfaces section.

4.2 Local Resources

Table 4-2 Local Resources

Feature	Details	
Processor	PowerPC 7447A at 1000 MHz, 7448 at 1400 MHz or above	
DDR SDRAM	64 to 1024 MB with ECC	
Flash	Up to 512 MB, with 8 MB reserved for Boot Flash banks	
RTC	I²C RTC backed up by connection to VMEbus 5VSTDBY pin	
NVRAM	32 KB	
PCI-X/PCI	1 at 64-bit @ up to 133 MHz 1 at 64-bit @ up to 100 MHz	
Ethernet	2 off, Ethernet 10/100/1000BaseT via the P2 & P0 connector	
PMC Slots	Air-cooled: Two 5V or 3V3, 32/64-bit IEEE P1386.1 compliant slots with front panel and P0 I/O, and restricted P2 I/O	
AFIX Slot	Air-cooled: 5V or 3V3, 32-bit @ 33 MHz with rear IO on P2 connector	
Serial I/O	COM1 & COM2: Fixed RS232 up to 150 kbaud COM3 & COM4: Equipped with clocks for synchronised operation. RS422/RS485 up to 10 Mbaud or RS232 up to 150 kbaud COM5 & COM6: RS422/RS485 up to 1.5 Mbaud or RS232 up to 150 kbaud Note: COM3 & 4	
Keyboard and Mouse	PS/2 compatible Keyboard and Mouse interface via the P2 connector	
Parallel I/O	Centronics style port via the P2 connector	
Floppy Disk Interface	MFM 1.44/2.88 Mbyte via P2 connector	
USB	5 USB 2.0 Ports connections via the P2 connector	
Counter/Timers	Four 32-bit timers with a resolution of one bus clock (133 MHz)	
Reset/Abort switch	Front panel mounted	
Operating Systems	LynxOS VxWorks/Tornado RTEMS	
PCI Expansion	PCI through P0 via PMCPCI card	
I/O Modules	P2 (3U mounting)	Six serial, Parallel, floppy Mouse and keyboard, Ethernet: 10/100/1000BaseT
	Miscellaneous	P2 transition module

4.3 EMC Regulatory Compliance and Safety

Air-cooled versions of PPC7D are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

All PCBs are manufactured by UL approved manufacturers and have a flammability rating of 94V-0.

4.4 Power Requirements

Table 4-3 Power Requirements

Supply Voltage	PPC7D-7447A 128 MB SDRAM	PPC7D-7447A 512 MB SDRAM	PPC7D-7448 512 MB SDRAM
+5V +5 %, -2.5 %	7A	7A	9A

These figures are based on a 1167 MHz MPC7447A running at 1133 MHz with a 133 MHz processor bus or MPC7448 running at 1400 MHz with a 133 MHz processor bus. The card was running a comprehensive memory test and gave measured values for +5V supply current of 5.1A for the 128 MB SDRAM version and 5.1A for the 512 MB SDRAM version.



NOTE

When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded, especially from the +5V supply. The VME specification allows a maximum of 7.5 Amps to be drawn from the +5V supply in a single slot over the PPC7's specified operating temperature range. It may not be possible to support all combinations of SDRAM and PMCs within this limit.

The PPC7D uses the undefined pins (rows a, c, d and z) of the VMEbus P2 connector for I/O and power/ground connections. 3.3V is connected to both of the PMC sites.



WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly.

If such conditions occur, toxic fumes may be produced due to the destruction of components.



CAUTION

Only use the PPC7D in backplanes that supply power on both the J1 and J2 connectors.

4.5 VMEbus Compliance

The PPC7D conforms to the ANSI/VITA 1-1994 standard for VME64.

Table 4-4 VMEbus Compliance

Function	Details
Master:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Slave:	A16, A24 and A32 ADO, ADOH A16:LCK, A24:LCK, A32:LCK D08(EO), D08(EO):RMW, D08(EO):BLT D16, D16:RMW, D16:BLT D32, D32:RMW, D32:BLT, D32:UAT D64:MBLT
Interrupt Handler:	D08(O), IH(1-7)
Interrupter:	I(1-7)
VMEbus Arbiter:	SGL, RRS, PRI, BCLR~ generation
VMEbus Requester:	ROR, RWD Early BBSY~ release Bus capture and hold
Bus Time-out Module:	16, 32, 64, 128, 256, 512, 1024 µS, disabled
Other Slot 1 Functions:	Slot 1 detector, IACK~ daisy chain driver, SYSCLK driver
Auto Slot ID:	VME64 specified and SCV64 compatible modes or geographical addressing via 5-row P1 connector

4.6 Reliability (MTBF)

The following table shows the predicted values for reliability as mean time between failures (MTBF) and failures per million hours (fpmh).

The predictions are carried out using MIL-HDBK-217F Notices 1 and 2, parts count method. To complement the 217 failure rates, some manufacturers' data is included where appropriate; πQ values have been modified according to industry practice.

Table 4-5 PPC7D MTBF

Environment	Fail Rate (Failures Per Million Hours)	MTBF (Hours)
Ground benign 30°c	5.26077637	190,086
Ground fixed 40°c	14.16823	70,580
Ground mobile 45°c	28.64494	34,910
Naval sheltered 40°c	23.84286	41,941
Naval unsheltered 45°c	44.53262	22,455
Airborne inhabited cargo 55°c	31.88514	31,363
Airborne inhabited fighter 55°c	44.41306	22,516
Airborne uninhabited cargo 70°c	58.26652	17,163
Airborne uninhabited fighter 70°c	88.25236	11,331
Airborne rotary wing 55°c	62.07256	16,110
Space flight 30°c	4.8155461	207,661
Missile flight 45°c	66.17372	15,112
Missile launch 55°c	158.4469	6,311

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted PMCs.

4.7 Ordering Information

This product configuration matrix is subject to change. Additional options may be available, and some configurations might not be available. Minimum order quantities may also apply. Please contact Abaco Systems for questions at https://www.abaco.com/support.

0	-	X	X	X	X	X	X	X	X	
										AFIX
										0 = No AFIX fitted
										1 = AFIX1553 (single channel)
										2 = AFIX1553 (dual channel)
										3 = AFIXSG (8 bit SCSI)
										4 = AFIXSG (16 bit SCSI)
										5 = AFIX1553 (single channel with side-band signals)
										6 = AFIX1553 (dual channel with side-band signals)
										7 = AFIXM (1GB Flash memory)
										8 = AFIXM (2GB Flash memory)
										9 = AFIXDIO1 RS232/422 Digital IO
										A = AFIXDIO1 USB2.0 Router
										SOFTWARE
										1 = SilverChip
										2 = BIT/SilverChip
										3 = VxWorks
										4 = BIT/VxWorks
										5 = PPCBoot
										6 = BIT/PPCBoot
								P0 CONNECTOR OPTIONS		
										O = No P0
										A = TYPE A
										B = TYPE B
							COMMS OPTIONS/P2 PMC I/O			
							1 = 1 x 10/100/1000 P2 + 1 x 10/100/1000 P0, P2 PMC I/O			
							2 = 2 x 10/100 P2, P2 PMC I/O			
							A = 1 x 10/100/1000 P2 + 10/100/1000 P0, COMS 3/4/5/6			
							B = 2 x 10/100 P2, COMS 3/4/5/6			
							C = 1 x P2 & P0, P2 PMC I/O, COMS 3/4/5/6			
							D = 2 x P2, P2PMC I/O, COMS 3/4/5/6			
					Flash / USB					
							0 – 3 = Reserved			
							4 = 128MB USB			
							5 = 128MB Keyboard, Mouse			
							6 - 7 = Reserved			
							8 = 256MB, USB			
							9 = 256MB, Keyboard, Mouse			
							A = 512MB, USB			
							B = 512MB, Keyboard, Mouse			
				MEMORY						
							0 - 4 = Reserved			
							5 = 512MB			
							6 - 8 = Reserved			
							9 = 1GB			
			PROCESSOR							
							0 – F = Reserved			
							G = 7448 @ 1.4 GHz			
							H = 7448 @ 1 GHz			
		BUILD LEVEL								
		1, 2, 3, 4, 5								

NOTES

P0 options are available on all build levels.

Due to the large amount of I/O required to be handled by the PPC7D, Type B (95-way) connectors are preferred to Type A (80-pin) and are fitted by default no particular type is specified.

4.8 P2 I/O Modules (3U)

The Backplane Transition Module for the PPC7D is the P25X606A.

LINK

For installation instructions and pin assignment information, refer to the I/O Modules Manual, Publication Number RT5154.

5 • Troubleshooting

If you are experiencing a problem with your PPC7D, there follow some general suggestions of actions you may take, which may resolve the problem without the need to contact Abaco's technical support.

- Ensure that the board is firmly seated and secured in the rack and that all male/female connectors mate together correctly
- Check the links on the board and the system backplane
- If you are unsure of which link configuration to use, try the default configuration (see the Link Settings section) initially
- Check that the VME rack has terminators, if these are not built in (the manual for your rack should tell you whether the terminators are built in)
- Using a digital voltmeter, check that the power supply is within VME limits on +5V, +12V and -12V



WARNING

Power supply problems should only be dealt with by qualified personnel.

- Check that there is only one board configured as system controller in a system and that this is in slot 1 of the rack
- Check that there are no vacant slots in the rack without jumpers (or that an automatic daisy chaining backplane is being used)
- Prove the PPC7D's operation in isolation before adding it into a multi-board system
- If you have made your own cable for connection between P7 or P2 and a terminal/hyperterminal, check that the pinout is correct
- Check that the terminal is set up for DTE (9.6 kbaud, 8 bits/character, 1 stop bit, parity disabled)
- Ensure that air-cooled PPC7Ds receive sufficient airflow. If you need to operate your PPC7D on an extender card, this requires an additional fan to supply the necessary air flow
- Ensure that conduction cooled PPC7Ds are fully installed in the conduction cooled box and that the wedgelocks are correctly tightened. If, for any reason, you need to operate a conduction cooled PPC7D on an extender card, you must maintain an airflow of at least 300 feet/minute over it

If you are having problems programming the Flash, then check that the appropriate write enable link, E10 or E11, is fitted, and that the backplane signal, Flash_WP~ (P0 pin A2) is connected to GND or E9 is fitted. See the Flash section and the E9, E10 and E11 descriptions in the Link Settings section for more details.

6 • Glossary

NOTE

See the general Abaco Glossary, Publication Number RT5116.

BCS

Background Condition Screening.

CR/CSR

Configuration ROM/Control and Status Register.

LRU

Line Replaceable Unit.

PPC7D

Abaco's PowerPC-based processor card. The PPC7D is based on the PowerPC 7447A or 7448 processor with integral L2 cache controller and uses DDR SDRAM.

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