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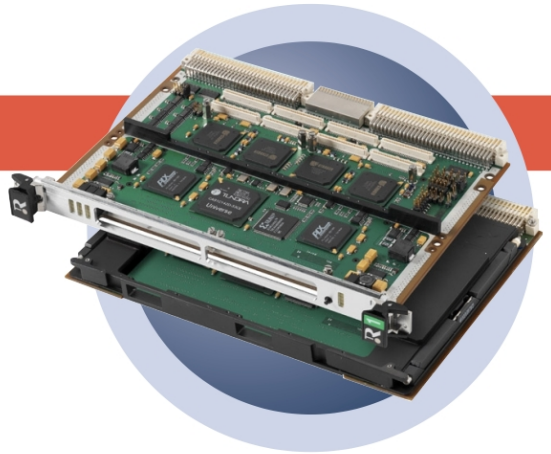
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HARDWARE PRODUCT MANUAL



StarSwitch Product Manual
Publication No. STARSW-0HH/2
2nd Edition, May 2007

FANUC | RADSTONE EMBEDDED COMPUTING

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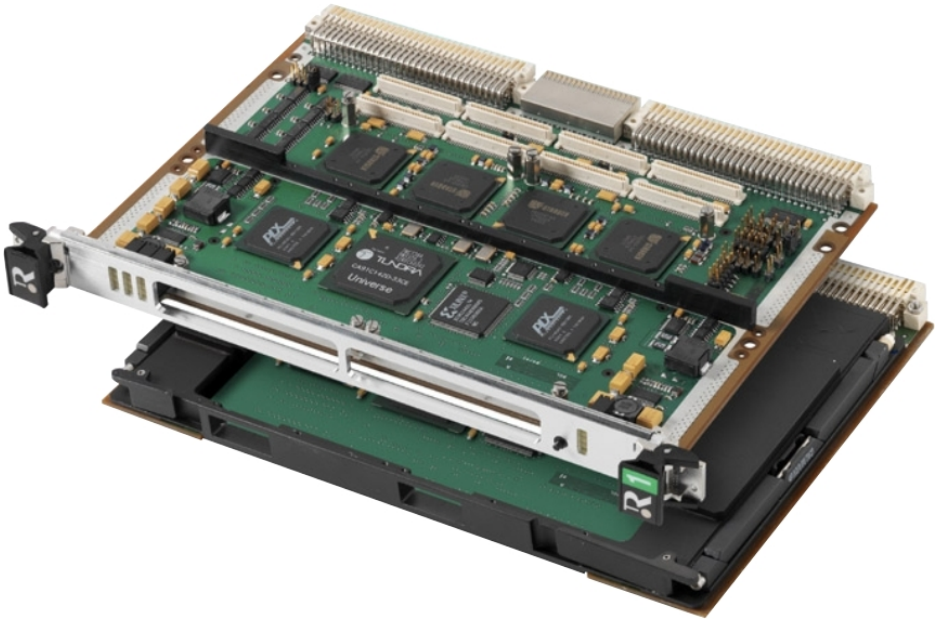
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1. Introduction



StarSwitch is a multipurpose StarFabric Switch/ Dual PMC Carrier Card. It operates as a 4-port switch to support a 3 or 5-slot P0-StarFabric point-to point backplane or chassis-to-chassis connection. P0-StarFabric offers much higher bandwidth than PCI solutions. The StarSwitch is primarily aimed at supporting Radstone's flagship G4DSP-XE StarFabric-enabled multiprocessor host.

StarFabric is currently the fastest datacomms technology available for use with the VME P0 connector standard. It has a signaling speed of 622 Mbits/s per signal pair, which equates to 2.5 Gbits/s per StarFabric port.

StarSwitch's four P0-StarFabric ports can be used as a pair of bundled links for small high performance systems, allowing a high sustained bandwidth to both PMC sites concurrently. Interrupts from the PMC sites are routed either via StarFabric or directly off-board for minimized latency using an interrupt mapper. StarSwitch's use of both switch and bridge functions allow traffic on any port to be routed to either PMC site, or switched (re-routed) off-board. Any number of StarSwitches can be used together with one or more StarFabric-enabled host to form large fabric networks

StarSwitch additionally allows VME access to both PMC sites. The on-board bridges permit PCI-X-enabled PMCs to be used at 100 MHz and to isolate PMC traffic from each other. The combination of VME and StarFabric access to PMCs provides a means of separating low-latency control-plane data from bulk data transfers such as DMAs.

Features

- Dual StarFabric PMC access
- StarFabric P0-backplane switch functionality
- Dual VME access allowing PCI-X enabled PMCs to bridge to VME
- PMC sites have all 64 pins of user I/O mapped to P2 or P0 connectors
- Support for 100 ohm differential pairs to P2 for high speed 3rd party I/O
- High power on-board supplies to support processor PMCs, X-PMCs
- Semi-redundant architecture for restricted maintenance applications

Associated Documents

Radstone Documents

The Radstone Product Manuals CD-ROM allows privileged access to an Internet resource containing the latest updated documents.

Radstone PMC Installation Note, publication number HN4/3-99.

Radstone I/O Modules Manual, publication number RT5154

Radstone G4DSP-XE VxWorks BSP Application Notes, publication number G4DSP-XE-BSPTOR-YN1

Radstone StarSwitch BIT User Guide, publication number - Not Yet Available.

Product Data

Due to the complexity of some of the parts used on the StarSwitch, it is not possible to include all the detailed data on all such devices in this manual. The following is a list of the specifications and data sheets that provide any additional information required:

VME

VME64 Specification ANSI/VITA 1-1994 April 1995. *VMEbus International Trade Association*

VME64 Extensions Specification. Not Yet Published. *VMEbus International Trade Association*

ProcessorPMC Specifications. ANSI/VITA-32. July 2003. *VMEbus International Trade Association*

Universe II User Manual 1998. *Tundra Microsystems ON K2K 2M5 Canada.*

PCI

PCI Local Bus Specification, Draft Rev 2.2. 8 June 1998. *PCI Special Interest Group OR 98214 USA.*

IEEE P1386 Draft Standard for a Common Mezzanine Card Family.

IEEE P1386.1 Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards.

StarFabric

StarFabric is a proprietary Standard. Its protocol is not covered by a world-wide standards association

Though it is qualified for use in CompactPCI racks by PICMG. See PICMG 2.17. *(PCI Industrial Computers Manufacturers Group)*

StarFabric also has its own Trade Association. Information is best Obtained Via Stargen Incorporated, MA, USA / www.Stargen.com

World Wide Web Sites

Radstone on the world-wide-web is available at:

http://www.radstone.co.uk

or

http://www.radstone.com

Conventions Used in this Manual

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a 'D' subscript and binary numbers have a 'b' subscript. The prefix '0x' shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12D = 0x0C = 1100b

The multipliers 'k', 'M' and 'G' have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when 'K', 'M' and 'G' mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.

When describing transfer rates, 'k' 'M' and 'G' mean $*10^3$, $*10^6$ and $*10^9$ not $*2^{10}$, $*2^{20}$ and $*2^{30}$. In PowerPC terminology, multiple bit fields are numbered from 0 to n, where 0 is the MSB and n is the LSB. PCI and VMEbus terminology follows the more familiar convention that bit 0 is the LSB and bit n is the MSB.

Signal names ending with a tilde (~) denote active low signals; all other signals are active high.

Filenames are shown in bold, e.g. **apps/code.exe**.

System messages and function names are shown in courier typeface, e.g. `mapvme`. User input is shown in bold courier typeface, e.g. **`user input`**.

'↵' represents the Enter, ↵, Return etc. key on your keyboard.

This manual uses three types of notice: notes, cautions and warnings.

1. Notes call attention to important features or instructions, and are shown as follows:

Note: This is an example note entry.

2. Cautions, which take the following form, alert you to system danger or loss of data.

CAUTION

This is the form a caution takes

3. Warnings, which take the following form, alert you to the risk of severe personal injury.

WARNING

This is the form a warning takes

Safety Notices

Safety Summary

Observe the following general safety precautions during operation, service and repair of this equipment. Failure to comply with these precautions or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Radstone Limited trading as Radstone Technology assumes no liability for the user's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Radstone is aware. Take note of these warnings and take all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Equipment

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

⚠ WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components

⚠ WARNING

Power supply problems to be dealt with only by qualified personnel

All Radstone circuit boards are manufactured by UL-recognized manufacturers and have a flammability rating of 94V-0.

⚠ CAUTION

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection

Radstone boards are designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

Radstone boards also comply with EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

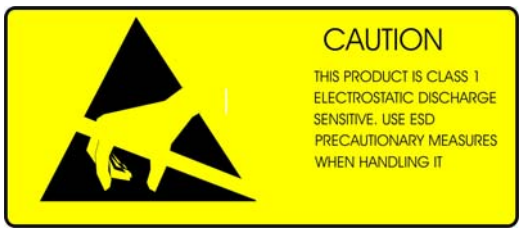
There are ***no*** PROMs or other user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should not attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it (e.g. the processors). Removal and re-attachment of the heatsink should only be carried out by Radstone.



2. Inspection

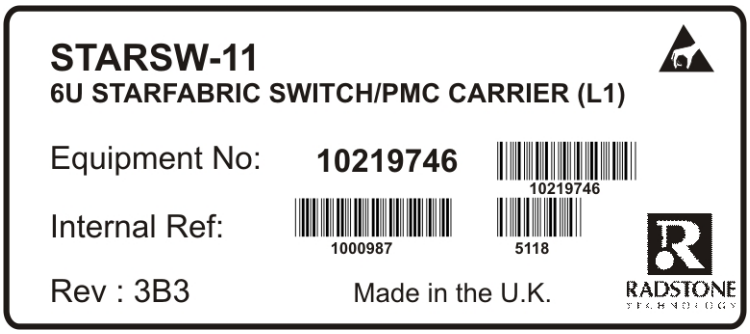
Observe antistatic precautions (wear an antistatic wrist-strap connected to an Earth point and work at an approved antistatic work station) when handling the board.



Product Identification

Radstone hardware products are identified by labels fixed at strategic positions. You can cross-check these against the Advice Note provided as a separate note with your delivery.

On the outside of the shipping box, and the antistatic bag, there is a label similar to the following form:



On the card within the antistatic bag, there are identifying labels, similar to the following, attached to the printed wiring board. These are fitted in the most suitable locations, which may include the reverse of the board.

The label gives the board's Product Code (see Appendix A for more details), Equipment Number and Revision. An example follows:

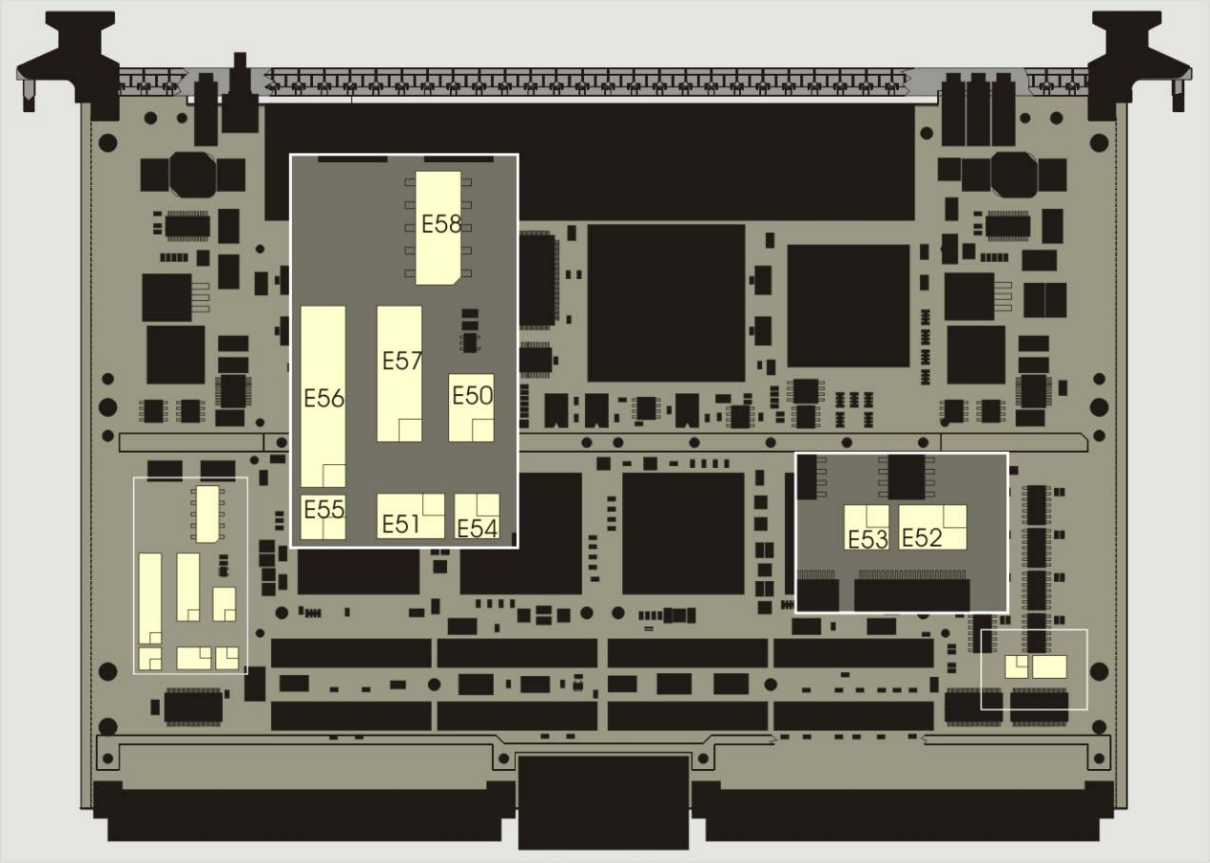
MADE IN UK	STARSW-11	REV
Equ No.	10219746	3B3

On conduction-cooled versions of the board, there is also a label attached to the front panel giving the board's order number, as follows:



3. Configuration

Positions of Headers and Links



Shown are standard 2.54mm pitch headers for general use.

CAUTION

Jumper links, which are included in the Radstone standard kit of parts, are suitable for level 1-3 low vibration applications. Additional jumpers may be obtained from Radstone if required. However, for Level 4 products it is advised that jumper links are made by wire-wrapping between the pin posts and then covering the wire wrapped links with the same conformal coating as that used on the board. This will provide a reliable connection under heavy shock and vibration conditions and further prevent oxidation of the connection due to moisture ingress.

Jumper Descriptions

Note: Ordinary operation of the board requires no links to be fitted.

Header/ Link	Link	Description	Standard Configuration	Function
E50	Pin 1-2	VCC (5V for programming)	Not fitted	Provides 5 Volt to programming cable
	Pin 3-4	CPLD only loop	Not fitted	Fit only to program CPLD
	Pin 5-6	Full JTAG loop	Not fitted	Fit only for Electrical test
E51	Pin 1-2	PMC site 2 : FID	Not fitted	Multiple redundant fabric troubleshooting
	Pin 3-4	PMC site 2: force 33MHz	Not fitted	To debug problems with 66 MHz PMCs
	Pin 5-6	PMC site 2: ROM_HOLD	Not fitted	To recover SROM after corruption
E52	Pin 1-2	PMC site 1: FID	Not fitted	Multiple redundant fabric troubleshooting
	Pin 3-4	PMC site 1: force 33MHz	Not fitted	To debug problems with 66 MHz PMCs
	Pin 5-6	PMC site 1: ROM_HOLD	Not fitted	To recover SROM after corruption
E53		PMC site 1 VIO select	Match PMC VIO 5/3V3	See Configuring PMC sites
E54		PMC site 2 VIO select	Match PMC VIO 5/3V3	See Configuring PMC sites
E55		Select VME Address Space for Universe registers at power up	A32, A24 or A16 space (see VME section)	See Configuring VME Address Space
E56		Select VME Address for Universe registers at power up	VME base address (see VME section)	See Configuring VME Address
E57	Pin 1-2	PMC 2 Monarch	Not fitted	Use with Monarch PMCs
	Pin 3-4	PMC 1 Monarch	Not fitted	Use with Monarch PMCs
	Pin 5-6	PMC2 SG2010 Bridge Mode Enable	Not fitted	Bridge Enable 2
	Pin 7-8	PMC1 SG2010 Bridge Mode Enable	Not fitted	Bridge Enable 1
	Pin 9-10	Configuration_2	Not fitted	Reserved/ CPLD config2
	Pin 11-12	Configuration_1	Fit to enable VME interrupts	Reserved/ CPLD config1
E58		JTAG connector header	Not fitted	Only use for Firmware update

JTAG Chain (E50)

There should be no need for a customer to use these links apart from in the case of an in-field firmware upgrade, which will normally be carried out by a Radstone Field Applications Engineer.

PMC Site Special Links (E51, E52)

There should be no need to have any of the links fitted on E51 or E52 during normal operation of the board. During development, some of these special functions may prove valuable in debugging. See the Troubleshooting section for more details.

Configuring the PMC Sites (E53, E54)

The VIO supply for the PCI signalling of the PMC sites is determined by the position of the link on either the E53 header (for PMC site 1) or the E54 header (for PMC site 2). The correct position of the link for both headers is shown below:

StarSwitch routes 5V power to each PMC site from the backplane, which is decoupled near the PMC site connectors. StarSwitch also provides 3V3 volts to the PMC sites from its on-board 3V3 power supplies. A maximum current of 4.5 Amps should be drawn from the 3V3 by each PMC site. This additional 15 watts (approx) of power should be sufficient to power dual processor-PMCs and other high performance PMCs on the market.

PMC SELECTED FOR 3.3V VIO



PMC SELECTED FOR 5V VIO



Configuring the VME Address and Address Space (E56, E55)

To access PMCs via VME using StarSwitch it is essential that the Tundra Universe registers can be set up externally over VME by the host processor. As no software runs on StarSwitch, jumpers set up the location of the Universe registers in VME address space from power-up, as shown below. Subsequently, software can set the VME base address and size of the windows needed to allow access to the PMC sites over the VME bus. The location of the Universe registers can also be changed.

Note: If two or more StarSwitches are included in a system, their jumpers must be set differently to ensure exclusive access by the host from power up. StarSwitch allows VME bus access to the Universe's 4 KByte Register Access Image at power up.

E55 – VME Address Space

E55 JUMPER LINK POSITION			VME ADDRESS BIT	
PINS 1 TO 2	PINS 3 TO 4	ADDRESS SPACE	A30	A29
No link	No link	A16	0	0
No link	Link fitted	A24	0	1
Link fitted	No link	A32	1	0
Link fitted	Link fitted	Illegal	1	1

Continued

E56 – VME Address

	VME Address Bit							
	A28	A27	A26	A25	A24	A23	A22	A21
E56 Jumper Link Position	1/2	3/4	5/6	7/8	9/10	11/12	13/14	15/16

However, the actual address that is set depends also on the VME space according to the following table taken from the Tundra Universe manual.

Address Space	Address bits		
	31:24	23:16	15:12
A16	00	00	E55 setting
A24	00	E55 setting	00
A32	E55 setting	00	00

Examples

1. If all links are fitted on E56, and pins 1-2 of E55 are fitted, the VME register Image is at 0xFF0 0000 in A32 space.
2. If links are fitted to pins 1-2, 3-4, 5-6, 7-8 on E56 and no links are fitted to E55, the VME register Image is at 0x0000 F000 in A16 space.

VME Interrupts (E57)

The routing of interrupts on StarSwitch is under firmware control. By default, StarSwitch combines interrupts from the PMC sites to the P0 connector, as more fully explained in the interrupt mapper section.

Radstone intend to support a number of interrupt mapping options, which are to be developed according to customers wishes, without the need for any special configuration control. Customers should contact Radstone Technology to ensure they have the latest information on interrupt routing.

4. Power Up and Reset

First Time Switch On

No special precautions are required for first time use. It is not possible to damage the board with incorrect jumper settings.

Ideally, the jumper links should be set up before powering. Generally, only the VME address and (if used) the PMC IO voltages need to be considered.

LED Display

On power-up, before any external connections are made or any PMCs fitted, StarSwitch should light 6 blue power LEDs, plus 12/24 (depending on level) yellow LEDs, which may be flashing from power up. This indicates that all the voltage rails are powered and that all the on-board StarFabric links are intact.

Reset Sequence and Timing

From the application of 5 volt power to all components being out of reset takes (typically) 250 ms.

Since the ramp-up times of the 5V system PSU and the on-board 3V3 PSUs will vary with load, the time taken for the board to come out of reset will vary from system to system. It is the responsibility of software to account for this.

The StarSwitch power-on-reset sequence has the following order:-

1. Wait for 5V rail to reach 4.6 volts
2. Start P3V3 power supplies
3. Wait for Power Good signal
4. Start P1V5 power supplies
5. Wait for Power Good signal
6. Synchronous delay to allow PLLs to synchronise
7. Release Reset to SG2010, and PMC sites 1 and 2 synchronized to respective PCI clocks
8. Wait for SG2010 Reset output
9. Release Reset to SG1010
10. Release Reset to Universe II and PLX PCI-PCI Bridges

Note: The sequence and timing of releasing the resets, once the PSUs are stable, are configurable in code and may be changed if there is any particular requirement for a given system, e.g. Fast VME access on start up. Customers should contact Radstone if they have particular reset requirements.

VME Reset Capabilities of StarSwitch

With ordinary (non processor PMCs fitted):

- The board receives VME_SYSRESET, but does not drive it.
- VME_SYSRESET is directly coupled to the VR_SYSRESET of the Tundra.
- The Tundra receives PON_RESET at power up and loads in its default power up options.
- Excepting the power-on defaults of the Tundra, all other functions are reset when it receives VR_RESET.

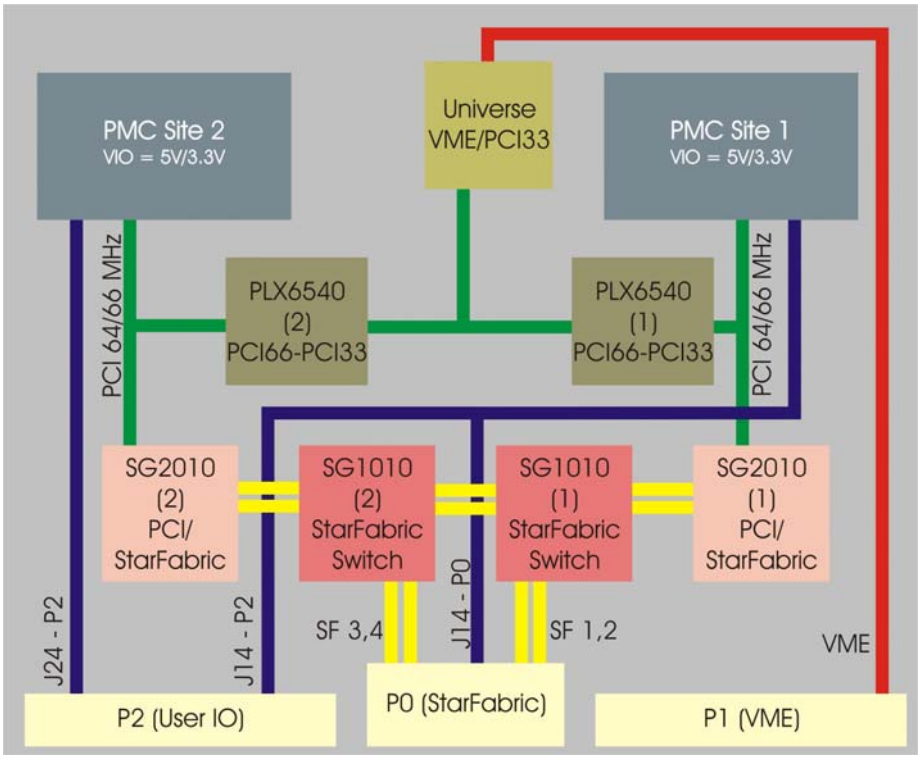
In response to VR_RESET, the Tundra generates a LOCAL_RESET as an output. LOCAL_RESET is used to reset all of StarSwitch's StarFabric and PCI devices, plus any PMC mounted on StarSwitch.

The default configuration means that the Tundra can not be reset by any PCI device, but only over VME by an external board.

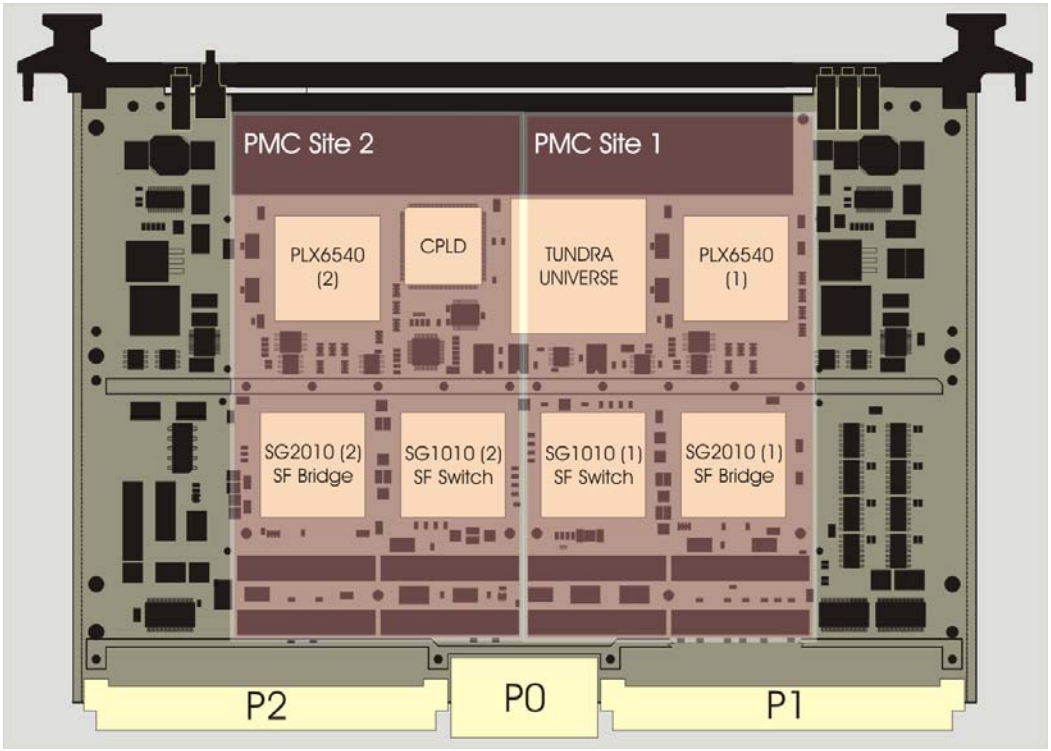
All devices can be reset by a front-panel reset on level 1 cards, and this is equivalent to a power–up hard reset, even though there is no power cycling. The Tundra will reload its power up defaults.

5. Functional Description

Functional Block Diagram



Component Layout



VME Operation

VME Access of PMCs

The Tundra Universe IID is used as the VME interface on the StarSwitch. It can access both PMC sites via the PLX6540 PCI-PCI bridge devices, and it includes a DMA engine with Linked-List mode (Scatter/Gather) support.

While StarFabric is extremely well suited to large bulk data movements such as DMA-based writes, the VME protocol still retains advantages for small control-plane, low byte-count, read and write operations that involve rapid bus reversal. StarFabric may incur significant latency in read operations when obtaining the first byte of the information, say. Therefore, it is not an efficient use of bandwidth to use StarFabric for read-write-read-write ping-pong accesses. The overall rate will be disappointing.

For example, a PMC that streams out live video can make use of StarFabric for its main data output, but could use VME write accesses to set up or read its control registers.

VMEbus Master Access

Four general purpose software-programmable PCI slave images are available for access to the VMEbus. All of these can be configured to access VMEbus A32, A24 or A16 address space.
The following points also apply:

- An offset may be applied to translate the local address to a different address on the VMEbus, allowing any local address to access any VMEbus address.
- The start and end addresses of the A32, A24, and A16 PCI slave images may be set on any 64 KByte boundary in the 1 GByte (approx.) of PCI bus memory or I/O space (addressable by the processor) that is not allocated to other PCI attached devices.
- One image may be set on 4 KByte boundaries to accommodate access to A16 space.

One further ‘special purpose’ PCI slave image allows mapping of A16 and A24 space. The image uses a 64 MByte window, aligned to any 64 MByte address in PCI memory space.

The window is divided into four 16 MByte quadrants. The top 64 KBytes of each quadrant maps to A16 space, while the rest maps to A24 space. The Address Modifiers generated are software configurable for each quadrant.

VMEbus master cycles may be either coupled or write-posted.

- Coupled cycles are retried on the PCI bus until the Universe II has ownership of the VMEbus and are not terminated on the PCI bus until all data has been transferred over the VMEbus.
- Posted writes are queued in a FIFO until the VMEbus is available for the data to be transferred.

VMEbus Slave Access

Four general purpose software-programmable VMEbus slave images are available. All of these may be defined in VMEbus A32, A24 or A16 space. An offset may be applied to translate the VMEbus address to a different address on the local bus, allowing any VMEbus address to access any on-board address. The start and end addresses of the A32, A24 and A16 images may be set on any 64 KByte boundary.

One further special purpose VMEbus slave image, the Register Access Slave Image, allows a VMEbus master to access the Universe’s control and status registers.

VMEbus slave accesses to the G4DSP-XE may be coupled, write-posted or pre-fetched block read.

- Coupled slave transfers can only proceed once the slave posted-write FIFO is empty.
- Slave posted-write cycles are queued in a FIFO until the PCI bus is available for the data to be transferred.

Indivisible Cycles on VME

The Universe can be programmed to generate Read-Modify-Write (RMW) cycles on the VMEbus. Data from the read portion is compared with a 32-bit compare value, qualified with a 32-bit mask. If the comparison is true, then those bits enabled by the mask are swapped with a 32-bit swap field.

Alternatively, the Universe chip's VMEbus-ownership-bit may be set to cause it to acquire and hold ownership of the VMEbus. This method can be used in combination with VMEbus LOCK cycles to guarantee exclusive access to a VMEbus resource.

The Universe also supports VMEbus lock commands using ADOH cycles.

Slave RMW cycles on the VMEbus are handled by programming the Universe II to transform all incoming non-block read cycles into locked PCI cycles.

VMEbus Master Block Transfers (MBLTs)

The Universe's DMA controller can be used to transfer data between the PCI bus and the VMEbus using D32 or D64 transfers. DMA operations on the two buses are decoupled through a bi-directional FIFO. The DMA controller can:

- Transfer multiple blocks of data using entries in a linked-list
- Pack and unpack data to support differing data widths on the PCI bus and the VMEbus
- Generate an interrupt on completion or on encountering an error condition

VMEbus Slave Block Transfers (BLTs)

The VMEbus slave interface can respond to D32:BLT and D64:MBLT. For VMEbus slave block transfers, the Universe chip may be programmed to pre-fetch read data, which is queued in a FIFO.

Mailboxes

The Universe II contains four 32-bit mailboxes that, when written to, can generate interrupts on the PCI bus or on the VMEbus. Each mailbox has separate status, enable and interrupt mapping bits.

Semaphore Register

The Universe II provides a 32-bit register containing four semaphores, one in each byte. Each of the four semaphores is a 7-bit data field plus a 1-bit lock field.

Ownership of the semaphore is obtained by writing a unique value to the 7-bit field whilst setting the lock bit. The write is only accepted if the lock bit is not already set. Ownership can be confirmed by reading back the value in the 7-bit field after the write, and comparing it with the unique value written.

The semaphores can be used to guarantee exclusivity of access to a resource shared between:

- Multiple processes
- Processes and bus masters (PCI or VME)
- Bus masters (PCI or VME)

VMEbus Interrupts

The Universe II can be used to generate VMEbus interrupts It can not, however, be set to receive VME born interrupts, nor handle VME interrupts, unless a processor PMC is mounted on at least one of the PMC sites. The Universe II can be programmed to generate any level of VMEbus interrupt (IRQ0 – IRQ7) when it receives an interrupt on IRQ0 (PMC1) or IRQ1 (PMC2) on its PCI side.

VME Bus Errors

Assertion of VMEbus BERR~ during a coupled VMEbus master cycle causes a target-abort (bus error) on the PCI bus. A PCI target-abort during a coupled VMEbus slave cycle causes BERR~ on the VMEbus.

A bus error during posted write transfers raises an interrupt (if enabled) to the processor. Several options are available, including stopping the operation and purging the offending transaction.

A bus error during a DMA operation raises an interrupt and stops the DMA operation on the bus where the error was detected.

VMEbus Retries

The StarSwitch does not support the VMEbus RETRY~ signal.

Default VME Power Up Options

Default VME Power Up Options are:

- VME register Access Slave Window: Enabled
- Address Space of Slave Window: A16, A24 or A32
- Address of Slave Window: Top 8 bit jumper selectable
- VME CR/CSR Slave Image Space: Memory
- VME CR/CSR Slave Image Offset: 0x00
- Auto-ID features: All Disabled
- BI-Mode: Disabled
- Auto Syscon Detect: Senses slot 1 but cannot be slot 1 card
- Auto /SYSFAIL assertion: Enabled
- PCI Target Image: Disabled

Interrupts

StarSwitch routes all interrupts through a CPLD, which enables flexible interrupt mapping. The CPLD code is identified as TB0667-xxx, where xxx is the production release revision.

With reference to the CPLD interrupt mapper, all interrupts are bi-directional and hence can be either outputs or inputs or both.

Interrupt sources supported by the default CPLD code are:

- PMC site 1 INTA, B, C, D Outputs from PMC1 to CPLD
- PMC site 2 INT A, B, C, D Outputs from PMC2 to CPLD
- SG2010 1 Input from PMC1 : INTA or INT B or INT C or INT D
- SG2010 2 Input from PMC2 : INTA or INT B or INT C or INT D
- Tundra PCI IRQ0 Input from PMC1 : INTA or INT B or INT C or INT D
- Tundra PCI IRQ1 Input from PMC2 : INTA or INT B or INT C or INT D
- PLX Primary 1 Disconnected
- PLX Primary 2 Disconnected
- PLX Secondary 1 Disconnected
- PLX secondary 2 Disconnected
- P0 pin A10 (*tristate*) output from PMC1 INTA or PMC2 INT B
- P0 pin B10 (*tristate*) output from PMC2 INTA or PMC2 INT B
- P0 pin C10 (*open drain*) output from PMC1: A,B,C,D or PMC2: A,B,C,D
- Rear Side Test PMC site Disconnected (debug only)

Interrupts are routed to SG2010 devices to be handled inside StarFabric, but they are also routed off board for direct connection to an External Host/ Interrupt handler. The STARPIO development rear IO transition module enables direct interrupt connection between a PMC hosted on StarSwitch and Radstone's G4DSP-XE.

The default configuration also allows for interrupts to be seen over VME via the Universe II.

The use of P0 pin C10, which is a logical OR of the interrupts from both PMC sites, is for larger systems. Since the G4DSP-XE has provision for four interrupts on its P0 connector (plus one more on P2), up to four StarSwitch boards can be supported by a single G4DSP-XE, but the interrupt handler must determine which PMC is sourcing the interrupt.
Small systems, with up to four PMCs hosted on two StarSwitches, would not need to use P0 pin C10

The P0:A10, P0:B10 interrupts from the StarSwitch are used as direct connections to the host interrupt handler and are not bussed with any other signal. Very large systems that require many StarSwitches must use the P0:C10 output only, and the interrupt handler software must determine the source of the interrupt.

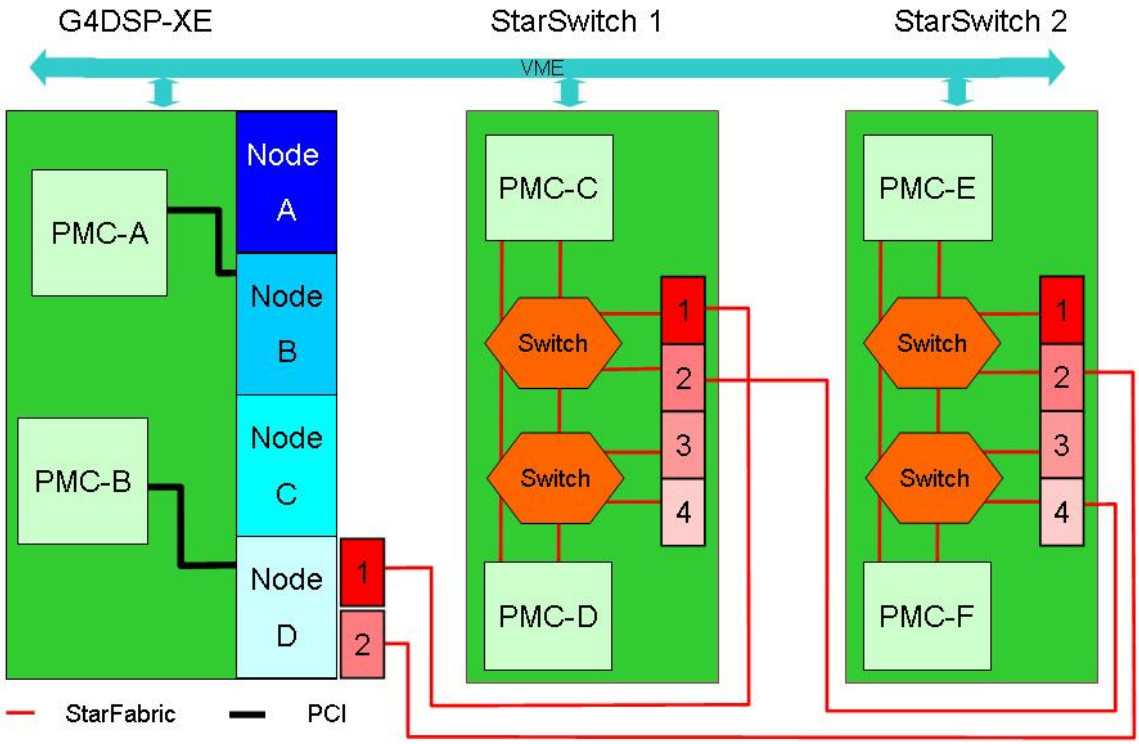
Note: The default CPLD code does not support Interrupts *to* PMC sites as required by processor PMCs. Customers requiring this facility should contact Radstone.

Interrupt Options

Radstone are aware that system developers may want to change interrupt configuration and are able to alter the interrupt connectivity for a particular system if so required. Options include:

1. A small number of different interrupt connectivity variations can be accommodated by the use of jumper selections without the need for customers to pay any configuration costs.
2. For development, Radstone may provide custom code free of charge – but it would be the customer's responsibility to reprogram the code into the boards. This is now a relatively simple operation.

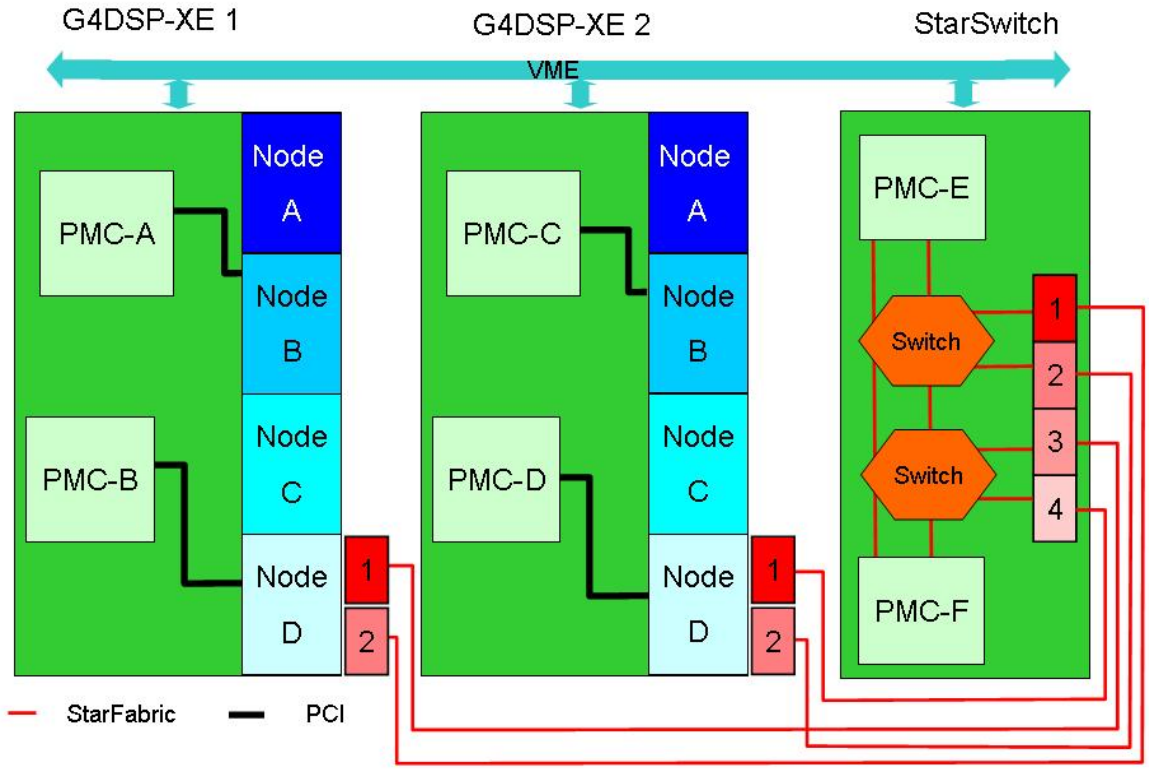
Example StarFabric System Connections



Example 1 – Typical System Diagram:

(2 G4DSP-XEs, 1 StarSwitch, 6 PMCs)

In Example 1, one G4DSP-XE supports four off-board PMCs via two StarSwitches. It can access any two off-board PMCs simultaneously. It can also access all off-board PMCs simultaneously using StarFabric multicasts. (Multicasts only available with non transparent bridging (path routing))



Example 2 - Higher Bandwidth and more balanced connection of entire system:
(2 G4DSP-XEs, 1 StarSwitch, 6 PMCs)

In Example 2, G4DSP-XE 1 can talk to PMC-E while G4DSP-XE 2 talks to PMC-F.

The G4DSP-XEs can also talk to each other simultaneously through their other SF Port.

Driver Software

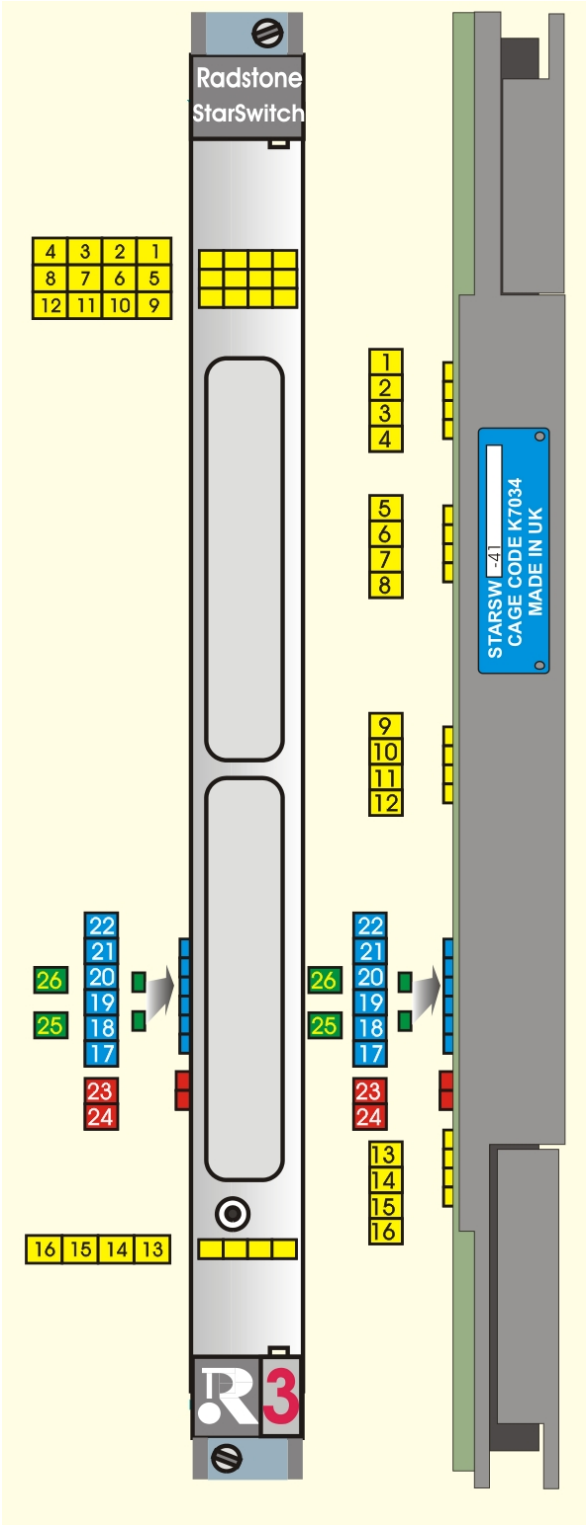
The StarSwitch driver software is incorporated into the G4DSP-XE BSP. Details of the functions and the required parameter settings can be found in the VxWorks On-line Help document **rsg4dspx.htm**, under *starSwitchDriver*. See the G4DSP-XE VxWorks BSP Application Notes for details.

6. Front Panel and LED Display

The table and diagram below describes the nomenclature and function of the LEDs for all build levels.

LED Number (Schematic)	LED Number (As Shown)	Description
DS523	1	SG1010_2_PORT_0 (on-board)
DS522	2	SG1010_2_PORT_1 (on-board)
DS521	3	SG2010_2_PORT_0 (on-board)
DS520	4	SG2010_2_PORT_1 (on-board)
DS519	5	SG1010_1_PORT_0 (on-board)
DS518	6	SG1010_1_PORT_1 (on-board)
DS517	7	SG2010_1_PORT_0 (on-board)
DS516	8	SG2010_1_PORT_1 (on-board)
DS515	9	SG1010_1_PORT_2 (on-board)
DS514	10	SG1010_1_PORT_3 (on-board)
DS513	11	SG1010_2_PORT_2 (on-board)
DS512	12	SG1010_2_PORT_3 (on-board)
DS503	13	SG1010_1_PORT_5 (off-board)
DS502	14	SG1010_1_PORT_4 (off-board)
DS501	15	SG1010_2_PORT_5 (off-board)
DS500	16	SG1010_2_PORT_4 (off-board)
DS506	17	5V (power)
DS507	18	P2V5 (power)
DS508	19	P1V5_PMC2 (power)
DS509	20	P3V3_PMC2 (power)
DS510	21	P1V5_PMC1 (power)
DS511	22	P3V3_PMC1 (power)
DS505	23	BIT Fail 1(PMC 1)
DS504	24	BIT Fail 2 (PMC 2)
DS900	25	User LED 2
DS901	26	User LED 1

Level 1 to 3 **Level 4**



LED Operation

For correct operation LEDs 1 to 12 should be constantly lit, (following software enumeration) indicating all on-board StarFabric links are active and traffic is enabled. Blinking LEDs show traffic is disabled or there is a corrupted link.

LEDs 13 to 16 should be lit if an off-board connection is made.

LEDs 17 to 22 are power supply ‘good’ indicators and all should be lit whilst StarSwitch is operable.

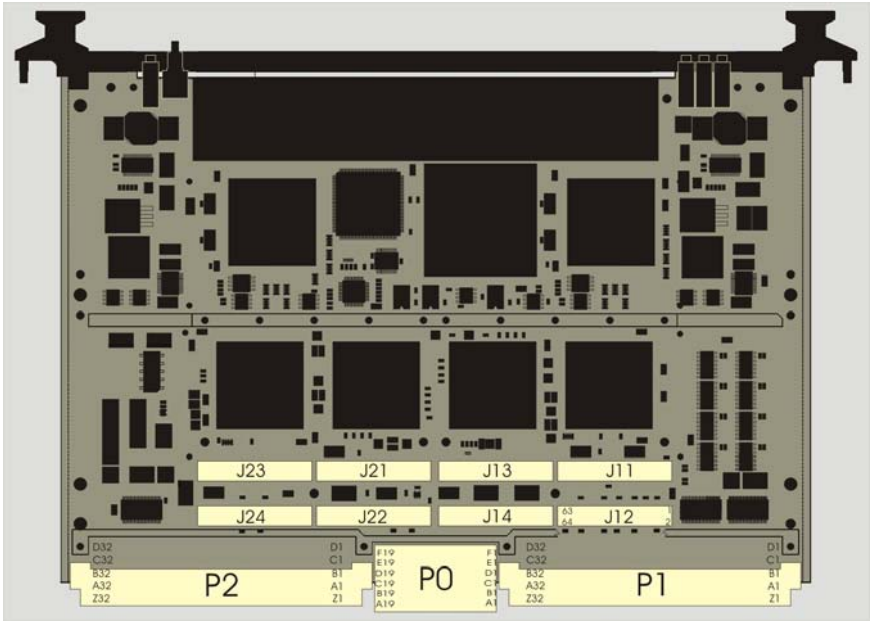
LEDs 23 and 24 remain lit after BIT has run and an error has been detected. These LEDs have no meaning if Radstone StarSwitch BIT is not being used.

LEDs 25 and 26 are not used by current firmware and will remain unlit.

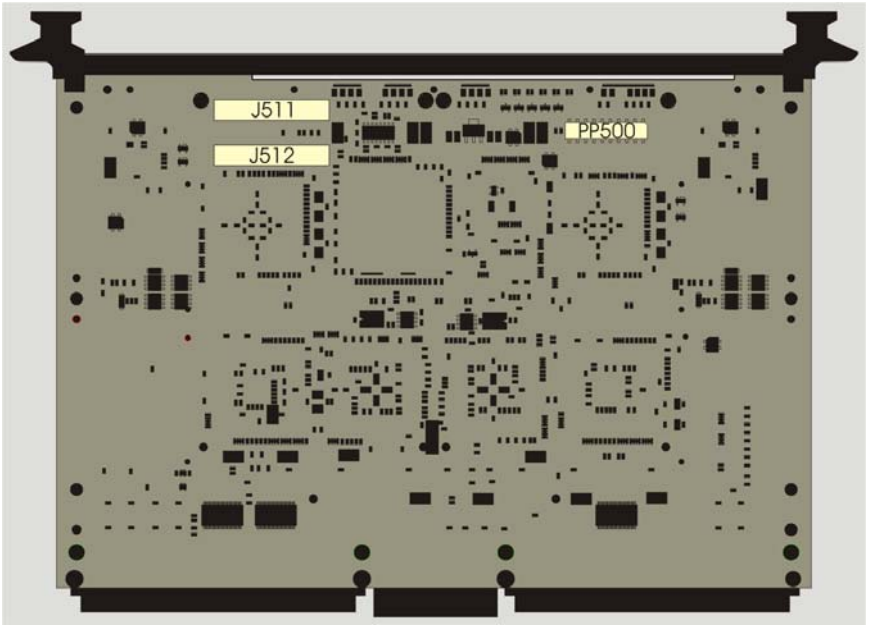
7. Connectors

Connector Positions

Front Layout



Rear Layout Showing Development Options



J511 and J512 indicate vacant header locations. Fixing headers in these positions enables interrogative access to the PCI bus between the Tundra Universe and the PLX bridges.

PP500, similarly, can provide debugging opportunities when used in conjunction with StarView software.

Note: Fitting headers to the J511, J512, and PP500 locations is an operation that must be performed at Radstone to maintain the validity of the warranty on the StarSwitch.

P1 (VMEbus) Connector Pin out

Pin ID	Row Z	Row A	Row B	Row C	Row D
1	NC	D00	BBSY~	D08	VCC
2	GND	D01	BCLR~	D09	GND
3	NC	D02	ACFAIL~	D10	NC
4	GND	D03	BG0IN~	D11	NC
5	NC	D04	BG0OUT~	D12	NC
6	GND	D05	BG1IN~	D13	NC
7	NC	D06	BG1OUT~	D14	NC
8	GND	D07	BG2IN~	D15	NC
9	NC	GND	BG2OUT~	GND	GAP~
10	GND	SYSCLK	BG3IN~	SYSFAIL~	GA0~
11	NC	GND	BG3OUT~	BERR~	GA1~
12	GND	DS1~	BR0~	SYSRESET~	P3V3
13	NC	DS0~	BR1~	LWORD~	GA2~
14	GND	WRITE~	BR2~	AM5	P3V3
15	NC	GND	BR3~	A23	GA3~
16	GND	DTACK~	AM0	A22	P3V3
17	NC	GND	AM1	A21	GA4~
18	GND	AS~	AM2	A20	P3V3
19	NC	GND	AM3	A19	NC
20	GND	IACK~	GND	A18	P3V3
21	NC	IACKIN~	NC	A17	NC
22	GND	IACKOUT~	NC	A16	P3V3
23	NC	AM4	GND	A15	NC
24	GND	A07	IRQ7~	A14	P3V3
25	NC	A06	IRQ6~	A13	NC
26	GND	A05	IRQ5~	A12	P3V3
27	NC	A04	IRQ4~	A11	NC
28	GND	A03	IRQ3~	A10	P3V3
29	NC	A02	IRQ2~	A09	NC
30	GND	A01	IRQ1~	A08	P3V3
31	NC	N12V	NC	P12V	GND
32	GND	VCC	VCC	VCC	VCC

VMEbus Signal Descriptions

The VMEbus signals occupy rows Z, A, B, C, and D of the P1 connector and row b of the P2 connector.

MNEMONIC	SIGNAL DESCRIPTION
A01 to A15	**Address Bus (bits 1 to 15).** Address lines that are used to broadcast a short address
A16 to A23	**Address Bus (bits 16 to 23).** Address lines that are used with A01 to A15 and LWORD~ to broadcast a standard address
ACFAIL~	**AC Failure.** This shows that the AC input to the power supply is no longer being provided or that the required AC input voltage levels are not being met
AM0 to AM5	**Address Modifier (bits 0 to 5).** These are used to broadcast information such as the address size, cycle type, master identification or any combination of these
AS~	**Address Strobe.** This shows when a valid address has been placed on the address bus
BBSY~	**Bus Busy.** This is driven low by the requester associated with the current bus master to show that the master is using the bus
BCLR~	**Bus Clear.** This is generated by an arbiter to show that there is a higher priority request for the bus than the one being processed. This requests the current master to release the bus
BERR~	**Bus Error.** This is generated by a slave or bus timer to tell the master that the data transfer did not complete
BG0IN~ to BG3IN~	**Bus Grant In (0 to 3) .** These signals are generated by the arbiter to tell the board receiving it that if it is requesting the bus on that level, then it has been granted use of the bus. Otherwise the board should pass the signal down the daisy chain. The BGxIN~/BGxOUT~ signals form the bus grant daisy chain, i.e. the BGxOUT~ of one board forms the BGxIN~ of the next board in the daisy chain
BG0OUT~ to BG3OUT~	**Bus Grant Out (0 to 3) .** These signals are generated by requesters to tell the next board in the daisy chain that if it is requesting the bus on that level, then it can use the bus. Otherwise the board should pass the signal down the daisy chain
BR0~ to BR3~	**Bus Request (0 to 3).** A low level, generated by a requester, on one of these lines, shows that some master needs to use the bus.
D00 to D15	**Data Bus.** These are used to transfer data between masters and slaves, and status/ID information from interrupters to interrupt handlers
DS0~, DS1~	**Data Strobe 0, 1.** These are used with LWORD~ and A01 to show how many byte locations are being accessed (1, 2, 3 or 4). Also, during a write cycle, the falling edge of the first data strobe shows that valid data is available on the bus. On a read cycle, the rising edge of the first data strobe shows that data has been accepted from the data bus
DTACK~	**Data Transfer Acknowledge.** This signal is generated by a slave. The falling edge shows that valid data is available on the data bus during a read cycle, or that data has been accepted from the data bus during a write cycle. The rising edge shows that the slave has released the data bus at the end of a read cycle
GA0~ to GA4~	**Geographic Address**. These are used to set the slave VME address of the board.
GAP~	**Geographic Address Parity**
GND	The DC voltage reference for the system
IACK~	**Interrupt Acknowledge**. This is used by the interrupt handler to acknowledge an interrupt request. It is routed to the IACKIN~ pin of slot 1, where it is monitored by the IACK daisy chain driver
IACKIN~	**Interrupt Acknowledge In.** This tells the board receiving it that that board can respond to the interrupt acknowledge cycle in process or pass it down the daisy chain. IACKIN~/IACKOUT~ form the interrupt acknowledge daisy chain
IACKOUT~	**Interrupt Acknowledge Out.** This is sent by a board to tell the next board in the daisy chain that it can respond to the interrupt acknowledge cycle in progress
IRQ1~ to IRQ7~	**Interrupt Request (1 to 7).** These are driven low by interrupters to request an interrupt on the corresponding level
LWORD~	**Longword.** This is used with DS0~, DS1~ and A01 to select which byte location(s) within the 4-Byte group are accessed during the data transfer
N12V	-12 Volts DC power
P12V	+12 Volts DC power
P3V3	+3.3 Volts DC power
Reserved	This signal is reserved for future enhancements of the VME specification
SYSCLK	**System Clock.** This provides a constant 16 MHz clock signal that is independent of any other bus timing
SYSFAIL~	**System Fail.** This shows that a failure has occurred in the system. This signal can be generated by any board in the system
SYSRESET~	**System Reset.** When this is low, it causes the system to be reset
VCC	+5 Volts DC power
WRITE~	**Write.** This is generated by a master to show whether the data transfer cycle is a read or a write

PMC Site User IO

All 64 pins of user IO are routed to either P2 or P0 connectors from both PMC sites for maximum connectivity.

PMC 1 has 46 pins routed to P2 rows D and Z and the remaining 18 pins to P0 row C.

Routing is optimised for Radstone's series of Graphics PMC adapters.

All 64 pins of PMC2 J24 are routed to P2 rows A and C in differential pair mode to support Radstone's PMCStarLite. This is useful if the StarSwitch is to be used as a StarFabric switch as the combination of a PMCStarLite and a StarSwitch creates a 6 port StarFabric Switch in one slot.

P2 Connector Pin out

Pin Id	Row Z	Row A	Row B	Row C	Row D
1	J14 pin 3	J24 pin 2	VCC	J24 pin 1	J14 pin 2
2	GND	J24 pin 4	GND	J24 pin 3	J14 pin 5
3	J14 pin 1	J24 pin 6	NC	J24 pin 5	J14 pin 4
4	GND	J24 pin 8	A24	J24 pin 7	J14 pin 7
5	J14 pin 10	J24 pin 10	A25	J24 pin 9	J14 pin 6
6	GND	J24 pin 12	A26	J24 pin 11	J14 pin 9
7	J14 pin 11	J24 pin 14	A27	J24 pin 13	J14 pin 8
8	GND	J24 pin 16	A28	J24 pin 15	J14 pin 16
9	J14 pin 14	J24 pin 18	A29	J24 pin 17	J14 pin 12
10	GND	J24 pin 20	A30	J24 pin 19	J14 pin 17
11	J14 pin 15	J24 pin 22	A31	J24 pin 21	J14 pin 13
12	GND	J24 pin 24	GND	J24 pin 23	J14 pin 22
13	J14 pin 20	J24 pin 26	VCC	J24 pin 25	J14 pin 18
14	GND	J24 pin 28	D16	J24 pin 27	J14 pin 23
15	J14 pin 21	J24 pin 30	D17	J24 pin 29	J14 pin 19
16	GND	J24 pin 32	D18	J24 pin 31	J14 pin 24
17	J14 pin 26	J24 pin 34	D19	J24 pin 33	J14 pin 25
18	GND	J24 pin 36	D20	J24 pin 35	J14 pin 27
19	J14 pin 29	J24 pin 38	D21	J24 pin 37	J14 pin 31
20	GND	J24 pin 40	D22	J24 pin 39	J14 pin 28
21	J14 pin 30	J24 pin 42	D23	J24 pin 41	J14 pin 32
22	GND	J24 pin 44	GND	J24 pin 43	J14 pin 33
23	J14 pin 35	J24 pin 46	D24	J24 pin 45	J14 pin 37
24	GND	J24 pin 48	D25	J24 pin 47	J14 pin 34
25	J14 pin 36	J24 pin 50	D26	J24 pin 49	J14 pin 38
26	GND	J24 pin 52	D27	J24 pin 51	J14 pin 39
27	J14 pin 41	J24 pin 54	D28	J24 pin 53	J14 pin 43
28	GND	J24 pin 56	D29	J24 pin 55	J14 pin 40
29	J14 pin 42	J24 pin 58	D30	J24 pin 57	J14 pin 44
30	GND	J24 pin 60	D31	J24 pin 59	J14 pin 45
31	J14 pin 46	J24 pin 62	GND	J24 pin 61	GND
32	GND	J24 pin 64	VCC	J24 pin 63	VCC

P0 Connector Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
1	SF1_TX0P	SF2_TX0P	PMC1_47	SF3_TX0P	SF4_TX0P	GND
2	SF1_TX0N	SF2_TX0N	PMC1_53	SF3_TX0N	SF4_TX0N	GND
3	SF1_TX1P	SF2_TX1P	PMC1_49	SF3_TX1P	SF4_TX1P	GND
4	SF1_TX1N	SF2_TX1N	PMC1_51	SF3_TX1N	SF4_TX1N	GND
5	SF1_TX2P	SF2_TX2P	PMC1_55	SF3_TX2P	SF4_TX2P	GND
6	SF1_TX2N	SF2_TX2N	PMC1_57	SF3_TX2N	SF4_TX2N	GND
7	SF1_TX3P	SF2_TX3P	PMC1_59	SF3_TX3P	SF4_TX3P	GND
8	SF1_TX3N	SF2_TX3N	PMC1_61	SF3_TX3N	SF4_TX3N	GND
9	GND	GND	PMC1_63	JT_TMS	JT_TDI	GND
10	INTA_PMC1	INTA_PMC2	PO_INT_EITHER_OD	JT_CLK	JT_TDO	GND
11	GND	GND	PMC1_64	GND	JT_TRST~	GND
12	SF1_RX0P	SF2_RX0P	PMC1_62	SF3_RX0P	SF4_RX0P	GND
13	SF1_RX0N	SF2_RX0N	PMC1_60	SF3_RX0N	SF4_RX0N	GND
14	SF1_RX1P	SF2_RX1P	PMC1_56	SF3_RX1P	SF4_RX1P	GND
15	SF1_RX1N	SF2_RX1N	PMC1_58	SF3_RX1N	SF4_RX1N	GND
16	SF1_RX2P	SF2_RX2P	PMC1_50	SF3_RX2P	SF4_RX2P	GND
17	SF1_RX2N	SF2_RX2N	PMC1_52	SF3_RX2N	SF4_RX2N	GND
18	SF1_RX3P	SF2_RX3P	PMC1_54	SF3_RX3P	SF4_RX3P	GND
19	SF1_RX3N	SF2_RX3N	PMC1_48	SF3_RX3N	SF4_RX3N	GND

Note: These are JTAG signals used for production test and programmable-logic programming only

Note: SF1 and SF2 connect to SF Switch 1, and SF3 and SF4 connect to SF Switch 2, as shown in the StarSwich Functional Block Diagram.

P0 Signal Descriptions

Name	Signal Description
INTA_PMCn	Interrupt signal from PMC site 1 or 2.
PMC1_[47..64]	These signals are routed to PMC site 1 connector J14.
SF[1..4]_TX[0..3]	**StarFabric Port 1/2/3/4, TRANSMIT Pair 0/1/2/3**
SF[1..4]_RX[0..3]	**StarFabric Port 1/2/3/4, RECEIVE Pair 0/1/2/3**

Erratum
May 2007

PMC Connectors Pinouts

For a description of the signals listed below see PMC Signal Descriptions later in this section.

J11/J21 (PMC1) Connector Pinout

Note: For J11, read '1' for 'n' and similarly, for J21, read '2' for 'n' e.g. PMCn = PMC1 or PMC2.

Pin	Signal Name	Pin	Signal Name
1	PMCn_TCK	2	N12V
3	GND	4	PMCn_INTA~
5	VCC (pulled up only)	6	VCC (pulled up only)
7	NC	8	VCC
9	VCC (pulled up only)	10	RESERVED
11	GND	12	RESERVED
13	PMCn_CLK	14	GND
15	GND	16	GNT_PMCn~
17	PMCn_REQ~	18	VCC
19	VIO (P3V3 or 5V)	20	PMCn_AD(31)
21	PMCn_AD(28)	22	PMCn_AD(27)
23	PMCn_AD(25)	24	GND
25	GND	26	PMCn_CBE(3)~
27	PMCn_AD(22)	28	PMCn_AD(21)
29	PMCn_AD(19)	30	VCC
31	VIO (P3V3 or 5V)	32	PMCn_AD(17)
33	PMCn_FRAME~	34	GND
35	GND	36	PMCn_IRDY~
37	PMCn_DEVSEL~	38	VCC
39	GND	40	PMCn_LOCK
41	NC	42	NC
43	PMCn_PAR	44	GND
45	VIO (P3V3 or 5V)	46	PMCn_AD(15)
47	PMCn_AD(12)	48	PMCn_AD(11)
49	PMCn_AD(9)	50	VCC
51	GND	52	PMCn_CBE(0)~
53	PMCn_AD(6)	54	PMCn_AD(5)
55	PMCn_AD(4)	56	GND
57	VIO (P3V3 or 5V)	58	PMCn_AD(3)
59	PMCn_AD(2)	60	PMCn_AD(1)
61	PMCn_AD(0)	62	VCC
63	GND	64	PMCn_REQ64~

J12/22 (PMC1/PMC2) Connector Pinout

For a description of the signals listed below see PMC Signal Descriptions later in this section.

Notes: For J12, read '1' for 'n' and similarly, for J22, read '2' for 'n' e.g. PMCn = PMC1 or PMC2

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	P12V	2	PMCn_TRST
3	PMCn_TMS	4	PMCn_TDI
5	PMCn_TD0	6	GND
7	GND	8	RESERVED
9	RESERVED	10	RESERVED
11	BUSMODE2~	12	P3V3
13	PMCn_RSTOUT~	14	BUSMODE3~ (N/C)
15	P3V3	16	BUSMODE4~ (N/C)
17	RESERVED	18	GND
19	PMCn_AD(30)	20	PMCn_AD(29)
21	GND	22	PMCn_AD(26)
23	PMCn_AD(24)	24	P3V3
25	PMCn_IDSEL	26	PMCn_AD(23)
27	P3V3	28	PMCn_AD(20)
29	PMCn_AD(18)	30	GND
31	PMCn_AD(16)	32	PMCn_CBE2~
33	GND	34	RSVD
35	PMCn_TRDY~	36	P3V3
37	GND	38	PMCn_STOP~
39	PMCn_PERR~	40	GND
41	P3V3	42	PMCn_SERR~
43	PMCn_CBE(1)~	44	GND
45	PMCn_AD(14)	46	PMCn_AD(13)
47	PMCn_M66EN	48	PMCn_AD(10)
49	PMCn_AD(8)	50	P3V3
51	PMCn_AD(7)	52	RESERVED
53	P3V3	54	RESERVED
55	RESERVED	56	GND
57	RESERVED	58	RSVD
59	GND	60	RSVD
61	PMCn_ACK64~	62	P3V3
63	GND	64	RSVD

Note: These are JTAG signals used for production test and programmable-logic programming only

J13/J23 (PMC1/PMC2) Connector Pinout

For a description of the signals listed below see PMC Signal Descriptions later in this section.

Note: For J13, read '1' for 'n', e.g. PMCn = PMC1. Similarly, for J23, read '2' for 'n'.

Pin	Signal Name	Pin	Signal Name
1	RESERVED	2	GND
3	GND	4	PMCn_CBE(7)~
5	PMCn_CBE(6)~	6	PMCn_CBE(5)~
7	PMCn_CBE(4)~	8	GND
9	VIO (P3V3 or 5V)	10	PMCn_PAR64
11	PMCn_AD(63)	12	PMCn_AD(62)
13	PMCn_AD(61)	14	GND
15	GND	16	PMC_AD_(60)
17	PMCn_AD(59)	18	PMCn_AD(58)
19	PMCn_AD(57)	20	GND
21	VIO (P3V3 or 5V)	22	PMCn_AD(56)
23	PMCn_AD(55)	24	PMCn_AD(54)
25	PMCn_AD(53)	26	GND
27	GND	28	PMCn_AD(52)
29	PMCn_AD(51)	30	PMCn_AD(50)
31	PMCn_AD(49)	32	GND
33	GND	34	PMCn_AD(48)
35	PMCn_AD(47)	36	PMCn_AD(46)
37	PMCn_AD(45)	38	GND
39	VIO (P3V3 or 5V)	40	PMCn_AD(44)
41	PMCn_AD(43)	42	PMCn_AD(42)
43	PMCn_AD(41)	44	GND
45	GND	46	PMCn_AD(40)
47	PMCn_AD(39)	48	PMCn_AD(38)
49	PMCn_AD(37)	50	GND
51	GND	52	PMCn_AD(36)
53	PMCn_AD(35)	54	PMCn_AD(34)
55	PMCn_AD(33)	56	GND
57	VIO (P3V3 or 5V)	58	PMCn_AD(32)
59	RESERVED	60	RESERVED
61	RESERVED	62	GND
63	GND	64	RSVD

PMC Signal Descriptions

Mnemonic	Signal Description
ACK64~	**Acknowledge 64 Bit**. Driven low by PCI agent in response to REQ64. Only connected to a 4.7 kΩ pull-up on the G4DSP-XE
AD0 to AD63	**Address/Data bits.** Multiplexed address and data bus
BUSMODE1~	**Bus Mode 1.** Driven low by a PMC if it supports the current bus mode
BUSMODE2~,	**Bus mode.** Driven by the host to indicate the bus mode. On the G4DSP-XE this is always PCI. BUSMODE2~ is only connected to a 4.7 kΩ pull-up
C_BE0 to C_BE7	**Command/Byte Enables.** During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
CLK	**Clock.** All PCI bus signals except RST~ are synchronous to this 33 MHz clock
DEVSEL~	**Device Select.** Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
FRAME~	**FRAME.** Driven low by the current master to signal the start and duration of an access
GNT~	**Grant.** Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSEL	**Initialisation Device Select.** Device chip select during configuration cycles
INTA~ to INTD~	**Interrupt lines.** Level-sensitive, active-low interrupt requests
IRDY~	**Initiator Ready.** Driven low by the initiator to signal its ability to complete the current data phase
M66EN	**Enable 66MHz**
N12V	-12 Volts DC power
NC	**No connection**
P3V3	On-board +3.3V DC Power
PAR	**Parity.** Parity protection bit for AD0 to AD31 and BE0 to BE3
PAR64	**Parity.** Parity protection bit for AD32 to AD63 and BE4 to BE7
PERR~	**Parity Error.** Driven low by a PCI agent to signal a parity error
REQ~	**Request.** Driven low by a PCI agent to request ownership of the PCI bus
REQ64~	**Request 64 Bit**. Driven low by a PCI master to request 64-bit transfer. Only connected to a 4.7 kΩ pull-up on the G4DSP-XE
RST~	**Reset.** Driven low to reset the PCI bus
RSVD	**Reserved**
SERR~	**System Error.** Driven low by a PCI agent to signal a system error
STOP~	**Stop.** Driven low by a PCI target to signal a disconnect or target-abort
TCLK	**Test Clock.** Clock for the PMC JTAG
TDI	**Test Data In.** Input data for PMC JTAG chain
TDO	**Test Data Out.** Data from a PMC JTAG chain
TMS	**Test Mode Select.** Select Test Mode for PMC JTAG
TRDY~	**Target Ready.** Driven low by the current target to signal its ability to complete the current data phase
TRST~	**Test Reset.** Reset any PMC JTAG devices
VIO	Supply voltage for PMC IO circuitry
5V	+5V external supply (VCC)

J14 Connector Pinout

The signals on J14 are routed to P2 rows D and Z, and to P0 row C.

PIN	IO PIN	PIN	IO PIN
1	P2 pin Z3	2	P2 pin D1
3	P2 pin Z1	4	P2 pin D3
5	P2 pin D2	6	P2 pin D5
7	P2 pin D4	8	P2 pin D7
9	P2 pin D5	10	P2 pin Z5
11	P2 pin Z7	12	P2 pin D9
13	P2 pin D11	14	P2 pin Z9
15	P2 pin Z11	16	P2 pin D8
17	P2 pin D10	18	P2 pin D13
19	P2 pin D15	20	P2 pin Z13
21	P2 pin Z15	22	P2 pin D12
23	P2 pin D14	24	P2 pin D16
25	P2 pin D17	26	P2 pin Z17
27	P2 pin D18	28	P2 pin D20
29	P2 pin Z19	30	P2 pin Z21
31	P2 pin D19	32	P2 pin D21
33	P2 pin D22	34	P2 pin D24
35	P2 pin Z23	36	P2 pin Z25
37	P2 pin D23	38	P2 pin D25
39	P2 pin D26	40	P2 pin D28
41	P2 pin Z27	42	P2 pin Z29
43	P2 pin D27	44	P2 pin D29
45	P2 pin D30	46	P2 pin Z31
47	P0 pin C1	48	P0 pin C19
49	P0 pin C3	50	P0 pin C16
51	P0 pin C4	52	P0 pin C17
53	P0 pin C2	54	P0 pin C18
55	P0 pin C5	56	P0 pin C14
57	P0 pin C6	58	P0 pin C15
59	P0 pin C7	60	P0 pin C13
61	P0 pin C8	62	P0 pin C12
63	P0 pin C9	64	P0 pin C11

J24 Connector Pinout

The signals on J24 are routed to P2 rows A and C.

PIN	IO PIN	PIN	IO PIN
1	P2 pin C1	2	P2 pin A1
3	P2 pin C2	4	P2 pin A2
5	P2 pin C3	6	P2 pin A3
7	P2 pin C4	8	P2 pin A4
9	P2 pin C5	10	P2 pin A5
11	P2 pin C6	12	P2 pin A6
13	P2 pin C7	14	P2 pin A7
15	P2 pin C8	16	P2 pin A8
17	P2 pin C9	18	P2 pin A9
19	P2 pin C10	20	P2 pin A10
21	P2 pin C11	22	P2 pin A11
23	P2 pin C12	24	P2 pin A12
25	P2 pin C13	26	P2 pin A13
27	P2 pin C14	28	P2 pin A14
29	P2 pin C15	30	P2 pin A15
31	P2 pin C16	32	P2 pin A16
33	P2 pin C17	34	P2 pin A17
35	P2 pin C18	36	P2 pin A18
37	P2 pin C19	38	P2 pin A19
39	P2 pin C20	40	P2 pin A20
41	P2 pin C21	42	P2 pin A21
43	P2 pin C22	44	P2 pin A22
45	P2 pin C23	46	P2 pin A23
47	P2 pin C24	48	P2 pin A24
49	P2 pin C25	50	P2 pin A25
51	P2 pin C26	52	P2 pin A26
53	P2 pin C27	54	P2 pin A27
55	P2 pin C28	56	P2 pin A28
57	P2 pin C29	58	P2 pin A29
59	P2 pin C30	60	P2 pin A30
61	P2 pin C31	62	P2 pin A31
63	P2 pin C32	64	P2 pin A32

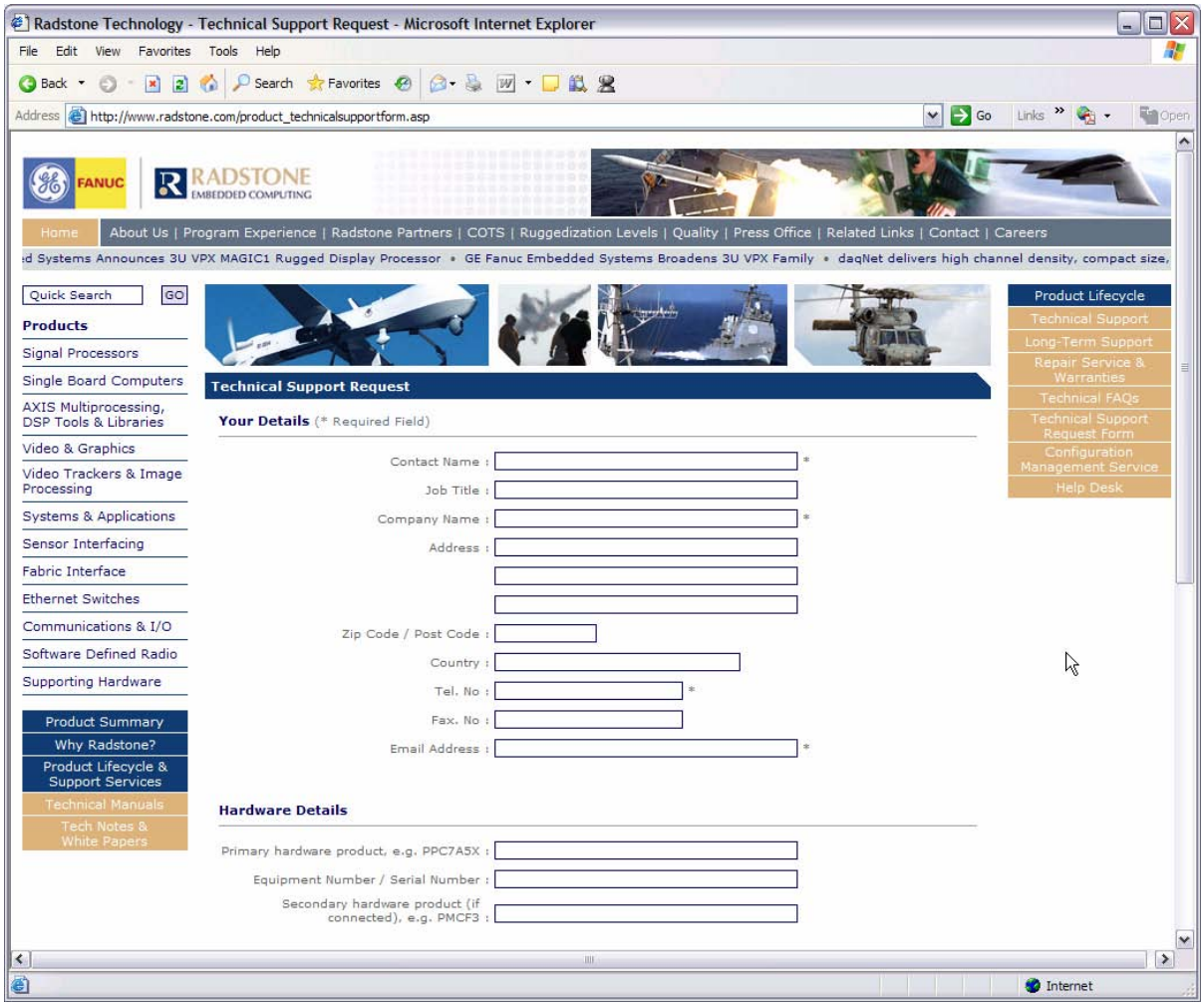
STARPIO I/O Module

Access to the StarSwitch signals is made easier during development by attaching the STARPIO I/O module to the P0 and P2 connectors. The STARPIO provides access to four transmit/receive pairs of StarFabric channels and three interrupt signals. See the Product Code Information for details.

8. Technical Support

Radstone Contact Information

For technical assistance please register support requests using the Technical Support Request Form available through the Radstone web site at http://www.radstone.com/product_technicalsupportform.asp. This form looks like:



Your query will be logged on Radstone's Technical Support database and allocated a unique Call Reference Number (CRN) for use in future correspondence.

Alternatively, you may also contact Radstone's Technical Support on:

Email

Support@radstone.co.uk

Telephone -

+44 (0)1327 359804

Troubleshooting

PMC Site Special Links (E51, E52)

There should be no need to have any of the links fitted on E51 or E52 during normal operation of the board. During development, some of these special functions may prove valuable in debugging:

FID – Fabric ID: Pins 1-2 on both E51 and E52 are only for use in a parallel redundant StarFabric network and their settings can be overridden in software. For a single StarFabric Fabric, there is only one ROOT node and the first part of the Fabric ID will be zero. Customers who want to implement redundant fabrics need to contact Radstone for more information about software driver support of multiple ROOT networks.

Force – 33 MHz: Pins 3-4. A very simple way of looking into any PCI timing problems that may occur between Stargen SG2010 devices and PCI bridges on third party 66 MHz PMC cards is to reduce the bus speed to 33 MHz to see if the problem remains. Radstone are able to qualify timings of our own PMC cards for use with the StarSwitch but are unable to test PMC cards by other suppliers. Radstone's experience is that marginal timing problems can sometimes be eliminated by using reduced bus speeds which enables a developer to continue with S/ware development while any timing anomaly is investigated. (Fitting the link forces the PCI clock speed to the PMC to be 33 MHz)

ROM_Hold: Pins 5-6. The SG2010 devices on the StarSwitch each have associated SROMs that store a number of BAR (Base-Address-Register values). These values are user configurable. It is possible for users to change these BAR values and anything else stored in the SROM using function calls in the StarSwitch driver. It is possible that non-valid values may be entered into the SROM that prevent the StarFabric initializing properly. Fitting the ROM_HOLD jumper prevents the SROM downloading its contents to the SG2010 on power up and hence the SG2010 loads safe defaults. The jumpers can then be removed and the SROMs reprogrammed with corrected values. This feature is included to reduce the chances of a user having to return the board after corrupting the SROM values.

Appendix A - Specifications

General Specifications

On Board Clocks

PCI Clock	66 MHz. (33 MHz if a 33 MHz PMC is fitted)
StarFabric reference clock.	62.208 MHz
VME system clock	64 MHz.
SG2010 and SG1010 PLL bypass	77 MHz and 112.5 MHz respectively/

All clock oscillators are Vite VCC1 series. Industrial temperature range qualified . 45/55, 50ppm drift.

ICS-8701 clock distribution IC for PCI clocks

VME

VMEbus Compliance - ANSI/VITA 1-1994 Specification

Tundra Universe IID Bridge

Standard 74ABT16245 series high – drive 5 volt buffers

5 volt 33 MHz PCI-side operation.

StarFabric

2x SG2010 rev A4 (or higher) silicon bridges

2x SG1010 rev A3 (or higher) silicon switches

PCI-PCI bridges

2x PLX6540 (ex HINT HB8) (For protection of PMC site traffic from each other)

Programmable Logic

Xilinx XC95XL144-TQ144 CPLD.

PMC Sites

2 independent PMC Sites (The PLX bridges operate in non-transparent mode to ensure this)

StarSwitch is capable of driving ordinary PMCs, including single and dual processor PMCs:

- 32Bit/33 MHz: (5V or 3V3)
- 32Bit/66MHz.: (3V3 only according to the standard PCI specification 2.2)
- 64Bit/33MHz: (5V or 3V3)
- 64Bit/66MHz: (3V3 only according to the standard PCI specification 2.2)

Note: StarSwitch's on board SG2010 components are 5 Volt tolerant but drive at 3V3.

StarSwitch changes the PMC PCI clock speeds automatically by sensing the PMC. The mechanism is that a 33 MHz PMC will ground the M66EN signal.

The signalling voltage 5V or 3V3 is set independently for each site using jumpers – see Configuring the PMC sites.

Connectors

J11, 12, 13, 14, 21, 22, 23, 24	EIA E700 AAAB
P1, P2	160 way DIN VME compatible, male
P0	95 way Type B PCI compatible, male

Build Levels

The StarSwitch is available in 4 electrically compatible build levels. Each level is carefully tailored to a particular set of requirements and environments. The 4 build levels have two basic mechanical configurations: convection-cooled in accordance with IEEE P1386, and conduction-cooled in accordance with the proposed CCPMC standard being prepared by VITA.

Convection-cooled builds include:

Level 1
Level 2
Level 3

Conduction-cooled builds include:

Level 4

A brief description of each build style follows:

Level 1

Intended for use in benign environments, the level 1 board also provides the ideal cost effective method of complete system development. The level 1 assembly comprises an IEEE P1386 size assembly with high quality commercial grade (plastic encapsulated) components. As software compatibility throughout the build styles is absolute, a system intended for final implementation in a severe tactical environment can be developed and debugged at low cost, switching over to the target style only in the final stages of system integration.

Level 2

As level 1, but conformally coated and tested in manufacture to provide an extended operating range.

Level 3

Level 3 boards are intended for applications that have extended temperature, shock and vibration requirements, but can be served by conventional, forced-air cooled, racking systems. These rugged boards comprise an IEEE P1386 size assembly fitted with wide temperature range components and are conformally coated as standard.

Level 4

Designed primarily for use in sealed ATR chassis and other conduction-cooled environments, the level 4 board features wide temperature range devices, an integral thermal management layer and incorporates a central stiffening bar for additional strength. Cooling is achieved through conduction of heat from the thermal management layer to the cold wall of the rack, to which the boards are secured by screw driven wedgelocks. Level 4 boards are temperature characterised and conformally coated during manufacture.

Level 4 boards are mechanically compliant with the proposed CCPMC standard.

Electrical Specification

Power-supplies and ground are shared between the connectors.

Power Consumption

18 watts (StarFabric only)

20 Watts (StarFabric plus VME (DMAs))

Voltage Requirements

+5V +5% -2.5% DC total excursion, including all transients
Vripple (+5V) = 50mV RMS maximum contained in the total excursion

Mechanical Specification

Weight

The approximate weight of the StarSwitch is:

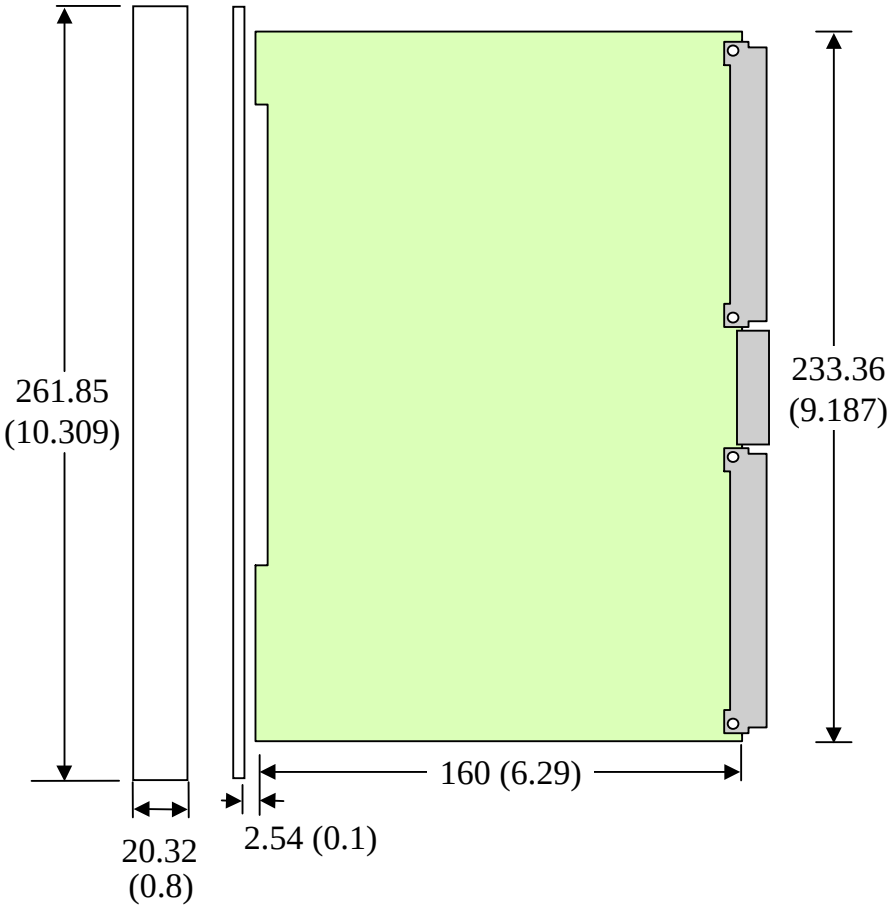
378 g: Level -1

532 g: Level - 4

Dimensions

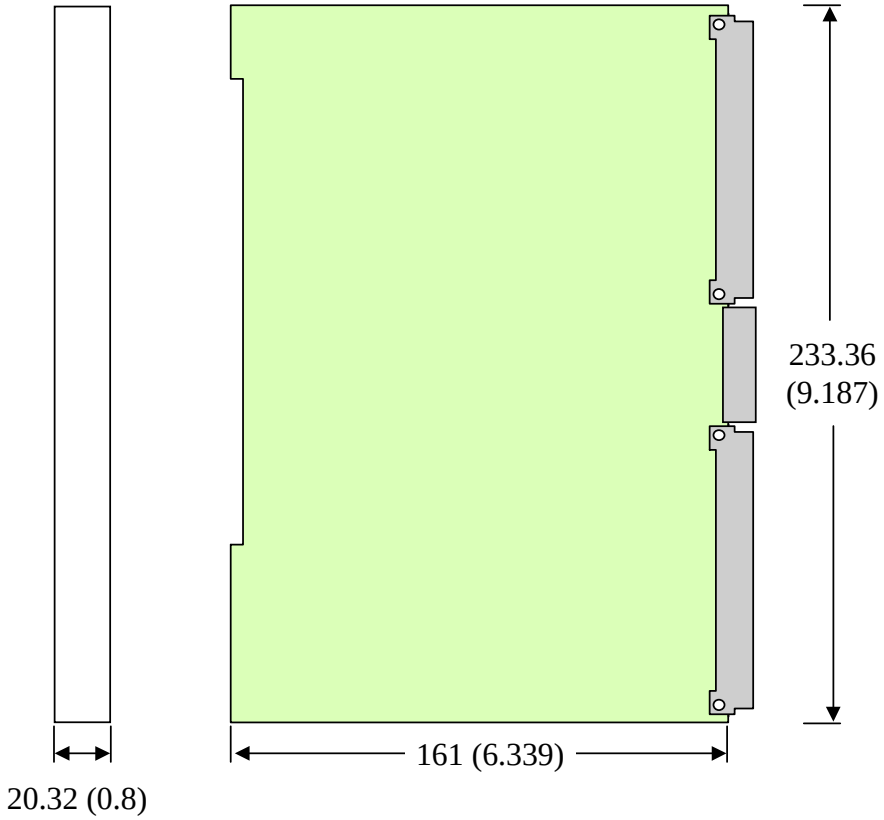
Air-cooled Boards

The air-cooled StarSwitch is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the ANSI/VITA 1-1994 specification. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.



Conduction-cooled Boards

The Conduction-cooled StarSwitch is constructed on a multi-layer double Eurocard and conforms to the dimensions specified in the IEEE 1101.2. The dimensions shown below are in millimeters, with inches (in parentheses) for general guidance only.



Reliability

Using MIL-HBK-217F Notice 1 as a database and the parts count method, the following provisional estimates have been made of the MTBF for the StarSwitch Rev 03 (see the Product Code Information section for details of variants).

Environment	Fail Rate (Failures Per Million Hours)	MTBF (Hours)
Ground Benign 30°C	3.260756	306,677
Ground Fixed 40°C	9.17208	109,027
Ground Mobile 45°C	18.17997	55,006
Naval Sheltered 40°C	15.54836	64,315
Naval Unsheltered 45°C	26.64327	37,533
Airborne Inhabited Cargo 55°C	20.26864	49,337
Airborne Inhabited Fighter 45°C	27.15553	36,825
Airborne Rotary Wing 55°C	40.35597	24,779
Airborne Uninhabited Cargo 70°C	36.13337	27,675
Airborne Uninhabited Fighter 70°C	55.10985	18,146
Space Flight 30°C	3.0352518	329,432
Missile Flight 45°C	22.16463	45,117
Missile Launch 55°C	56.25453	17,776

Environmental Specifications

Provided that the build style of the PMCGA4 and host are the same (for Radstone hosts), or the environmental specifications of the PMCGA4 and host are more or less equivalent (for non-Radstone hosts), the PMCGA4 will operate and may be stored or transported without damage within the same limitations as the host.

Convection-cooled Boards

Build Style	Temperature (°C)	Low Pressure (feet)	Vibration	Shock	Humidity/ Salt Fog	Comments
Standard (Level 1)	**Operating**: 0 to +55 with airflow of 300 feet/minute. **Storage**: -40 to +85 **Shock**: 10°C/minute over range	**Operating**: 15,000 **Storage**: 50,000	**Random**: $0.002g^2$/Hz from 10 to 2000 Hz **Sine**: 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating
Extended Temp (Level 2)	**Operating**: -20 to +65 with airflow of 300 feet/minute **Storage**: -40 to +85 **Shock**: 10°C/minute over range	**Operating**: 15,000 **Storage**: 50,000	**Random**: $0.002g^2$/Hz from 10 to 2000 Hz **Sine**: 2g from 10 to 500 Hz	20g peak sawtooth, 11ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterised.
Rugged Air-cooled (Level 3)	**Operating**: -40 to +75 with airflow of 600 feet/minute **Storage**: -50 to +100 **Shock**: 10°C/minute over range	**Operating**: 15,000 **Storage**: 50,000 **Rapid Decompression**: 0 to 50,000	**Random**: $0.04g^2$/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine**: 5g from 5 to 2000 Hz	20g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection.

Conduction-cooled Boards

Build Style	Temperature (°C)	Low Pressure (feet)	Vibration	Shock	Humidity/ Salt Fog	Comments
Rugged Conduction-cooled (Level 4)	**Operating**: -40 to +75 at the thermal interface **Storage**: -50 to +100 **Shock**: 10°C/minute over range	**Operating**: 70,000 **Storage**: 70,000 **Rapid Decompression**: 0 to 70,000	**Random**: $0.1g^2$/Hz with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz. **Sine**: 5g from 5 to 2000 Hz	40g peak sawtooth, 11ms duration. Bench handling	Up to 95% RH with varying temperature. 10 cycles, 240 hours. 5% salt 48 hours	Mechanically compliant with IEEE 1101.2-1992. Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.

Product Code Information

StarSwitch

Product Code	Description
STARSW-L1	Combined P0 and P2 interface adapter, provides access to four transmit/receive pairs of StarFabric channels and three interrupt signals. Available in four build styles – L = 1, 2, 3, or 4.

I/O Module

Product Code	Description
STARPIO-11	Combined P0 and P2 interface adapter, provides access to four transmit/receive pairs of StarFabric channels and three interrupt signals, for development purposes. Available in build style 1 only.

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