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PMC474F Fourth Generation PMC High Speed TAXI Interface w/Fiber Connection

Product Overview

The PMC474F provides a uniquely effective solution for integrating serial I/O requirements into a VMEbus or cPCI system. Implemented on a single PMC card, the PMC474F is fully compatible with the current of generation VMEbus and cPCI Single Board Computers, as well as any special purpose processor that includes a PMC connector. In addition, card edge PCI systems can be accommodated using a GE Fanuc Embedded Systems PMC239 adapter for rapid prototype and development.

Additional Information

Specifications

Features

- IBM PPC440GP CPU for local processing
- One receive and one transmit
- PCI 64/66Mhz interface
- Support from 100 Mbit up to 200 Mbit
- 32Kbyte FIFO for each port (option for 64K or 128K)
- 64 MBytes of DDR SDRAM (option for 128M)
- 8 Mbytes of on-board Flash
- The TAXI clock can be driven externally
- The input clock can be skewed

Traditional Serial Interfaces place a high overhead on the host processor by requiring per-character-attention. (i.e. each received and transmitted data generates interrupts and programmed I/O from the host). Two features of the PMC474F remove this overhead:

- On-card CPU for data blocking/unblocking
- Deep FIFO buffers to avoid data overrun (32K Bytes per RX/TX) plus 64MB DDR SDRAM on-board

Direct control of the TAXI Serial link is provided by the on-board processor, a 32 bit RISC CPU, which includes DMA engines for efficient transfers over the PCI (over 512Mbytes/sec). Data is buffered in on-card DDR SDRAM between transfer to/from the TAXI interface. The FIFO can be increased to 128K Bytes for RX/TX if needed. In addition to off-loading basic data manipulation, special data handling

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routines can readily be added to the local processor. Examples include special protocol handling, error correction, etc.

The PMC474F can be viewed as four functional components:

PCI Hardware Interface
Processor Resources
Logical Transaction Interface
TAXI port

PCI Interface

The PMC474F PCI interface is Revision 2.2 compatible, supporting 64/66Mhz transactions. Both slave and master operations are available, the latter including DMA engines capable of long PCI bursts. As data is buffered in local DDR SDRAM, large blocking factors can be used (when application level protocols allow). Both programmed I/O and message-based control is supported. The messaging system follows I2O hardware specifications.

Processor Resources

The on board 32 bit RISC CPU (IBM PPC 440GP) provides an external Memory bus that runs at over 1Gbytes/sec and an internal processor clock rate of 400Mhz. The higher CPU clock rate ensures sufficient bandwidth for all protocols (e.g. encryption) and Data manipulation at high, multi-port data rates. Local DDR SDRAM (64 Mbytes) is used for firmware execution and data buffering. Firmware is loaded automatically on power-up from local FLASH memory. New firmware (e.g. upgrades) may be loaded in the field without removing the PMC474F from the host. The processor directly controls both the TAXI and the on board UART for full software configuration.

Programming Interface

Flexibility, efficiency and use with both new and existing applications were all considered during the design of the Application Interface. Several modes of data transfer are supported, including a traditional programmed I/O (i.e. pseudo register) and high performance messaging. The "pseudo register" interface allows a host to use programmed I/O cycles to set characteristics and transmit/receive data. While less efficient, this mode can be appropriate for simple (low-speed) operation as well as when adapting legacy code. The messaging interface allows simple, efficient transfers between host software and the PMC474F. A control block contains transaction-specific information such as configuration, data or location of data buffers. A message queuing system makes transfer of the control blocks between the host and PMC474F very simple, requiring minimal software development. Once submitted to the PMC474F, the transaction information is loaded by the local processor; for large data blocks, the DMA engines are utilized to execute the data movement. This improves PCI bus utilization as well as allowing scatter/gather operation (useful in virtual memory operating systems).

TAXI Port

The data stream is controlled with a Cypress CY7C9689, responsible for Serialization/De-Serialization. The TAXI chip is clocked using a dedicated oscillator to reduce jitter. The TAXI oscillator speed is specific to the customer application (by default 12.8Mhz is loaded, unless specified by the customer). The PMC474F can be configured for the loop back to check for system integrity.

Software support

GE Fanuc Embedded Systems provides full software support for all the popular software environments (e.g. VxWorks, LynxOS, Windows NT, Linux, Solaris etc.).

External Connection

The PMC474F offers SC or ST connectors (in single or multi-mode flavor) through the front I/O.

The PMC474F is also available in a copper version, the GE Fanuc Embedded Systems PMC474C.

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Functional Specifications: PMC474F Fourth Generation PMC High Speed TAXI Interface w/Fiber Connection

Power	7 Total Watts
@ 3.3 V	1.5 Amps
@ 5 V	0.4 Amp
Form Factor	
PMC	Single Slot
MTBF	
MIL 217-F Nav Shel 25 Deg. C	205000 Hours
Temperature	
Operating	0 to +60° C
Storage	-40 to +85° C
Humidity	
Operating	5% to 95% Non-Condensing
Storage	5% to 95% Non-Condensing
Conformal Coating	Yes, additional charge
PCI Bus Characteristics	
Signaling	3 & 5V
Specification	2.2
Speed	33/66MHz
Width	32/64

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