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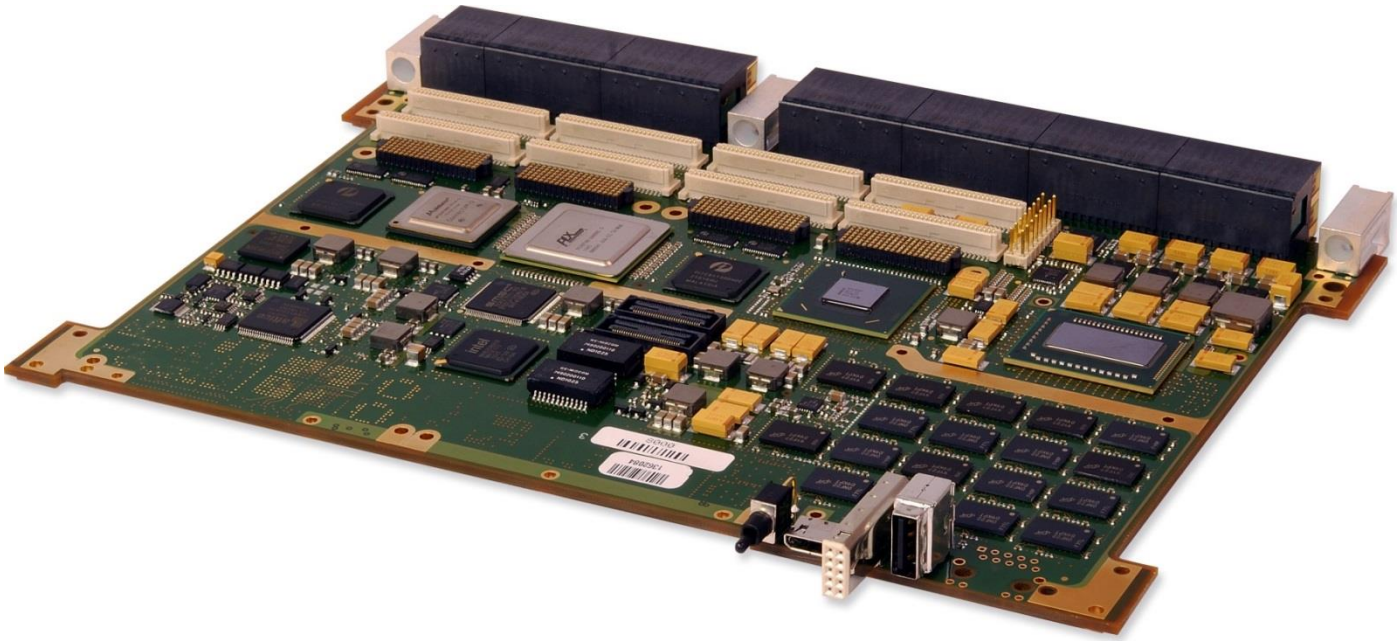
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Hardware Reference Manual

SBC624 6U VPX Single Board Computer

Edition 2QD

Publication No. SBC624-HRM/2QD



abaco SYSTEMS

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Document History

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1	September 2011	Rev 2
2	May 2012	Rev 3
2 + Errata	October 2013	Errata pages 63, 121 & 128
2QD	November 2016	No technical content change, rebranding only

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About This Manual

Conventions

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a "D" subscript and binary numbers have a "b" subscript. The prefix "0x" shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers "k", "M" and "G" have their conventional scientific and engineering meanings of $*10^3$, $*10^6$ and $*10^9$ respectively. The only exception to this is in the description of the size of memory areas, when "K", "M" and "G" mean $*2^{10}$, $*2^{20}$ and $*2^{30}$ respectively.



NOTE

When describing transfer rates, "k", "M" and "G" mean $*10^3$, $*10^6$ and $*10^9$ *not* $*2^{10}$, $*2^{20}$ and $*2^{30}$.

Multiple bit fields are numbered from 0 to n, where 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (~) denote active low signals; all other signals are active high. "N" and "P" denote the low and high components of a differential signal respectively.

Notices

This manual may use the following types of notice:



NOTE

Notes call attention to important features or instructions.



WARNING

Warnings alert you to the risk of severe personal injury.



CAUTION

Cautions alert you to system danger or loss of data.



TIP

Tips give guidance on procedures that may be tackled in a number of ways.



LINK

Links take you to other documents or websites. The purple link color may also be used within a body of text or paragraph to indicate a link (or hyperlink) to a different part of the same document.

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Further Information

Abaco Systems Documents

You may register for access to all manuals via the website whose link is given overleaf.

LINKS

PMC Installation Note, publication number HN4/3-99.

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

FBIT for SBC624 Software Reference Manual, publication number FBIT-SBC624-SRM.

NOTE

Cross-document links are intended for use where the document files are saved under their original file names in the same directory on a server, PC hard drive, or similar. If accessing this document via the Abaco website, cross-doc links will not work.

Third Party Documents

Due to the complexity of some of the parts used on the SBC624, it is not possible to include all the detailed data on all such devices in this manual. A list of the specifications and data sheets that provide additional information follows:

Specifications

IEEE 1101.1-1998	IEEE Standard for Mechanical Core Specifications for Microcomputers.
IEEE 1101.2-1992	Conduction cooled VME mechanics.
IEEE 1101.10-1996	Additional Mechanical Specifications.
ANSI/VITA 20-2001	Conduction Cooled PMC.
ANSI/VITA 32-2003	Processor PMC.
ANSI/VITA 39-2003	PCI-X for PMC and Processor PMC.
ANSI/VITA 42.0-2008	XMC.
ANSI/VITA 42.3-2006	XMC PCI Express Protocol Layer Standard.
ANSI/VITA 46.0-2007	VPX Baseline Standard.
VITA46.3 (Draft)	Serial RapidIO on VPX.
VITA46.4 (Draft)	PCI Express on VPX.
ANSI/VITA46.9-2010	XMC and PMC User I/O Mapping for VPX.
VITA 46.11 (Draft)	System Management on VPX.
ANSI/VITA65-2010	OpenVPX System Specification.

PCI Local Bus Specification Revision 2.1, PCI Special Interest Group.

These are the latest versions at time of writing; check associated web sites for later updates.

NOTE

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LINK

https://www.abaco.com

Third Party Web Sites

Manufacturers of many of the devices used on the SBC624 maintain FTP or web sites. Some useful sites are:

http://www.vita.com	For VPX (VITA 46) and PMC (VITA 32) standards.
http://www.ieee.com	For IEEE standards.
http://www.pcisig.org	For PCI Bus standards.
http://www.intel.com	For processor, chip set and Ethernet controller information.
http://www.plxtech.com	For PCIe switch device information.
http://www.latticesemi.com	For FPGA and PSU Monitor device information.
http://www.national.com	For USB and LM92 temperature sensor device information.
http://www.onsemi.com	For Temperature Sensor device information.
http://www.maxim-ic.com	For Elapsed Time Indicator device information.
http://www.siliconmotion.com	For Solid State Drive information.
http://www.everspin.com	For MRAM device information.
http://www.mellanox.com	For 10G Ethernet/Infiniband bridge device information.
http://www.smsc.com	For SuperIO device information.
http://www.nxp.com	For DIP Switch and I^2C buffer information.
http://www.renesas.com	For BMC device information.
http://www.firecron.com	For JTAG device information.
http://www.pericom.com	For PCIe to PCI Bridge information.
http://www.harting.co.uk	For connector information.
http://www.molex.com	For connector information.
http://www.samtec.com	For connector information.



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If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.



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Do not return products without first contacting the Abaco Repairs facility.

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1 • Introduction

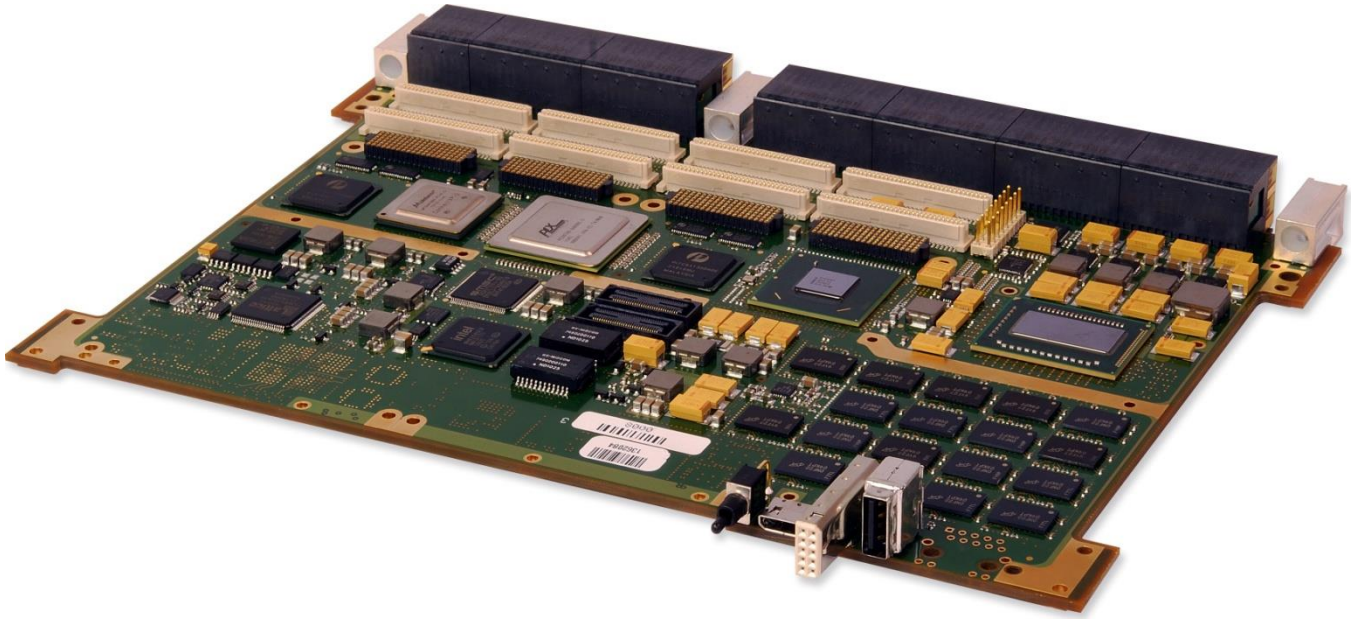
The Abaco Systems SBC624 is a member of the VPXcel6 family of 6U VPX Intel processor-based Single Board Computers. This family is aimed at processing, communications and display applications in the military and aerospace market.

The PC-like SBC624 implements the Intel Huron River Mobile (+ECC) architecture at up to 2.5 GHz, and has I/O interfaces including 10Gigabit and 1Gigabit Ethernet, USB 2.0, SATA and GPIO. The Core i7 processor also provides a DDR3 SDRAM interface with ECC. An Intel Series 6 PCH bridge provides two SATA interfaces, seven USB 2.0 ports, an LPC Bus and a Serial Peripheral Interface (supporting SPI boot Flash). Two PMC/XMC sites running at up to 133 MHz PCI-X with full 64-bit I/O are connected directly to the VPX backplane. XMC implements a 4-lane PCIe connection to site 1 and a 4- or 8-lane PCIe connection to site 2.

The SBC624 supports sixteen PCI Express lanes with various configurations to the backplane for connection to other cards in the system.

The SBC624 is supplied with a BIOS, supporting operating systems such as Microsoft Windows XP, Windows XP Embedded, Linux and VxWorks.

Figure 1-1 SBC624



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1.1 Safety Notices

The following general safety precautions represent warnings of certain dangers of which Abaco Systems is aware. Failure to comply with these or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Abaco assumes no liability for the user's failure to comply with these requirements.

Also follow all warning instructions contained in associated system equipment manuals.



WARNINGS

Use extreme caution when handling, testing and adjusting this equipment. This device may operate in an environment containing potentially dangerous voltages.

Ensure that all power to the system is removed before installing any device.

To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

1.1.1 Flammability

The SBC624 circuit board is made by a UL-recognized manufacturer and has a flammability rating of UL94V-1.

1.1.2 EMI/EMC Regulatory Compliance



CAUTION

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to EMI if not installed and used in a cabinet with adequate EMI protection.

The SBC624 is designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system. The SBC624 also complies with EN60950 (product safety), which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

Air-cooled build levels of the SBC624 are designed for use in systems meeting VDE class B, EN and FCC regulations for EMC emissions and susceptibility.

Conduction-cooled build levels of the SBC624 are intended for integration into EMC hardened cabinets/boxes.

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1.1.3 Cooling

CAUTION

The SBC624 requires air-flow of at least 300 lfm for build levels 1 and 2, and at least 600 lfm for build level 3. If a conduction-cooled (level 4 or 5) SBC624 is operating on an extender card, it requires air-flow of at least 300 lfm across it.

1.1.4 Handling

CAUTION

Only handle the SBC624 by the edges or front panel.

Figure 1-2 ESD Label (Present on Board Packaging)



1.1.5 Heatsink

CAUTIONS

Do not remove the heatsink. There are no user-alterable components underneath the heatsink, so users should have no reason to remove it.

Users should not attempt reattachment of the heatsink, as this requires precise torque on the screws attaching the heatsink to the PCB. Over-tightening the screws may cause the heatsink to damage components beneath it. *Removal and re-attachment of the heatsink should only be carried out by the factory.*

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2 • Unpacking

On receipt of the shipping container, if there is any evidence of physical damage, the Terms and Conditions of Sale (provided with your delivery) give information on what to do. If you need to return the product, contact your local Abaco sales office or agent.

The SBC624 is sealed into an antistatic bag and housed in a padded cardboard box. Failure to use the correct packaging when storing or shipping the board may invalidate the warranty.

2.1 Box Contents Checklist

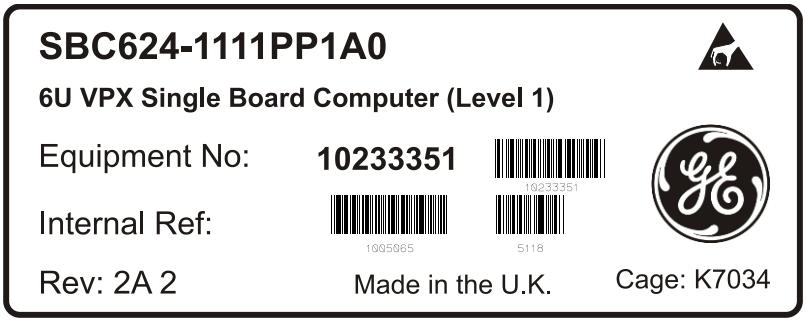
1. SBC624 in antistatic packaging.
2. Embedded Software License Agreement (GFJ-353).

2.2 Identifying Your Board

The SBC624 is identified by labels at strategic positions. These can be cross-checked against the Advice Note provided with your delivery.

Identification labels, similar to the example shown in Figure 2-1, attached to the shipping box and the antistatic bag give identical information: product code, product description, equipment number and board revision.

Figure 2-1 Product Label (Packaging)



On the board within the antistatic bag, there is an identifying label, similar to the example shown in Figure 2-2, attached to the PCB.

Figure 2-2 Product Label (Product)



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On conduction-cooled versions of the board (build levels 4 and 5), there is also a label, similar to the example shown in Figure 2-3, attached to the front panel.

Figure 2-3 Product Label (Conduction-cooled Product)



See the Product Codes section in Appendix A for more details on the product code (SBC624-xxxxxxxxx).

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3 • Configuration

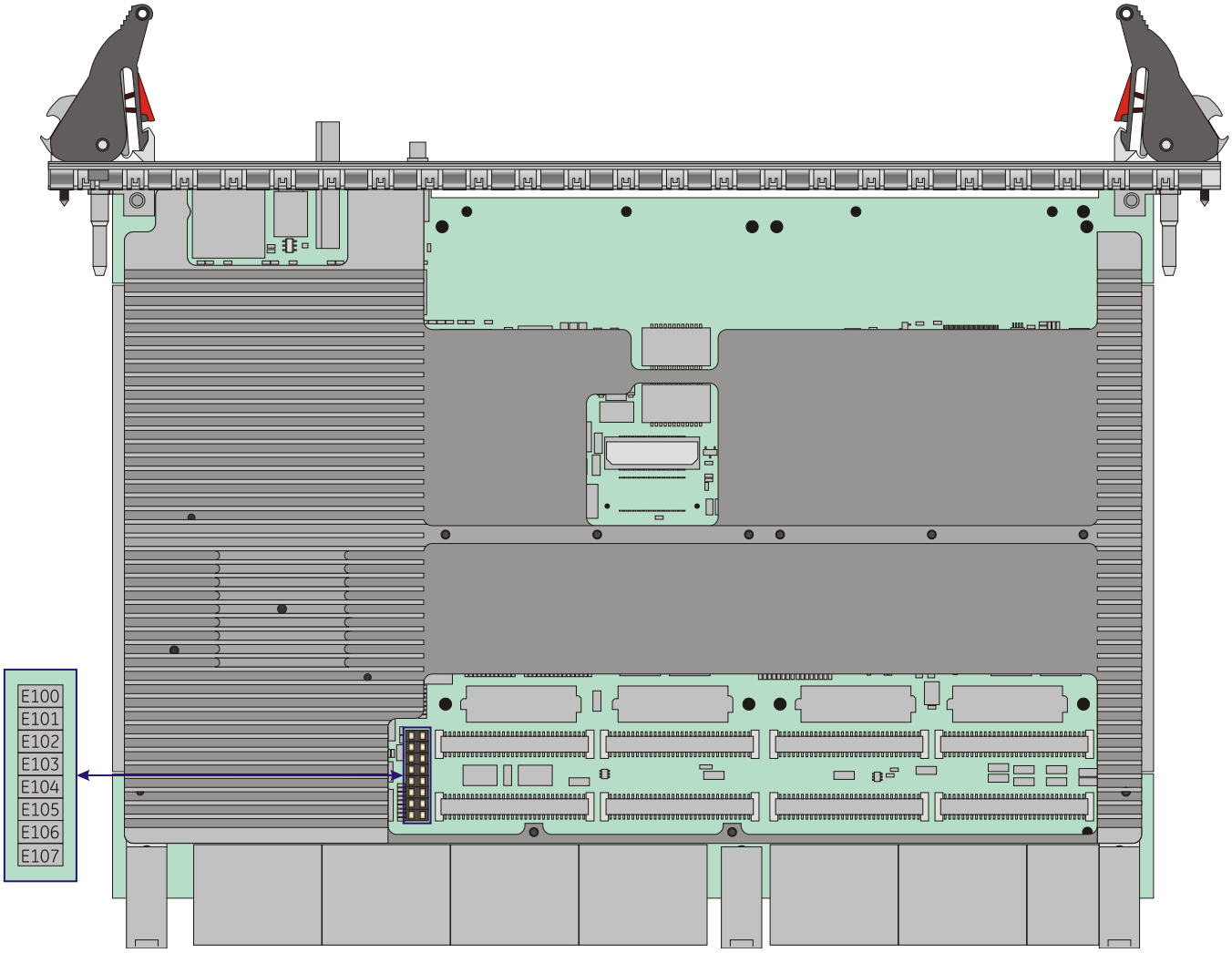
3.1 Link Configuration

The SBC624 has push-on jumpers included in the standard kit of parts; additional jumpers may be obtained on request. These are suitable for level 1 to 3 low vibration applications.

TIP

For Level 4 and 5 products, make links by wire-wrapping between the pin posts and then cover these wire wrapped links with the same conformal coating as that used on the board. This will provide a reliable connection under heavy shock and vibration conditions and further prevent oxidation of the connection due to moisture ingress.

Figure 3-1 Link Positions



The diagram above shows standard 2.54 mm pitch headers for general use.

This manual refers to jumper settings as In or Out. Meanings are as follows:

In = jumper fitted - 

Out = jumper not fitted - 

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3.2 Inspection

The SBC624 is shipped from the factory with no jumpers fitted.

3.3 Link Descriptions

NOTES

Ordinary operation requires no jumpers to be fitted.

The state of the links can be read from the FPGA Link Status Register (offset 0x607).

TIP

If you are about to install your board and power-up for the first time, leaving your board in the default configuration will enable board operation to be proven before tackling any further configuration issues.

3.3.1 Recovery Boot Link (E100)

This link allows user selection of the SPI Flash device from which the SBC624 boots, as follows:

Table 3-1 E100 Link Setting

Setting	Meaning
In	SBC624 boots from Recovery device
Out	SBC624 boots from Main device (default)

The factory-programmed Recovery device is for use if the Main device is corrupted. In normal operation, this link is not fitted and the SBC624 boots from the Main device.

Booting from the Recovery device puts the SBC624 into Recovery mode. Here, on-board configuration EEPROMs are disabled, allowing devices to come up using default strapping.

3.3.2 NVRAM Write Enable Link (E101)

This link controls the write protection for the user NVRAM device on the SBC624, as follows:

Table 3-2 E101 Link Setting

Setting	Meaning
In	NVRAM is write enabled when the backplane NVMRO signal is negated
Out	NVRAM is write protected (default)

NOTE

The VPX backplane Non-Volatile Memory Read Only (NVMRO) signal (on connector P0 pin A4) must also be set inactive low before the NVRAM can be written.

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3.3.3 Configuration EEPROM Write Enable Link (E102)

The non-volatile configuration EEPROM devices on the board are used to configure the initial state of the bridges, fabric switches and board configuration options controlled by software.

NOTE

This link controls the *hardware* write protection of the configuration EEPROM devices. Some devices also require software write protection, which must be provided by the Operating System or the BIOS.

Table 3-3 E102 Link Setting

Setting	Meaning
In	Configuration EEPROM hardware write protection is disabled
Out	Configuration EEPROM hardware write protection is enabled (default)

NOTE

The VPX backplane Non-Volatile Memory Read Only (NVMRO) signal (on connector P0 pin A4) must also be set inactive low before the configuration EEPROM can be written.

3.3.4 COM1 Routing Link (E103)

As COM1 is the default active debug port for some operating systems, it can be routed to the front panel J3 connector, allowing serial port connectivity without the need for an RTM.

Table 3-4 E103 Link Setting

Setting	Meaning
In	COM1 routed to front panel connector, COM3 not routed
Out	COM1 routed to backplane connector,COM3 routed to front panel connector (default)

When routed to the front panel, COM1 is not available on the backplane connector.

NOTES

This functionality can also be set in Control Register 5 (register offset 0x626) via BIOS configuration.

3.3.5 ETH1 Routing Link (E104)

ETH1 can be routed to the front panel J1 connector, allowing Ethernet port connectivity without the need for an RTM.

Table 3-5 E104 Link Setting

Setting	Meaning
In	ETH1 routed to front panel connector
Out	ETH1 routed to backplane connector (default)

When routed to the front panel, ETH1 is not available on the backplane connector.

NOTES

This functionality can also be set in Control Register 5 (register offset 0x626) via BIOS configuration.

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3.3.6 Scanbridge Enable Link (E105)

The SBC624 uses a JTAG Scanbridge device to connect all of the JTAG-compliant devices on the board. This link is provided to enable the Scanbridge during boundary scan; it should not normally be fitted in deployed systems.

Table 3-6 E105 Link Setting

Setting	Meaning
In	Scanbridge enabled
Out	Scanbridge disabled (default)

3.3.7 PMC1 and PMC2 VIO Selection Links (E106 and E107)

PMCs may use +5V or +3.3 V for the VIO signaling voltage. These links control the VIO signaling voltage provided by the SBC624 at the PMC sites (E106 for site 1 and E107 for site 2). These links should only be fitted when a PMC that uses 5V signaling is installed, and should be left not fitted otherwise.



CAUTION

Selection of the wrong VIO signaling voltage may cause damage to the PMC.

Table 3-7 E106 and E107 Link Setting

Setting	Meaning
In	PMC VIO signaling voltage is 5V
Out	PMC VIO signaling voltage is 3.3 V (default)

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3.4 Mezzanine Installation

As shown in Figure 3-2, the SBC624 has two mezzanine sites that both support suitably compliant PMCs or XMCs (including support for front-panel I/O). The two sites allow for the fitting of a double-width PMC/XMC if required.

3.4.1 PMC Installation

Each PMC site is factory-configurable to support either 3.3 V or 5 V VIO signaling voltage.

CAUTION

Ensure that the PMC1 and PMC2 VIO Selection Links (E106 and E107) are set according to the requirements of the corresponding PMC(s). Damage to the PMC(s) may otherwise result.

PMCs supplied by Abaco are delivered with a full kit of parts for mounting them. A PMC ordered with an SBC624 can be supplied factory fitted, if required.

LINK

PMC Installation Note, publication number HN4/3-99.

CAUTION

Observe handling and anti-static precautions when fitting the PMC.

It will usually be necessary to install driver software or implement other firmware configuration to achieve full functionality of a PMC (see the specific PMC manual for the exact procedure).

TIP

Where a PMC is not pre-installed, prove operation of the SBC624 *before* installing the PMC.

3.4.2 XMC Installation

XMCs supplied by Abaco are delivered with a full kit of parts for mounting them. Fitting is similar to a PMC. An XMC ordered with an SBC624 can be supplied factory fitted, if required.

CAUTION

Observe handling and anti-static precautions when fitting the XMC.

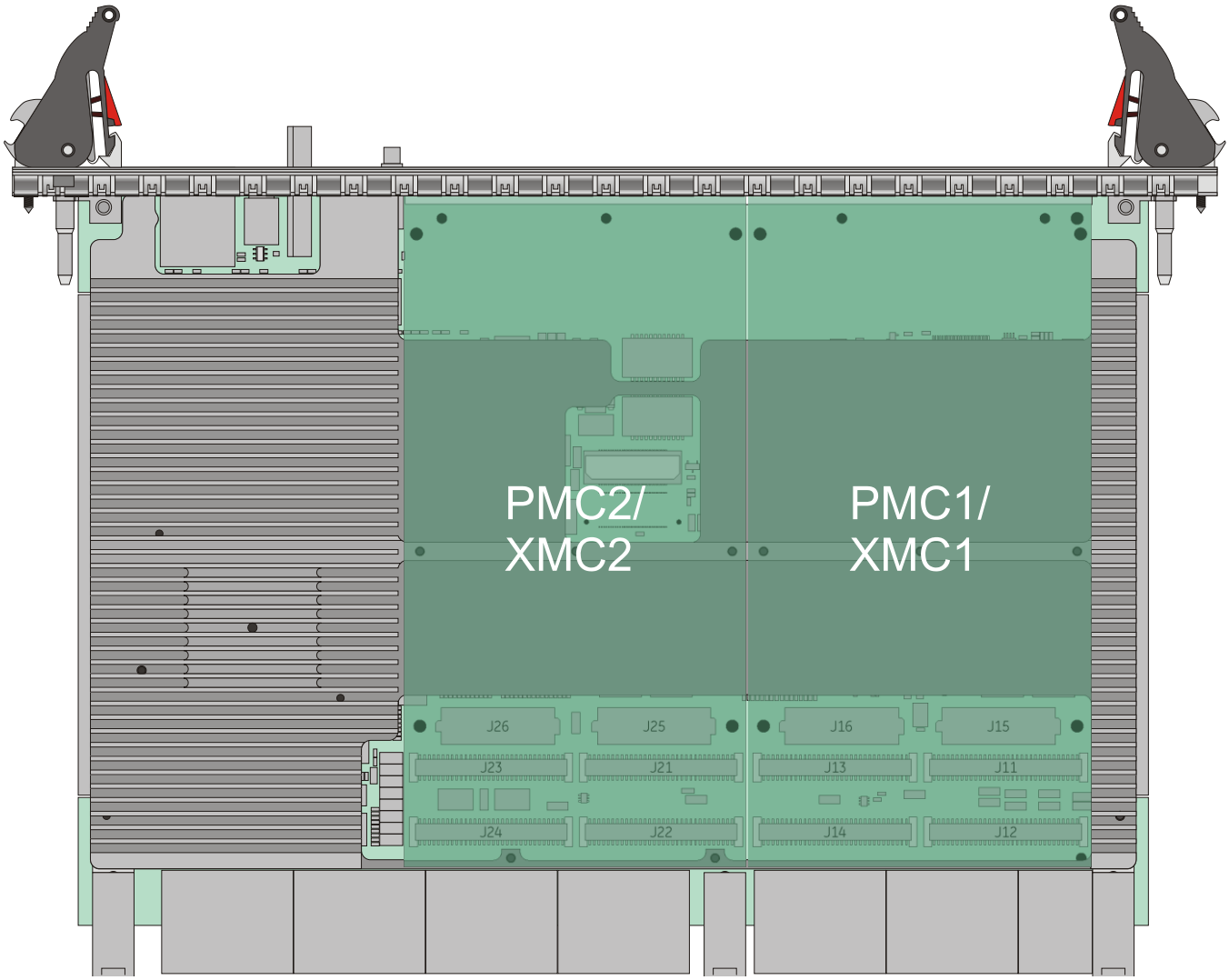
It will usually be necessary to install driver software or implement other firmware configuration to achieve full functionality of an XMC (see the specific XMC manual for the exact procedure).

TIP

Where an XMC is not pre-installed, prove operation of the SBC624 *before* installing the XMC.

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Figure 3-2 Mezzanine Positions



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4 • Installation and Power Up/Reset

Review the Safety Notices section before installing the SBC624. The following notices also apply:



CAUTION

Consult the enclosure documentation to ensure that the SBC624's power requirements are compatible with those supplied by the backplane.

4.1 Power Supply Requirements

The SBC624 requires the backplane to provide 12V (VS1 and VS2), 5V (VS3) and 3V3_AUX supplies. Requirements are as follows:

Table 4-1 Power Supply Requirements

Supply	Current Requirement	VPX Specification Limits
VS1 and VS2	Up to 7A	+12 V ± 5%
VS3	Up to 1A	+5 V +5% -2.5%
3V3_AUX	Up to 1A	+3.3 V ±5 %

P12V_AUX and N12V_AUX are not required for board operation, but are used to supply the ±12 V pins of the PMC sites and the auxiliary supplies of the XMC sites.

The VBAT supply may be used to power the Real-Time Clock in isolation when the board is powered down, to maintain the time/date information. This requires up to 6 µA at 3.3 V ±5%.

See the Electrical Specification section for more details.

4.2 Board Keying

The VPX specification defines three keying pins.

The keying pin at Position 1 (adjacent to the P0 connector) is used to define the voltage present on the VS1 and Vs2 supply pins on the backplane J0 connector. As the SBC624 may use these supplies, the module keying device in this position is of the keyed-315° type. This is also as required by the VITA65 OpenVPX Specification.

The keying pins at Position 2 (adjacent to the P2 connector) and Position 3 (adjacent to the P6 connector) are used to define slot-specific keying. The SBC624 is delivered with module keying devices of the unkeyed type in these positions to allow the board to be fitted to any backplane slot.

Contact the factory to discuss any specific keying requirements.

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4.3 Board Installation Notes

The VPX specification allows for a variety of different backplane pinouts depending on the mix of differential and single ended connectors. Take care to ensure that the pinout of the SBC624 matches that of the backplane slot before insertion.



CAUTION

The SBC624 has been specifically designed for use with 6U VPX backplanes designed to accommodate a differential pin out on the J2 connector and is *not* compatible with 6U backplanes where the J2 connector is intended for single-ended signaling. Plugging the SBC624 into such a 6U backplane may cause permanent component damage.

Air-cooled versions of the SBC624 have an injector/ejector handle to ensure that the backplane connectors mate properly with the backplane. The captive screws at the top and bottom of the front panel allow the board to be tightly secured in position, which provides continuity with the chassis ground of the system.

Conduction-cooled versions of the SBC624 have screw-driven wedgelocks at the top and bottom of the SBC624 to provide the necessary mechanical/thermal interface. Correct adjustment requires a calibrated torque wrench with a hexagonal head of size $^{3}/_{32}$" (2.38 mm), set to between 0.6 and 0.8 Nm.

In an air-cooled development enclosure, when taking I/O connections from the backplane connectors, use of Abaco I/O modules (or some equivalent system) ensures optimum operation of the SBC624 with regard to EMI. See the VPX I/O Modules manual for more details.



LINK

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

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4.4 Connecting to SBC624

To interact with on-board firmware requires the SBC624 to have, as a minimum, a terminal connection present on the serial COM1 port. Ethernet, video and USB connections may also be required, depending on Operating System requirements. These ports may be accessed either through the backplane pins, using a rear transition module, or via the front I/O connectors on air-cooled boards.

COM1 is configured as DTE with default settings of 115200 baud, 8 bits/character, 1 stop bit, parity disabled and no flow control.

4.4.1 Rear Transition Module

For development systems, connection to the Serial and Ethernet I/O can be achieved using a Rear Transition Module (RTM). This converts the condensed pin out of the backplane connectors to pinouts suitable for use by industry standard connectors.

The following items are required:

- The SBC624
- The appropriate RTM (VPX6UX604)
- A null-modem 9-way D to 9-way D-type cable for connecting COM1 to a control terminal or PC running terminal emulation software
- For the Ethernet port, a CAT5 (or better) straight-through patch cable for 10/100/1000BaseTX
- For video, a DVI or VGA monitor with cable (DVI-D or DVI-I connection for DVI or DE-15 connection for VGA)
- For USB, the required peripheral with a standard type A connector

The VPX I/O Modules manual contains more details on fitting RTMs. Similar antistatic and safety precautions apply when handling and/or installing RTMs as for the SBC624.



LINKS

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

VPX6UX604 Hardware Reference Manual, publication number 522-9300527824-000.

See Appendix B for the mapping of ports between SBC624 and VPX6UX604.

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4.4.2 Front I/O (Air-Cooled Boards Only)

It is also possible to access COM1, Ethernet, DVI/HDMI video and USB ports on air-cooled boards through front-panel I/O connectors. The following items are required:

- The SBC624
- A serial 9-way adapter cable (contact your nearest sales office or agent)
- A null-modem 9-way D-type cable for connecting COM1 to a control terminal or PC running terminal emulation software
- For the Ethernet ports, a CAT5 (or better) straight-through patch cable for 10/100/1000BaseTX
- For video, a DVI or HDMI monitor with a mini HDMI cable or adapter
- For USB, the required peripheral with a standard type A connector



CAUTION

Front Panel I/O cables should only be inserted or removed when power to the board is off. Inserting the connectors while the SBC624 is powered on may cause permanent component damage.

4.5 Reset and Power-up Sequence

A power sequencer monitors the backplane supply voltages and will hold the SBC624 in reset or shut down the on-board power supplies if the backplane supplies are not within specified limits.

The green Power Good LED (DS6) on the back of the PWB is lit when the backplane and all on-board supplies are within specification.

The +5V supply to the mezzanine cards is switched, under the control of the power manager device, so that the 5V and 3.3V supplies are applied to the mezzanines at approximately the same time.

The SBC624 supports the PSU_SEQ_IN/PSU_SEQ_OUT power sequencing signals (on the P1 connector pins G9 and G11) in line with other Abaco boards. When connected in a power-sequencing daisy chain, the on-board power supplies will only power up when SEQ_IN pin is asserted or floated high. An automatic override function is used which will power-up the board if the SEQ_IN pin has been low for more than 500ms. See the Inter-board Sequencing section for more details.

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4.6 BIOS Setup Utility

Various aspects of the SBC624's functionality may be configured through the BIOS Setup utility. The following sections give a brief overview of the Setup menus available in the BIOS firmware.

4.6.1 Accessing the Setup Menus

To access the First Boot menu, press the F7 key as the SBC624 is booting.
To access the Setup menus, press the Delete key as the SBC624 is booting. The main BIOS set-up screen is displayed.

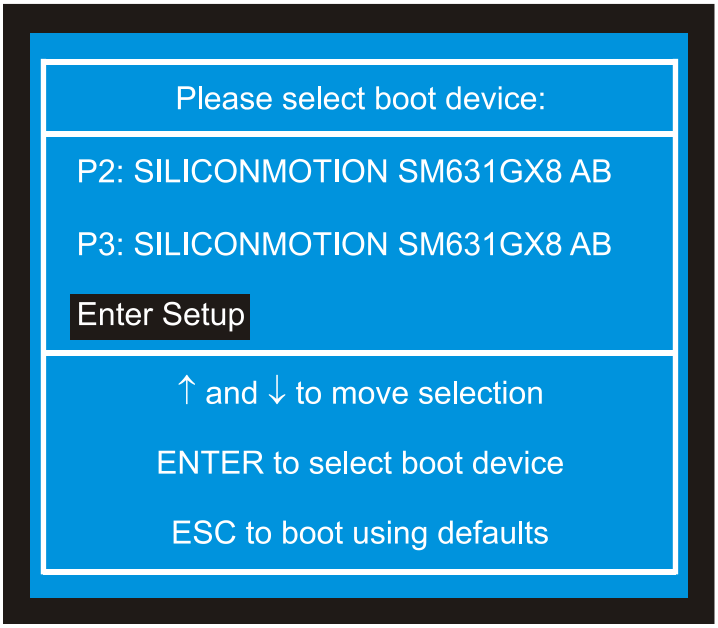
4.7 First Boot Menu

This enables the user, *for one time only*, to select a drive device from which to boot. This feature is useful when installing from a bootable disk. For example, when installing an operating system from a CD, enter this menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with the boot.

The First Boot menu is accessed by pressing the F7 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the SBC624.

If you have trouble accessing the First Boot menu, from the Boot menu, disable Fast Boot. Exit, saving changes and retry accessing this feature.

Figure 4-1 First Boot Menu



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4.8 About the Setup Menus

The Setup menus are accessed by pressing the Delete key at the very beginning of the boot cycle.

The Setup menus have two main areas. The left frame displays status data and the options or sub-menus that can be configured. Here, text in black is for information only, and options and sub-menus are in blue text (or greyed out if unavailable) with sub-menus being distinguished by "▶". Selecting an option or sub-menu, highlights it in white. Where there is more text than will fit into this frame (e.g. the Main men), a scrollbar is displayed.

The right frame displays the key legend. Above this is an area that, when an option or sub-menu is selected in the left frame, displays a text message giving a brief description of that option or sub-menu.

As shown in the key legend, use the left and right arrow keys to select the required Setup menu. Use the up and down arrows to select an option or sub-menu, then press Enter to pick that sub-menu or option for altering. To step through the range of available settings (e.g. enabled/disabled) for that option, use the '+' and '-' keys.

When in a sub-menu, the Setup menu selection line shows the top-level menu selection only.

This section shows examples from a working SBC624. While the general type and level of information displayed should be similar for your board, expect some details to differ. Available options may also differ from those shown here.



CAUTION

Changes made from some menus can cause the SBC624 to malfunction. If problems are detected after changes have been made, reboot the board and access the Setup. Select the Save & Exit menu, pick Restore Defaults then save these changes and reboot the board (e.g. by picking Save Changes and Reset).



NOTE

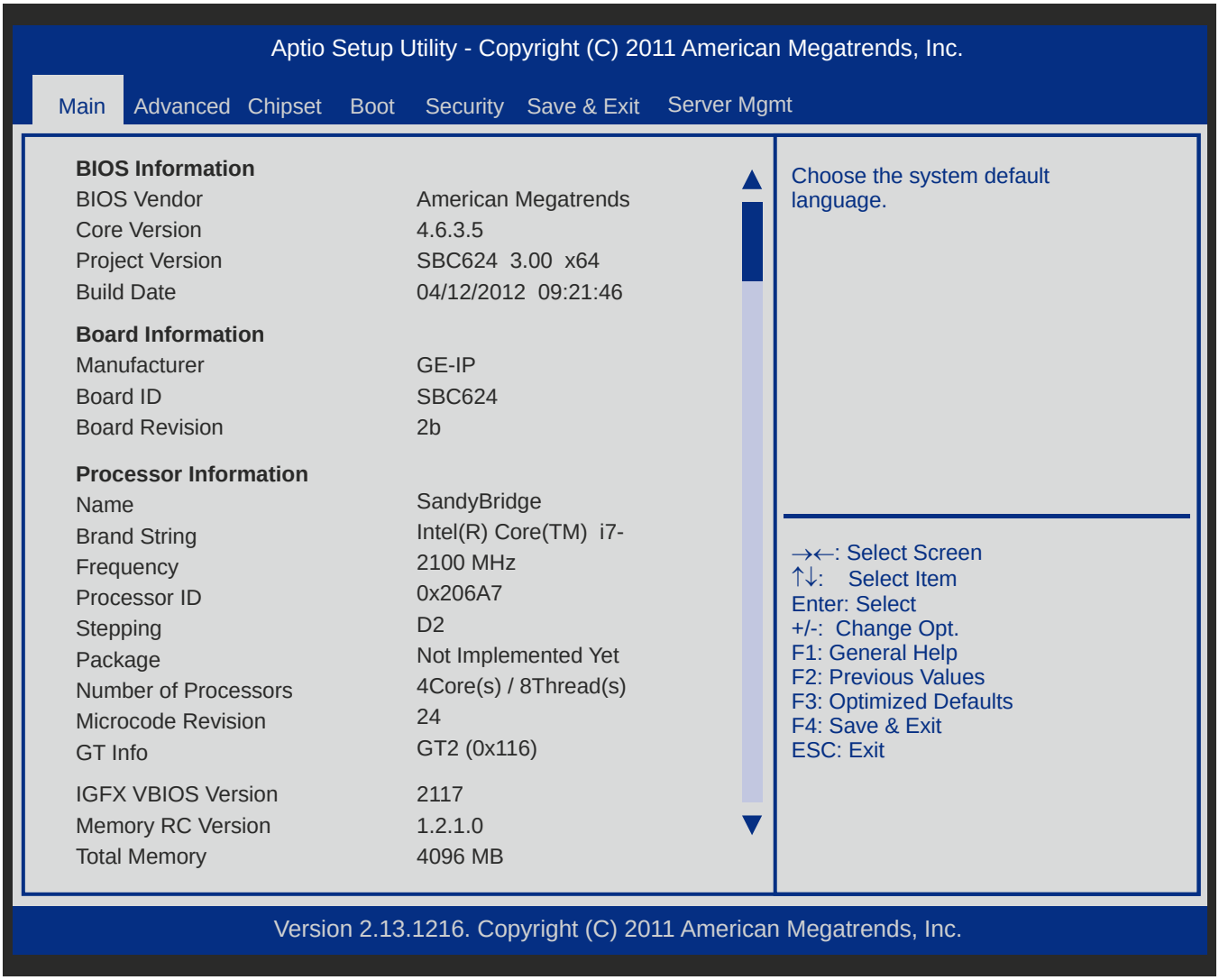
When Save & Exit is activated, the BIOS itself decides whether a reboot (power cycle) is required before running the following operating system and, if so, initiates one automatically. Thus, if (for instance) a boot option change does not lead to a reboot when Save & Exit is activated, this is because one is not required, *not* because the user is then expected to reboot the board manually.

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4.9 Main Menu

This is the menu shown on entry to Setup. It reports details on the BIOS firmware, the board and the processor. It also allows the user to set the System Language (English is the default and currently the only option) and the SBC624 clock/calendar (although without battery back-up, any power cycle will reset the clock).

Figure 4-2 Main Menu



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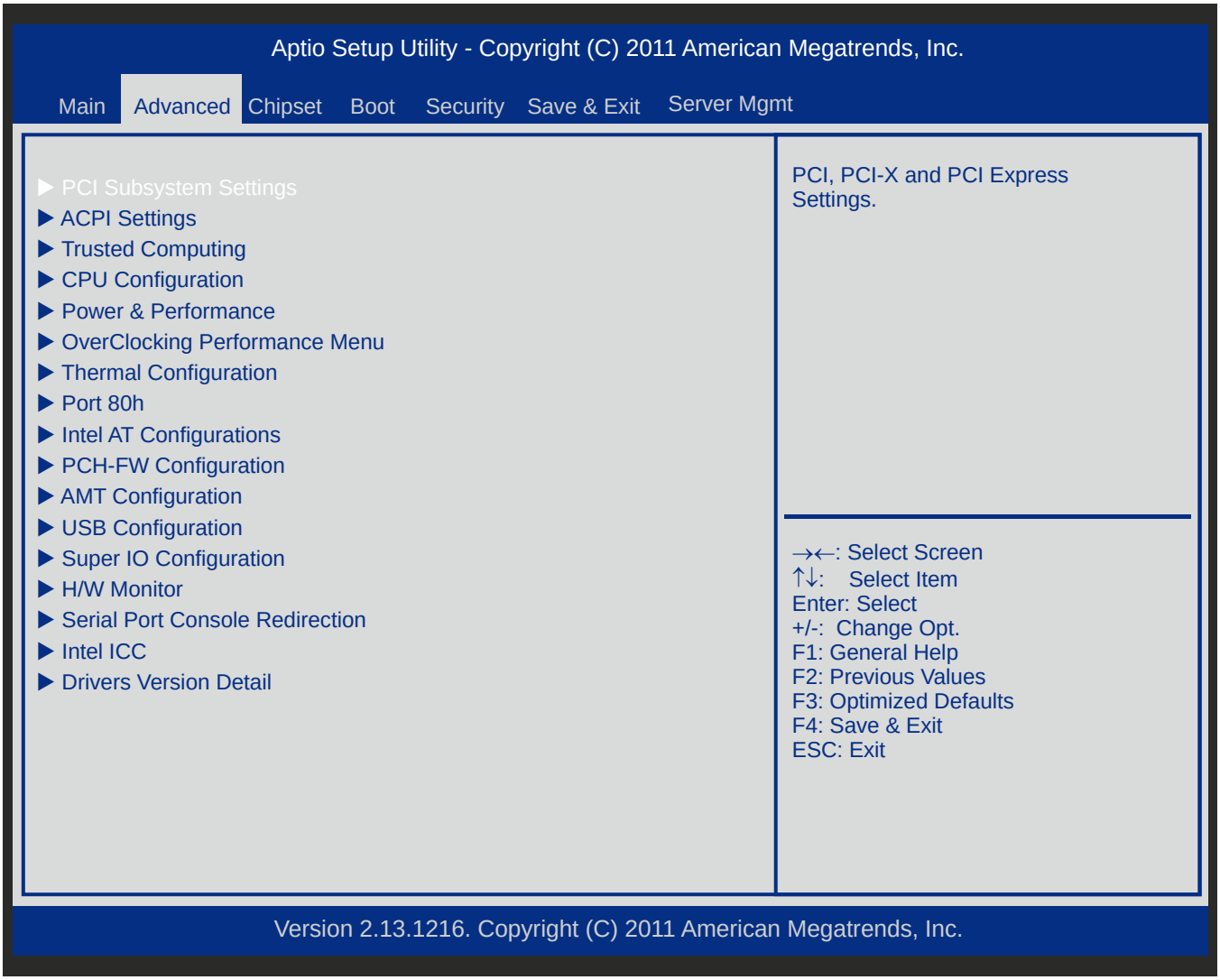
4.10 Advanced Menu

This allows configuration of many CPU and chipset settings.

CAUTION

Changes made from some menus can cause the SBC624 to malfunction. If problems are detected after changes have been made, reboot the board and access the Setup. Select the Save & Exit menu, pick Restore Defaults then save these changes and reboot the board (e.g. by picking Save Changes and Reset).

Figure 4-3 Advanced Menu



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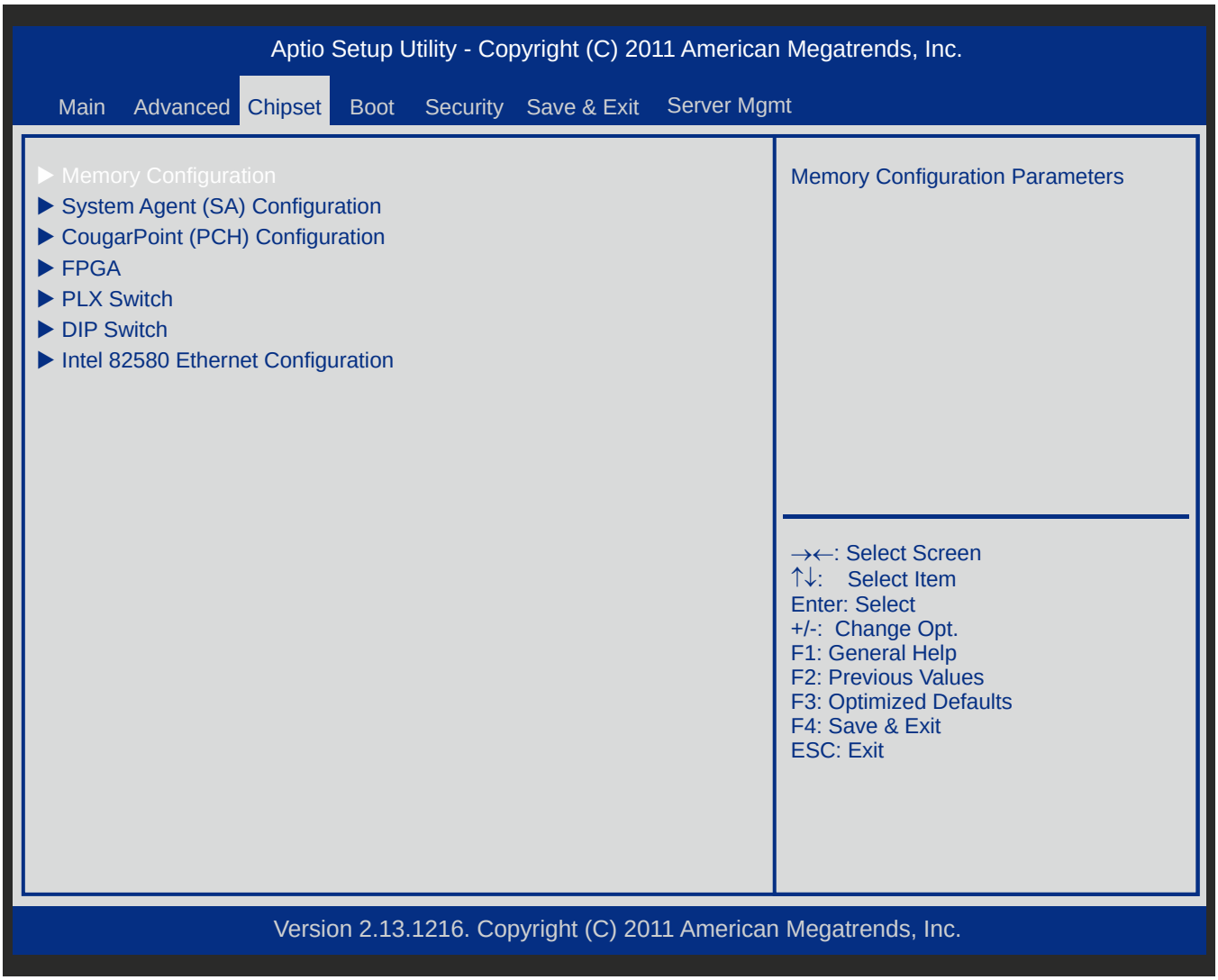
4.11 Chipset Menu

This allows selection of the various options for the chipsets on the board (for example, the CPU configuration and configurations for the PCH). The settings for the chipsets are processor-dependent; take care when changing settings from the defaults set at the factory.

CAUTION

Changes made from some menus can cause the SBC624 to malfunction. If problems are detected after changes have been made, reboot the board and access the Setup. Select the Save & Exit menu, pick Restore Defaults then save these changes and reboot the board (e.g. by picking Save Changes and Reset).

Figure 4-4 Chipset Menu



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4.11.1 Enabling Booting Over a Network

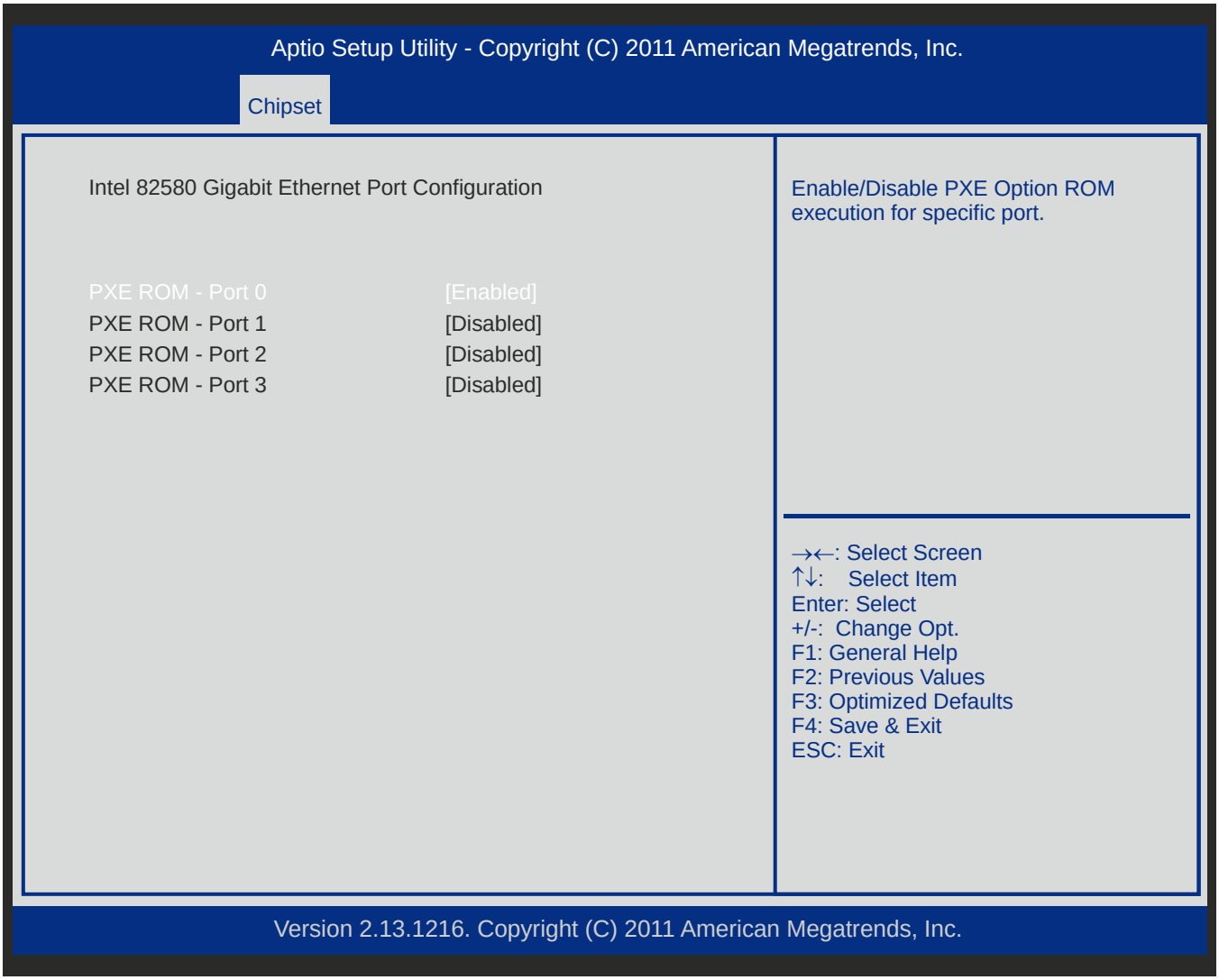
The BIOS firmware provides support for booting over a Gigabit Ethernet LAN (sometimes called PXE booting). This is disabled by default.

To enable booting from the network, pick Intel 82580 Ethernet Configuration from the Chipset menu to display a sub-menu similar to the one shown below. This allows enabling of PXE boot on each network port.

NOTE

The backplane Ethernet ports on the SBC624 are ports 2 and 3.

Figure 4-5 Ethernet Boot Selection Sub-menu



Press F4 to save and exit the BIOS Setup menus.

NOTE

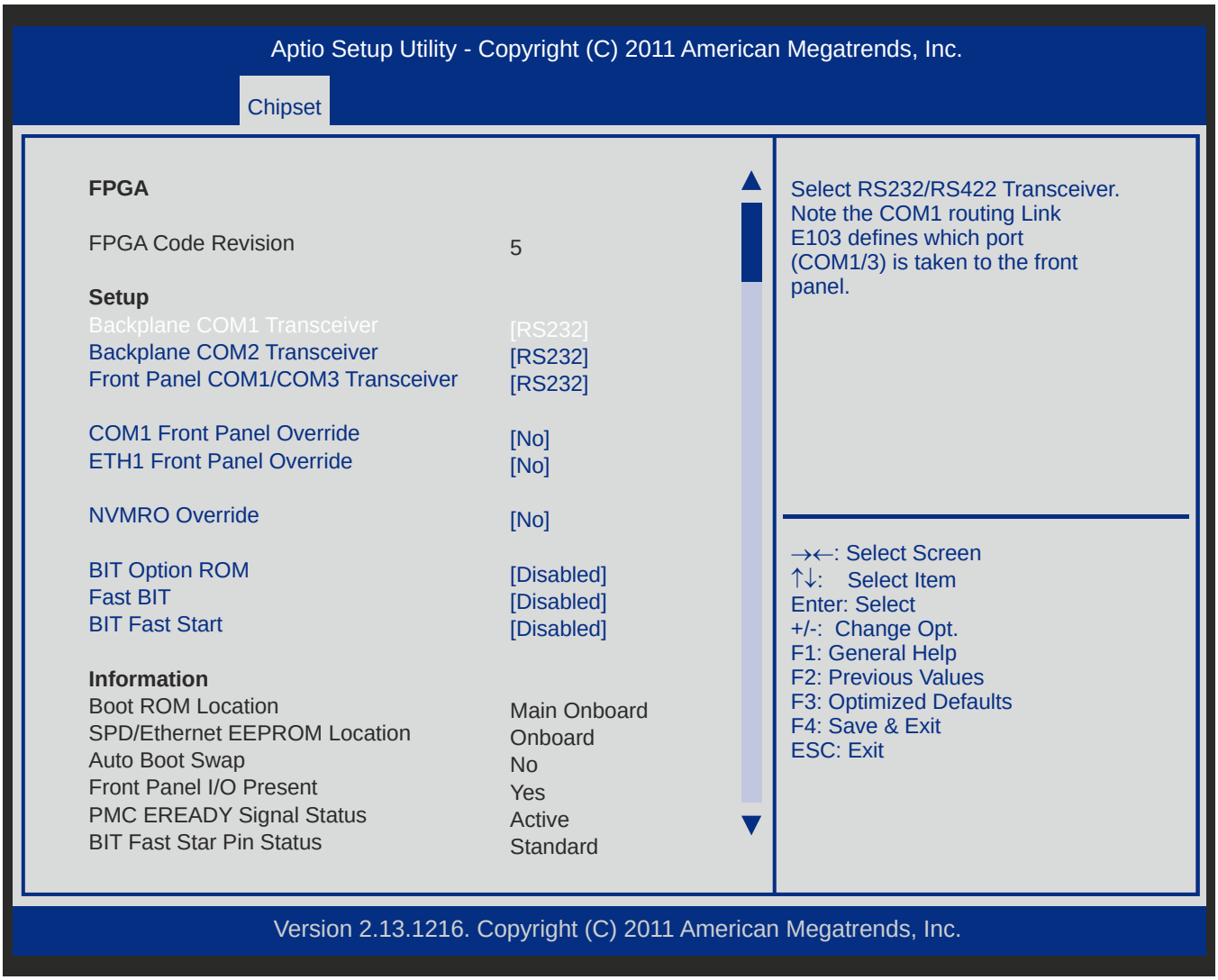
To boot from the network, some operating systems require that the network driver be set to 'boot' in the Control Panel.

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4.11.2 FPGA Setup/Status

The Setup allows some on-board functions that are controlled by the FPGA to be configured and/or their status reported. To access these options, pick FPGA from the Chipset menu to display a sub-menu similar to the one shown below:

Figure 4-6 FPGA Setup/Status Sub-menu

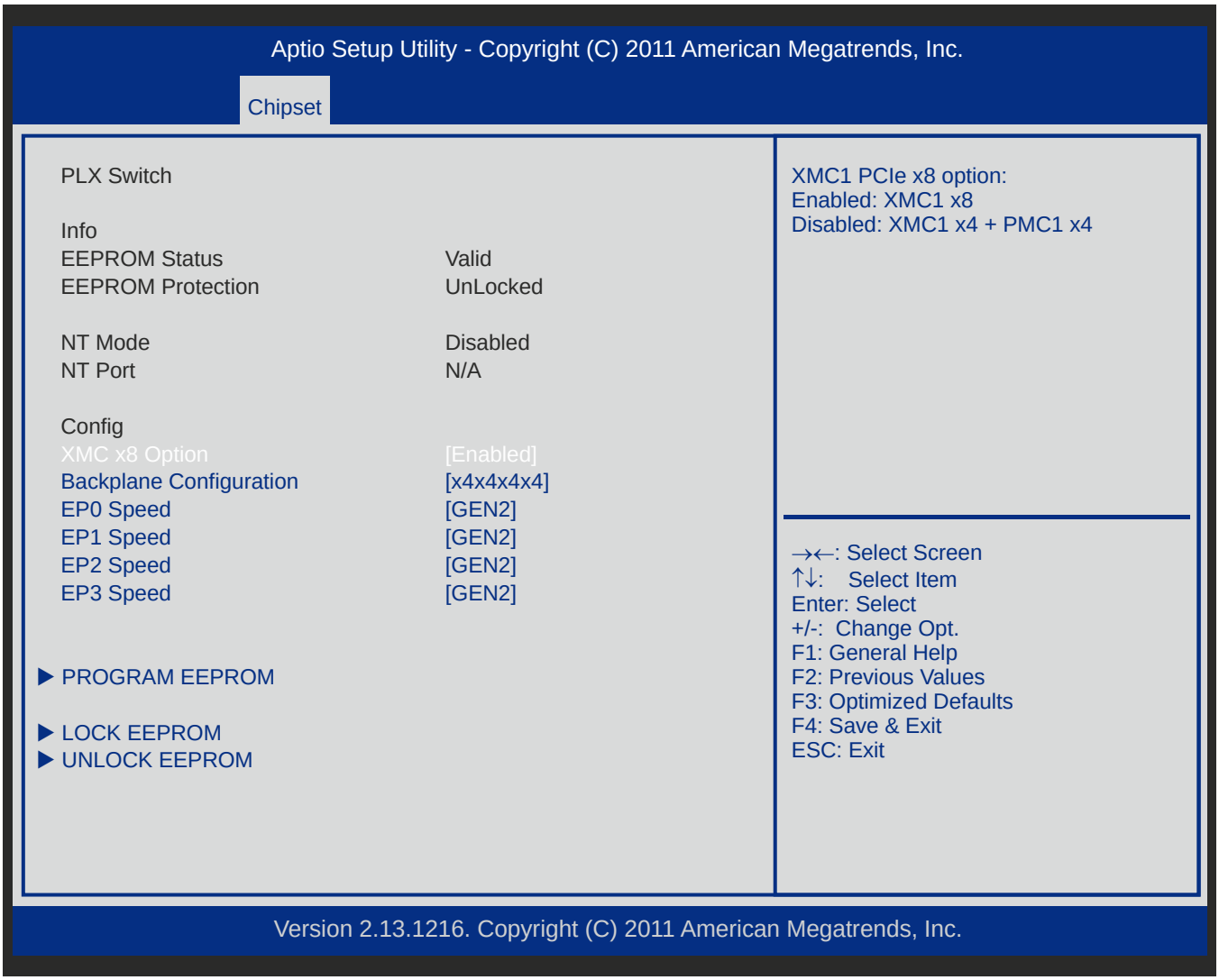


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4.11.3 PLX Switch Setup/Status

This menu allows the user to set some aspects of the on-board PCIe switch configuration. Settings are selected via this menu, then activated by programming them into the configuration EEPROM. They are then loaded into the switch configuration registers the next time the board is reset or power cycled.

Figure 4-7 PLX Switch Sub-menu



XMC x8 Option

This can be used to select whether the XMC1 site is connected with a x8 link (Enabled) or a x4 link (Disabled). When x8 mode is disabled, it is possible to link to both an XMC and the PCI-X Bridge, allowing mezzanine cards that have both interfaces fitted to be used.

The x8 mode is enabled by default. This is the recommended setting for most applications.

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Backplane Configuration

This can be used to configure the backplane Expansion Plane PCIe configuration. Allowable configurations are x16, x8+x8, x8+x4+x4, x4+x4+x4+x4.

The OpenVPX naming convention is followed, where "EPx" relates to one of four fat pipes (x4) available on P2 (EP0 is the top-most fat pipe; EP3 is the bottom-most).



NOTE

If an operating system has configured the SBC624 for NT operation, it is not possible to alter the backplane configuration using this menu, and the option will be greyed-out. In this configuration, only the operating system can change this setting.

EPx Speed

This allows the speed (Gen1 @ 2.5 Gbits/second or Gen2 @ 5 Gbits/second) of each EP link to be set. This is useful when it is desirable to force the SBC624 to operate at a lower link speed. For instance, when cables are being used in a development backplane to connect the Expansion Plane, forcing Gen1 mode using this method is recommended.

By default, the speed of each EP link is Gen2 (5 Gbits/second).

Program EEPROM

Once the required PCIe switch settings have been made, select this option to program the configuration into the EEPROM. The new configuration is only activated *after* the board has been reset or power cycled.



NOTE

Ensure that the EEPROM is write-enabled before selecting this option, i.e. a jumper is fitted on the Configuration EEPROM Write Enable Link (E102), and the backplane NVMRO signal is inactive.

Lock EEPROM

This locks the EEPROM. When locked, the EEPROM *cannot* be overwritten by third party software (such as PLX development tools), regardless of the state of the write protect links and NVMRO.

By default, the EEPROM is unlocked.

Unlock EEPROM

This unlocks previously locked EEPROM. The EEPROM is unlocked by default.



NOTE

Once locked, the EEPROM can only be unlocked when it is write-enabled, i.e. a jumper is fitted on the Configuration EEPROM Write Enable Link (E102), and the backplane NVMRO signal is inactive.

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4.11.4 DIP Switch Setup

The SBC624 has an on-board EEPROM DIP switch that provides non-volatile configuration settings. The DIP switch can be used to enable or disable hardware write protection of the on-board SSDs. By default, the SSDs are write-enabled. To activate a new configuration, select the required settings and then select the PROGRAM DIP SWITCH option.

NOTE

Ensure that the DIP switch is write-enabled before selecting the PROGRAM DIP SWITCH option, i.e. a jumper is fitted on the Configuration EEPROM Write Enable Link (E102), and the backplane NVMRO signal is inactive.

Figure 4-8 DIP Switch Sub-menu



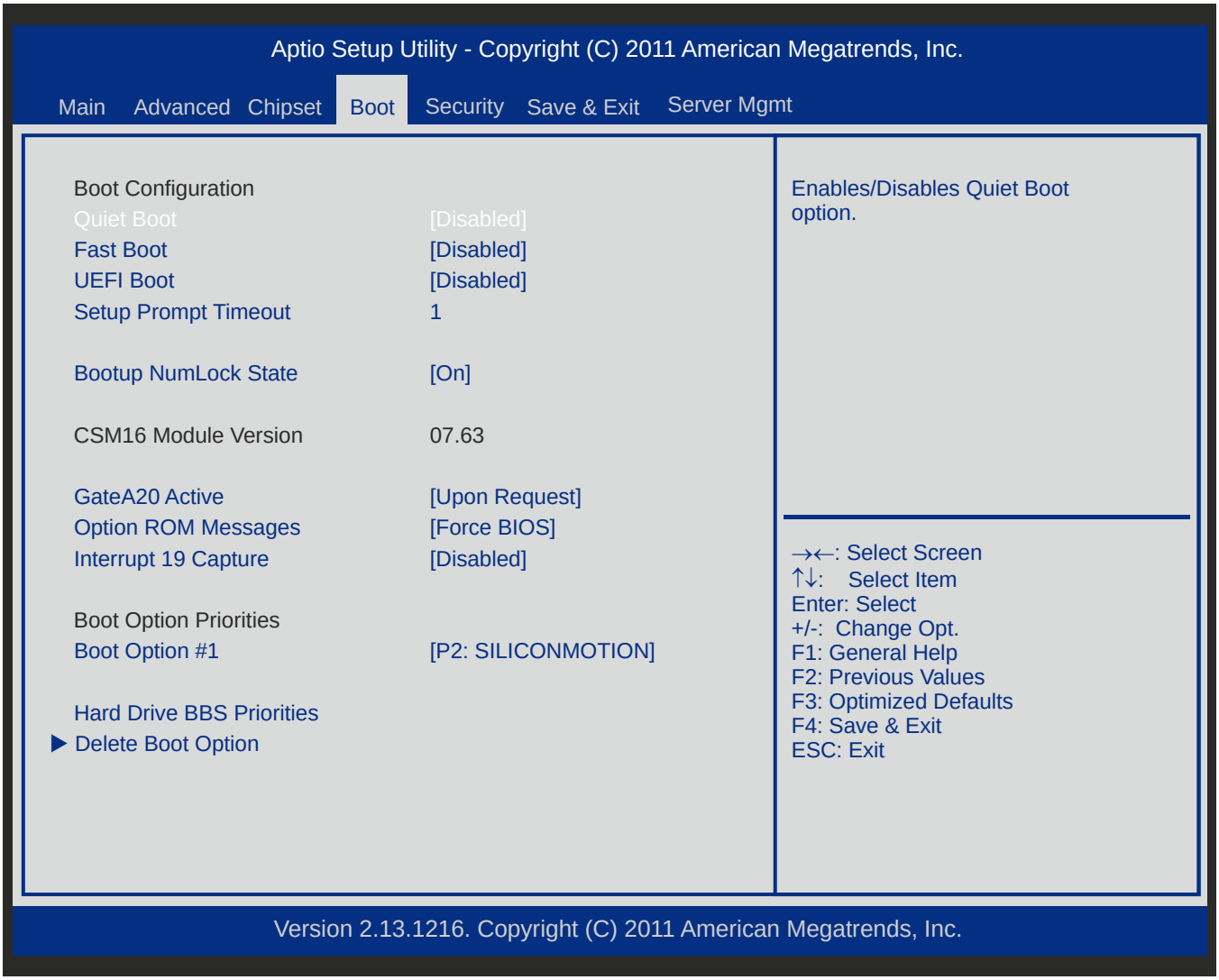
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4.12 Boot Menu

This sets the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If an installed drive does not appear, verify the hardware installation.

Also available in this menu are Boot Configuration settings that allow the user to set how the SBC624 acts, for example, whether to use 'Fast Boot'.

Figure 4-9 Boot Menu



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4.13 Security Menu

This menu allows setup of both an Administrator and a User password. The on-screen description covers use of these passwords. If both passwords are to be used, the Administrator password must be set first.

Figure 4-10 Security Menu



CAUTION

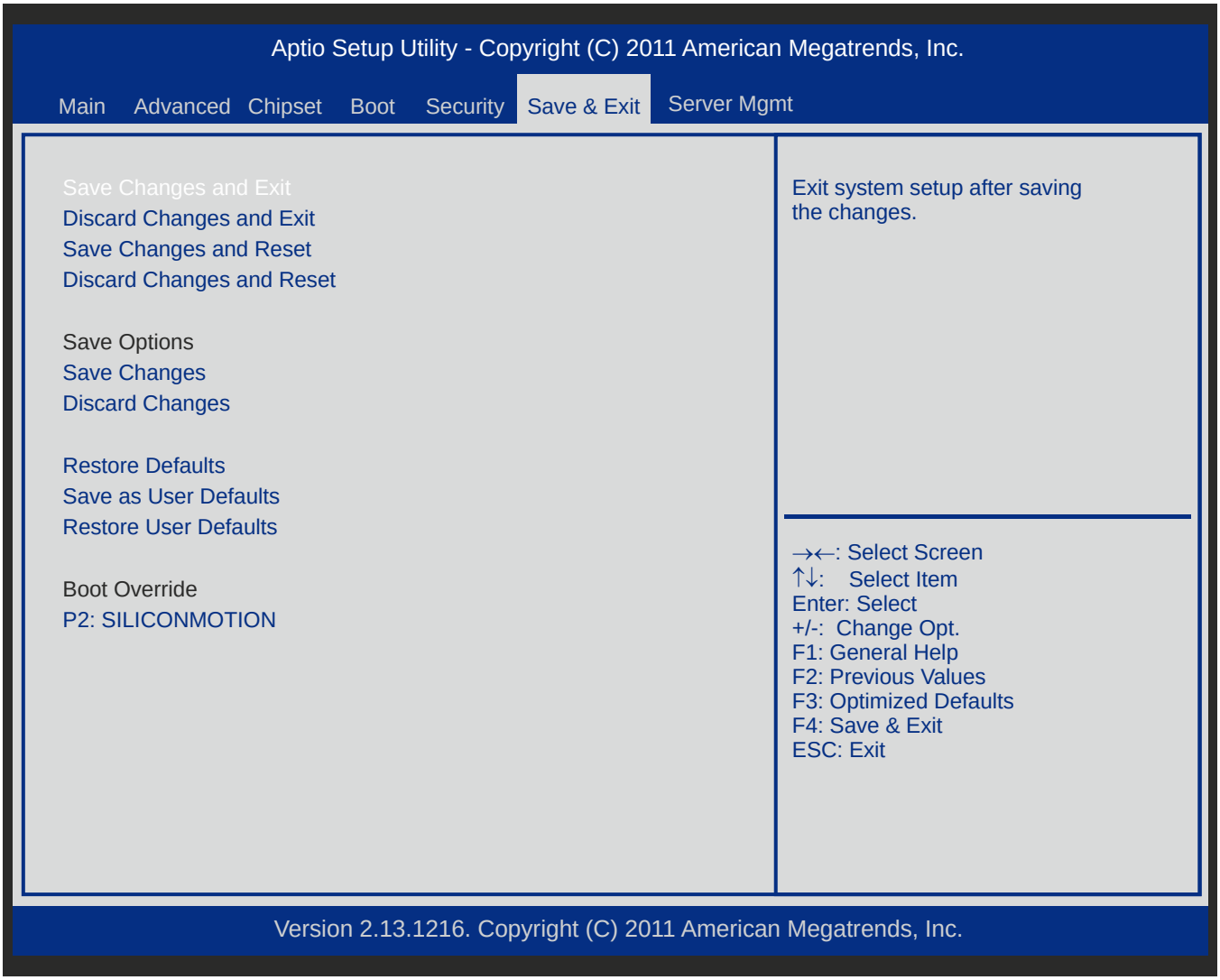
Take care when setting passwords. Once a password is set, there is no method available to the user to reset it without using that original password. If a password is lost, the BIOS will need to be reprogrammed. Should this event occur, contact technical support for assistance.

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4.14 Save & Exit Menu

This provides options on saving Setup selections and exiting Setup.

Figure 4-11 Save & Exit Menu



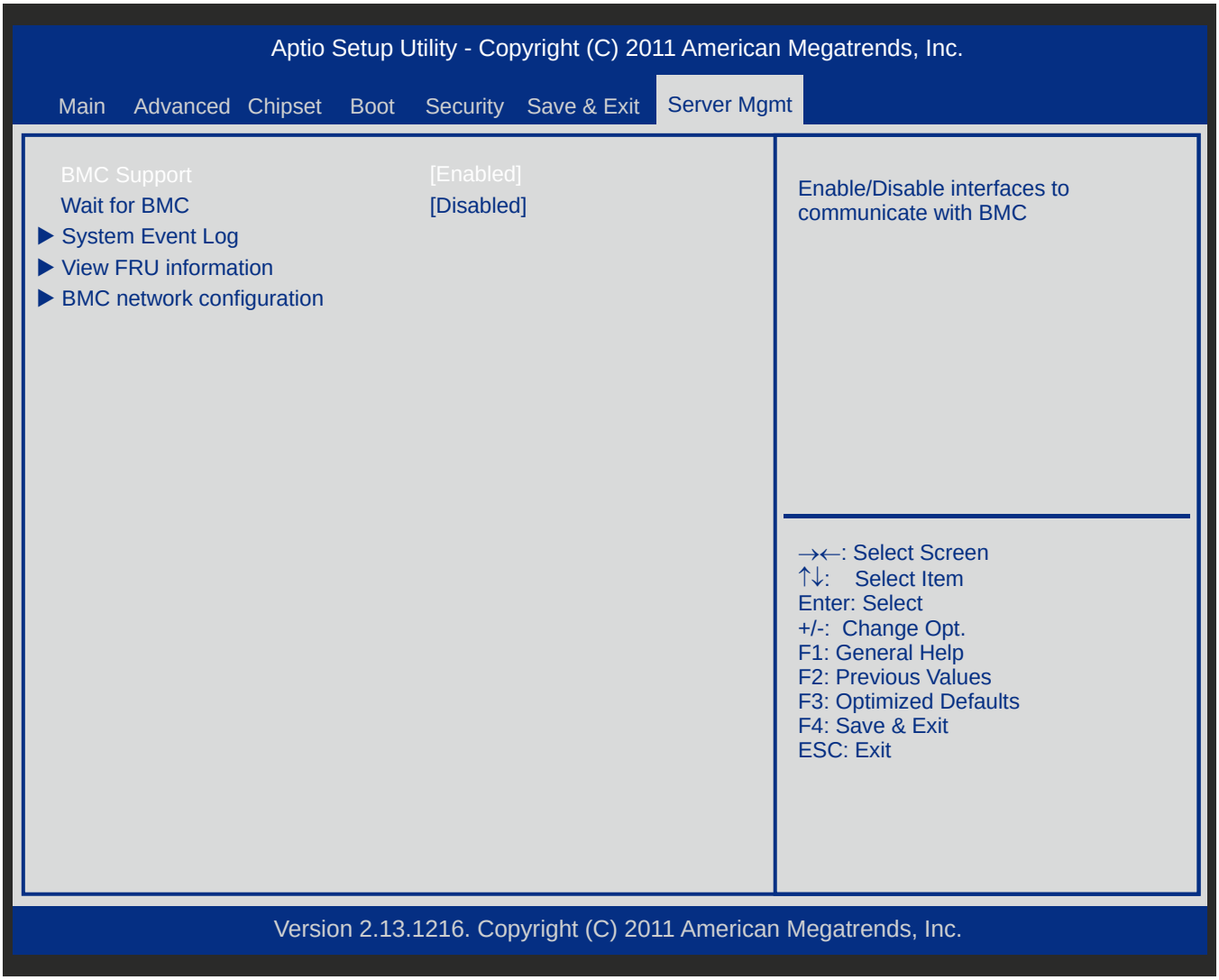
If changes have previously been made from the Setup menus, and the SBC624 malfunctions, reboot the board and select this screen. Pick Restore Defaults then save these changes and reboot the board (e.g. by picking Save Changes and Reset).

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4.15 Server Management Menu

This menu provides options for configuring the BMC (see section 5.9.7) and displaying Field Replaceable Unit (FRU) data.

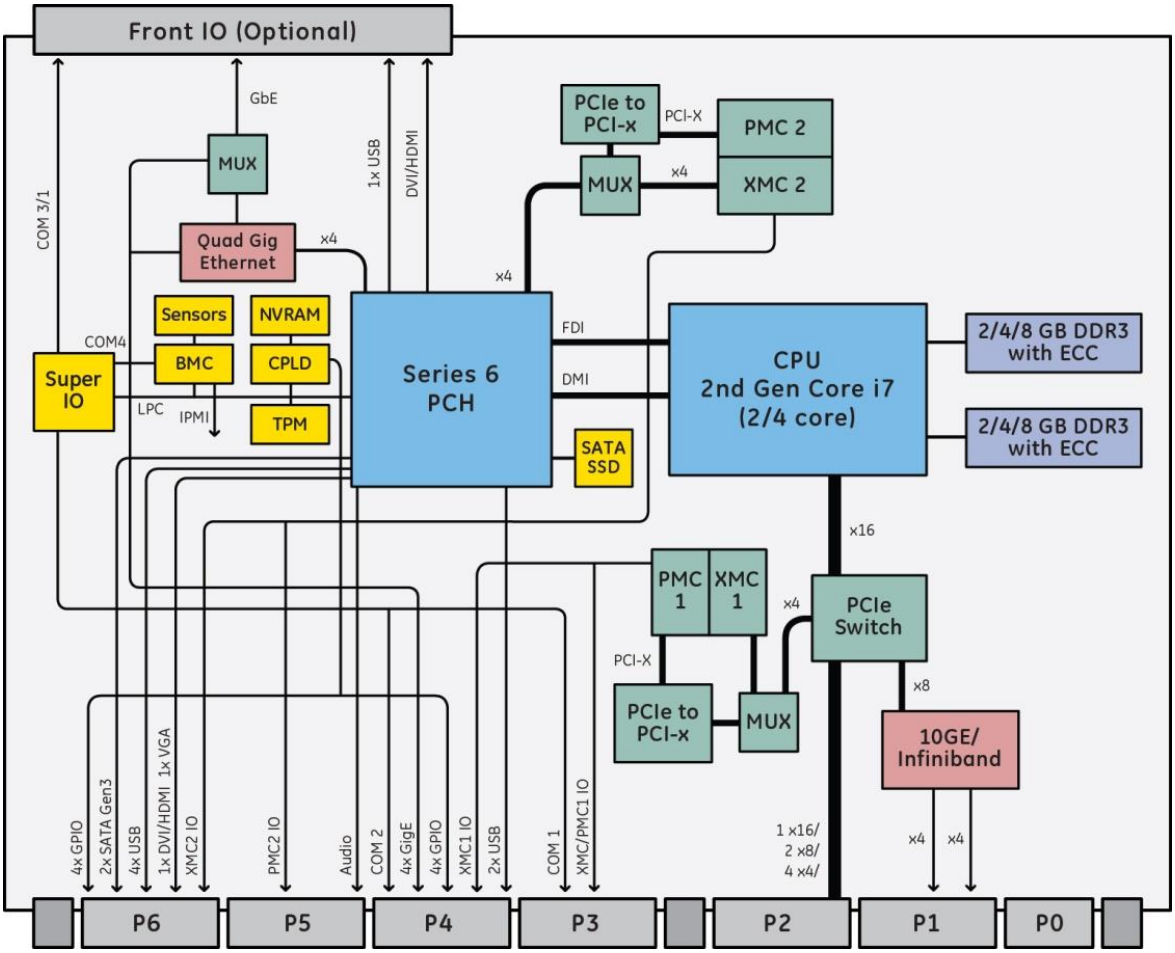
Figure 4-12 Server Mgmt Menu



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5 • Functional Description

Figure 5-1 Block Diagram



NOTES

Due to the increasingly short lifetimes of system components, the I/O devices used on the SBC624 are not guaranteed to remain fixed in the future.

Hardware should be accessed only through mechanisms provided by the Operating System's Board Support Package, and not directly by application software.

If a standard operating system is not being used, then it is recommended that applications are written in such a way as to minimize direct access to hardware resources, bearing in mind that changes may be necessary to support future iterations of the hardware.

Abaco-supported Operating Systems guarantee compatibility at the application level through hardware independent mechanisms.

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5.1 Features

- Intel Huron River Mobile (+ECC) platform-based SBC
- Intel second generation Core i7 processor, with up to four cores, at up to 2.5 GHz
- Up to 16 GBytes of dual channel DDR3 SDRAM with ECC (8 GBytes per controller)
- Up to 32 GByte SATA Solid State drive storage
- Two 512 KByte Non-Volatile MRAM boot devices
- Two channels of 1000BaseBX Ethernet
- Two channels of 1000BaseT Ethernet
- One VGA video port
- Up to two DVI/HDMI video ports
- Three serial COM ports
- Six channels of USB 2.0 connectivity to the VPX backplane
- Three SATA channels connected to the VPX backplane
- Two channels of 10G Ethernet or two channels of x4 Infiniband
- 16-lanes of PCI Express in various configurations to the backplane with non-transparent operation
- 8 bits of General Purpose I/O with interrupt capability
- Two mezzanine sites:
- Site 1: PMC: 64-bit/133 MHz PCI-X. XMC: x8 PCIe
- Site 2: PMC: 64-bit/133 MHz PCI-X. XMC: x4 PCIe
- Elapsed time indicator
- Watchdog timers
- Ambient and chip temperature sensors
- System Management via BMC
- 6U VPX form factor
- Compatible with requirements of VITA65 OpenVPX specification
- Capable of being used as a payload board within systems designed around it
- MOD6-PAY-4F1Q2U2T-12.2.1-8 module profile
- I/O configurations that are pin-compatible with the SBC622
- Five environmental build levels

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5.2 Microprocessor Subsystem

The core chipset is based on Intel's Huron River Mobile (+ECC) platform and consists of:

- Intel 2nd generation Core i7 processor, with up to four cores, at up to 2.5 GHz
- Intel 6 Series chipset (Platform Hub Controller)



LINK

For more details on the processor and chipset, see http://www.intel.com.

5.2.1 Second Generation Core i7 Processor

This includes the following features:

- Four or two execution cores
- Intel Advanced Vector Extensions (AVX)
- A 32 KByte instruction and 32 KByte data first-level cache (L1) for each core
- A 256 KByte shared instruction/data second-level cache (L2) for each core
- Up to 8 MByte shared instruction/data third-level cache (L3), shared among all cores
- One x16 or two x8 PCIe Gen 2 interfaces
- Dual 64-bit memory controllers with ECC
- Integrated Graphics controller

The following table shows the Processor Stock Keep Units (SKUs) supported. Contact your nearest Abaco sales office or agent for the latest processor options and speeds.

Table 5-1 Supported Processor SKUs

SKU	Core Frequency (GHz)	Number of Cores	Cache Size (MBytes)	Estimated TDP (Watts)
Core i7-2610UE (ULV)	1.5	2	3	17
Core i7-2655LE (LV)	2.2	2	4	25
Core i5-2515E (SV)	2.5	2	3	35
Core i7-2715QE (SV)	2.1	4	6	45



NOTE

The CPU operating frequency and the temperature are inter-dependent. This means that for a given temperature, a maximum CPU operating frequency is achievable, and conversely for a given CPU operating frequency, a maximum temperature is achievable. This is further affected by the build level, which dictates the maximum ambient temperature at which the board can operate (see the Environmental Specification section). For more details, contact your nearest Abaco sales office or agent.

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5.2.2 6 Series Chipset (PCH)

The following features of the PCH are implemented on the SBC624:

- Two PCIe Gen2 x4 root ports
- Two SATA host controllers supporting five ports. Two ports support 6 Gbits/second (Gen3) while all ports support 3 Gbits/second (Gen2) and 1.5 Gbits/second (Gen1
- LPC interface
- SPI interface for boot Flash
- APIC interrupt controller
- 2xUSB EHCI controllers supporting seven USB 2.0 ports
- RTC – Mot MC146818B compatible
- Enhanced Power Management
- SMBus 2.0 (I^2C)
- High Definition Audio Controller
- Integrated Clock controller
- Intruder detect

Currently only the QM67 version of the 6 Series chipset is supported.

5.3 Memory

5.3.1 SDRAM

The SBC624 provides four banks of DDR3 SDRAM with ECC. Two banks are connected to each of the memory controllers within the Core i7 processor. The following table shows supported RAM configurations:

Table 5-2 Supported RAM Configurations

Total RAM (GBytes)	Total Number of Devices	Device Density (Gbit)	Number of Ranks per Controller
4	36	1	2
8	36	2	2
16	36	4	2

Interface speeds of 1066 megatransfers/second (PC3-8500) and 1333 megatransfers/second (PC3-10600) are supported.

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5.3.2 Boot Flash

The SBC624 has three 4 MByte SPI Flash devices fitted: for Management Engine (ME), BIOS and BIT code storage.

One device acts as the main ME/BIOS ROM device, and the processor boots from this device by default. The second device acts as a recovery ROM and the processor boots from this device when the Recovery Boot Link (E100) is fitted. The SBC624 also has the facility for the hardware to auto-swap the boot location to the Recovery area if corruption of the Main area is detected. If this auto-swap occurs, it is shown in the Board Configuration Register 1 (register offset 0x602).

The third device holds BIT code, and is visible when the SBC624 is booting from either Main or Recovery Flash devices.

5.3.3 Flash Hard Drives

Two SATA ports from the PCH (port 2 and port 3) are each connected to a Silicon Motion SM631 series SATA Solid State Drive (SSD). This device integrates a Single Level Cell (SLC) NAND array and a controller with a SATA Gen2 interface. The controller uses ECC and wear leveling to provide a robust storage area. Two LEDs per SSD device show link and activity status. See the LEDs section.



LINK

For more details on the SSD, see http://www.siliconmotion.com.

Overall drive capacity is dictated by available technology. Currently, the SBC624 can support up to 32 GBytes of NAND memory (two 16 GByte SSDs).

Hardware write protection is implemented by bits in the EEPROM DIP switch, which is controlled by a BIOS setup screen. The write protection status, along with the SSD presence, is shown in the Board Configuration Register 3 (register offset 0x604) for SATA port 2 and the Board Configuration Register 6 (register offset 0x60A) for SATA port 3. There is also a Fast Erase facility, initiated via Control Register 5 (register offset 0x626).

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5.3.4 NVRAM

Two 512 KByte Everspin MR2A08 MRAM devices provide memory mapped non-volatile memory on the SBC624. One device is allocated as user space; this device is write-protected by the NVRAM Write Enable Link (E101) and the backplane NVMRO signal (on the P0 connector pin A4).

The second device is allocated for system use only, and is permanently write-enabled. This provides system-level software such as BIT and BCS with an area of non-volatile memory that is always available.

Access to the devices is through 32-byte pages mapped into into I/O space (0x660 to 0x67F for User NVRAM and 0x680 to 0x69F for System NVRAM). The addresses of the pages within the devices are set by the appropriate NVRAM page register at 0x62E to 0x631.

The devices have unlimited read/write endurance and stated data retention is greater than 20 years.



LINK

For more details on the MRAM, see http://www.everspin.com.

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5.4 VPX Interface

The interface to the VPX backplane is compatible with the following specifications:

- VITA46.0
- VITA46.4 (for PCI Express I/O on the P2 connector)
- VITA46.9 (for PMC/XMC rear I/O mapping)
- VITA65

5.4.1 OpenVPX Compatibility

The SBC624 is compatible with the following module profiles, as defined by the VITA65 OpenVPX Specification:

- MOD6-PAY-4F1Q2U2T-12.2.1-8

5.4.2 REF_CLK

The VPX REF_CLK signal, on the P0 connector pins E8 and F8, is bused between all boards in the backplane. It is driven with a 25 MHz differential output when the SBC624 is configured as the System Controller. This can be subsequently altered by software using Control Register 4 (register offset 0x625).

The REF_CLK input can also be used to clock the timers present in the FPGA. See the Timer Registers section for more details.

5.4.3 AUX_CLK

OpenVPX also supports a bussed AUX_CLK signal on the VPX RES_BUS+/- pins (P0 pins B8 and C8). This is intended to support a 1 pulse-per-second periodic reference timing pulse, but could be used for any other system timing function as required. The AUX_CLK input can also be used to clock the timers in the FPGA. See the Timer Registers section for more details.

The SBC624 can also drive the AUX_CLK signal to test the functionality of the timer or to implement the timing function, under software control, via Control Register 4 (register offset 0x625).

5.4.4 Module Maskable Reset

OpenVPX supports a second reset input from the backplane (P1 pin G15), which may be masked under software control.

The SBC624 is hard reset when the Maskable Reset backplane signal is asserted for more than 10 µS, unless the mask bit in Control Register 4 (register offset 0x625) is set by software. The reset is not masked by default.

The SBC624 is also able to drive the Maskable Reset under software control, for example to reset a subset of other boards in the system, by setting a bit in Control Register 4 (register offset 0x625).

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5.4.5 Global Discrete

OpenVPX supports a single open-drain GPIO signal, GDiscrete1 (P1 pin G1), which is bused to all module slots in the backplane. Its function is not defined by the specification, but it could be used to provide a common control or status function to all boards in the system.

The SBC624 provides a register to drive the GDiscrete1 pin under software control, to read its status and to generate an interrupt (with programmable polarity and edge/level selection). See the GDiscrete1 Control and Status Register (register offset 0x627) for more information.

5.5 I/O

5.5.1 Data Plane Fabric

In accordance with the Open VPX Specification, the P1connector is allocated for the data plane connection and complies with Open VPX module profile MOD6-PAY-4F1Q2U2T-12.2.1-8. The data plane supports two fat pipe (x4) fabric connections.

The supported fabric types on the SBC624 are 10GBaseKX4 and Infiniband (dual data rate). The required type is software-selectable in the Mellanox ConnectX-2 Adapter device, which provides the interface to all data plane fabrics. This device is completely software configurable, and allows mixed connections (i.e. one pipe Infiniband and one pipe 10G Ethernet), giving a very flexible data plane interface. The adapter also supports a Remote DMA (RDMA) protocol, allowing a high degree of processor off-loading.

Table 5-3 Data Plane Pin Mapping

Signal (10GBaseKX4)	Signal (Infiniband)	Pipe 0 P1 Pin	Pipe1 P1 Pin	Signal (10GBaseKX4)	Signal (Infiniband)	Pipe 0 P1 Pin	Pipe1 P1 Pin
10Gx_RP0	IBx_RP0	A1	A5	10Gx_TP0	IBx_TP0	D1	D5
10Gx_RN0	IBx_RN0	B1	B5	10Gx_TN0	IBx_TN0	E1	E5
10Gx_RP1	IBx_RP1	B2	B6	10Gx_TP1	IBx_TP1	E2	E6
10Gx_RN1	IBx_RN1	C2	C6	10Gx_TN1	IBx_TN1	F2	F6
10Gx_RP2	IBx_RP2	A3	A7	10Gx_TP2	IBx_TP2	D3	D7
10Gx_RN2	IBx_RN2	B3	B7	10Gx_TN2	IBx_TN2	E3	E7
10Gx_RP3	IBx_RP3	B4	B8	10Gx_TP3	IBx_TP3	E4	E8
10Gx_RN3	IBx_RN3	C4	C8	10Gx_TN3	IBx_TN3	F4	F8

x = 0 for pipe 0 or 1 for pipe 1.

Associated LEDs show physical and logical links for each port. See the LEDs section.

LINK

For more details on the Mellanox device, see http://www.mellanox.com.

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5.5.2 Expansion Plane Fabric

The SBC624 provides 16 lanes of PCI Express to the P2 connector. These lanes are Gen2-capable, operating at either 2.5 or 5 Gbps, and may be configured as follows:

- One x16 port
- Two x8 ports
- Four x4 ports

Any one port can be configured as non-transparent (NT), for connecting to other intelligent hosts, to provide address translation and mailboxes. The configuration of these ports can be altered by writing to the PCIe Switch configuration EEPROM under software control, either by the user via a BIOS setup screen or by the Operating System.

The SBC624 has the capability to drive 100 MHz PCIe REFCLK signals on the OpenVPX defined signals EPCLOCK1 and EPCLOCK2. This capability is not enabled by default; contact Technical Support if it is required.

All lanes are provided by a PCIe switch. See below for more details.



NOTE

When connecting PCIe fabrics through fabric RTMs and cables such as those provided for use with the Abaco OpenVPX starter chassis (SCVPX6U and SCVPX3U), 5 GHz operation may be possible but *cannot be guaranteed*. To set up a reliable link when using the development RTMs and cables, users may need to set the processor card's PCIe signaling speeds to 2.5 GHz, at least initially. This can be achieved by forcing the links to GEN1 mode using the PLX set-up menu in the BIOS setup Utility (see section 4.11.3)

5.5.3 Control Plane Fabric/Gigabit Ethernet

The SBC624 supports a total of four Gigabit Ethernet channels, which collectively make up the control plane interface. Two channels are configured as 10/100/1000BaseT Ethernet with on-board magnetics, and are connected to the VPX P4 connector as follows:

Table 5-4 ETH0/ETH1 Pin Mapping

Signal	P4 Pin	Signal	P4 Pin
ETH0_0P	A15	ETH1_0P	A13
ETH0_0N	B15	ETH1_0N	B13
ETH0_1P	D15	ETH1_1P	D13
ETH0_1N	E15	ETH1_1N	E13
ETH0_2P	B16	ETH1_2P	B14
ETH0_2N	C16	ETH1_2N	C14
ETH0_3P	E16	ETH1_3P	E14
ETH0_3N	F16	ETH1_3N	F14

ETH1 can be routed to the front panel J1 connector, allowing full Ethernet port connectivity without the need for an RTM. This is selected by a hardware link (E104). When routed to J1, COM1 is not available on P4.

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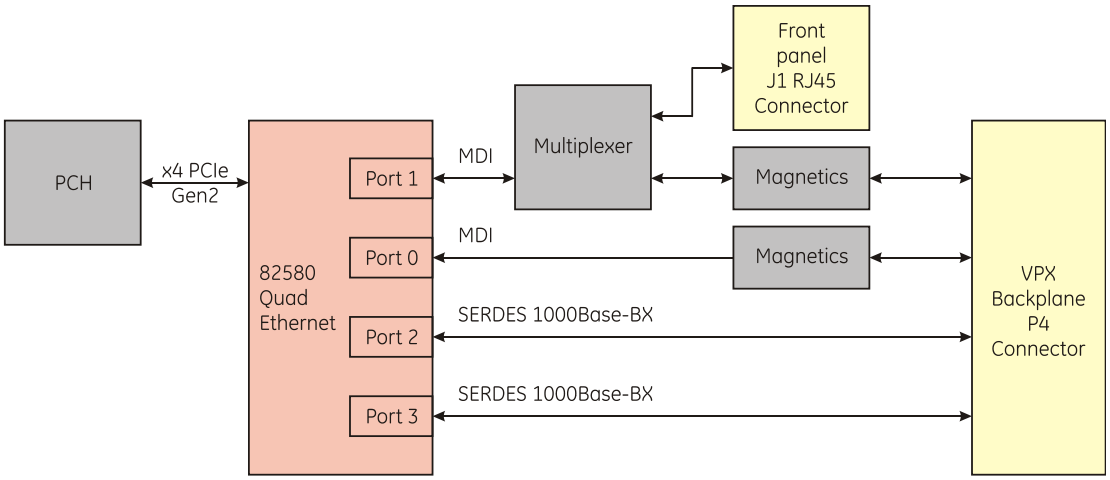
The other two channels are connected directly to the backplane as 10/100/1000BaseBX interfaces, and are connected to the VPX P4 connector, in accordance with Open VPX requirements for backplane Ethernet, as follows:

Table 5-5 ETH2/ETH3 Pin Mapping

Signal	P4 Pin	Signal	P4 Pin
ETH2_RP	B12	ETH3_RP	A11
ETH2_RN	C12	ETH3_RN	B11
ETH2_TP	E12	ETH3_TP	D11
ETH2_TN	F12	ETH3_TN	E11

The following diagram shows this configuration.

Figure 5-2 Ethernet Connectivity



An Intel 82580 Quad Ethernet controller provides all Gigabit Ethernet channels. This device consists of four independent MACs and PHYs integrated into one package. The device interfaces to the PCH using a x4 Gen2 PCIe link. A configuration EEPROM is connected to the 82580. This contains register settings loaded by the device on power-up or reset.

The 82580 device supports loopback modes on all MAC/PHYs allowing packets to be looped back at either the MAC level, SERDES level, internal PHY level or external level. These modes are enabled under software control allowing test software to carry out device testing. The network (MAC) addresses of the Ethernet ports are factory configured and may be displayed by software.

The 82580 device connects directly to LEDs on the rear of the board, which indicate link status and activity.

LINK

For more details on the 82580, see http://www.intel.com.

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5.5.4 PCI Express Switch

A PEX8748 or PEX8749 48-lane PCIe switch connects the x16 PCIe link from the processor to the backplane (P2 expansion plane), XMC/PMC1 and the Mellanox ConnectX-2 10GE/Infiniband bridge.

LINK

For more details on the PEX8748 and PEX8749 devices, see http://www.plxtech.com.

The PEX8749 PCIe switch contains DMA engines which can be used by software to increase inter-board performance when using the expansion plane to connect to other processor boards in a multi-peer PCIe system.

A serial EEPROM is connected to the switch to allow the initial configuration to be programmed by software. Write protection of this EEPROM is controlled by a BIOS setup option, which is interlocked with the Configuration EEPROM Write Enable Link (E102) and NVMRO (i.e. the link must be fitted, and NVMRO must be low before the write protection status can be changed by the BIOS setup option).

CAUTION

If third party tools such as those provided by PLX are being used to program the EEPROM, take extreme care to ensure that erroneous values are not programmed into the EEPROM, as this could prevent the board from booting.

NOTE

If third party tools are being used to program the EEPROM, it must first be write-enabled by the BIOS setup option.

Link status LEDs on the rear of the board are also connected to the switch.

The switch is configured as follows:

Table 5-6 PCIe Switch Port Configuration

Connection	Width	Port Number	Station Number	comments
CPU	x16	0	0	Upstream port
ConnectX-2	x8	8	1	
XMC1/PMC1	x8/x4	9	1	x8 when XMC fitted, x4 when PMC fitted (controlled by strapping)
Backplane link 0	x4	16	2	Can be aggregated into two x8 or one x16
Backplane link 1	x4	17	2	
Backplane link 2	x4	18	2	
Backplane link 3	x4	19	2	

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5.5.5 USB

The PCH provides seven USB 2.0 ports using two independent ECHI controllers. Six ports are available on VPX P4 and P6 connectors, and one port is available on the front-panel J2 connector.

National Semiconductor LM3526 devices are used to switch power to the USB ports. This device provides power switching, over current protection (OCP), thermal protection and supply fault flag for each port. Output current threshold is limited to 1.2 A typical and 1 mS fault flag delay.

NOTE

The PCH does not support OCP for each port independently, and OCP inputs are shared across ports.

LINK

For more details see http://www.national.com/mpf/LM/LM3526.html.

For each USB port, the following table shows where it is connected, which EHCI controller provides it, and which OCP input it uses:

Table 5-7 USB Signal Availability

Port	PCH EHCI Controller	OCP Input	USBx_P	USBx_N	USBx_POWER
0	1	0	P4/A9	P4/B9	P4/B10
1	1	0	P4/D9	P4/E9	P4/C10
2	1	1	P6/B7	P6/A7	P6/B8
3	1	1	P6/B9	P6/A9	P6/B10
9	2	4	J2/3	J2/2	J2/1
10	2	5	P6/D9	P6/E9	P6/B12
11	2	5	P6/B13	P6/A13	P6/B14

5.5.6 Serial Ports

The SMSC SCH3116 SuperIO device provides a total of four RS232/RS422/RS485 COM ports, of which three are available to the user. The following table summarizes the COM port connections:

Table 5-8 COM Port Connections

COM Port	Routing	RS232 Signal Set	RS422/RS485 Signal Set
COM1	P3 (default) or front panel	When routed to backplane: 8-wire (TXD, RXD, RTS, CTS, DCD, RI, DTR, DSR) When routed to front panel: 7-wire (TXD, RXD, RTS, CTS, DCD, DTR, DSR)	4-wire (TXD_A, TXD_B, RXD_A, RXD_B)
COM2	Permanent connection to P4	8-wire (TXD, RXD, RTS, CTS, DCD, RI, DTR, DSR)	4-wire (TXD_A, TXD_B, RXD_A, RXD_B)
COM3	Front panel J3 connector (when COM1 not routed instead)	7-wire (TXD, RXD, RTS, CTS, DCD, DTR, DSR)	4-wire (TXD_A, TXD_B, RXD_A, RXD_B)
COM4	Permanent connection to BMC as an additional interface to the LPC	4-wire (TXD, RXD, CTS, RTS) TTL level	N/A

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The following table shows the COM1 and COM2 routing to the P3 and P4 VPX backplane connectors:

Table 5-9 COM1/COM2 Signal Availability

RS232 Signal	RS422/485 Signal	P3 Pin	RS232 Signal	RS422/485 Signal	P4 Pin
COM1_RXD	COM1_RXD_A	G1	COM2_RXD	COM2_RXD_A	G1
COM1_TXD	COM1_TXD_A	G3	COM2_TXD	COM2_TXD_A	G3
COM1_CTS	COM1_RXD_B	G5	COM2_CTS	COM2_RXD_B	G5
COM1_RTS	COM1_TXD_B	G7	COM2_RTS	COM2_TXD_B	G7
COM1_DSR		G9	COM1_DSR		G9
COM1_DCD		G11	COM1_DCD		G11
COM1_RI		G13	COM1_RI		G13
COM1_DTR		G15	COM1_DTR		G15

As COM1 is the default active debug port for some operating systems, it can be routed to the front panel J3 connector on build level 1 to 3 boards, allowing full serial port connectivity without the need for an RTM. This is selected by fitting a hardware link (E103) or by selecting the relevant option in the BIOS setup screen (see section 4.11.2). When routed to J3, COM1 is not available on P3 and COM3 is not available at all.

COM ports 1 to 3 are connected using Intersil ISL 41334 transceiver devices, which provide 15 kVolts ESD protection. The transceiver mode of operation (i.e. RS423/RS422 selection, loopback mode, on/off mode) is set by Control Register 2 (register offset 0x621) for the backplane ports and Control Register 5 (register offset 0x626) for the front panel port. These registers can be configured in the BIOS, by selecting the relevant option in the BIOS setup screen (see section 4.11.2).



NOTE

When operating in RS422 mode, application software must set the RTS signal high, by writing to the appropriate SIO register, to enable the differential transmitters.



LINKS

For more details on the SuperIO device, see http://www.smsc.com.

For more details on the transceiver device, see http://www.intersil.com.

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5.5.7 SATA

The SBC624 provides five SATA interfaces. Three are routed to the VPX P6 connector for connection to off-board peripherals such as hard disk drives or CD/DVD drives and the other two ports are connected directly to the on-board SSD devices.

The SATA function in the PCH has three modes of operation to support different operating system conditions. For Native IDE enabled operating systems, the PCH uses two controllers to enable all of the ports. For AHCI or RAID mode, only one controller (controller 1) is used for all ports.

The following table summarizes each port connection, controller assignment and bandwidth capability:

Table 5-10 SATA Signal Availability

PCH Port Number	IDE Mode Controller Number/ Primary/Secondary Master/Slave	Maximum Bandwidth (Gb/s)[a]	SATAx_TXP	SATAx_TXN	SATAx_RXP	SATAx_RXN
0	1/primary master	6	P6/A11	P6/B11	P6/E11	P6/D11
1	1/secondary master	6	P6/D13	P6/E13	P6/B15	P6/A15
2	1/primary slave	3	On-board SSD1			
3	1/secondary slave	3	On-board SSD2			
4	2/primary master	3	P6/B16	P6/C16	P6/D15	P6/E15

a. 6 Gbps = Gen3/Gen2/Gen1; 3Gbps = Gen2/Gen1 only.

A single LED (DS28) on the rear of the PWB shows activity on any of the SATA ports.

5.5.8 GPIO

The SBC624 provides 8 lines of General Purpose I/O, each with interrupt generation capabilities, through the P4 and P6 connectors, as shown below:

Table 5-11 GPIO Line Signal Availability

GPIO Line	Pin
0	P6/C8
1	P6/C10
2	P6/C12
3	P6/C14
4	P4/F8
5	P4/F10
6	P4/E8
7	P4/E10

These are 3.3 V single-ended signals with 5 V tolerance. These signals are controlled by the FPGA and can be configured as inputs, with the ability to generate level- or edge-triggered interrupts, or outputs, with totem-pole or open-drain drivers. See section 6.29 for more details.

The GPIO signals are intended only to be used by Abaco software drivers. See the relevant software manual for details.

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5.5.9 Video

The SBC624 provides one VGA and up to two DVI video ports to the VPX backplane P6 connector. The DVI port is also available at the J4 mini HDMI connector on the front panel. The following table summarizes the video port connections:

Table 5-12 Video Port Summary

PCH Display Port	Build Option	XMC2 I/O	Video Protocol	Destination	Connection Method
A	Permanent	-	VGA	P6	DE15 connector on RTM
B	Permanent	-	HDMI/DVI	P6	DVI-I connector on RTM
C	Front video	Available	HDMI/DVI	J4	Mini HMDI connector on front panel
C	Rear video	Not available	HDMI/DVI	P6	DVI-I connector on MEZZIO, on RTM

The second backplane DVI channel shares pins with XMC2 I/O signals (P4) and is only available as a build option.

Table 5-13 VGA Signal Availability

VGA Signal	P6 Pin
DDC_CLK	G3
DDC_DATA	G5
VSYNC	G7
HSYNC	G9
RED	G11
GREEN	G13
BLUE	G15

Table 5-14 DVI Signal Availability

DVI Signal	P6 Pin (Port B)	J4 Pin (Port C)	P6 Pin (Port C)
DDC_CLK	E7	15	A1
DDC_DATA	D7	16	B2
TX0_N	E8	9	E5
TX0_P	F8	8	D5
TX1_N	E10	6	F6
TX1_P	F10	5	E6
TX2_N	E12	3	B5
TX2_P	F12	2	A5
TXC_N	E14	12	C6
TXC_P	F14	11	B6
HPD	E16	-	C2

The graphics controller is integrated into the Core i7 processor, and the video signals are driven by the PCH. Video data from the graphics controller is sent to the PCH via the Intel Flexible Display Interface (FDI). Filtering and ESD protection is provided on the VGA signals. Active HDMI level shifters, which also provide ESD protection, are used on all digital ports.

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5.5.10 High Definition Audio

The PCH contains a High Definition Audio (HDA) controller that communicates with an external codec. The controller consists of a set of DMA engines that can move data between the PCH and the codec.

The HDA interface signals are connected directly to the backplane P5 connector, for connection to an external hardware codec, as follows:

Table 5-15 HDA Signal Availability

HDA Signal	P5 Pin
SDO	G1
RSTN	G3
BCLK	G5
SYNC	G7
SDIN0	G9
SPKR	G11

5.5.11 PS/2 Keyboard and Mouse

The SMSC SCH3116 Super I/O device also provides a PS/2 keyboard and mouse interface. This is connected to the backplane P4 connector, as follows:

Table 5-16 Keyboard and Mouse Signal Availability

PS/2 Signal	P4 Pin
KBCLK	A7
KBDAT	B7
MSCLK	D7
MSDAT	E7



NOTE

PS/2 signals are only available on board artwork revisions 3 and above.

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5.6 LPC Bus

The PCH is the master of an LPC bus, which is connected to the devices below.

5.6.1 FPGA

A Lattice MACH-XO provides various functions. See section 5.15 for more details.

5.6.2 Trusted Platform Monitor

The SBC624 includes a Trusted Platform Monitor (TPM) device as a means to generate and store security key generation. The device includes internal EEPROM for key storage. The device is compliant with Trusted Computing Group (TCG) PC Client Specific TPM Interface Specification version 1.2 and can generate 2048-bit RSA keys in 500ms.

5.6.3 Baseboard Management Controller

A BMC implements the VPX system management function in accordance with VITA 46.11. See Section 5.9.7 for more details.

5.6.4 Super I/O Device

An SMSC SCH3116 device provides the following legacy I/O and monitoring functions:

- Four UART ports (two to the backplane, one to the front panel, one to BMC)
- Thermal monitoring functions
- Keyboard/Mouse interface

5.6.5 Test Access Card Connector

The SBC624 supports the addition of a TAC to the board. See section A.9 for more details.

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5.7 Mezzanines

The SBC624 has two mezzanine sites that both support suitably compliant PMCs or XMCs (including support for front-panel I/O). The two mezzanine sites are spaced to allow fitting of a double-width PMC/XMC if required.

5.7.1 PMCs

Each PMC site has Jn1, Jn2, Jn3 and Jn4 connectors to provide a 64-bit PCI bus capable of PCI-X operation at frequencies of up to 133 MHz. The interface is also 5 V-tolerant and supports the use of 5 V PMCs at 33 MHz signaling rate only.



CAUTION

Ensure that the PMC1 and PMC2 VIO Selection Links (E106 and E107) are set according to the requirements of any corresponding PMC(s) fitted. Damage to the PMC may otherwise result.

Each PCI bus is connected to a Pericom PI7C9X130 PCI-Express to PCI Bridge, which provides clocks and arbitration for the bus. The speed of the bus is based on the capability of the PMC, and is determined by the bridge during reset. The current operating frequency of each bus may be ascertained by reading registers within the appropriate bridge.



LINK

For more details on the Pericom device, see http://www.pericom.com/products/pci/PI7C9X130/.

A multiplexer routes four lanes to the PMC bridge if the PMC_PRESENT ~ signal is pulled low at reset by a fitted PMC. Otherwise, the four lanes are routed to the XMC site.

The PMC site supports Processor PMCs (as defined by VITA32-2002) operating in non-Monarch mode only. This includes support for PMCs with two PCI masters.

Each PMC site has a dedicated PCI bus, so fitting a PMC that runs at a lower frequency does not limit the other PMC or the performance of other functions of the SBC624.

The presence of a PMC in a site is shown in the Board Configuration Register 4 (register offset 0x608).

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5.7.2 XMCs

Each site provides Jn5 and Jn6 connectors. For XMC1, J15 provides a x8 PCI Express link to the PCI Express Switch. For XMC2, J25 provides a x4 PCI Express link to the PCH. For both sites, Jn6 is used to route XMC I/O to the backplane, depending on build options (see the I/O Routing section below).

A board configuration option allows XMC power to be provided from either the 12 V (VS1 and VS2) or 5 V (VS3) backplane supplies, as the VITA 42.0 specification supports both possibilities. The Board Configuration Register 5 (offset 0x609) shows the selected configuration.

The System Management pins of the XMC sites are connected to a dedicated I^2C interface on the BMC. The geographic address of XMC site 1 is configured to 000_b and XMC site 2 is configured to 001_b.

The presence of an XMC in a site is shown in the Board Configuration Register 4 (register offset 0x608).

5.7.3 I/O Routing

Rear I/O tracking is provided from the Jn4 and Jn6 connectors of both PMC/XMC sites to the rear VPX connectors in accordance with VITA 46.9.

The I/O from mezzanine site 1 is routed to the P3 connector and P4 connector, and is available in the following configurations:

Erratum October 2013
Corrected PMC/XMC I/O routing as per VITA 46.9

- Full PMC I/O from J14 and 12 differential pairs of XMC I/O from J16 (P3w1-P64s+X12d)
- Full XMC I/O (20 differential pairs and 38 single-ended) from J16 (P3w3-X38s+X8d+X12d)

Resistor packs are used to select the required configuration as build options. The option selected is shown in the Board Configuration Register 5 (offset 0x609).

The I/O from mezzanine site 2 is routed to the P5 connector and P6 connector, and is available in the following configurations:

Erratum October 2013
Corrected PMC/XMC I/O routing as per VITA 46.9

- Full PMC I/O from J24 and 12 differential pairs of XMC I/O from J26 (P5w1-P64s+X12d)
- Full PMC I/O from J24 only (P5w1-P64s)

When configured for PMC I/O only (to allow backplane pins to be used for an additional video port), connector J26 is not fitted. The selected build option is shown in Board Configuration Register 5 (offset 0x609).

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Table 5-17 PMC/XMC Site 1 Signal Availability

P64s+X12d Option						X38s+X8d+X12d Option					
PMC I/O	P3 Pin	PMC I/O	P3 Pin	XMC I/O	P4 Pin	XMC I/O	P3 Pin	XMC I/O	P3 Pin	XMC I/O	P4 Pin
J14_IO_1	E1	J14_IO_33	E9	J16_IO_A05	E1	J16_IO_C01	B3	J16_IO_C15	E10	J16_IO_A05	E1
J14_IO_2	B1	J14_IO_34	B9	J16_IO_B05	D1	J16_IO_F01	A3	J16_IO_F14	C10	J16_IO_B05	D1
J14_IO_3	D1	J14_IO_35	D9	J16_IO_D05	B1	J16_IO_C02	F4	J16_IO_F15	B10	J16_IO_D05	B1
J14_IO_4	A1	J14_IO_36	A9	J16_IO_E05	A1	J16_IO_C03	E4	J16_IO_C16	E11	J16_IO_E05	A1
J14_IO_5	F2	J14_IO_37	F10	J16_IO_A07	F2	J16_IO_F02	C4	J16_IO_C17	D11	J16_IO_A07	F2
J14_IO_6	C2	J14_IO_38	C10	J16_IO_B07	E2	J16_IO_F03	B4	J16_IO_F16	B11	J16_IO_B07	E2
J14_IO_7	E2	J14_IO_39	E10	J16_IO_D07	C2	J16_IO_C04	E5	J16_IO_F17	A11	J16_IO_D07	C2
J14_IO_8	B2	J14_IO_40	B10	J16_IO_E07	B2	J16_IO_C05	D5	J16_IO_C18	F12	J16_IO_E07	B2
J14_IO_9	E3	J14_IO_41	E11	J16_IO_A09	E3	J16_IO_F04	B5	J16_IO_C19	E12	J16_IO_A09	E3
J14_IO_10	B3	J14_IO_42	B11	J16_IO_B09	D3	J16_IO_F05	A5	J16_IO_F18	C12	J16_IO_B09	D3
J14_IO_11	D3	J14_IO_43	D11	J16_IO_D09	B3	J16_IO_C06	F6	J16_IO_F19	B12	J16_IO_D09	B3
J14_IO_12	A3	J14_IO_44	A11	J16_IO_E09	A3	J16_IO_C07	E6	J16_IO_A01	E13	J16_IO_E09	A3
J14_IO_13	F4	J14_IO_45	F12	J16_IO_A15	F4	J16_IO_F06	C6	J16_IO_B01	D13	J16_IO_A15	F4
J14_IO_14	C4	J14_IO_46	C12	J16_IO_B15	E4	J16_IO_F07	B6	J16_IO_D01	B13	J16_IO_B15	E4
J14_IO_15	E4	J14_IO_47	E12	J16_IO_D15	C4	J16_IO_C08	E7	J16_IO_E01	A13	J16_IO_D15	C4
J14_IO_16	B4	J14_IO_48	B12	J16_IO_E15	B4	J16_IO_C09	D7	J16_IO_A03	F14	J16_IO_E15	B4
J14_IO_17	E5	J14_IO_49	E13	J16_IO_A17	E5	J16_IO_F08	B7	J16_IO_B03	E14	J16_IO_A17	E5
J14_IO_18	B5	J14_IO_50	B13	J16_IO_B17	D5	J16_IO_F09	A7	J16_IO_D03	C14	J16_IO_B17	D5
J14_IO_19	D5	J14_IO_51	D13	J16_IO_D17	B5	J16_IO_C10	F8	J16_IO_E03	B14	J16_IO_D17	B5
J14_IO_20	A5	J14_IO_52	A13	J16_IO_E17	A5	J16_IO_C11	E8	J16_IO_A11	E15	J16_IO_E17	A5
J14_IO_21	F6	J14_IO_53	F14	J16_IO_A19	F6	J16_IO_F10	C8	J16_IO_B11	D15	J16_IO_A19	F6
J14_IO_22	C6	J14_IO_54	C14	J16_IO_B19	E6	J16_IO_F11	B8	J16_IO_D11	B15	J16_IO_B19	E6
J14_IO_23	E6	J14_IO_55	E14	J16_IO_D19	C6	J16_IO_C12	E9	J16_IO_E11	A15	J16_IO_D19	C6
J14_IO_24	B6	J14_IO_56	B14	J16_IO_E19	B6	J16_IO_C13	D9	J16_IO_A13	F16	J16_IO_E19	B6
J14_IO_25	E7	J14_IO_57	E15			J16_IO_F12	B9	J16_IO_B13	E16		
J14_IO_26	B7	J14_IO_58	B15			J16_IO_F13	A9	J16_IO_D13	C16		
J14_IO_27	D7	J14_IO_59	D15			J16_IO_C14	F10	J16_IO_E13	B16		
J14_IO_28	A7	J14_IO_60	A15								
J14_IO_29	F8	J14_IO_61	F16								
J14_IO_30	C8	J14_IO_62	C16							= Differential pairs	
J14_IO_31	E8	J14_IO_63	E16								
J14_IO_32	B8	J14_IO_64	B16								

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Table 5-18 PMC/XMC Site 2 Signal Availability (Full PMC I/O)

PMC I/O	P5 Pin	PMC I/O	P5 Pin	XMC I/O	P6 Pin
J24_IO_1	E1	J24_IO_33	E9	J26_IO_A05	E1
J24_IO_2	B1	J24_IO_34	B9	J26_IO_B05	D1
J24_IO_3	D1	J24_IO_35	D9	J26_IO_D05	B1
J24_IO_4	A1	J24_IO_36	A9	J26_IO_E05	A1
J24_IO_5	F2	J24_IO_37	F10	J26_IO_A07	F2
J24_IO_6	C2	J24_IO_38	C10	J26_IO_B07	E2
J24_IO_7	E2	J24_IO_39	E10	J26_IO_D07	C2
J24_IO_8	B2	J24_IO_40	B10	J26_IO_E07	B2
J24_IO_9	E3	J24_IO_41	E11	J26_IO_A09	E3
J24_IO_10	B3	J24_IO_42	B11	J26_IO_B09	D3
J24_IO_11	D3	J24_IO_43	D11	J26_IO_D09	B3
J24_IO_12	A3	J24_IO_44	A11	J26_IO_E09	A3
J24_IO_13	F4	J24_IO_45	F12	J26_IO_A15	F4
J24_IO_14	C4	J24_IO_46	C12	J26_IO_B15	E4
J24_IO_15	E4	J24_IO_47	E12	J26_IO_D15	C4
J24_IO_16	B4	J24_IO_48	B12	J26_IO_E15	B4
J24_IO_17	E5	J24_IO_49	E13	J26_IO_A17	E5
J24_IO_18	B5	J24_IO_50	B13	J26_IO_B17	D5
J24_IO_19	D5	J24_IO_51	D13	J26_IO_D17	B5
J24_IO_20	A5	J24_IO_52	A13	J26_IO_E17	A5
J24_IO_21	F6	J24_IO_53	F14	J26_IO_A19	F6
J24_IO_22	C6	J24_IO_54	C14	J26_IO_B19	E6
J24_IO_23	E6	J24_IO_55	E14	J26_IO_D19	C6
J24_IO_24	B6	J24_IO_56	B14	J26_IO_E19	B6
J24_IO_25	E7	J24_IO_57	E15		
J24_IO_26	B7	J24_IO_58	B15		
J24_IO_27	D7	J24_IO_59	D15		
J24_IO_28	A7	J24_IO_60	A15		
J24_IO_29	F8	J24_IO_61	F16		
J24_IO_30	C8	J24_IO_62	C16		
J24_IO_31	E8	J24_IO_63	E16		
J24_IO_32	B8	J24_IO_64	B16		

= Differential pairs

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5.8 Real Time Clock

The PCH provides an RTC, powered from the P3V3_AUX or the VBAT supply. When either of these supplies is present, the system clock is maintained; if all power is removed, the RTC is reset. The RTC module comprises a clock with 1 second resolution, two banks of static RAM and the following interrupt features:

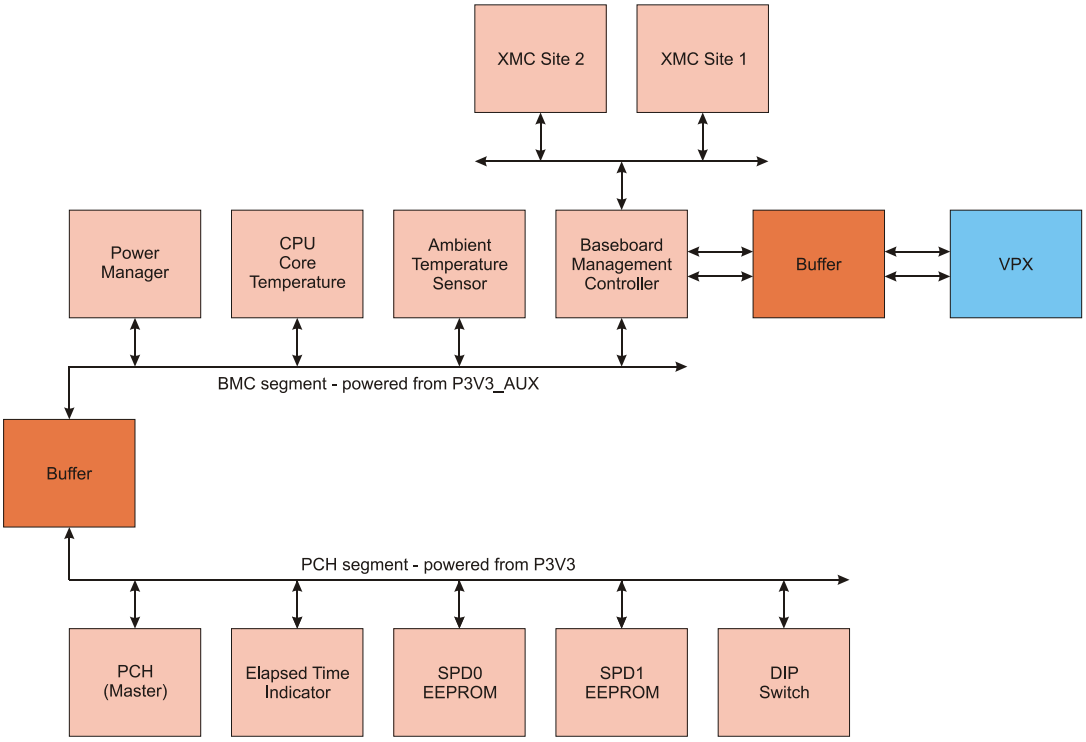
- Time of day alarm, with once a second to once a month range
- Periodic rate 122 µS to 500 mS
- End of update

The RTC function uses the first 14 bytes of the lower static RAM block, with the first 10 bytes being used for time and date information and the last 4 bytes being used to configure and report the RTC function. The leap year determination for adding a 29th day to February does not take into account the end-of-the-century exceptions.

5.9 I²C Bus

The PCH has a single I²C bus, supporting SMBus 2.0.
I²C devices on the board are connected to this bus as shown below:

Figure 5-3 I²C Bus Structure



The I²C bus is partitioned into two segments. The first (PCH segment) contains the SPD EEPROMs, DIP switch and ETI, which are devices available to software running on the host processor. The second (BMC segment) contains the power and temperature sensors and is intended only to be accessed by the BMC. If software on the host requires access to these sensors, it should request the data via the BMC.

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The two segments are separated by a PCA9511 I²C buffer, which is normally disabled. It may be enabled under software control when the functionality of the BMC is not used or for testing of the sensors. This buffer also provides isolation for those devices that are powered from the backplane P3V3_AUX power rail.

The table below summarizes the I²C slave addresses of the devices in the system. Where I²C addresses are quoted, the 8-bit address is the value that would be used to write to the device on the bus (i.e. the 7-bit device address and the LSB set to '0').

Table 5-19 I²C Bus Addresses

Device	Segment	7-bit Address	8-bit Write Address
PCH (Master)	PCH	Master only	Master only
PCA9560 DIP switch	PCH	0x4D	0x9A
SPD0 EEPROM (on-board)[a]	PCH	0x50 or 0x54	0xA0 or 0xA8
SPD1 EEPROM (on-board)[a]	PCH	0x52 or 0x56	0xA4 or 0xAC
SPD0 EEPROM (on TAC)[a]	PCH	0x54 or 0x50	0xA8 or 0xA0
SPD1 EEPROM (on TAC)[a]	PCH	0x56 or 0x52	0xAC or 0xA4
DS1682 ETI	PCH	0x6B	0xD6
ispPOWR-1220AT8 Power Manager	BMC	0x40	0x80
LM92 Board temperature sensor	BMC	0x48	0x90
ADT461 CPU core temperature	BMC	0x4C	0x98
BMC (Master)	BMC	Master only	Master only

a. The location of the enabled EEPROMs is shown in the Board Configuration Register 1 (register offset 0x602).

5.9.1 EEPROM DIP Switch

A PCA9560 device is used to configure the following aspects of board operation:

Table 5-20 DIP Switch Options

Output	Function
MUX_A	XMC1 Test Mode (factory use only, disabled by default)
MUX_B	Not used
MUX_C	SSD1 write protect 0 = Writes to SDD1 enabled (default) 1 = Writes to SDD1 disabled
MUX_D	SSD2 write protect 0 = Writes to SDD2 enabled (default) 1 = Writes to SDD2 disabled

NOTE

This device is write-enabled only when the Configuration EEPROM Write Enable Link (E102) is fitted and the backplane NVMRO signal (on P0 pin A4) is low.

The SSD write protection settings can be altered via a BIOS set-up screen, and are reflected in Board Configuration Register 3 (register offset 0x604) for SSD1 and Board Configuration Register 6 (register offset 0x60A) for SSD2.

LINK

For more details on the DIP switch and I²C buffer devices, see http://www.nxp.com.

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5.9.2 RAM SPD EEPROMs

Two SPD EEPROMs are fitted, one for each memory controller. The EEPROMs contain data regarding the configuration of the RAM. The format of this data conforms to the JEDEC standard.

5.9.3 Elapsed Time Indicator

A Dallas DS1682 Elapsed Time Indicator logs the amount of time the SBC624 has been powered and the number of power cycles.



LINK

For more details on the ETI device, see http://www.maxim-ic.com.

5.9.4 Power Manager/Monitor

The SBC624 uses a Lattice ispPOWR-1220AT8 programmable power manager to control all of the on-board power supplies to meet supply sequencing requirements.



LINK

For more details on the Power Manager device, see http://www.latticesemi.com.

In addition to controlling the on-board supplies, the power manager also monitors each rail, and its voltage can be read from registers internal to the device, across the I^2C interface.

The following table lists the software monitor points:

Table 5-21 Power Manager Monitor Input Connections

Input	Rail Monitored	Nominal Voltage
VMON1	P3V3	+3.3
VMON2	VCORE_PLX	0.9
VMON3	P1V2	+1.2
VMON4	P1V8	+1.8
VMON5	P1V5	+1.5
VMON6	VCCIO	1.05
VMON7	Not used	Not applicable
VMON8	VGFXCORE	1 (variable)
VMON9	VCCSA	0.85 (variable)
VMON10	P5V	+5
VMON11	P3V3_AUX	+3.3
VMON12	P12V	+12[a]

a. The VMON pins of the device can only tolerate a maximum of 6.0 V and so the 12 V input is divided by 3 using a resistor divider and needs to be multiplied by 3 again by software to give an actual input value.

The Power Manager drives a green Power Good LED (DS6) when all on-board power supplies are within tolerance. See the LEDs section.

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5.9.5 Board Temperature Sensor

An LM92 monitors the ambient temperature on the PCB. This device can only be accessed via the BMC using IPMI commands.



LINK

For more details on the LM92 device, see http://www.national.com.

5.9.6 CPU Core Temperature Sensor

An ADT7461 device monitors the on-die temperature of the CPU. This sensor is intended to allow off-board IPMI controllers to read the core temperature of the CPU. On-board software should determine the CPU temperature from dedicated registers within the CPU.



LINK

For more details on the ADT7461 device, see http://www.onsemi.com.

5.9.7 Baseboard Management Controller

The SBC624 contains a Renesas H8S/2168 microcontroller functioning as a Baseboard Management Controller (BMC) for implementation of the VPX System Management function in accordance with VITA 46.11.



LINK

For more details on the BMC device, see http://www.renesas.com.

The BMC is connected to the following interfaces:

- LPC interface
- RS232 interface (connected to COM4)
- Backplane System Management buses (on the P0 connector) via isolation buffers
- I²C bus (for access to sensor devices)
- I²C bus to XMC sites
- I²C bus to Ethernet controller, allowing IPMI packets to be received over Ethernet
- VPX geographic address
- Debug serial interface to backplane
- FRU (Field Replaceable Unit) ROM containing the board part number and serial number

The BMC can reset or power off the SBC624 in response to a System Management request and can assert an interrupt to the FPGA interrupt controller if it requires interaction with the host processor.

The BMC can control the state of the BIT Fail LED (DS4) to indicate BIT status.

The SBC624 can function with the BMC not fitted or unprogrammed.

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5.10 Timers

5.10.1 General Purpose Timers

The timer/counter block within the PCH contains three counters that are equivalent in function to those found in one 82C54 programmable interval timer. These three counters are combined to provide the system timer function and speaker tone. The 14.31818 MHz clock (derived internally within the PCH) provides the clock source for these three counters.

The FPGA provides two additional 32-bit counters. The source clock for these counters is software selectable (see the Timer Registers section) from the following sources:

- On-board 2 MHz clock (default)
- VPX REF_CLK
- VPX AUX_CLK
- On-board 25 MHz clock

5.10.2 Watchdog Timers

The FPGA provides one watchdog timer, capable of resetting the SBC624 on expiry. This has a timeout interval selectable from the following:

- 2 milliseconds
- 32 milliseconds
- 131 milliseconds
- 262 milliseconds
- 524 milliseconds
- 2.1 seconds
- 33 seconds
- 66 seconds

Following reset, the watchdog timer is initially disabled. It can be enabled in the Watchdog Timer Control/Status LSB Register (register offset 0x60E) and the timeout period selected in the Watchdog Timer Control/Status MSB Register (register offset 0x60F).

Once enabled, the watchdog must be serviced periodically via the Watchdog Timer Refresh Register (register offset 0x60D). If the timeout expires before the watchdog is serviced, then a hard reset is generated.

The watchdog timer can be disabled in the Watchdog Timer Control/Status LSB Register (register offset 0x60E).

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5.11 Power Sequencing

5.11.1 On-board Sequencing

The Lattice ispPAC Power Manager device (see section 5.9.4) sequences the power supplies in the required order for on-board devices. It also monitors the backplane supply voltages and shuts down the on-board supplies if these fall below their specified levels. It is connected to the I²C Bus, allowing software read-out of the voltages of all on and off-board supplies.

When the BMC asserts the BMC_POWER_OFF signal, the Power Manager will shut down all on-board supplies (except P3V3_AUX).

5.11.2 Inter-board Sequencing

The SBC624 supports a proprietary inter-board power sequencing mechanism. This allows for the sequencing of power between several boards in a system to be controlled (limiting overall inrush current), and is achieved via the PSU_SEQ_OUT and PSU_SEQ_IN signals on the P1 connector, which can be daisy-chained between boards.

The SBC624 drives the PSU_SEQ_OUT signal low when the backplane supplies are out of specification and holds it low until all on-board supplies are within specification. The PSU_SEQ_OUT signal is not driven low when the power is removed as a result of the BMC_POWER_OFF signal being asserted.

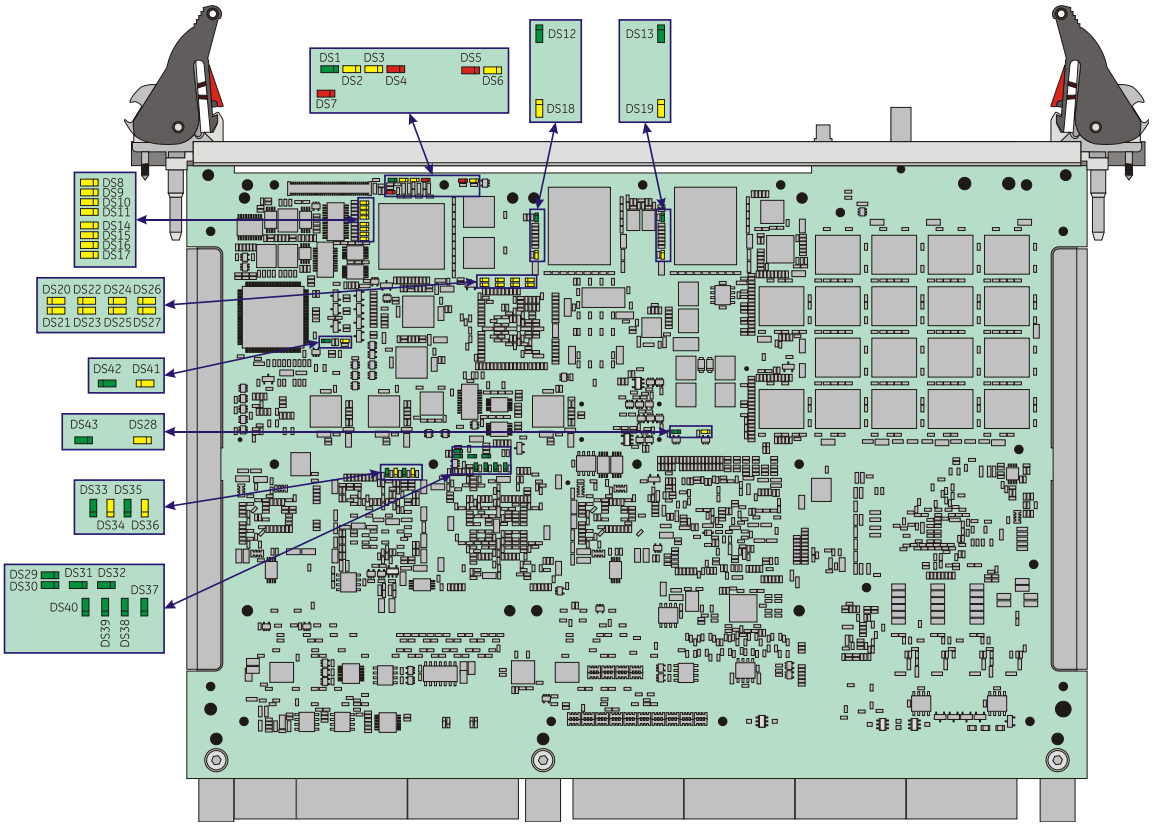
The SBC624 holds off all on-board supplies (except P3V3_AUX) while the PSU_SEQ_IN signal is held low. The power-on sequence is initiated if the PSU_SEQ_IN signal remains low 500 ms after the off-board supplies are within specification, which may occur if the previous board in the chain fails.

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5.12 LEDs

The SBC624 has several LEDs mounted on the rear of the card, as shown below.

Figure 5-4 Rear LED Positions



5.12.1 BIT LEDs (DS1 to DS4)

The SBC624 has four software-controlled LEDs, visible on the front panel, to reflect the status of BIT or other boot software. When used by BIT, the LEDs have the following meanings:

Table 5-22 BIT LED Meanings

LEDs	Color	Meaning When Lit
DS4	Red	BIT Fail
DS1	Green	BIT Pass
DS2	Yellow	BIT status 2 (see BIT documentation)
DS3	Yellow	BIT status 1 (see BIT documentation)

LINK

FBIT for SBC624 Software Reference Manual, publication number FBIT-SBC624-SRM.

The BIT Fail LED is controlled by the BMC. It is powered from the auxiliary power supply so that it can remain lit even when the main power supplies are not active or have failed.

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The two yellow and one green LEDs are unlit after reset and are driven by the FPGA under software control. See the Control Register 3 (register offset 0x622) for details.

When used by BIT, the red LED either shows that BIT has not yet run (straight after a reset) or has run but failed. The yellow LEDs show progress through BIT, and so may provide information for debugging purposes in the event of failure. The green LED shows that BIT has passed.

Table 5-23 BIT Status LED Meanings

BIT Fail LED (DS4)	BIT Passed LED (DS1)	Status
On	Off	BIT not yet run (Reset state) or BIT failed
Off	On	BIT complete and passed

The BITFAIL~ (P6 F16) backplane signal is driven active low using an open-drain driver when the red LED is lit.

5.12.2 Board Reset LED (DS5)

The main board reset signal drives this red LED to show that the SBC624 is in reset.

5.12.3 Board Power Good LED (DS6)

The Power Manager drives this green LED. When lit, it indicates that all on-board power supplies (including the processor supply) are within tolerance.

5.12.4 Processor Status LED (DS7)

This red LED illuminates when either the CPU Catastrophic error output is active (indicating that a non-recoverable error has occurred), or when the CPU Thermal trip output is active (indicating that the processor has shut down because the die temperature has exceeded approximately 130˚C).

5.12.5 POST Code LEDs (DS8 to DS11 and DS14 to DS17)

These yellow LEDs reflect the POST code returned by the BIOS.

5.12.6 SSD Link/Activity LEDs (DS12, DS13, DS18 and DS19)

There are two LEDs for each of the Solid State Disks (see section 5.3.3), as shown in the following table:

Table 5-24 SSD Link/Activity LED Meanings

LED	SSD Device	Color	Meaning When Lit	Meaning When Off
DS12	1	Green	SATA link is present	No link
DS18	1	Yellow	SSD activity	No activity
DS13	2	Green	SATA link is present	No link
DS19	2	Yellow	SSD activity	No activity

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5.12.7 Ethernet Link Status LEDs (DS20 to DS27)

Each Ethernet port has two yellow LEDs to show the link status and activity. The function of these LEDs is determined by the Ethernet controller's EEPROM settings, or can be overwritten by software.

Table 5-25 Board Ethernet LED Meanings

LED	Ethernet Channel	Type	Meaning When Lit	Meaning When Off	Meaning When Flashing
DS20	0	BaseT	Link is present	No link	Activity
DS21	0	BaseT	Speed = 1000 Mbps	Speed = 10/100 Mbps or no link	-
DS22	1	BaseT	Link is present	No link	Activity
DS23	1	BaseT	Speed = 1000 Mbps	Speed = 10/100 Mbps or no link	-
DS24	2	BaseBX	Link is present	No link	Activity
DS25	2	BaseBX	Speed = 1000 Mbps	Speed = 10/100 Mbps or no link	-
DS26	3	BaseBX	Link is present	No link	Activity
DS27	3	BaseBX	Speed = 1000 Mbps	Speed = 10/100 Mbps or no link	-

When port 1 is configured to connect to the front panel Ethernet connector, two LEDs integrated into the connector indicate the status of the link, as shown in the following table:

Table 5-26 Front Panel Ethernet LED Meanings

LED	Color	Meaning When Lit	Meaning When Off	Meaning When Flashing
LED2	Orange	Link is present	No link	Activity
LED1	Orange	Speed = 1000 Mbps	Speed = 10 Mbps or no link	-
	Green	Speed = 100 Mbps	Speed = 10 Mbps or no link	-

See Figure 5-6 for the location of these LEDs.

5.12.8 SATA Activity LED (DS28)

This yellow LED, when lit, shows that there is SATA activity on any port.

5.12.9 PCI Express Link Status LEDs (DS29 to DS32 & DS37 to DS40)

Green LEDs show the status of certain PCIe links connected to the PCIe switch. These LEDs are driven directly by the PCIe switch and when a valid link is present, they indicate the connected speed. The following links have status LEDs:

Table 5-27 PCIe Port Good LED Meanings

Device Link	Port	LED	Operation
CPU (x16 or x8)	0	DS29	Off = no link Flashing @ 1 Hz = Gen 1 link Flashing @ 2 Hz = Gen 2 link
CPU (second x8 link if present)[a]	1	DS30	
Mellanox ConnectX-2	8	DS32	
PMC PCI-X bridge or XMC	9	DS31	
Backplane PCIe port EP0[b]	16	DS37	
Backplane PCIe port EP1[b]	17	DS38	
Backplane PCIe port EP2[b]	18	DS39	
Backplane PCIe port EP3[b]	19	DS40	

a. Only lit in multi-host mode.
b. Not supported on all revisions of PCIe switch silicon.

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5.12.10 Data Plane Link Status LEDs (DS33 to DS36)

The Mellanox ConnectX-2 device drives two LEDs (one yellow, one green) for each fat pipe. The green LED indicates a physical link connection (i.e. PHYs connected). The yellow LED indicates a logical link connection (the port is linked from a software point of view).

Table 5-28 Data Plane Link Status LED Meanings

LEDs	Color	Meaning When Lit
DS33	Green	Port 1 physical link is present
DS34	Yellow	Port 1 logical link is present
DS35	Green	Port 2 physical link is present
DS36	Yellow	Port 2 logical link is present

5.12.11 Sleep Status LED (DS41)

This yellow LED illuminates when the platform is in one of the S3, S4 or S5 sleep states.

5.12.12 Backplane Power Good LED (DS42)

This green LED illuminates when all required backplane supplies (3.3V_AUX, VS1 and VS3) are on and within VPX specifications.

5.12.13 Core Supplies Power Good LED (DS43)

This green LED illumintes when all on-board supplies except the processor (i.e. all supplies that are controlled by the power manager) are on and within specification.

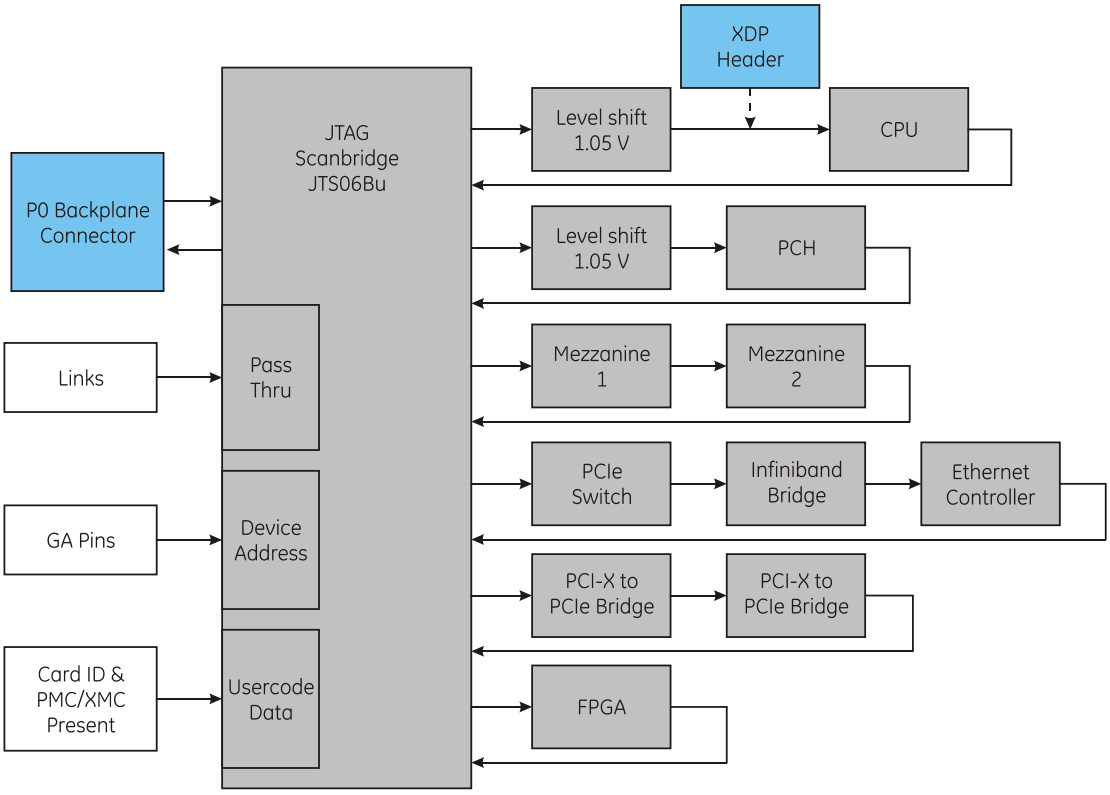
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5.13 JTAG

5.13.1 Boundary Scan

The SBC624 provides JTAG boundary scan facilities for all IEEE 1149.1 and IEEE 1149.6-compliant devices. A Firecron JTS06Bu Scanbridge device partitions the JTAG chain to aid debugging. The primary interface to the Scanbridge chain is from the standard pins on the backplane VPX P0 connector. The JTAG structure is shown below.

Figure 5-5 JTAG Chains



Mezzanine cards (XMCs and PMCs) are on their own JTAG chain and each site is automatically bypassed (using on-board buffers) when no mezzanine card is fitted.

The Scanbridge supports six Test Access Ports (TAPs) and can be enabled by fitting link E105. The Scanbridge can be set into pass-through mode, to aid initial test development and debug via hardware links on the TAC.

The backplane address of the JTAG Scanbridge is derived from the VPX geographic address. This is used when operating a bused JTAG system with multiple boards.

The SBC624 provides standard termination for JTAG chains, to drive the signals correctly in the event that the Scanbridge is disabled.

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The USR-STATUS_BYTE register in the Scanbridge (accessible through the primary TAP) has the following format:

Table 5-29 USR_STATUS_BYTE Register Format

7	6	5	4	3	2	1	0
		1	1	1	1	0	0
X/PMC2	X/PMC1				ID		

Bits 4 to 0 hold the Abaco card ID, which is 28 (0x1C).

Bits 7 to 5 are used to determine what mezzanine cards are fitted to the SBC624 as follows:
Bit 7 = Mezzanine 2 (0 when PMC or XMC fitted, 1 otherwise).
Bit 6 = Mezzanine 1 (0 when PMC or XMC fitted, 1 otherwise).
Bit 5 = Always 1.



LINK

For more details on the Scanbridge device, see http://www.firecron.com.

5.13.2 Processor Debug Header

The SBC624 provides a connector to access the debug port on the processor. The JTAG port is also connected to the Scanbridge to allow Boundary-scan testing.

The connector used is the Samtec 60-way BSH-030-01-L-D-A in accordance with Intel recommendations. This connector uses the Intel eXtended Debug Port (XDP) standard pin-out, allowing probes from various vendors to be used.

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5.14 Resets, Interrupts and Error Reporting

5.14.1 Interrupt Controllers

The PCH provides an ISA-compatible Programmable Interrupt Controller (PIC) that incorporates the functionality of two 82C59 interrupt controllers. These are cascaded so that 14 external and two internal interrupts are possible. In addition, the PCH supports a serial interrupt scheme.

The PCH also incorporates an Advanced Programmable Interrupt Controller (APIC).

5.14.2 Hard Reset

All resets on the SBC624 are derived from the PLATFORM_RESET~ signal generated by the PCH. The PCH generates PLATFORM_RESET~ when RESUME_RESET~ is asserted (power up reset) or when the SYSRESET~ input is asserted, or when POWER_GOOD is negated.

PLATFORM_RESET~ is generated when any of the following events occur, and will not be negated until the reset source is negated. This allows these reset sources to hold the SBC624 in its reset state:

- The VPX SYSRESET~ signal is asserted (when not System Controller)
- The MSKRST~ (maskable reset) signal (on the P1 connector pin G15) is asserted and the reset is unmasked in the Control Register 4 (register offset 0x625)
- The Watchdog timer expires

PLATFORM_RESET~ is generated when any of the following events occur, and is edge triggered only (i.e. PLATFORM_RESET~ is generated on an active going edge, and negates after 10 ms):

- Front panel RESET_SWITCH~ asserted
- BIT Reset Request (bit 7 of the BIT Control and Status Register [register offset 0x629] is set)
- BMC_RESET_OUT~ signal asserted
- RESET_OUT~ signal from any PMC/XMC asserted
- RTM_RST~ signal (on the P5 connector pin G13) is asserted

The duration of PLATFORM_RESET~ is a minimum of 10 ms.

When operating as the VPX System Controller, the SBC624 asserts the VPX SYSRESET~ signal when any reset source is asserted.

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5.14.3 External Interrupts

The FPGA provides the option to route the following internal and external interrupt sources as serial LPC interrupts:

- FPGA timer interrupts
- Backplane GDISC1~ input interrupt
- BMC interrupt
- GPIO interrupts

Interrupts can be independently masked/unmasked via registers in the FPGA. By default, all interrupt sources are masked.

5.14.4 Intruder Detect

The SBC624 has an intruder detect input (on the backplane P1 connector pin G13) that can be connected to a system level switch. When activated, the PCH can be programmed to generate a System Management Interrupt (SMI) or Total Cost of Ownership (TCO) interrupt.

5.15 FPGA

The FPGA is a Lattice LCMXO2280C device that provides the following facilities:

- Board Configuration, Control and Status registers (see Chapter 6)
- Watchdog timer
- GPIO controller (see the GPIO Registers section)
- General purpose timers (see the Timer Registers section)
- NVRAM interface
- Secondary interrupt controller
- Reset control
- Ancillary logic functions



LINK

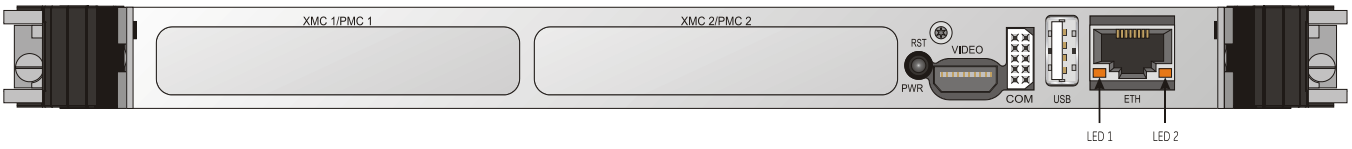
For more details on the FPGA device, see http://www.latticesemi.com.

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5.16 Front Panel

5.16.1 Air-cooled Versions (Build Levels 1 to 3)

Figure 5-6 Air-cooled Front Panel



PMC Slots

The SBC624 front panel has provision for front I/O from both PMC/XMC sites. If PMCs have not been ordered as part of an assembly with the SBC624, then Abaco will fit a blanking plate in the slot(s) for EMC protection.

If you are fitting a non-Abaco PMC, it must comply with the appropriate standard for air-cooled mezzanines to ensure that it mates correctly with the SBC624 mechanics. Abaco PMCs comply with this standard.

If you are fitting a PMC yourself, before fitting the module, remove the corresponding blanking plate from the desired PMC slot. The PMC's bezel should fill the slot and may provide front panel connection to the module. Abaco PMCs are delivered with a full kit of parts for mounting, plus fitting instructions.

LEDs

Two LEDs are visible on the front panel, indicating the link status of the front panel Ethernet link. See the LEDs section for more details.

Switch

A center-biased, 3-way, momentary action toggle switch is fitted through the front panel. This generates a hard reset to the processor when the switch is moved right and a power button signal to the PCH when the switch is moved left

Connectors

The following connections are provided on the front panel:

- 1 x USB (USB type A)
- 1 x Gigabit Ethernet (RJ45)
- 1 x RS232 – COM3 or COM1 (adapter cable available – contact the factory)
- 1 x mini HDMI connector (adapter cable available – contact the factory)

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5.16.2 Conduction-cooled Versions (Build Levels 4 and 5)

Figure 5-7 Conduction-cooled Front Panel



PMC Slots There is no access to front I/O from PMCs in a conduction-cooled environment.

If you are fitting a non-Abaco PMC, it must comply with the standard for rugged, conduction-cooled PMCs (VITA20-2001) to ensure that it mates correctly with the SBC624 mechanics. Abaco PMCs comply with this standard.

LEDs No LEDs are visible from the front.

Switch No reset switch is available on the front panel at these build levels, although the RTM_RST~ signal (P5 pin G13) or the MSKRST~ signal (P1 pin G15) could be used for this purpose.

Connectors No connectors are provided on the front panel at these build levels.

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6 • FPGA Registers

The FPGA provides the following Control and Status registers, which appear in the I/O memory map (for reading and writing) starting at address 0x600:

Table 6-1 Control/Status Registers

LPC I/O Port (Hex)	Description	Access	LPC I/O Port (Hex)	Description	Access
600	Board ID	Read Only	631	System NVRAM Page MSB	Read/Write
601	Board Revision	Read Only	632 to 634	Reserved	N/A
602	Board Configuration 1	Read Only	635	Reserved[a]	Read/Write
603	Board Configuration 2	Read Only	636 to 63F	Unallocated	N/A
604	Board Configuration 3	Read Only	640	GPIO Out	Read/Write
605	VPX Geographical Address	Read Only	641	GPIO In	Read Only
606	Alarm Status	Read Only	642	GPIO Direction	Read/Write
607	Link Status	Read Only	643	GPIO Interrupt Enable	Read/Write
608	Board Configuration 4	Read Only	644	GPIO Interrupt Level/Edge	Read/Write
609	Board Configuration 5	Read Only	645	GPIO Interrupt Low/High	Read/Write
60A	Board Configuration 6	Read Only	646	GPIO Both Edges	Read/Write
60B	FPGA Revision	Read Only	647	GPIO Interrupt Status	Read/Write to clear IRQ
60C	Unallocated	N/A	648 to 64D	AXIS Timestamp	Read Only
60D	Watchdog Timer Refresh	Write to clear	64E and 64F	Unallocated	N/A
60E	Watchdog Timer C&S (LSB)	Read/Write	650	Timer 0 Control and Status 1	
60F	Watchdog Timer C&S (MSB)	Read/Write	651	Timer 0 Control and Status 2	
610 to 615	Board ID String	Read Only	652	Timer 0 IRQ Clear	
616 to 61F	Unallocated	N/A	653	Reserved	N/A
620	Control 1	Read/Write	654	Timer 0 Data 0	
621	Control 2	Read/Write	655	Timer 0 Data 1	
622	Control 3	Read/Write	656	Timer 0 Data 2	
623	IRQ Enable 1	Read/Write	657	Timer 0 Data 3	
624	IRQ Enable 2	Read/Write	658	Timer 1 Control and Status 1	
625	Control 4	Read/Write	659	Timer 1 Control and Status 2	
626	Control 5	Read/Write	65A	Timer 1 IRQ Clear	
627	Gdisc1 Control and Status	Read/Write	65B	Reserved	N/A
628	Reserved	N/A	65C	Timer 1 Data 0	
629	BIT Control and Status	Read/Write	65D	Timer 1 Data 1	
62A to 62D	Unallocated	N/A	65E	Timer 1 Data 2	
62E	User NVRAM Page LSB	Read/Write	65F	Timer 1 Data 3	
62F	User NVRAM Page MSB	Read/Write	660 to 67F	User NVRAM 32-byte window	Read/Write
630	System NVRAM Page LSB	Read/Write	680 to 69F	System NVRAM 32-byte window	Read/Write

a. Reserved for memory mapped NVRAM page register

The control and status registers exist for controlling or reading the status of the hardware. The addresses are as seen by the processor.

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In the following register descriptions, the bit significance is shown in little-endian mode (i.e. from the viewpoint of the processor). MSB = D7, LSB = D0

6.1 Board ID Register (0x600)

This reads back 0x54.

6.2 Board Revision Register (0x601)

This provides information on the build state of the SBC624.

Table 6-2 Board Revision Register

Bits	Meaning
D7 to D4	Major revision (artwork level) of the hardware build state: 1 = Revision 1 2 = Revision 2 etc.
D3 to D0	Minor revision of the hardware build state[a]: 0x0 = Revision A 0x1 = Revision B etc.

a. This does not necessarily represent the actual board revision.

6.3 Board Configuration Register 1 (0x602)

Table 6-3 Board Configuration Register 1

Bits	Meaning
D7	Reserved. Reads '0'
D6	Location of SPD/Ethernet Configuration EEPROMs 1 = SPD and Ethernet configuration EEPROMs enabled on TAC 0 = SPD and Ethernet configuration EEPROMs enabled on-board
D5	Front Panel I/O Present 1 = Front panel connectors are fitted (build levels 1 to 3 only) 0 = No front panel connectors (COM1 and ETH1 go to the rear only)
D4	Auto Boot Swap[a] 1 = Hardware has auto-swapped the boot location to the Recovery area (Main area corruption detected) 0 = Hardware has not auto-swapped the boot ROM location
D3	Boot ROM Location 1 = Board booted from the TAC[b] 0 = Board booted from on-board ROM
D2	Recovery Boot (shows setting of link)[a] 1 = Board booted from Recovery (BANC) ROM 0 = Board booted from Main ROM
D1 and D0	Reserved. Read '00_b'

a. Bit D2 only shows the setting of the Recovery Boot Link (E100). Bit D4 should also be taken into account when determining the cause for a boot mode swap.
b. The TAC is for Factory/Field Application Engineer use only.

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6.4 Board Configuration Register 2 (0x603)

Table 6-4 Board Configuration Register 2

Bits	Meaning
D7	PMC EREADY 1 = EREADY from both PMCs is asserted; software can enumerate PCI 0 = EREADY from one or both PMCs is negated; hold off PCI enumeration
D6	Memory SPD Configuration EEPROM Write Protection status[a] 1 = EEPROM is hardware write protected 0 = EEPROM is not hardware write protected
D5	PCIe Switch Configuration EEPROM Write Protection status[b c] 1 = EEPROM is hardware write protected 0 = EEPROM is not hardware write protected (default)
D4	Ethernet Configuration EEPROM Write Protection status[a c] 1 = EEPROM is hardware write protected 0 = EEPROM is not hardware write protected
D3 and D2	Reserved. Read '00_b'
D1	VPX NVMRO pin (shows the status of the VPX P0 connector pin A4) 1 = Non-volatile memory is write-protected 0 = Non-volatile memory may be write-enabled (depending on link settings)
D0	VPX System Controller 1 = SBC624 is in the System Controller slot 0 = SBC624 is not in the System Controller slot

a. Write protection is determined by the Configuration EEPROM Write Enable Link (E102) and the NVMRO signal (connector P0 pin A4).
b. Write protection is determined by the NVMRO signal (on connector P0 A4).
c. This bit shows the status of the hardware Write Protect input to the EEPROM device. Actual write protection status is determined by Status registers within the EEPROM.

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6.5 Board Configuration Register 3 (0x604)

Table 6-5 Board Configuration Register 3

Bits	Meaning
D7 and D6	Reserved. Read '00_b'
D5	Recovery BIOS ROM Write Protection Status[a] 1 = Write-protected 0 = Writes enabled
D4	Reserved. Reads '0'
D3	SSD1 Presence 1 = Fitted 0 = Not fitted
D2	NVRAM Write Protection Status[b] 1 = Write-protected 0 = Writes enabled
D1	SSD1 Write Protection Status[c] 1 = Write-protected 0 = Writes enabled
D0	Main BIOS ROM Write Protection Status[b] 1 = Write-protected 0 = Writes enabled

a. Write protection is determined by the Configuration EEPROM Write Enable Link (E102) and the NVMRO signal (connector P0 pin A4).
b. Write protection is determined by the NVRAM Write Enable Link (E101) and the NVMRO signal (on connector P0 pin A4).
c. Write protection is determined by the SSD1 Write Enable link (DIP switch).

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6.6 VPX Geographical Address Register (0x605)

Table 6-6 VPX Geographical Address Register

Bits	Meaning
D7 and D6	Reserved. Read '00_b'
D5	Holds the GAP~ pin status
D4	Holds the GA4~ pin status
D3	Holds the GA3~ pin status
D2	Holds the GA2~ pin status
D1	Holds the GA1~ pin status
D0	Holds the GA0~ pin status

All bits read logic '0' for a grounded pin and logic '1' for open circuit pin (pulled up with 4.7 kΩ resistors on the SBC624).

Table 6-7 Geographic Addressing

GAP~	GA4~	GA3~	GA2~	GA1~	GA0~	Hex	Slot Number
1	1	1	1	1	0	3E	1
1	1	1	1	0	1	3D	2
0	1	1	1	0	0	1C	3
1	1	1	0	1	1	3B	4
0	1	1	0	1	0	1A	5
0	1	1	0	0	1	19	6
1	1	1	0	0	0	38	7
1	1	0	1	1	1	37	8
0	1	0	1	1	0	16	9
0	1	0	1	0	1	15	10
1	1	0	1	0	0	34	11
0	1	0	0	1	1	13	12
1	1	0	0	1	0	32	13
1	1	0	0	0	1	31	14
0	1	0	0	0	0	10	15
1	0	1	1	1	1	2F	16
0	0	1	1	1	0	0E	17
0	0	1	1	0	1	0D	18
1	0	1	1	0	0	2C	19
0	0	1	0	1	1	0B	20
1	0	1	0	1	0	2A	21

GAP~ is the Geographic Address Parity line, and can optionally be used to validate the slot location defined by the values of GA[4:0]~. If not used, GAP~ is not connected to the backplane, although the backplane should have the signal tied high or low (as appropriate, depending on the slot location).

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6.7 Alarm Status Register (0x606)

Table 6-8 Alarm Status Register

Bits	Meaning
D7	PCIe Switch Status 1 = Fatal error 0 = No error
D6	CPU PROHOT Status (IRQ) 1 = Alarm 0 = No alarm
D5 to D0	Reserved. Read '000000_b'

6.8 Link Status Register (0x607)

Table 6-9 Link Settings Register

Bit	Meaning
D7	NVRAM Write Enable Link (E101) 1 = Jumper fitted 0 = Jumper not fitted
D6	Recovery Boot Link (E100) 1 = Jumper fitted 0 = Jumper not fitted
D5	Configuration EEPROM Write Enable Link (E102) 1 = Jumper fitted 0 = Jumper not fitted
D4	Reserved
D3	PMC2 VIO Signaling Voltage Link (E107) 1 = Jumper fitted (5V VIO) 0 = Jumper not fitted (3.3V VIO)
D2	PMC1 VIO Signaling Voltage Link (E106) 1 = Jumper fitted (5V VIO) 0 = Jumper not fitted (3.3V VIO)
D1	Enable Front Panel Ethernet Link (E104) 1 = Jumper fitted (ETH1 routed to front panel) 0 = Jumper not fitted (ETH1 routed to backplane)
D0	Enable Front Panel COM1 Link (E103) 1 = Jumper fitted (COM1 routed to front panel) 0 = Jumper not fitted (COM1 routed to backplane)

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6.9 Board Configuration Register 4 (0x608)

This shows what mezzanines are fitted.

Table 6-10 Board Configuration Register 4

Bits	Meaning
D7	PMC2 1 = Fitted 0 = Not fitted
D6	XMC2 1 = Fitted 0 = Not fitted
D5	PMC1 1 = Fitted 0 = Not fitted
D4	XMC1 1 = Fitted 0 = Not fitted
D3 to D0	Reserved. Read '0000_b'

6.10 Board Configuration Register 5 (0x609)

Table 6-11 Board Configuration Register 5

Bits	Meaning
D7 to D5	Reserved. Read '000_b'
D4	XMC2 I/O configuration 1 = XMC2 I/O not available. DVI2 available on P6 0 = XMC2 I/O available on P6. DVI2 not available
D3	XMC2 power configuration 1 = Power input is 12 V 0 = Power input is 5 V
D2	XMC1 power configuration 1 = Power input is 12 V 0 = Power input is 5 V
D1	Reserved. Reads '0'
D0	XMC1/PMC1 I/O configuration 1 = XMC1 I/O signals routed to P3 (P3W3P4-X38s+X8d+X12d) 0 = PMC1 I/O signals routed to P3 (P3W3P4-P64s+X12d)

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6.11 Board Configuration Register 6 (0x60A)

Table 6-12 Board Configuration Register 6

Bits	Meaning
D7 to D4	Reserved. Read '0000_b'
D3	SSD2 Presence 1 = Fitted 0 = Not fitted
D1	SSD2 Write Protection Status[a] 1 = Write-protected 0 = Writes enabled
D1	XMC2 BIST 1 = Active 0 = Inactive
D0	XMC1 BIST 1 = Active 0 = Inactive

a. The write protection is determined by the SSD2 Write Enable link (DIP switch).

6.12 FPGA Revision Register (0x60B)

This holds the revision of the FPGA code.

6.13 Watchdog Timer Refresh Register (0x60D)

Any write to this register re-loads the Watchdog Timer. This must be done periodically after the Watchdog Timer is enabled to keep it from causing a board reset.

6.14 Watchdog Timer Control/Status LSB Register (0x60E)

Table 6-13 Watchdog Timer Control/Status LSB Register

Bits	Meaning
D7 to D1	Reserved. Read '0000000_b'
D0	Watchdog Timer Count Enable 1 = Watchdog enabled 0 = Watchdog disabled (default)

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6.15 Watchdog Timer Control/Status MSB Register (0x60F)

Table 6-14 Watchdog Timer Control/Status MSB Register

Bits	Meaning
D7 to D3	Reserved. Read '00000_b'
D2 to D0	Watchdog Timer Timeout Selection (see below)

Table 6-15 Watchdog Timer Timeout Selection

D2	D1	D0	Timeout
1	1	1	2 ms (default)
1	1	0	32 ms
1	0	1	131 ms
1	0	0	262 ms
0	1	1	524 ms
0	1	0	2.1 seconds
0	0	1	33 seconds
0	0	0	66 seconds

6.16 Board ID String Registers (0x610 to 0x615)

These read back "SBC624".

6.17 Control Register 1 (0x620)

Table 6-16 Control Register 1

Bits	Meaning
D7 and D6	Sticky bits[a]
D5 to D0	Reserved. Read '000000_b'

a. These bits are used by the BIOS to know when SBC624 has been power cycled. They are only cleared to logic '0' by a power cycle or sleep state entry (any loss of +3.3V). On a reset, they contain the value that was previously written to them.

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6.18 Control Register 2 (0x621)

This controls the COM ports.

Table 6-17 Control Register 2

Bits	Meaning
D7 to D4	Reserved. Read '0000_b'
D3	COM2 RS422 Selection 1 = RS422 mode 0 = RS232 (default)
D2	COM1 RS422 Selection 1 = RS422 mode 0 = RS232 (default)
D1	COM1/COM2 TX/RX Buffer Loopback[a b] 1 = Loopback enabled 0 = Loopback disabled (default)
D0	COM1/COM2 Enable[b] 1 = Enabled 0 = Disabled (default)

a. This only controls the loopback for the TX/RX buffers, not the modem signals.
b. This has no effect on COM1 when it is routed to the front panel.

6.19 Control Register 3 (0x622)

This controls the BIT LEDs.

Table 6-18 Control Register 3

Bits	Meaning
D7	BIT Pass LED[a] 1 = LED lit 0 = LED off (default)
D6	BIT Fail LED[ab] 1 = LED lit (default) 0 = LED off
D5	BIT Status 1 LED[a] 1 = LED lit 0 = LED off (default)
D4	BIT Status 2 LED[a] 1 = LED lit 0 = LED off (default)
D3 to D0	Reserved. Read '0000_b'

a. This bit is sticky when the SBC624 is reset by the BIT Control and Status Register (register offset 0x629) bit 7 being set.

b. This output is combined with the BMC BIT Fail output using a logical Or operation, before driving the LED and also the BIT_FAIL pin on the backplane.

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6.20 IRQ Enable Register 1 (0x623)

Table 6-19 IRQ Enable Register 1

Bits	Meaning
D7 to D0	Reserved. Read '$0x00_b$'

6.21 IRQ Enable Register 2 (0x624)

Table 6-20 IRQ Enable Register 2

Bits	Meaning
D7 to D3	Reserved. Read '00000_b'
D2	BMC interrupt (connected to IRQ11 using SERIRQ) 1 = Enabled 0 = Disabled (default)
D1 and D0	Reserved. Read '00_b'

6.22 Control Register 4 (0x625)

Table 6-21 Control Register 4

Bits	Meaning
D7	Other BIOS Select[a] 1 = Selects the other BIOS to that selected by the Recovery Boot Link (E100) 0 = Active BIOS selected by the Recovery Boot Link (E100)
D6	Reserved. Reads '0'
D5	AUX_CLK Enable 1 = Enable the differential AUX_CLK driver onto the AUX_CLK pins on the P0 connector 0 = Do not drive AUX_CLK (default)
D4	REF_CLK Enable 1 = Enable the differential 25 MHz REF_CLK onto the REF_CLK pins on the P0 connector 0 = Do not drive REF_CLK (default)
D3	AUX_CLK Out[b] 1 = Drive logic '1' onto the AUX_CLK pins using the differential driver 0 = Drive logic '0' onto the AUX_CLK pins using the differential driver
D2	Maskable Reset (MSKRST~ on P1 connector pin G15) Mask 1 = Enable the MSKRST input (a logic '0' on this pin will reset the SBC624) 0 = Mask the MSKRST input (default)
D1	MSKRST Out 1 = Drive the MSKRST~ signal low 0 = Do not drive MSKRST~ (default)
D0	NVMRO Overrided[c] 1 = Drive the NVMRO signal low 0 = Do not drive NVMRO (default)

a. This bit can be used to target the other BIOS site for reprogramming.
b. The differential driver must be enabled by register bit D5 for the value to be driven out onto the backplane.
c. The NVMRO signal (on P0 pin A4) is only driven out onto the backplane if the SBC624 is System Controller.

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6.23 Control Register 5 (0x626)

Table 6-22 Control Register 5

Bit	Meaning
D7	Front Panel COM Port Mode[a] 1 = COM port is in RS422 mode 0 = COM port is in RS232 mode (default)
D6	Front Panel COM Port Loopback Mode[a] 1 = COM port is in loopback mode 0 = COM port is not in loopback mode (default)
D5	COM1 Front Panel Override[b] 1 = Force COM1 to the front panel, regardless of the E103 link state 0 = COM1 or COM3 is connected to the front panel depending on the link state (default)
D4	ETH1 Front Panel Override[b] 1 = Force ETH1 to the front panel, regardless of the E104 link state 0 = ETH1 routing to the front panel is determined by the link state (default)
D3	Reserved. Reads '0'
D2	SSD1 Fast Erase 1 = Trigger fast erase of SSD1 0 = Fast erase is disabled (default)
D1	Reserved. Reads '0'
D0	SSD2 Fast Erase 1 = Trigger fast erase of SSD2 0 = Fast erase is disabled (default)

a. The front panel COM port is either COM1 or COM3, depending on link settings and the state of bit D5.
b. This bit has no effect when no front panel I/O is present (i.e. bit D5 of Board Configuration Register 1 is '0').

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6.24 Gdiscrete1 Control and Status Register (0x627)

Gdiscrete1 (GDISC1~) is on P1 connector G1.

Table 6-23 Gdiscrete1 Control and Status Register

Bit	Meaning
D7	Gdiscrete1 In 1 = Gdiscrete1 backplane pin is high 0 = Gdiscrete1 backplane pin is low
D6	Gdiscrete1 IRQ Status 1 = IRQ is pending 0 = No IRQ pending (default)
D5	Gdiscrete1 Out[a] 1 = Drive Gdiscrete1 high 0 = Drive Gdiscrete1 low
D4	Gdiscrete1 Direction 1 = Output 0 = Input (default)
D3	Gdiscrete1 Interrupt Enable 1 = Interrupt generation is enabled 0 = Interrupt generation is masked (default)
D2	Gdiscrete1 Interrupt Sensitivity 1 = Edge sensitive 0 = Level sensitive (default)
D1	Gdiscrete1 Interrupt Level Sensitivity 1 = Active high/rising edge 0 = Active low/falling edge (default)
D0	Gdiscrete1 Interrupt Edge Sensitivity[b] 1 = Both edges 0 = Single edge (default)

a. This is only valid if the Gdiscrete1 Direction bit (D4) is set to output.
b. This is only valid if the Gdiscrete1 Interrupt Sensitivity bit (D2) is set to Edge sensitive.

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6.25 BIT Control and Status Register (0x629)

Table 6-24 BIT Control and Status Register

Bits	Function	Read/Write	Setting	Notes
D7	Board reset on completion of BIT	Read/write	1 = HRESET requested 0 = HRESET not requested (default)	
D6 and D5	BIT type run[a]	Read/write	00 = BIT has not run previously 01 = Fast BIT performed 10 = Full BIT performed 11 = Fast Start performed	
D4	BIT Pass/Fail[a]	Read/write	1 = BIT failed 0 = BIT passed	
D3	Fast BIT Enable (BIOS)	Read/write	1 = Fast BIT enabled via BIOS 0 = Fast BIT disabled (default)	The BIOS has a Fast BIT setting. This setting is written to this register bit.
D2	Fast Start Enable (BIOS)	Read/write	1 = Fast Start enabled via BIOS 0 = Fast Start disabled (default)	The BIOS has a Fast Start setting. This setting is written to this register bit.
D1	Fast Start Enable (Hardware)	Read only	1 = Run BIT (signal high) 0 = Fast Start (signal low)	From the dedicated FASTSTART~ signal on the backplane (P6 G1)
D0	BIT run[a]	Read/write	1 = BIT has run 0 = BIT has not run (default)	Cleared at power-up and during S5 (Soft Off). Can be set by software

a. Sticky bits when the SBC624 is reset by bit 7 being set.

6.26 User NVRAM Page LSB Register (0x62E) and User NVRAM Page MSB Register (0x62F)

These respectively hold bits 12 to 5 and 19 to 13 of the address driven onto the NVRAM bus when the User NVRAM is accessed. This selects a 32-byte page in the 512 Kbyte device, which can be accessed via the User NVRAM 32-byte Window I/O space between 0x660 and 0x67F.

The LSB Register defaults to 0x00.

Table 6-25 User NVRAM I/O Space Page MSB Register

Bits	Meaning
D7	Reserved. Reads '0'
D6 to D0	NVRAM address 19:13. Default is 0000000_b

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6.27 System NVRAM Page LSB Register (0x630) and System NVRAM Page MSB Register (0x631)

These respectively hold bits 12 to 5 and 19 to 13 of the address driven onto the NVRAM bus when the System NVRAM is accessed. This selects a 32-byte page in the 512 Kbyte device, which can be accessed via the System NVRAM 32-byte Window I/O space between 0x680 and 0x69F.

The LSB Register defaults to 0x00.

Table 6-26 System NVRAM I/O Space Page MSB Register

Bits	Meaning
D7	NVRAM Device Selection 1 = System NVRAM device selected 0 = User NVRAM device selected (default)
D6 to D0	NVRAM address 19:13. Default is 0000000_b

6.28 AXIS Timestamp Registers 0 to 5 (0x648 to 0x64E)

These read-only registers are used to obtain the 48-bit timestamp. Register 0 contains the least significant byte and register 5 contains the most significant byte. When register 0 is read, the current timestamp value is latched in registers 1 to 5, so register 0 must always be read first.

The AXIS timestamp counter is clocked by a divided version of the VPX REFCLK input, at a fixed frequency of 10 MHz, assuming an OpenVPX-compliant REFCLK of 25 MHz. The VPX System Controller (which may be the SBC624 itself) should generate REFCLK. The counter is reset whenever the VPX SYSRESET signal is asserted.

Table 6-27 AXIS Timestamp Registers 0 to 5

Bits	Meaning
D7 to D0	Timestamp value. Register 0 for byte 0 of 48-bit value, Register 1 for byte 1 etc.

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6.29 GPIO Registers

In all these registers, the GPIO pins are mapped onto the register bits as follows:

Table 6-28 GPIO Pin to Register Bit Mapping

Bit	GPIO Pin
D7	GPIO7
D6	GPIO6
D5	GPIO5
D4	GPIO4
D3	GPIO3
D2	GPIO2
D1	GPIO1
D0	GPIO0

6.29.1 GPIO Out Register (0x640)

This holds the GPIO out data.

NOTE
This register is only cleared on a power cycle.

6.29.2 GPIO In Register (0x641)

This reflects the current state of the GPIO pins regardless of whether they are configured as inputs or outputs.

6.29.3 GPIO Direction Register (0x642)

This defines the data direction of the GPIO pins, as follows:

1 = Output
0 = Input (default)

6.29.4 GPIO Interrupt Enable Register (0x643)

This defines which GPIO cells have interrupt generation enabled, as follows:

1 = Enabled
0 = Masked (default)

6.29.5 GPIO Interrupt Level/Edge Register (0x644)

This sets the interrupt detection sensitivity of each pin, as follows:

1 = Edge sensitive
0 = Level sensitive (default)

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6.29.6 GPIO Interrupt Low/High Register (0x645)

Depending on whether a GPIO pin is in level or edge mode, this defines the level or edge on which it generates interrupts, as follows:

1 = Active high or going-high edge
0 = Active low or going-low edge (default)

6.29.7 GPIO Both Edges Register (0x646)

If a GPIO pin is in edge mode, this defines whether it generates interrupts on one or both edges, as follows:

1 = Both edges
0 = One edge (default)

6.29.8 GPIO Interrupt Status Register (0x647)

This shows which GPIO pin is causing an interrupt, as follows:

1 = Interrupt pending
0 = No interrupt

Writing a logic '1' to a bit in this register will clear that pending interrupt.

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6.30 Timer Registers

The FPGA provides two identical 32-bit counter/timers. The default source clock for these counters is 2 MHz.

6.30.1 Timer 0 Control and Status Register 1 (0x650) and Timer 1 Control and Status Register 1 (0x658)

Table 6-29 Timer Control and Status Register 1

Bits	Meaning
D7	Timer IRQ Status 1 = Interrupt pending 0 = No interrupt
D6	Reserved. Reads '0'
D5 and D4	Clock Source Selection 00 = Use 2 MHz FPGA clock (default) 01 = Use OpenVPX REF_CLK 10 = Use OpenVPX AUX_CLK 11 = Use 25 MHz board clock
D3	Timer Read Selection 1 = Read Timer Load value 0 = Read Current Time value
D2 and D1	Clock Divider (when 2 MHz FPGA clock is used) 00 = 1:1 (2 MHz) 01 = 1:2 (1 MHz) 10 = 1:4 (500 kHz) 11 = 1:8 (250 kHz)
D0	Enable Timer IRQ 1 = IRQ enabled (SERIRQ 6) 0= IRQ masked

6.30.2 Timer 0 Control and Status Register 2 (0x651) and Timer 1 Control and Status Register 2 (0x659)

Table 6-30 Timer Control and Status Register 2

Bits	Meaning
D7 to D5	Reserved. Read '000_b'
D4	Timer Read Latch Select 1 = Latch all timers on read of Timer 0 LSB[a] 0 = Latch an Individual timer on the read of that individual timer's LSB
D3 to D1	Reserved. Read '000'
D0	Timer Enable 1 = Timer enabled 0 = Timer disabled

a. Setting this bit in *either* Timer CSR2 has the same effect of latching all timers on a read of the timer 0 LSB.

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6.30.3 Timer 0 IRQ Clear Register (0x652) and Timer 1 IRQ Clear Register (0x65A)

Any write to this register clears the Timer IRQ.

6.30.4 Timer Data Registers

These hold the timer current data value, as follows:

Table 6-31 Timer Data Registers

Offset	Timer	Data Value Bits
0x654	0	7:0 (least significant byte)
0x655	0	15:8
0x656	0	23:16
0x657	0	31:24 (most significant byte)
0x65C	1	7:0 (least significant byte)
0x65D	1	15:8
0x65E	1	23:16
0x65F	1	31:24 (most significant byte)

These registers all default to 0x00.

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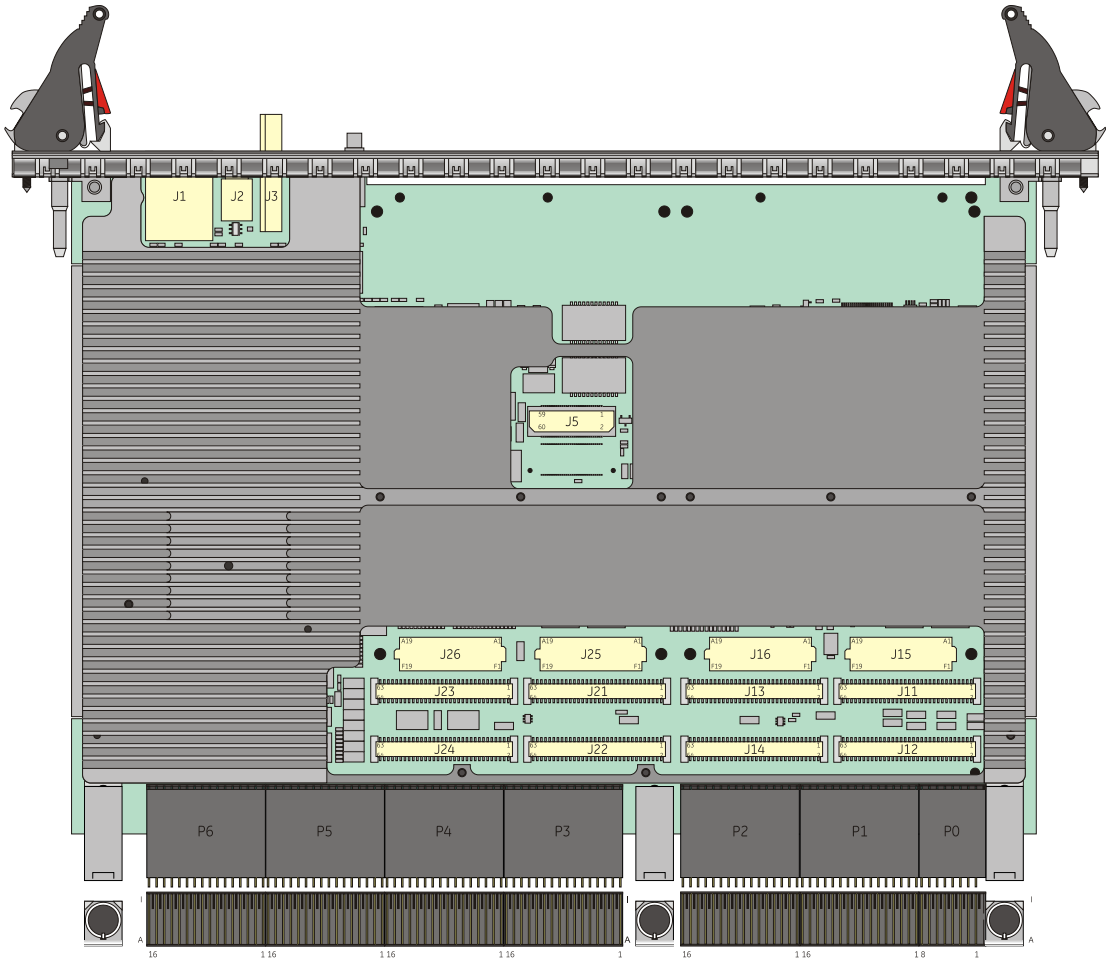
7 • Connectors

The following table shows the function of the connectors on the SBC624:

Table 7-1 Connector Functions

Connector	Function	Connector	Function
P0, P1, P2, P3, P4, P5, P6	VPX interface	J1 (front panel)	Ethernet channel 1
J11, J12, J13, J14	PMC site 1	J2 (front panel)	USB
J21, J22, J23, J24	PMC site 2	J3 (front panel)	Serial debug (COM1 or COM3)
J15, J16	XMC site 1	J4 (front panel)	DVI/HDMI
J25, J26	XMC site 2	P10 (on rear of PCB)	Test interface (factory use only)
J5	Processor debug (XDP)		

Figure 7-1 Front Connector Positions and Numbering

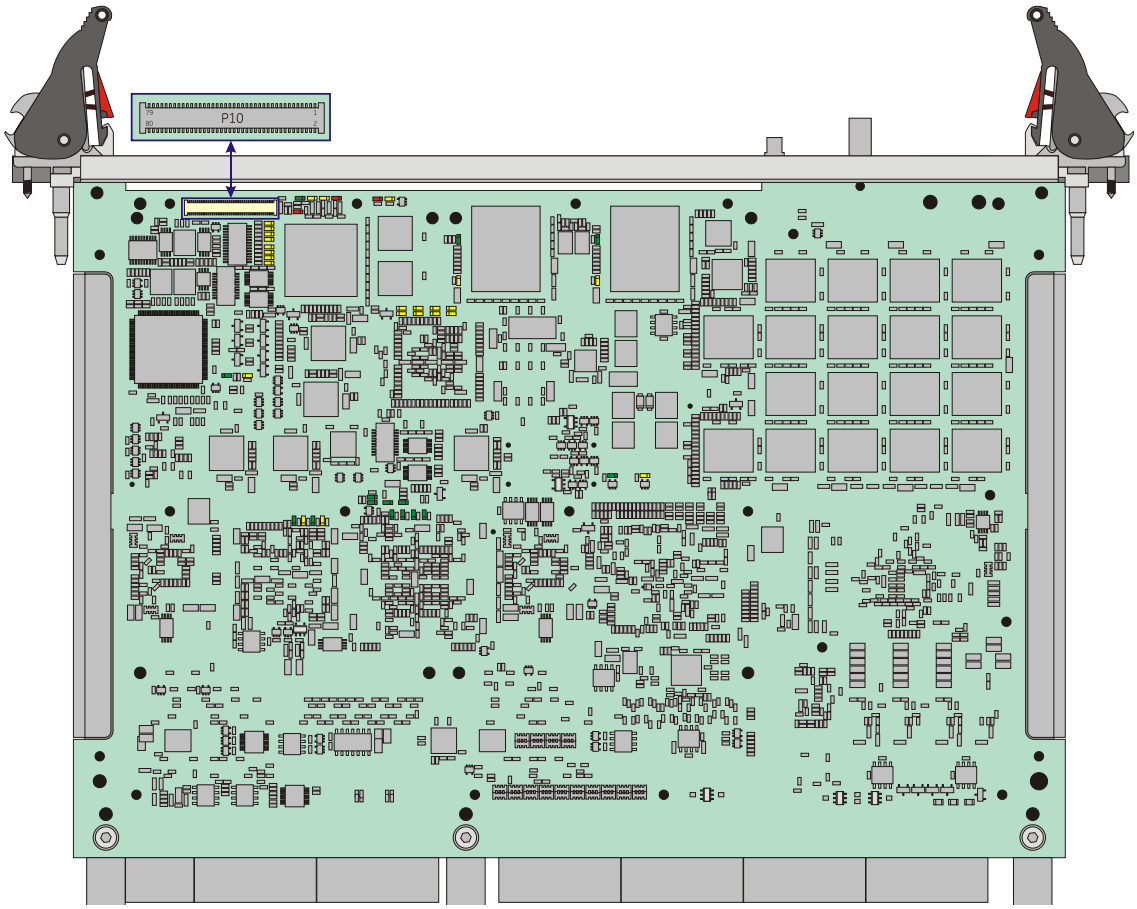


NOTE

The SBC624's guide pin receptacles are unkeyed by default, but may be keyed to customer requirements. Contact the factory for more details.

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Figure 7-2 Rear Connector Position and Numbering



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7.1 Backplane Connectors

The following sections show the pin assignments of the SBC624 VPX backplane connectors (P0 to P6). These are shown in the 7-row format as used in the VPX specifications.

Also provided are the corresponding pinouts for the J0 to J6 backplane connectors. These are shown in the 9-row format.



NOTE

Direction of fabrics is shown such that TX is an output from the SBC624 and RX is an input to the SBC624.

7.1.1 P0

Table 7-2 P0 Pin Assignments

Pin	A	B	C	D	E	F	G
1	VS2	VS2	VS2	None	VS1	VS1	VS1
2	VS2	VS2	VS2	None	VS1	VS1	VS1
3	VS3	VS3	VS3	None	VS3	VS3	VS3
4	NVMRO	SYSRESET~	GND	N12V_AUX	GND	IPMB_B_DATA	IPMB_B_CLK
5	IPMB_A_DATA	IPMB_A_CLK	GND	P3V3_AUX	GND	GA4~	GAP~
6	GA0~	GA1~	GND	P12V_AUX	GND	GA2~	GA3~
7	JTAG_TRST~	JTAG_TMS	GND	JTAG_TDI	JTAG_TDO	GND	JTAG_TCLK
8	GND	AUX_CLK_P	AUX_CLK_N	GND	REF_CLK_P	REF_CLK_N	GND

7.1.2 Backplane J0

Table 7-3 J0 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	VS2	VS2	VS2	VS2	None	VS1	VS1	VS1	VS1
2	VS2	VS2	VS2	VS2	None	VS1	VS1	VS1	VS1
3	VS3	VS3	VS3	VS3	None	VS3	VS3	VS3	VS3
4	GND	NVMRO	SYSRESET~	GND	N12V_AUX	GND	IPMB_B_DATA	IPMB_B_CLK	GND
5	GND	IPMB_A_DATA	IPMB_A_CLK	GND	P3V3_AUX	GND	GA4~	GAP~	GND
6	GND	GA0~	GA1~	GND	P12V_AUX	GND	GA2~	GA3~	GND
7	JTAG_TRST~	JTAG_TMS	GND	GND	JTAG_TDI	JTAG_TDO	GND	GND	JTAG_TCLK
8	GND	GND	AUX_CLK_P	AUX_CLK_N	GND	GND	REF_CLK_P	REF_CLK_N	GND

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7.1.3 P1

Table 7-4 P1 Pin Assignments

Pin	A	B	C	D	E	F	G
1	10GIB0_RP0	10GIB0_RN0	GND	10GIB0_TP0	10GIB0_TN0	GND	GDISC1~
2	GND	10GIB0_RP1	10GIB0_RN1	GND	10GIB0_TP1	10GIB0_TN1	GND
3	10GIB0_RP2	10GIB0_RN2	GND	10GIB0_TP2	10GIB0_TN2	GND	VBAT
4	GND	10GIB0_RP3	10GIB0_RN3	GND	10GIB0_TP3	10GIB0_TN3	GND
5	10GIB1_RP0	10GIB1_RN0	GND	10GIB1_TP0	10GIB1_TN0	GND	SYSCON~
6	GND	10GIB1_RP1	10GIB1_RN1	GND	10GIB1_TP1	10GIB1_TN1	GND
7	10GIB1_RP2	10GIB1_RN2	GND	10GIB1_TP2	10GIB1_TN2	GND	N/C
8	GND	10GIB1_RP3	10GIB1_RN3	GND	10GIB1_TP3	10GIB1_TN3	GND
9	N/C	N/C	GND	N/C	N/C	GND	PSU_SEQ_IN
10	GND	N/C	N/C	GND	N/C	N/C	GND
11	N/C	N/C	GND	N/C	N/C	GND	PSU_SEQ_OUT
12	GND	N/C	N/C	GND	N/C	N/C	GND
13	N/C	N/C	GND	N/C	N/C	GND	INTRUDER_DTECT~
14	GND	N/C	N/C	GND	N/C	N/C	GND
15	N/C	N/C	GND	N/C	N/C	GND	MSKRST~
16	GND	N/C	N/C	GND	N/C	N/C	GND

7.1.4 Backplane J1

Table 7-5 J1 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	10GIB0_RP0	10GIB0_RN0	GND	GND	10GIB0_TP0	10GIB0_TN0	GND	GND	GDISC1~
2	GND	GND	10GIB0_RP1	10GIB0_RN1	GND	GND	10GIB0_TP1	10GIB0_TN1	GND
3	10GIB0_RP2	10GIB0_RN2	GND	GND	10GIB0_TP2	10GIB0_TN2	GND	GND	VBAT
4	GND	GND	10GIB0_RP3	10GIB0_RN3	GND	GND	10GIB0_TP3	10GIB0_TN3	GND
5	10GIB1_RP0	10GIB1_RN0	GND	GND	10GIB1_TP0	10GIB1_TN0	GND	GND	SYS_CON~
6	GND	GND	10GIB1_RP1	10GIB1_RN1	GND	GND	10GIB1_TP1	10GIB1_TN1	GND
7	10GIB1_RP2	10GIB1_RN2	GND	GND	10GIB1_TP2	10GIB1_TN2	GND	GND	N/C
8	GND	GND	10GIB1_RP3	10GIB1_RN3	GND	GND	10GIB1_TP3	10GIB1_TN3	GND
9	N/C	N/C	GND	GND	N/C	N/C	GND	GND	PSU_SEQ_IN
10	GND	GND	N/C	N/C	GND	GND	N/C	N/C	GND
11	N/C	N/C	GND	GND	N/C	N/C	GND	GND	PSU_SEQ_OUT
12	GND	GND	N/C	N/C	GND	GND	N/C	N/C	GND
13	N/C	N/C	GND	GND	N/C	N/C	GND	GND	INTRUDER_DTECT~
14	GND	GND	N/C	N/C	GND	GND	N/C	N/C	GND
15	N/C	N/C	GND	GND	N/C	N/C	GND	GND	MSKRST~
16	GND	GND	N/C	N/C	GND	GND	N/C	N/C	GND

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7.1.5 P2

Table 7-6 P2 Pin Assignments

Pin	A	B	C	D	E	F	G
1	PCIE_RX0P	PCIE_RX0N	GND	PCIE_TX0P	PCIE_TX0N	GND	N/C
2	GND	PCIE_RX1P	PCIE_RX1N	GND	PCIE_TX1P	PCIE_TX1N	GND
3	PCIE_RX2P	PCIE_RX2N	GND	PCIE_TX2P	PCIE_TX2N	GND	N/C
4	GND	PCIE_RX3P	PCIE_RX3N	GND	PCIE_TX3P	PCIE_TX3N	GND
5	PCIE_RX4P	PCIE_RX4N	GND	PCIE_TX4P	PCIE_TX4N	GND	N/C
6	GND	PCIE_RX5P	PCIE_RX5N	GND	PCIE_TX5P	PCIE_TX5N	GND
7	PCIE_RX6P	PCIE_RX6N	GND	PCIE_TX6P	PCIE_TX6N	GND	N/C
8	GND	PCIE_RX7P	PCIE_RX7N	GND	PCIE_TX7P	PCIE_TX7N	GND
9	PCIE_RX8P	PCIE_RX8N	GND	PCIE_TX8P	PCIE_TX8N	GND	N/C (EPCLOCK1N)
10	GND	PCIE_RX9P	PCIE_RX9N	GND	PCIE_TX9P	PCIE_TX9N	GND
11	PCIE_RX10P	PCIE_RX10N	GND	PCIE_TX10P	PCIE_TX10N	GND	N/C (EPCLOCK1P)
12	GND	PCIE_RX11P	PCIE_RX11N	GND	PCIE_TX11P	PCIE_TX11N	GND
13	PCIE_RX12P	PCIE_RX12N	GND	PCIE_TX12P	PCIE_TX12N	GND	N/C (EPCLOCK2N)
14	GND	PCIE_RX13P	PCIE_RX13N	GND	PCIE_TX13P	PCIE_TX13N	GND
15	PCIE_RX14P	PCIE_RX14N	GND	PCIE_TX14P	PCIE_TX14N	GND	N/C (EPCLOCK2P)
16	GND	PCIE_RX15P	PCIE_RX15N	GND	PCIE_TX15P	PCIE_TX15N	GND

7.1.6 Backplane J2



CAUTION

The SBC624 has been specifically designed for use with 6U VPX backplanes designed to accommodate a differential pin out on the J2 connector and is *not* compatible with 6U backplanes where the J2 connector is intended for single ended signaling. Plugging the SBC624 into such a 6U backplane may cause permanent component damage.

Table 7-7 J2 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	PCIE_RX0P	PCIE_RX0N	GND	GND	PCIE_TX0P	PCIE_TX0N	GND	GND	N/C
2	GND	GND	PCIE_RX1P	PCIE_RX1N	GND	GND	PCIE_TX1P	PCIE_TX1N	GND
3	PCIE_RX2P	PCIE_RX2N	GND	GND	PCIE_TX2P	PCIE_TX2N	GND	GND	N/C
4	GND	GND	PCIE_RX3P	PCIE_RX3N	GND	GND	PCIE_TX3P	PCIE_TX3N	GND
5	PCIE_RX4P	PCIE_RX4N	GND	GND	PCIE_TX4P	PCIE_TX4N	GND	GND	N/C
6	GND	GND	PCIE_RX5P	PCIE_RX5N	GND	GND	PCIE_TX5P	PCIE_TX5N	GND
7	PCIE_RX6P	PCIE_RX6N	GND	GND	PCIE_TX6P	PCIE_TX6N	GND	GND	N/C
8	GND	GND	PCIE_RX7P	PCIE_RX7N	GND	GND	PCIE_TX7P	PCIE_TX7N	GND
9	PCIE_RX8P	PCIE_RX8N	GND	GND	PCIE_TX8P	PCIE_TX8N	GND	GND	N/C (EPCLOCK1N)
10	GND	GND	PCIE_RX9P	PCIE_RX9N	GND	GND	PCIE_TX9P	PCIE_TX9N	GND
11	PCIE_RX10P	PCIE_RX10N	GND	GND	PCIE_TX10P	PCIE_TX10N	GND	GND	N/C (EPCLOCK1P)
12	GND	GND	PCIE_RX11P	PCIE_RX11N	GND	GND	PCIE_TX11P	PCIE_TX11N	GND
13	PCIE_RX12P	PCIE_RX12N	GND	GND	PCIE_TX12P	PCIE_TX12N	GND	GND	N/C (EPCLOCK2N)
14	GND	GND	PCIE_RX13P	PCIE_RX13N	GND	GND	PCIE_TX13P	PCIE_TX13N	GND
15	PCIE_RX14P	PCIE_RX14N	GND	GND	PCIE_TX14P	PCIE_TX14N	GND	GND	N/C (EPCLOCK2P)
16	GND	GND	PCIE_RX15P	PCIE_RX15N	GND	GND	PCIE_TX15P	PCIE_TX15N	GND

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7.1.7 P3

Table 7-8 P3 Pin Assignments

Pin	A	B	C	D	E	F	G
1	PMC1_IO_04	PMC1_IO_02	GND	PMC1_IO_03	PMC1_IO_01	GND	COM1_RXD/ RXD_A
2	GND	PMC1_IO_08	PMC1_IO_06	GND	PMC1_IO_07	PMC1_IO_05	GND
3	PMC1_IO_12/ XMC1_IO_F01	PMC1_IO_10/ XMC1_IO_C01	GND	PMC1_IO_11	PMC1_IO_09	GND	COM1_TXD/ TXD_A
4	GND	PMC1_IO_16/ XMC1_IO_F03	PMC1_IO_14/ XMC1_IO_F02	GND	PMC1_IO_15/ XMC1_IO_C03	PMC1_IO_13/ XMC1_IO_C02	GND
5	PMC1_IO_20/ XMC1_IO_F05	PMC1_IO_18/ XMC1_IO_F04	GND	PMC1_IO_19/ XMC1_IO_C05	PMC1_IO_17/ XMC1_IO_C04	GND	COM1_CTS/ RXD_B
6	GND	PMC1_IO_24/ XMC1_IO_F07	PMC1_IO_22/ XMC1_IO_F06	GND	PMC1_IO_23/ XMC1_IO_C07	PMC1_IO_21/ XMC1_IO_C06	GND
7	PMC1_IO_28/ XMC1_IO_F09	PMC1_IO_26/ XMC1_IO_F08	GND	PMC1_IO_27/ XMC1_IO_C09	PMC1_IO_25/ XMC1_IO_C08	GND	COM1_RTS/ TXD_B
8	GND	PMC1_IO_32/ XMC1_IO_F11	PMC1_IO_30/ XMC1_IO_F10	GND	PMC1_IO_31/ XMC1_IO_C11	PMC1_IO_29/ XMC1_IO_C10	GND
9	PMC1_IO_36/ XMC1_IO_F13	PMC1_IO_34/ XMC1_IO_F12	GND	PMC1_IO_35/ XMC1_IO_C13	PMC1_IO_33/ XMC1_IO_C12	GND	COM1_DSR
10	GND	PMC1_IO_40/ XMC1_IO_F15	PMC1_IO_38/ XMC1_IO_F14	GND	PMC1_IO_39/ XMC1_IO_C15	PMC1_IO_37/ XMC1_IO_C14	GND
11	PMC1_IO_44/ XMC1_IO_F17	PMC1_IO_42/ XMC1_IO_F16	GND	PMC1_IO_43/ XMC1_IO_C17	PMC1_IO_41/ XMC1_IO_C16	GND	COM1_DCD
12	GND	PMC1_IO_48/ XMC1_IO_F19	PMC1_IO_46/ XMC1_IO_F18	GND	PMC1_IO_47/ XMC1_IO_C19	PMC1_IO_45/ XMC1_IO_C18	GND
13	PMC1_IO_52/ XMC1_IO_E01	PMC1_IO_50/ XMC1_IO_D01	GND	PMC1_IO_51/ XMC1_IO_B01	PMC1_IO_49/ XMC1_IO_A01	GND	COM1_RI
14	GND	PMC1_IO_56/ XMC1_IO_E03	PMC1_IO_54/ XMC1_IO_D03	GND	PMC1_IO_55/ XMC1_IO_B03	PMC1_IO_53/ XMC1_IO_A03	GND
15	PMC1_IO_60/ XMC1_IO_E11	PMC1_IO_58/ XMC1_IO_D11	GND	PMC1_IO_59/ XMC1_IO_B11	PMC1_IO_57/ XMC1_IO_A11	GND	COM1_DTR
16	GND	PMC1_IO_64/ XMC1_IO_E13	PMC1_IO_62/ XMC1_IO_D13	GND	PMC1_IO_63/ XMC1_IO_B13	PMC1_IO_61/ XMC1_IO_A13	GND

PMC or XMC I/O is a build option. See the Mezzanine I/O Routing section for more details.

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7.1.8 Backplane J3

Table 7-9 J3 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	PMC1_IO_04	PMC1_IO_02	GND	GND	PMC1_IO_03	PMC1_IO_01	GND	GND	COM1_RXD/ RXD_A
2	GND	GND	PMC1_IO_08	PMC1_IO_06	GND	GND	PMC1_IO_07	PMC1_IO_05	GND
3	PMC1_IO_12/ XMC1_IO_F01	PMC1_IO_10/ XMC1_IO_C01	GND	GND	PMC1_IO_11	PMC1_IO_09	GND	GND	COM1_TXD/ TXD_A
4	GND	GND	PMC1_IO_16/ XMC1_IO_F03	PMC1_IO_14/ XMC1_IO_F02	GND	GND	PMC1_IO_15/ XMC1_IO_C03	PMC1_IO_13/ XMC1_IO_C02	GND
5	PMC1_IO_20/ XMC1_IO_F05	PMC1_IO_18/ XMC1_IO_F04	GND	GND	PMC1_IO_19/ XMC1_IO_C05	PMC1_IO_17/ XMC1_IO_C04	GND	GND	COM1_CTS/ RXD_B
6	GND	GND	PMC1_IO_24/ XMC1_IO_F07	PMC1_IO_22/ XMC1_IO_F06	GND	GND	PMC1_IO_23/ XMC1_IO_C07	PMC1_IO_21/ XMC1_IO_C06	GND
7	PMC1_IO_28/ XMC1_IO_F09	PMC1_IO_26/ XMC1_IO_F08	GND	GND	PMC1_IO_27/ XMC1_IO_C09	PMC1_IO_25/ XMC1_IO_C08	GND	GND	COM1_RTS/ TXD_B
8	GND	GND	PMC1_IO_32/ XMC1_IO_F11	PMC1_IO_30/ XMC1_IO_F10	GND	GND	PMC1_IO_31/ XMC1_IO_C11	PMC1_IO_29/ XMC1_IO_C10	GND
9	PMC1_IO_36/ XMC1_IO_F13	PMC1_IO_34/ XMC1_IO_F12	GND	GND	PMC1_IO_35/ XMC1_IO_C13	PMC1_IO_33/ XMC1_IO_C12	GND	GND	COM1_DSR
10	GND	GND	PMC1_IO_40/ XMC1_IO_F15	PMC1_IO_38/ XMC1_IO_F14	GND	GND	PMC1_IO_39/ XMC1_IO_C15	PMC1_IO_37/ XMC1_IO_C14	GND
11	PMC1_IO_44/ XMC1_IO_F17	PMC1_IO_42/ XMC1_IO_F16	GND	GND	PMC1_IO_43/ XMC1_IO_C17	PMC1_IO_41/ XMC1_IO_C16	GND	GND	COM1_DCD
12	GND	GND	PMC1_IO_48/ XMC1_IO_F19	PMC1_IO_46/ XMC1_IO_F18	GND	GND	PMC1_IO_47/ XMC1_IO_C19	PMC1_IO_45/ XMC1_IO_C18	GND
13	PMC1_IO_52/ XMC1_IO_E01	PMC1_IO_50/ XMC1_IO_D01	GND	GND	PMC1_IO_51/ XMC1_IO_B01	PMC1_IO_49/ XMC1_IO_A01	GND	GND	COM1_RI
14	GND	GND	PMC1_IO_56/ XMC1_IO_E03	PMC1_IO_54/ XMC1_IO_D03	GND	GND	PMC1_IO_55/ XMC1_IO_B03	PMC1_IO_53/ XMC1_IO_A03	GND
15	PMC1_IO_60/ XMC1_IO_E11	PMC1_IO_58/ XMC1_IO_D11	GND	GND	PMC1_IO_59/ XMC1_IO_B11	PMC1_IO_57/ XMC1_IO_A11	GND	GND	COM1_DTR
16	GND	GND	PMC1_IO_64/ XMC1_IO_E13	PMC1_IO_62/ XMC1_IO_D13	GND	GND	PMC1_IO_63/ XMC1_IO_B13	PMC1_IO_61/ XMC1_IO_A13	GND

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7.1.9 P4

Table 7-10 P4 Pin Assignments

Pin	A	B	C	D	E	F	G
1	XMC1_IO_E05	XMC1_IO_D05	GND	XMC1_IO_B05	XMC1_IO_A05	GND	COM2_RXD/RXD_A
2	GND	XMC1_IO_E07	XMC1_IO_D07	GND	XMC1_IO_B07	XMC1_IO_A07	GND
3	XMC1_IO_E09	XMC1_IO_D09	GND	XMC1_IO_B09	XMC1_IO_A09	GND	COM2_TXD/TXD_A
4	GND	XMC1_IO_E15	XMC1_IO_D15	GND	XMC1_IO_B15	XMC1_IO_A15	GND
5	XMC1_IO_E17	XMC1_IO_D17	GND	XMC1_IO_B17	XMC1_IO_A17	GND	COM2_CTS/RXD_B
6	GND	XMC1_IO_E19	XMC1_IO_D19	GND	XMC1_IO_B19	XMC1_IO_A19	GND
7	KBCLK	KBDAT	GND	MSCLK	MSDAT	GND	COM2_RTS/TXD_B
8	GND	N/C	N/C	GND	GPIO6	GPIO4	GND
9	USB0_P	USB0_N	GND	USB1_P	USB1_N	GND	COM2_DSR
10	GND	USB0_POWER	USB1_POWER	GND	GPIO7	GPIO5	GND
11	ETH3_RP	ETH3_RN	GND	ETH3_TP	ETH3_TN	GND	COM2_DCD
12	GND	ETH2_RP	ETH2_RN	GND	ETH2_TP	ETH2_TN	GND
13	ETH1_0P	ETH1_0N	GND	ETH1_1P	ETH1_1N	GND	COM2_RI
14	GND	ETH1_2P	ETH1_2N	GND	ETH1_3P	ETH1_3N	GND
15	ETH0_0P	ETH0_0N	GND	ETH0_1P	ETH0_1N	GND	COM2_DTR
16	GND	ETH0_2P	ETH0_2N	GND	ETH0_3P	ETH0_3N	GND

7.1.10 Backplane J4

Table 7-11 J4 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	XMC1_IO_E05	XMC1_IO_D05	GND	GND	XMC1_IO_B05	XMC1_IO_A05	GND	GND	COM2_RXD/RXD_A
2	GND	GND	XMC1_IO_E07	XMC1_IO_D07	GND	GND	XMC1_IO_B07	XMC1_IO_A07	GND
3	XMC1_IO_E09	XMC1_IO_D09	GND	GND	XMC1_IO_B09	XMC1_IO_A09	GND	GND	COM2_TXD/TXD_A
4	GND	GND	XMC1_IO_E15	XMC1_IO_D15	GND	GND	XMC1_IO_B15	XMC1_IO_A15	GND
5	XMC1_IO_E17	XMC1_IO_D17	GND	GND	XMC1_IO_B17	XMC1_IO_A17	GND	GND	COM2_CTS/RXD_B
6	GND	GND	XMC1_IO_E19	XMC1_IO_D19	GND	GND	XMC1_IO_B19	XMC1_IO_A19	GND
7	KBCLK	KBDAT	GND	GND	MSCLK	MSDAT	GND	GND	COM2_RTS/TXD_B
8	GND	GND	N/C	N/C	GND	GND	GPIO6	GPIO4	GND
9	USB0_P	USB0_N	GND	GND	USB1_P	USB1_N	GND	GND	COM2_DSR
10	GND	GND	USB0_POWER	USB1_POWER	GND	GND	GPIO7	GPIO5	GND
11	ETH3_RP	ETH3_RN	GND	GND	ETH3_TP	ETH3_TN	GND	GND	COM2_DCD
12	GND	GND	ETH2_RP	ETH2_RN	GND	GND	ETH2_TP	ETH2_TN	GND
13	ETH1_0P	ETH1_0N	GND	GND	ETH1_1P	ETH1_1N	GND	GND	COM2_RI
14	GND	GND	ETH1_2P	ETH1_2N	GND	GND	ETH1_3P	ETH1_3N	GND
15	ETH0_0P	ETH0_0N	GND	GND	ETH0_1P	ETH0_1N	GND	GND	COM2_DTR
16	GND	GND	ETH0_2P	ETH0_2N	GND	GND	ETH0_3P	ETH0_3N	GND

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7.1.11 P5

Table 7-12 P5 Pin Assignments

Pin	A	B	C	D	E	F	G
1	PMC2_IO_04	PMC2_IO_02	GND	PMC2_IO_03	PMC2_IO_01	GND	HDA_SDO
2	GND	PMC2_IO_08	PMC2_IO_06	GND	PMC2_IO_07	PMC2_IO_05	GND
3	PMC2_IO_12	PMC2_IO_10	GND	PMC2_IO_11	PMC2_IO_09	GND	HDA_RST~
4	GND	PMC2_IO_16	PMC2_IO_14	GND	PMC2_IO_15	PMC2_IO_13	GND
5	PMC2_IO_20	PMC2_IO_18	GND	PMC2_IO_19	PMC2_IO_17	GND	HDA_BCLK
6	GND	PMC2_IO_24	PMC2_IO_22	GND	PMC2_IO_23	PMC2_IO_21	GND
7	PMC2_IO_28	PMC2_IO_26	GND	PMC2_IO_27	PMC2_IO_25	GND	HDA_SYNC
8	GND	PMC2_IO_32	PMC2_IO_30	GND	PMC2_IO_31	PMC2_IO_290	GND
9	PMC2_IO_36	PMC2_IO_34	GND	PMC2_IO_35	PMC2_IO_33	GND	HDA_SDIN0
10	GND	PMC2_IO_40	PMC2_IO_38	GND	PMC2_IO_39	PMC2_IO_37	GND
11	PMC2_IO_44	PMC2_IO_42	GND	PMC2_IO_43	PMC2_IO_41	GND	SPKR
12	GND	PMC2_IO_48	PMC2_IO_46	GND	PMC2_IO_47	PMC2_IO_45	GND
13	PMC2_IO_52	PMC2_IO_50	GND	PMC2_IO_51	PMC2_IO_49	GND	RTM_RST~
14	GND	PMC2_IO_56	PMC2_IO_54	GND	PMC2_IO_55	PMC2_IO_53	GND
15	PMC2_IO_60	PMC2_IO_58	GND	PMC2_IO_59	PMC2_IO_57	GND	N/C
16	GND	PMC2_IO_64	PMC2_IO_62	GND	PMC2_IO_63	PMC2_IO_61	GND

7.1.12 Backplane J5

Table 7-13 J5 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	PMC2_IO_04	PMC2_IO_02	GND	GND	PMC2_IO_03	PMC2_IO_01	GND	GND	HDA_SDO
2	GND	GND	PMC2_IO_08	PMC2_IO_06	GND	GND	PMC2_IO_07	PMC2_IO_05	GND
3	PMC2_IO_12	PMC2_IO_10	GND	GND	PMC2_IO_11	PMC2_IO_09	GND	GND	HDA_RST~
4	GND	GND	PMC2_IO_16	PMC2_IO_14	GND	GND	PMC2_IO_15	PMC2_IO_13	GND
5	PMC2_IO_20	PMC2_IO_18	GND	GND	PMC2_IO_19	PMC2_IO_17	GND	GND	HDA_BCLK
6	GND	GND	PMC2_IO_24	PMC2_IO_22	GND	GND	PMC2_IO_23	PMC2_IO_21	GND
7	PMC2_IO_28	PMC2_IO_26	GND	GND	PMC2_IO_27	PMC2_IO_25	GND	GND	HDA_SYNC
8	GND	GND	PMC2_IO_32	PMC2_IO_30	GND	GND	PMC2_IO_31	PMC2_IO_29	GND
9	PMC2_IO_36	PMC2_IO_34	GND	GND	PMC2_IO_35	PMC2_IO_33	GND	GND	HDA_SDIN0
10	GND	GND	PMC2_IO_40	PMC2_IO_38	GND	GND	PMC2_IO_39	PMC2_IO_37	GND
11	PMC2_IO_44	PMC2_IO_42	GND	GND	PMC2_IO_43	PMC2_IO_41	GND	GND	SPKR
12	GND	GND	PMC2_IO_48	PMC2_IO_46	GND	GND	PMC2_IO_47	PMC2_IO_45	GND
13	PMC2_IO_52	PMC2_IO_50	GND	GND	PMC2_IO_51	PMC2_IO_49	GND	GND	RTM_RST~
14	GND	GND	PMC2_IO_56	PMC2_IO_54	GND	GND	PMC2_IO_55	PMC2_IO_533	GND
15	PMC2_IO_60	PMC2_IO_58	GND	GND	PMC2_IO_59	PMC2_IO_57	GND	GND	N/C
16	GND	GND	PMC2_IO_64	PMC2_IO_62	GND	GND	PMC2_IO_63	PMC2_IO_61	GND

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7.1.13 P6

Table 7-14 P6 Pin Assignments

Pin	A	B	C	D	E	F	G
1	XMC2_IO_E05/ DVI2_DDC_CLK	XMC2_IO_D05/ N/C	GND	XMC2_IO_B05/ N/C	XMC2_IO_A05/ N/C	GND	FASTSTART~
2	GND	XMC2_IO_E07/ DVI2_DDC_DATA	XMC2_IO_D07/ DVI2_HPD	GND	XMC2_IO_B07/ N/C	XMC2_IO_A07/ N/C	GND
3	XMC2_IO_E09/ N/C	XMC2_IO_D09/ N/C	GND	XMC2_IO_B09/ N/C	XMC2_IO_A09/ N/C	GND	VGA_DDC_CLK
4	GND	XMC2_IO_E15/ N/C	XMC2_IO_D15/ N/C	GND	XMC2_IO_B15/ N/C	XMC2_IO_A15/ N/C	GND
5	XMC2_IO_E17/ DVI2_TX2P	XMC2_IO_D17/ DVI2_TX2N	GND	XMC2_IO_B17/ DVI2_TX0P	XMC2_IO_A17/ DVI2_TX0N	GND	VGA_DDC_DATA
6	GND	XMC2_IO_E19/ DVI2_TXCP	XMC2_IO_D19/ DVI2_TXCN	GND	XMC2_IO_B19/ DVI2_TX1P	XMC2_IO_A19/ DVI2_TX1N	GND
7	USB2_N	USB2_P	GND	DVI1_DDC_DATA	DVI1_DDC_CLK	GND	VGA_VSYNC
8	GND	USB2_POWER	GPIO0	GND	DVI1_TX0N	DVI1_TX0P	GND
9	USB3_N	USB3_P	GND	USB10_P	USB10_N	GND	VGA_HSYNC
10	GND	USB3_POWER	GPIO1	GND	DVI1_TX1N	DVI1_TX1P	GND
11	SATA0_TXP	SATA0_TXN	GND	SATA0_RXN	SATA0_RXP	GND	VGA_RED
12	GND	USB10_POWER	GPIO2	GND	DVI1_TX2N	DVI1_TX2P	GND
13	USB11_N	USB11_P	GND	SATA1_TXP	SATA1_TXN	GND	VGA_GREEN
14	GND	USB11_POWER	GPIO3	GND	DVI1_TXCN	DVI1_TXCP	GND
15	SATA1_RXN	SATA1_RXP	GND	SATA4_RXP	SATA4_RXN	GND	VGA_BLUE
16	GND	SATA4_TXP	SATA4_TXN	GND	DVI1_HPD	BITFAIL~	GND

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7.1.14 Backplane J6

Table 7-15 J6 Pin Assignments

Pin	A	B	C	D	E	F	G	H	I
1	XMC2_IO_E05/ DVI2_DDC_CLK	XMC2_IO_D05/ N/C	GND	GND	XMC2_IO_B05/ N/C	XMC2_IO_A05/ N/C	GND	GND	FASTSTART~
2	GND	GND	XMC2_IO_E07/ DVI2_DDC_DATA	XMC2_IO_D07/ DVI2_HPD	GND	GND	XMC2_IO_B07/ N/C	XMC2_IO_A07/ N/C	GND
3	XMC2_IO_E09/ N/C	XMC2_IO_D09/ N/C	GND	GND	XMC2_IO_B09/ N/C	XMC2_IO_A09/ N/C	GND	GND	VGA_DDC_CLK
4	GND	GND	XMC2_IO_E15/ N/C	XMC2_IO_D15/ N/C	GND	GND	XMC2_IO_B15/ N/C	XMC2_IO_A15/ N/C	GND
5	XMC2_IO_E17/ DVI2_TX2P	XMC2_IO_D17/ DVI2_TX2N	GND	GND	XMC2_IO_B17/ DVI2_TX0P	XMC2_IO_A17/ DVI2_TX0N	GND	GND	VGA_DDC_DATA
6	GND	GND	XMC2_IO_E19/ DVI2_TXCP	XMC2_IO_D19/ DVI2_TXCN	GND	GND	XMC2_IO_B19/ DVI2_TX1P	XMC2_IO_A19/ DVI2_TX1N	GND
7	USB2_N	USB2_P	GND	GND	DVI1_DDC_DATA	DVI1_DDC_CLK	GND	GND	VGA_VSYNC
8	GND	GND	USB2_POWER	GPIO0	GND	GND	DVI1_TX0N	DVI1_TX0P	GND
9	USB3_N	USB3_P	GND	GND	USB10_P	USB10_N	GND	GND	VGA_HSYNC
10	GND	GND	USB3_POWER	GPIO1	GND	GND	DVI1_TX1N	DVI1_TX1P	GND
11	SATA0_TXP	SATA0_TXN	GND	GND	SATA0_RXN	SATA0_RXP	GND	GND	VGA_RED
12	GND	GND	USB10_POWER	GPIO2	GND	GND	DVI1_TX2N	DVI1_TX2P	GND
13	USB11_N	USB11_P	GND	GND	SATA1_TXP	SATA1_TXN	GND	GND	VGA_GREEN
14	GND	GND	USB11_POWER	GPIO3	GND	GND	DVI1_TXCN	DVI1_TXCP	GND
15	SATA1_RXN	SATA1_RXP	GND	GND	SATA4_RXP	SATA4_RXN	GND	GND	VGA_BLUE
16	GND	GND	SATA4_TXP	SATA4_TXN	GND	GND	DVI1_HPD	BITFAIL~	GND

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7.1.15 Signal Descriptions

Table 7-16 Backplane Connector Signal Descriptions

Name	Description
VS1, VS2, VS3	VPX Vs1 (+12 V), Vs2 (+12 V) and Vs3 (+5 V) power inputs. See the Electrical Specifications section for more details
P3V3_AUX	VPX +3.3 V DC auxiliary power input. See the Electrical Specifications section for more details
GND	The DC voltage reference for the system
None	No signals specified in VPX specification
P12V_AUX, N12V_AUX	VPX +12 V DC and -12 V DC auxiliary power inputs. Connected to the PMC/XMC sites, otherwise unused by the SBC624
GA[4:0]~	Geographical Addressing bits. These are used to set the slave address of the SBC624. The settings are reflected in the FPGA VPX Geographical Address Register (offset 0x605)
GAP~	Geographical addressing parity bit input. The sum of all GA bits, including the parity bit, should be an odd number. The setting is reflected in the FPGA VPX Geographical Address Register (offset 0x605)
IPMB_A/B_CLK, IPMB_A/B_DATA	System Management bus A and bus B clock and data. Connected to the BMC via I^2C buffers. These allow access to certain on-board resources from an external I^2C master
SYSRESET~	System Reset. When this is low, it causes the system to be reset. The SBC624 generates SYSREST~ when it is configured as System Controller
NVMRO	Non-Volatile Memory Read Only. When this signal is high, all on-board Non-volatile memory is write-protected. This signal can be externally pulled low (using a link on the backplane or RTM) or driven low under software control by the SBC624 if configured as System Controller. The state is shown in the Board Configuration Register 2 (register offset 0x603)
JTAG_TCLK, JTAG_TDO, JTAG_TDI, JTAG_TMS, JTAG_TRST~	JTAG Test Clock, Test Data Out (Tx from SBC624), Test Data In (Rx to SBC624 from test device), Test Mode Select and Test Reset
VBAT	3 V battery supply input to back up RTC
10GIBnTP/Ny, 10GIBnRP/Ny	Dataplane transmit and receive differential pairs. Software configurable as either 10GBaseKX4 Ethernet (10G) or Infiniband (IB). Configured as two x4 ports: n (port) = 1 or 2, y (lane) = 0 to 3
PCIE_TXnP/N, PCIE_RXnP/N	PCIe transmit and receive differential pairs
EPCLOCK1P/N EPCLOCK2P/N	OpenVPX Expansion Plane clock 1 and 2. See the Expansion Plane Fabric section for more details. Not connected by default.
SATAn_TXP/N	SATA interface n (n = 0, 1 or 4) transmit differential pair. From SBC624 to external SATA device. Ports SATA0 and SATA1 are Gen3 capable; port SATA4 is Gen2 capable
SATAn_RXP/N	SATA interface n (n = 0, 1 or 4) receive differential pair. From external SATA device to SBC624. Ports SATA0 and SATA1 are Gen3 capable; port SATA4 is Gen2 capable
USBn_P/N, USBn_POWER	USB port n (n = 0 to 3, 10, 11) differential pair and power
GPIO[7:0]	GPIO
ETH0_xP/N	Gigabit Ethernet channel 0 signal x (x = 0 to 3) differential pair. 10/100/1000BaseT operation
ETH1_xP/N	Gigabit Ethernet channel 1 signal x (x = 0 to 3) differential pair. 10/100/1000BaseT operation. This port is not available when the ETH1 Routing Link (E104) is fitted
ETHn_RP/N, ETHn_TP/N	Gigabit Ethernet channel n (n = 2 or 3) receive and transmit differential pairs. 10/100/1000Base-BX operation, for inter-board backplane connection only
COMn_TXD/TXD_A	Serial COM port n (n = 1 or 2) Transmit Data signal (RS232 mode) or Transmit Data A signal (RS422 mode)
COMn_RXD/RXD_A	Serial COM port n (n = 1 or 2) Receive Data signal (RS232 mode) or Receive Data A signal (RS422 mode)
COMn_RTS/TXD_B	Serial COM port n (n = 1 or 2) Ready To Send flow control signal (RS232 mode) or Transmit Data B signal (RS422 mode)
COMn_CTS/RXD_B	Serial COM port n (n = 1 or 2) Clear To Send flow control signal (RS232 mode) or Receive Data B signal (RS422 mode)

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Name	Description
COMn_DTR	Serial COM port n (n = 1 or 2) Data Terminal Ready flow control signal (RS232 mode). This pin has no function in RS422 mode
COMn_DSR	Serial COM port n (n = 1 or 2) Data Set Ready flow control signal (RS232 mode). This pin has no function in RS422 mode
COMn_DCD	Serial COM port n (n = 1 or 2) Data Carrier Detect flow control signal (RS232 mode). This pin has no function in RS422 mode
COMn_RI	Serial COM port n (n = 1 or 2) Ring Indicator flow control signal (RS232 mode). This pin has no function in RS422 mode
BITFAIL~	Open drain BIT Fail drive for system level BIT Fail
PMCn_IO_[64:01]	PMC I/O connections from the J14 connector (n = 1) or J24 connector (n = 2). For mezzanine site 1, I/O signals on P3 are configurable between PMC and XMC by a build option
XMC1_IO_xxx	XMC I/O connections from the J16 connector. For mezzanine site 1, I/O signals on P3 are configurable between PMC and XMC by a build option
XMC2_IO_xxx/ DVI2_xxx	XMC I/O connections from the J26 connector that are shared with DVI port 2 signals (build option dependent)
XMC2_IO_xxx/NC	XMC I/O connections from the J26 connector. These signals are not available when the board is configured for DVI2 access
PSU_SEQ_IN	Inter-board PSU Sequencing input. The board will not start its on-board supplies whilst this signal is driven low. This can be connected to the PSU_SEQ_OUT signal of another board to allow the boards to power up in sequence. A 500 ms timeout applies, in case the preceding board has a fault. This pin may be left unconnected if inter-board power sequencing is not required
PSU_SEQ_OUT	Inter-board PSU Sequencing output. Driven low when the backplane supplies are out of specification and held low until all on-board supplies are in specification
SYSCON~	Pulled low by the backplane to indicate that the board is the VPX System Controller. The state is shown in the Board Configuration Register 2 (register offset 0x603)
AUX_CLK_P/N	OpenVPX Auxiliary Clock differential signals
REF_CLK_P/N	OpenVPX Reference Clock differential signals
GDISC1	OpenVPX Gdiscrete1 signal
INTRUDER_DTECT~	Intruder detect input signal. This pin can be left unconnected if this functionality is not required.
MSKRST~	OpenVPX Maskable Reset signal. Pulling this input low for a minimum of 10 ms will cause a hard reset to the SBC624 unless it is masked (unmasked by default). This pin can also be driven by the SBC624. See Control Register 4 (offset 0x625) for details
KBCLK, KBDAT	PS/2 Keyboard clock and data lines
MSCLK, MSDAT	PS/2 Mouse clock and data lines
DVIn_DDC_DATA, DVIn_DDC_CLK, DVIn_TXnP/N, DVIn_TXCP/N, DVIn_HPD	DVI Display Data Channel Data signal, Display Data Channel clock output, Transmit data bit n (n = 0 to 2) differential signal pairs, Transmit clock differential signal pair Hot Plug Detect input signal
FASTSTART~	BIT Fast Start input. When asserted low by the system, BIT will run in Fast Start mode. See the BIT Control and Status Register (register offset 0x629) for more information on the operation of this signal
VGA_DDC_CLK, VGA_DDC_DATA, VGA_VSYNC, VGA_HSYNC, VGA_RED, VGA_BLUE, VGA_GREEN	VGA Display Data Channel Clock output, Display Data Channel Data signal, Horizontal synchronization output, Vertical synchronization output, Red signal, Blue signal and Green signal

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Name	Description
HDA_SDO, HDA_RST~, HDA_BCLK, HDA_SYNC, HDA_SDIN0	High Definition Audio Serial Data Out, Reset, Bus Clock, Synchronization, and Serial Data In. For connection to an external CODEC
SPKR	External speaker output
RTM_RST~	External hard reset input. Pulling this input low will cause a hard reset to the board. Any switch logic should be debounced externally
N/C	No connection

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7.2 PMC Connectors

Table 7-17 Jn1 to Jn3 Pin Assignments

7.2.1 Jn1 7.2.2 Jn2 7.2.3 Jn3

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	TCK	2	N12V_AUX	1	P12V_AUX	2	TRST~	1	N/C	2	GND
3	GND	4	INTA~	3	TMS	4	TDO	3	GND	4	C/BE7~
5	INTB~	6	INTC~	5	TDI	6	GND	5	C/BE6~	6	C/BE5~
7	BUSMODE1~	8	P5V	7	GND	8	N/C	7	C/BE4~	8	GND
9	INTD~	10	N/C	9	N/C	10	N/C	9	VIO	10	PAR64
11	GND	12	N/C	11	BUSMODE2	12	P3V3	11	AD63	12	AD62
13	CLK	14	GND	13	RESET_IN~	14	BUSMODE3	13	AD61	14	GND
15	GND	16	GNT_A~	15	P3V3	16	BUSMODE4	15	GND	16	AD60
17	REQ_A~	18	P5V	17	N/C	18	GND	17	AD59	18	AD58
19	VIO	20	AD31	19	AD30	20	AD29	19	AD57	20	GND
21	AD28	22	AD27	21	GND	22	AD26	21	VIO	22	AD56
23	AD25	24	GND	23	AD24	24	P3V3	23	AD55	24	AD54
25	GND	26	C/BE3~	25	IDSELA	26	AD23	25	AD53	26	GND
27	AD22	28	AD21	27	P3V3	28	AD20	27	GND	28	AD52
29	AD19	30	P5V	29	AD18	30	GND	29	AD51	30	AD50
31	VIO	32	AD17	31	AD16	32	C/BE2~	31	AD49	32	GND
33	FRAME~	34	GND	33	GND	34	IDSELB	33	GND	34	AD48
35	GND	36	IRDY~	35	TRDY~	36	P3V3	35	AD47	36	AD46
37	DEVSEL~	38	P5V	37	GND	38	STOP~	37	AD45	38	GND
39	XCAP	40	LOCK~	39	PERR~	40	GND	39	VIO	40	AD44
41	N/C	42	N/C	41	P3V3	42	SERR~	41	AD43	42	AD42
43	PAR	44	GND	43	C/BE1~	44	GND	43	AD41	44	GND
45	VIO	46	AD15	45	AD14	46	AD13	45	GND	46	AD40
47	AD12	48	AD11	47	M66EN	48	AD10	47	AD39	48	AD38
49	AD09	50	P5V	49	AD08	50	P3V3	49	AD37	50	GND
51	GND	52	C/BE0~	51	AD07	52	REQ_B~	51	GND	52	AD36
53	AD06	54	AD05	53	P3V3	54	GNT_B~	53	AD35	54	AD34
55	AD04	56	GND	55	N/C	56	GND	55	AD33	56	GND
57	VIO	58	AD03	57	N/C	58	EREADY	57	VIO	58	AD32
59	AD02	60	AD01	59	GND	60	RESET_OUT~	59	N/C	60	N/C
61	AD00	62	P5V	61	ACK64~	62	P3V3	61	N/C	62	GND
63	GND	64	REQ64~	63	GND	64	MONARCH~	63	GND	64	N/C

CAUTION

Do not fit a PMC that requires more than 8 Watts from the 3.3 V supply.

N = 1 or 2 for PMC sites 1 or 2.

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7.2.4 Jn4

Table 7-18 Jn4 Pin Assignments

Pin	Signal	Pin	Signal
1	PMCn_IO_01	2	PMCn_IO_02
3	PMCn_IO_03	4	PMCn_IO_04
5	PMCn_IO_05	6	PMCn_IO_06
7	PMCn_IO_07	8	PMCn_IO_08
9	PMCn_IO_09	10	PMCn_IO_10
11	PMCn_IO_11	12	PMCn_IO_12
13	PMCn_IO_13	14	PMCn_IO_14
15	PMCn_IO_15	16	PMCn_IO_16
17	PMCn_IO_17	18	PMCn_IO_18
19	PMCn_IO_19	20	PMCn_IO_20
21	PMCn_IO_21	22	PMCn_IO_22
23	PMCn_IO_23	24	PMCn_IO_24
25	PMCn_IO_25	26	PMCn_IO_26
27	PMCn_IO_27	28	PMCn_IO_28
29	PMCn_IO_29	30	PMCn_IO_30
31	PMCn_IO_31	32	PMCn_IO_32
33	PMCn_IO_33	34	PMCn_IO_34
35	PMCn_IO_35	36	PMCn_IO_36
37	PMCn_IO_37	38	PMCn_IO_38
39	PMCn_IO_39	40	PMCn_IO_40
41	PMCn_IO_41	42	PMCn_IO_42
43	PMCn_IO_43	44	PMCn_IO_44
45	PMCn_IO_45	46	PMCn_IO_46
47	PMCn_IO_47	48	PMCn_IO_48
49	PMCn_IO_49	50	PMCn_IO_50
51	PMCn_IO_51	52	PMCn_IO_52
53	PMCn_IO_53	54	PMCn_IO_54
55	PMCn_IO_55	56	PMCn_IO_56
57	PMCn_IO_57	58	PMCn_IO_58
59	PMCn_IO_59	60	PMCn_IO_60
61	PMCn_IO_61	62	PMCn_IO_62
63	PMCn_IO_63	64	PMCn_IO_64

n = 1 or 2 for PMC sites 1 or 2.

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7.2.5 Signal Descriptions

Table 7-19 PMC Signal Descriptions

Name	Description
AD[63:0]	Address/Data bits. Multiplexed address and data bus
C_BE[7:0]	Command/Byte Enables. During the address phase, these signals specify the type of cycle to carry out on the PCI bus. During the data phase the signals are byte enables that specify the active bytes on the bus
FRAME~	FRAME. Driven low by the current master to signal the start and duration of an access
DEVSEL~	Device Select. Driven low by a PCI agent to signal that it has decoded its address as the target of the current access
PAR	Parity. Parity protection bit for AD0 to AD31 and BE0 to BE3
PARR64	Parity. Parity protection bit for AD32 to AD63 and BE4 to BE7
IRDY~	Initiator Ready. Driven low by the initiator to signal its ability to complete the current data phase
LOCK~	LOCK. Driven low to indicate an atomic operation that may require multiple transactions to complete
BUSMODE1~	Bus Mode 1. Driven low by a PMC if it supports the current bus mode. Used to detect the presence of a PMC on the site
BUSMODE[4:2]	Bus mode. Driven by the host to indicate the bus mode. On the SBC624 this is always PCI. BUSMODE2 is connected to a 4.7 kΩ pull-up. BUSMODE3 and BUSMODE4 are pulled down to GND
RESET_IN~	Reset. Driven low to reset the PCI bus
TRDY~	Target Ready. Driven low by the current target to signal its ability to complete the current data phase
PERR~	Parity Error. Driven low by a PCI agent to signal a parity error
SERR~	System Error. Driven low by a PCI agent to signal a system error
STOP~	STOP. Driven low by a PCI target to signal a disconnect or target-abort
INT[A:D]~	Interrupt lines. Level-sensitive, active-low interrupt requests (rotated between PMC sites)
CLK	Clock. All PCI bus signals except RST~ are synchronous to this clock
REQ_A/B~	Request. Driven low by a PCI agent to request ownership of the PCI bus
GNT_A/B~	Grant. Driven low by the arbiter to grant PCI bus ownership to a PCI agent
IDSELA/B	Initialization Device Select. PCI Device chip select used during PCI configuration cycles
REQ64~	Request 64 Bit. Driven low by a PCI master to request 64-bit transfer
ACK64~	Acknowledge 64 Bit. Driven low by PCI agent in response to REQ64
EREADY	The PMC uses this signal to indicate when it is ready to be enumerated by the PCI software. The setting is reflected in the Board Configuration Register 2 (offset 0x603)
RESET_OUT~	Monarch PMC Reset output. Not supported on SBC624
MONARCH~	Monarch mode is not supported on the SBC624. This signal is pulled high
TCK	Test Clock. Clock for the PMC JTAG
TMS	Test Mode Select. Select Test Mode for PMC JTAG
TRST~	Test Reset. Reset any PMC JTAG devices
TDI	Test Data In. Input data for PMC JTAG chain
TDO	Test Data Out. Data from a PMC JTAG chain
P5V	+5 V DC power
P3V3	The 3.3 V pins are connected to the SBC624 main 3.3V switched supply
GND	The DC voltage reference for the system
VIO	The supply rail for the PCI bus I/O voltage. For I/O signaling only, *not* main supply
XCAP	PCI-X Capability detect. Used to determine whether a PMC is PCI-X capable
N12V_AUX	-12 Volts DC power from the backplane
P12V_AUX	+12 Volts DC power from the backplane
M66EN	66 MHz Operation. Connected to GND by the host for 33 MHz operation or left high for 66 MHz
PMCn_IO_xx	Rear I/O connection from PMC site n (n = 1 or 2)

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7.3 XMC Connectors

7.3.1 J15

J15 supplies the PCI Express interface signals for XMC site 1.

Table 7-20 J15 Pin Assignments

Pin	A	B	C	D	E	F
1	PCIE_TX0P	PCIE_TX0N	P3V3	PCIE_TX1P	PCIE_TX1N	VPWR
2	GND	GND	JTAG_TRST~	GND	GND	RESET_IN~
3	PCIE_TX2P	PCIE_TX2N	P3V3	PCIE_TX3P	PCIE_TX3N	VPWR
4	GND	GND	JTAG_TCK	GND	GND	RESET_OUT~
5	PCIE_TX4P	PCIE_TX4N	P3V3	PCIE_TX5P	PCIE_TX5N	VPWR
6	GND	GND	JTAG_TMS	GND	GND	P12V_AUX
7	PCIE_TX6P	PCIE_TX6N	P3V3	PCIE_TX7P	PCIE_TX7N	VPWR
8	GND	GND	JTAG_TDI	GND	GND	N12V_AUX
9	Reserved	Reserved	Reserved	Reserved	Reserved	VPWR
10	GND	GND	JTAG_TDO	GND	GND	GA0
11	PCIE_RX0P	PCIE_RX0N	MBIST~	PCIE_RX1P	PCIE_RX1N	VPWR
12	GND	GND	GA1	GND	GND	PRESENT~
13	PCIE_RX2P	PCIE_RX2N	P3V3_AUX	PCIE_RX3P	PCIE_RX3N	VPWR
14	GND	GND	GA2	GND	GND	SM_DATA
15	PCIE_RX4P	PCIE_R46N	Reserved	PCIE_RX5P	PCIE_RX5N	VPWR
16	GND	GND	NVMRO	GND	GND	SM_CLK
17	PCIE_RX6P	PCIE_RX6N	Reserved	PCIE_RX7P	PCIE_RX7N	Reserved
18	GND	GND	Reserved	GND	GND	Reserved
19	REFCLK_P	REFCLK_N	Reserved	N/C (WAKE~)	N/C (ROOT~)	Reserved

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7.3.2 J25

J25 supplies the PCI Express interface signals for XMC site 2. The PCIe bus connected to this site is x4 only, so PCIe lanes 3 to 7 are not connected.

Table 7-21 J25 Pin Assignments

Pin	A	B	C	D	E	F
1	PCIE_TX0P	PCIE_TX0N	P3V3	PCIE_TX1P	PCIE_TX1N	VPWR
2	GND	GND	JTAG_TRST~	GND	GND	RESET_IN~
3	PCIE_TX2P	PCIE_TX2N	P3V3	PCIE_TX3P	PCIE_TX3N	VPWR
4	GND	GND	JTAG_TCK	GND	GND	RESET_OUT~
5	N/C	N/C	P3V3	N/C	N/C	VPWR
6	GND	GND	JTAG_TMS	GND	GND	P12V_AUX
7	N/C	N/C	P3V3	N/C	N/C	VPWR
8	GND	GND	JTAG_TDI	GND	GND	N12V_AUX
9	Reserved	Reserved	Reserved	Reserved	Reserved	VPWR
10	GND	GND	JTAG_TDO	GND	GND	GA0
11	PCIE_RX0P	PCIE_RX0N	MBIST~	PCIE_RX1P	PCIE_RX1N	VPWR
12	GND	GND	GA1	GND	GND	PRESENT~
13	PCIE_RX2P	PCIE_RX2N	P3V3_AUX	PCIE_RX3P	PCIE_RX3N	VPWR
14	GND	GND	GA2	GND	GND	SM_DATA
15	N/C	N/C	Reserved	N/C	N/C	VPWR
16	GND	GND	NVMRO	GND	GND	SM_CLK
17	N/C	N/C	Reserved	N/C	N/C	Reserved
18	GND	GND	Reserved	GND	GND	Reserved
19	REFCLK_P	REFCLK_N	Reserved	N/C (WAKE~)	N/C (ROOT~)	Reserved

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7.3.3 J16

J16 provides the rear I/O connectivity for XMC1.

Table 7-22 J16 Pin Assignments

Pin	A	B	C	D	E	F
1	XMC1_IO_A01	XMC1_IO_B01	XMC1_IO_C01	XMC1_IO_D01	XMC1_IO_E01	XMC1_IO_F01
2	GND	GND	XMC1_IO_C02	GND	GND	XMC1_IO_F02
3	XMC1_IO_A03	XMC1_IO_B03	XMC1_IO_C03	XMC1_IO_D03	XMC1_IO_E03	XMC1_IO_F03
4	GND	GND	XMC1_IO_C04	GND	GND	XMC1_IO_F04
5	XMC1_IO_A05	XMC1_IO_B05	XMC1_IO_C05	XMC1_IO_D05	XMC1_IO_E05	XMC1_IO_F05
6	GND	GND	XMC1_IO_C06	GND	GND	XMC1_IO_F06
7	XMC1_IO_A07	XMC1_IO_B07	XMC1_IO_C07	XMC1_IO_D07	XMC1_IO_E07	XMC1_IO_F07
8	GND	GND	XMC1_IO_C08	GND	GND	XMC1_IO_F08
9	XMC1_IO_A09	XMC1_IO_B09	XMC1_IO_C09	XMC1_IO_D09	XMC1_IO_E09	XMC1_IO_F09
10	GND	GND	XMC1_IO_C10	GND	GND	XMC1_IO_F10
11	XMC1_IO_A11	XMC1_IO_B11	XMC1_IO_C11	XMC1_IO_D11	XMC1_IO_E11	XMC1_IO_F11
12	GND	GND	XMC1_IO_C12	GND	GND	XMC1_IO_F12
13	XMC1_IO_A13	XMC1_IO_B13	XMC1_IO_C13	XMC1_IO_D13	XMC1_IO_E13	XMC1_IO_F13
14	GND	GND	XMC1_IO_C14	GND	GND	XMC1_IO_F14
15	XMC1_IO_A15	XMC1_IO_B15	XMC1_IO_C15	XMC1_IO_D15	XMC1_IO_E15	XMC1_IO_F15
16	GND	GND	XMC1_IO_C16	GND	GND	XMC1_IO_F16
17	XMC1_IO_A17	XMC1_IO_B17	XMC1_IO_C17	XMC1_IO_D17	XMC1_IO_E17	XMC1_IO_F17
18	GND	GND	XMC1_IO_C18	GND	GND	XMC1_IO_F18
19	XMC1_IO_A19	XMC1_IO_B19	XMC1_IO_C19	XMC1_IO_D19	XMC1_IO_E19	XMC1_IO_F19

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7.3.4 J26

J26 provides the rear I/O connectivity for XMC2. If the SBC624 is configured for additional DVI video, this connector is not fitted.

Table 7-23 J26 Pin Assignments

Pin	A	B	C	D	E	F
1	N/C	N/C	N/C	N/C	N/C	N/C
2	GND	GND	N/C	GND	GND	N/C
3	N/C	N/C	N/C	N/C	N/C	N/C
4	GND	GND	N/C	GND	GND	N/C
5	XMC2_IO_A05	XMC2_IO_B05	N/C	XMC2_IO_D05	XMC2_IO_E05	N/C
6	GND	GND	N/C	GND	GND	N/C
7	XMC2_IO_A07	XMC2_IO_B07	N/C	XMC2_IO_D07	XMC2_IO_E07	N/C
8	GND	GND	N/C	GND	GND	N/C
9	XMC2_IO_A09	XMC2_IO_B09	N/C	XMC2_IO_D09	XMC2_IO_E09	N/C
10	GND	GND	N/C	GND	GND	N/C
11	N/C	N/C	N/C	N/C	N/C	N/C
12	GND	GND	N/C	GND	GND	N/C
13	N/C	N/C	N/C	N/C	N/C	N/C
14	GND	GND	N/C	GND	GND	N/C
15	XMC2_IO_A15	XMC2_IO_B15	N/C	XMC2_IO_D15	XMC2_IO_E15	N/C
16	GND	GND	N/C	GND	GND	N/C
17	XMC2_IO_A17	XMC2_IO_B17	N/C	XMC2_IO_D17	XMC2_IO_E17	N/C
18	GND	GND	N/C	GND	GND	N/C
19	XMC2_IO_A19	XMC2_IO_B19	N/C	XMC2_IO_D19	XMC2_IO_E19	N/C

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7.3.5 Signal Descriptions

Table 7-24 XMC Signal Descriptions

Name	Description
PCIE_TX[7:0]P/N	PCI Express Transmit Differential Pairs (from XMC to SBC624)
PCIE_RX[7:0]P/N	PCI Express Receive Differential Pairs (from SBC624 to XMC)
REFCLK_P/N	PCI Express Reference Clock. 100 MHz Differential clock to XMC
PRESENT~	XMC Present. Pulled low by the XMC to allow the SBC624 to detect if an XMC is fitted
RESET_IN~	XMC Reset In. Reset driven from the SBC624 to the XMC
RESET_OUT~	XMC Reset Out. Reset signal driven by the XMC to the SBC624 (from a front-panel switch for example)
SM_DATA, SM_CLK	Data and Clock lines for a two-wire I^2C system management bus. Connected to the BMC
MBIST~	XMC Built-in Self-Test. This signal can be held low by the XMC to indicate that it is not yet ready to be enumerated by the root complex
GA[2:0]	Geographic Address. Used to identify the address of the XMC on a shared I^2C bus (GA of 000_b for XMC site 1 and 001_b for XMC site 1)
NVMRO	Non-Volatile Memory Read Only. Used to write protect any non-volatile memory on the XMC. Connected directly to the VPX backplane signal NVMRO
JTAG_TCK, JTAG_TMS, JTAG_TRST~, JTAG_TDI, JTAG_TDO	XMC JTAG Test Clock, Test Mode Select, Test Reset, Test Data In and Test Data Out
XMCn_IO_xxx	Rear I/O connection from XMC site n (n = 1 or 2)
P12V_AUX	+12 V auxiliary supply pins
N12V_AUX	-12 V auxiliary supply pins
P3V3	+3.3 V supply pins
P3V3_AUX	+3.3 V auxiliary supply pins
VPWR	This may be +5 V or 12 V depending on the SBC624 configuration
GND	Signal Ground
N/C	No connection

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7.4 J5 Header (XDP Processor Debug)

This is a 60-way Samtec: BSH-030-01-L-D-A header in accordance with the Intel Huron-River Debug Port Design Guide. It uses the Intel XDP standard pinout, allowing probes from various vendors to be used.

Table 7-25 J5 Pin Assignments

Pin	Board Signal	XDP Probe Signal	Pin	Board Signal	XDP Probe Signal
1	GND	GND	2	GND	GND
3	PREQ~	OBSFN_A0	4	N/C	OBSFN_C0
5	PRDY~	OBSFN_A1	6	N/C	OBSFN_C1
7	GND	GND	8	GND	GND
9	BPM(0)~	OBSDATA_A0	10	N/C	OBSDATA_C0
11	BPM(1)~	OBSDATA_A1	12	N/C	OBSDATA_C1
13	GND	GND	14	GND	GND
15	BPM(2)~	OBSDATA_A2	16	N/C	OBSDATA_C2
17	BPM(3)~	OBSDATA_A3	18	N/C	OBSDATA_C3
19	GND	GND	20	GND	GND
21	N/C	OBSFN_B0	22	N/C	OBSFN_D0
23	N/C	OBSFN_B1	24	N/C	OBSFN_D1
25	GND	GND	26	GND	GND
27	BPM(4)~	OBSDATA_B0	28	N/C	OBSDATA_D0
29	BPM(5)~	OBSDATA_B1	30	N/C	OBSDATA_D1
31	GND	GND	32	GND	GND
33	BPM(6)~	OBSDATA_B2	34	N/C	OBSDATA_D2
35	BPM(7)~	OBSDATA_B3	36	N/C	OBSDATA_D3
37	GND	GND	38	GND	GND
39	PWRGOOD	HOOK0	40	ITPCLK	ITPCLK/HOOK4
41	BP_PWRGD_RST~	HOOK1	42	ITPCLK~	ITPCLK~/HOOK5
43	P1V05	VCC_OBS_AB	44	P1V05	VCC_OBS_CD
45	CPU_CFG(0)	HOOK2	46	RESET~	HOOK6/RESET~
47	SYS_PWROK	HOOK3	48	DBR~	HOOK7/DBR~
49	GND	GND	50	GND	GND
51	SDA	SDA	52	CPU_TDO	TDO
53	SCL	SCL	54	CPU_TRST~	TRST~
55	N/C	N/C	56	CPU_TDI	TDI
57	CPU_TCK	TCK0	58	CPU_TMS	TMS
59	GND	GND	60	GND	GND

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7.5 P10 Connector (TAC)

This 80-way Molex connector (where fitted) is for Factory/Field Application Engineer use only. It provides an interface between the TAC and on-board programmable devices.

7.6 Front I/O Connectors

These connectors are available on air-cooled build levels (levels 1 to 3) only.

7.6.1 J1 (RJ45)

This is provided to connect to Ethernet channel 1. ETH1 is only connected when the ETH1 Routing Link (E104) is fitted bit or D4 in Control Register 5 (register offset 0x626) is set, which may be done via a BIOS set-up screen.

Table 7-26 J1 Pin Assignments

Pin	Signal
1	ETH1_0P
2	ETH1_0N
3	ETH1_1P
4	ETH1_2P
5	ETH1_2N
6	ETH1_1N
7	ETH1_3P
8	ETH1_3N

Erratum October 2013
Pin assignments corrected.

7.6.2 J2 (USB)

This connector provides a type A connector for access to USB port 9.

Table 7-27 J2 Pin Assignments

Pin	Signal
1	USB9_PWR
2	USB9_N
3	USB9_P
4	GND

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7.6.3 J3 (Serial Debug)

This Harting 27-21-121-8000-type connector provides access to either COM3 (the default) or COM1, depending on the COM1 Routing Link (E103) and bit D5 in Control Register 5 (register offset 0x626), which may be set in a BIOS set-up screen.

Table 7-28 J3 Pin Assignments

Pin	COM3 Signal (RS232)	COM3 Signal (RS422)	COM1 Signal (RS232)	COM1 Signal (RS422)
A1	RXD	RXD_A	RXD	RXD_A
A2	RTS	TXD_B	RTS	TXD_B
B1	TXD	TXD_A	TXD	TXD_A
B2	N/C		RI	
C1	N/C		N/C	
C2	GND		GND	
D1	DTR		DTR	
D2	CTS	RXD_B	CTS	RXD_B
E1	DSR		DSR	
E2	DCD		DCD	

An adapter cable is available to convert this pinout to a standard 9-way D-type connector. Contact the factory for more details.

7.6.4 J4 (DVI)

This mini-HDMI type connector provides access to the second digital video port. This port can be configured in software to be DVI or HDMI.

Table 7-29 J4 Pin Assignments

Pin	Signal	Pin	Signal
1	GND	11	DVI2_TXCP
2	DVI2_TX2P	12	DVI2_TXCN
3	DVI2_TX2N	13	GND
4	GND	14	N/C
5	DVI2_TX1P	15	DVI2_DDC_CLK
6	DVI2_TX1N	16	DVI2_DDC_DATA
7	GND	17	N/C
8	DVI2_TX0P	18	P5V
9	DVI2_TX0N	19	HPD (Hot Plug Detect)
10	GND		

The connector can easily be converted to standard HDMI or DVI connectors using commercially available cables and adapters. Abaco can provide a mini-HMDI to full HMDI adapter cable. Contact the factory for more details.

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A • Specifications

A.1 Technical Specification

Table A-1 Technical Data

Features	Details	Comments
Processor	Core i7 dual/quad core	Various Intel SKUs supported
RAM	Up to 16 Gbytes DDR3 SDRAM with ECC	Dual memory controllers running at up to 1333 MHz data rate
NOVRAM	512 KBytes User/512 KBytes System	Non-volatile storage for data that must not be lost when power is removed
NAND Flash	Up to 64 Gbytes	SATA Solid State Drive. Maximum capacity dependent on available technology
Ethernet ports	2x10/100/1000BaseT and 2x1000BaseBX	
Serial ports	3xRS232/422/485 Async	Two ports available at backplane, one port available at the front panel
USB2.0	Up to 7 ports	Six backplane, 1 front
SATA	3 backplane channels	2 x Gen3/2/1, 1 x Gen2/1
Discrete Digital I/O	Up to 8 bits, TTL-compatible	Able to generate edge- or level-triggered interrupts
Fabrics	2x10G Ethernet (KX4) or 2xInfiniband, 2x1000BaseBX	
PCI Express	16 lanes on VPX P2	2.5 or 5 GHz. Configurable as one x16, two x8 or four x4 ports. One NT port available
Video	2xDVI/HDMI and 1xVGA	Second DVI channel is available either as front I/O or rear I/O depending on the build configuration
Audio	High Definition Audio to rear	External CODEC required
Keyboard/Mouse	PS/2	To rear
PMC/XMC sites	Two PMC/XMC Sites	64-bit PCI-X interface at up to 133 MHz. x8 PCI Express interface Options for full PMC or full XMC I/O from site 1, full PMC only from site 2
Thermal sensors	Board ambient, CPU die, PCIe Switch and Ethernet Controller die temperatures	
Timers	3x82C54-equivalent (internal to PCH) 2x32-bit timers	
Watchdog timer	32-bit timer	Programmable reset threshold
Real-Time Clock	Time Of Day/Calendar	1 second resolution. Standby power may be connected from the VBAT pin to maintain data during power down
ETI	Quarter second resolution	Logs the total accumulated time the board has been powered, and the number of power cycles
System Management	BMC	IPMI compliant
Key generation	Trusted Platform Monitor	
JTAG Interface	On-board Scanbridge	Access from J0. TAC also provides headers for factory test and software debug purposes
Front I/O	1 x USB, 1 x Gigabit Ethernet, 1 x Serial, 1 x DVI/HDMI	

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A.2 Electrical Specification

A.2.1 Voltage Supply Requirements

The VPX Vs1/Vs2 (+12V), Vs3 (+5V) and 3V3_AUX supplies are required. These supplies must remain within the specified limits as defined below. If any of these supplies is outside of these specifications at power-up, then the SBC624 will fail to start. If these supplies fall outside of these limits during a powered state, then the SBC624 will be held in reset and all on-board supplies will be shut down.

The VPX ±12V_AUX supplies are not used on the SBC624 and are not monitored but are connected to the PMC/XMC sites.

Table A-2 Voltage Supply Requirements

Supply	Minimum	Nominal	Maximum
VS1, VS2	+11.4 V	+12.0 V	+12.6 V
VS3	+4.88 V	+5.0 V	+5.25 V
3.3V_AUX	+3.14 V	+3.3 V	+3.46 V
+12V_AUX	+11.4 V	+12.0 V	+12.6 V
-12V_AUX	-11.4 V	-12.0 V	-12.6 V
VBAT	+3.14 V	+3.3 V	+3.46 V



WARNING

Do not exceed the maximum rated input voltages or apply reversed bias to the assembly. If such conditions occur, toxic fumes may be produced due to the destruction of components.

A.2.2 Current Consumption

The SBC624 is estimated to dissipate a maximum of 80 W from the power supply when operating with four processing cores at 2.1 GHz, with no mezzanine cards fitted.

Current consumption values for SBC624 are shown below. These are given at cold-wall temperatures of +25°C and +85°C in a conduction-cooled environment



TIP

The figures quoted below represent the requirements of the the SBC624 under certain conditions. When specifying system power supply parameters, you are strongly recommended to allow for higher requirements to allow for usage variation and technology insertion.

Table A-3 Current Consumption – 12 V Rails (Vs1 and Vs2)

Temperature	Operation	12V Current (A)		
		Core-i7-2610UE (DC, 1.5 GHz, 17 W TDP)	Core-i7-2655LE (DC, 2.2 GHz, 25 W TDP)	Core-i7-2715QE (QC, 2.1 GHz, 45 W TDP)
+25°C	Typical	TBA	3.0	3.0
	Maximum	TBA	4.5	6.5
+85°C	Typical	TBA	3.5	3.5
	Maximum	TBA	5.0	5.0

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Table A-4 Current Consumption – 5 V Rail (Vs3), All Variants

Temperature (°C)	Operation	5V Current (A)
All	Typical	0.75
	Maximum	1

Table A-5 Current Consumption – P3V3_AUX, All Variants

Temperature (°C)	Operation	P3V3_AUX Current (A)
All	Typical	0.5
	Maximum	0.5

This power was measured under the following conditions:

Table A-6 Power Measurement Conditions

Operation	Hardware connections	Software
Typical	• Gigabit Ethernet x2 (linked @ 1000baseT) • VGA monitor • COM1 serial port • 1x external SATA Gen2 drive	Windows 7 - idle
Maximum	• USB keyboard (including a USB1.0 hub) • USB mouse • No backplane fabric connected • No mezzanine sites populated	Proprietary test software configured to exercise all main functional blocks simultaneously. CPU usage @ 100%. Runs under Windows 7

NOTE

When using PMCs, ensure that they do not cause the specified maximum supply current to be exceeded. It may not be possible to support all combinations of PMCs within this limit.

A.2.3 3.3 V Auxiliary Supply

The following functions are powered from the 3.3 V Auxiliary supply (VPX P3V3_AUX line):

- Board Management Microcontroller and System Management bus
- Power supply sequencing/monitoring
- BIT Fail LED
- Real Time Clock (this can also be powered from the VPX VBAT supply)
- PCH resume functions

NOTE

A standard SBC624 requires the Auxiliary supply to be present, otherwise it will not start up.

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A.3 Mechanical Specification

Table A-7 Mechanical Construction

Form Factor	6U, single slot
Weight	SBC624 Level 4-5 = 825 g SBC624 Level 1-3 = 750 g
Dimensions	The air-cooled SBC624 is constructed on a multi-layer Eurocard and conforms to the dimensions specified in IEEE1101.1. The conduction-cooled SBC624 is constructed on a multi-layer Eurocard and conforms to the dimensions specified in IEEE 1101.2 (0.8" pitch).

A.4 Reliability (MTBF)

The following table shows the predicted values for reliability as Mean Time Between Failures (MTBF) and failures per million hours (fpmh) for the SBC624-x112PP1Ax (see Product Codes for variant details).

Table A-8 Reliability (MTBF)

Environment	Fail Rate (fpmh)	MTBF (Hours)
Ground Benign 30°C	5.4622	183 075
Ground Fixed 40°C	24.3991	40 985
Ground Mobile 45°C	62.0989	16 103
Naval Sheltered 40°C	40.2016	24 875
Naval Unsheltered 45°C	86.2276	11 597
Airborne Inhabited Cargo 55°C	55.8861	17 894
Airborne Inhabited Fighter 55°C	77.4701	12 908
Airborne Uninhabited Cargo 70°C	122.7285	8148
Airborne Uninhabited Fighter 70°C	173.2094	5773
Airborne Rotary Wing 55°C	160.6818	6223
Space Flight 30°C	4.2629	234 584
Missile Flight 45°C	76.4116	13 087
Missile Launch 55°C	221.1092	4523

The predictions are carried out using MIL-HDBK-217F Notice 2, Parts Stress method in Relex. πQ values have been modified according to the ANSI/VITA51.1 Specification.

These failure rates are based only on the components and connectors fitted to the board at delivery and take no account of user fitted mezzanines.

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A.5 Environmental Specifications

A.5.1 Convection-cooled Boards

Table A-9 Convection-cooled Environmental Specifications

Build Style	Temperature (°C)	Vibration	Shock	Humidity	Comments
Standard (Level 1)	**Operating:** 0 to +55 with airflow of 300 lfm. **Storage:** -50 to +100	**Random:** 0.002g^2/Hz from 10 to 2000 Hz **Sine:** 2g from 5 to 500 Hz	20g peak sawtooth, 11 ms duration	Up to 95% RH	Commercial grade cooled by forced air, for use in benign environments and software development applications. Optional conformal coating
Extended Temperature (Level 2)	**Operating:** -20 to +65 with airflow of 300 lfm **Storage:** -50 to +100	**Random:** 0.002g^2/Hz from 10 to 2000 Hz **Sine:** 2g from 5 to 500 Hz	20g peak sawtooth, 11 ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	As Standard but conformally coated and temperature characterized
Rugged Air-cooled (Level 3)	**Operating:** -40 to +75 with airflow of 600 lfm **Storage:** -50 to +100	**Random:** 0.04g^2/Hz from 20 to 2000 Hz, with a flat response to 1000 Hz. 6db/Octave roll-off from 1000 to 2000 Hz.	20g peak sawtooth, 11 ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Wide temperature rugged, cooled by forced air. Conformally coated for additional protection

A.5.2 Conduction-cooled Boards

Table A-10 Conduction-cooled Environmental Specifications

Build Style	Temperature (°C)	Vibration	Shock	Humidity	Comments
Rugged Conduction-cooled (Level 4)	**Operating:** -40 to +75 at the thermal interface **Storage:** -50 to +100	**Random:** 0.1g^2/Hz from 15 to 2000 Hz per MIL-STD-810E Fig 514.4 – 8 for high performance aircraft. 12g RMS	40g peak sawtooth, 11 ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.
Rugged Conduction-cooled (Level 5)	**Operating:** -40 to +85 at the thermal interface **Storage:** -50 to +100	**Random**: 0.1g^2/Hz from 15 to 2000 Hz per MIL-STD-810E Fig 514.4 – 8 for high performance aircraft. 12g RMS	40g peak sawtooth, 11 ms duration	Up to 95% RH with varying temperature. 10 cycles, 240 hours	Designed for severe environment applications with high levels of shock and vibration, small space envelope and restricted cooling supplies. Conformally-coated as standard. Optional ESS.



NOTE

As shown above, the build level dictates the maximum ambient temperature at which the board can operate. As the temperature affects the CPU operating frequency, this means that for a given build level, a maximum CPU operating frequency is achievable. For more details, contact your nearest Abaco sales office or agent.

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A.6 Product Codes

Table A-11 Product Options

SBC624 -	X	X	X	X	X	X	X	X	X
Mechanics									
Software									
XMC Power									
PMC/XMC2 I/O Option									
PMC/XMC1 I/O Option									
NAND Flash (SSD)									
SDRAM									
Processor and Frequency									
Ruggedization Level									

1 = 0.8″ slot pitch, VITA 46
3 = 1″ slot pitch, VITA 46
6 = 1″ slot pitch, VITA 48, air-cooled
B = 0.85″ slot pitch with rear side covers for 2LM[a]

0 = BIOS only
1 = BIOS + BIT
2 = Reserved
3 = BIOS + VxWorks
4 = BIOS + BIT + VxWorks

1 = XMC1 5 V, XMC2 5 V
2 = XMC1 12 V, XMC2 5 V
3 = XMC1 5 V, XMC2 12 V
4 = XMC1 12 V, XMC2 12 V

P = PMC2 I/O 1-64 + XMC2 I/O 12d (P5w1-P64s+X12d)
V = DVI channel routed to P6. No XMC2 I/O (P5w1-P64s)

P = PMC1 I/O 1-64 + XMC1 I/O 12d (P3w1-P64s+X12d)
X = PMC1 I/O 1-9,11 + XMC1 I/O Full (P3w3-X38s+X8d+X12d)

0 = No Flash
1 = 4 Gbytes
2 = 8 Gbytes
3 = 16 Gbytes
4 = 32 Gbytes (as technology becomes available)
5 = 64 Gbytes (as technology becomes available)

1 = 4 Gbytes
2 = 8 Gbytes
3 = 16 Gbytes

1 = Dual core, core-i7 (ULV), 1.5 GHz
2 = Dual core, core-i7 (LV) 2.2 GHz
3 = Dual core, core-i5 (SV) 2.5 GHz
4 = Quad core, core-i7 (SV) 2.1 GHz

1 = Build level 1, 2 = Build level 2, 3 = Build level 3, 4 = Build level 4, 5 = Build level 5

Erratum October 2013
Corrected PMC/XMC I/O routing as per VITA 46.9

a. Build level 4 or 5 only.

See the Environmental Specifications section for more details on the build levels.

NOTES

The above table represents the available codes/variants at the time of writing. Contact your nearest Abaco sales office or agent for details of the latest codes/variants.

The build level dictates the maximum ambient temperature at which the board can operate. As the temperature affects the CPU operating frequency, this means that for a given build level, a maximum CPU operating frequency is achievable. For more details, contact your nearest Abaco sales office or agent.

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A.7 Software Support

Abaco's software strategy allows fully integrated system-level solutions to be realized easily and with confidence. Off-the-shelf, layered software modules deliver the most from low-level hardware features while exploiting the best high level debug and run-time functionality of popular COTS operating systems and communications modules.

The software products described below build on those available for previous generations of products, so providing a common interface for technology inserts.

The Abaco software strategy ensures that customers can develop market-leading products using the O/S and development environment best suited to their long term program requirements.

A.7.1 BIOS

The BIOS provides a foundation layer to interface between the raw board hardware, with its highly programmable device set-ups and flexibility, and the supported Operating Systems, which require a straight-forward booting and device interface model. Much of the board configuration can be altered by the user using BIOS set-up screens, and these settings are stored in non-volatile memory.

A.7.2 Built In Test

BIT probes from the lowest level of discrete on-board hardware up to Line Replaceable Unit level within a system, ensuring the highest degree of confidence in system integrity. BIT includes comprehensive configuration facilities, allowing automatic initialization tests to be defined for the desired mix of system functionality and options. Further tests can be invoked interactively, giving BIT a valuable role as a field service tool. Both object and source code products are available.

A.7.3 Background Condition Screening

BCS supplements the BIT initialization test coverage with further health screening that can co-exist with a standard COTS Operating System.

In contrast to a traditional BIT-style test, the intensity and coverage of which makes it destructive to operating systems, the configurable BCS package allows functions such as periodic check-summing, memory scrubbing, and others to be tailored for operation alongside the application in on-line conditions. Results are stored in Flash in the same format as BIT results. Code is available for reading out BIT/BCS results under LynxOS and VxWorks.

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A.8 I/O Modules

The SBC624 can be used with the VPX6UX604 or VPX6UX605 RTMs. More information about RTMs can be found in the VPX I/O Modules manual.

An additional MEZZIO module, MEZZIODVI, is required to access the second rear DVI/HDMI video port. This MEZZIO module fits onto the VPX6UX604 or VPX6UX605.



LINKS

VPX I/O Modules Hardware Reference Manual, publication number VPXIOM-0HH.

VPX6UX604 Hardware Reference Manual, publication number 522-9300527824-000.

VPX6UX605 Hardware Reference Manual, publication number VPX6UX605-HRM.

MEZZIODVI Hardware Reference Manual, publication number MEZZIODVI-HRM.

A.9 Test Access Card

The SBC624 supports the addition of a Test Access Card (TAC) to the front of the board. This card provides the following functions:

- SPI Flash to allow the board to boot from the TAC
- Memory SPD (Serial Presence Detect) EEPROMs
- I2C, SPI and LPC breakout headers
- Factory links and programming headers
- Other miscellaneous debug functions

The TAC is for factory and Field Application Engineer use only.

A.10 Cables

The following cables are available for use with the SBC624:

- A serial 9-way adapter cable (part number YLB-CR12-01) for use with the front panel J3 connector (only present on air-cooled build levels)
- A mini-HMDI to full HMDI adapter cable (part number C-CBL000243-001) for use with the front panel J4 connector (only present on air-cooled build levels)

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B • VPX6UX604 Port Mapping

The following table shows the SBC624 port to VPX6UX604 connector mapping:

Table B-1 Port to Connector Mapping

SBC624 Port	VPX6UX604 Connector	VPX6UX604 Connector	SBC624 Port
COM1	P8	P8	COM1
COM2	P9	P9	COM2
ETH0	J10	J1	USB11
ETH1	J2	J2	ETH1
USB0	J14	J3	USB10
USB1	J12	J4	DVI_1
USB2	J11	J5	VGA
USB3	J13	J6	SATA0
USB10	J3	J7	SATA4
USB11	J1	J8	XMC2/PMC2 I/O
SATA0	J6	J9	XMC1/PMC1 I/O
SATA1	J17	J10	ETH0
SATA4	J7	J11	USB2
DVI_1	J4	J12	USB1
VGA	J5	J13	USB3
XMC1/PMC1 I/O	J9	J14	USB0
XMC2/PMC2 I/O	J8	J17	SATA1

An additional MEZZIO module, MEZZIODVI, is required to access the rear DVI_2 port. This MEZZIO module fits onto the J8 connector.



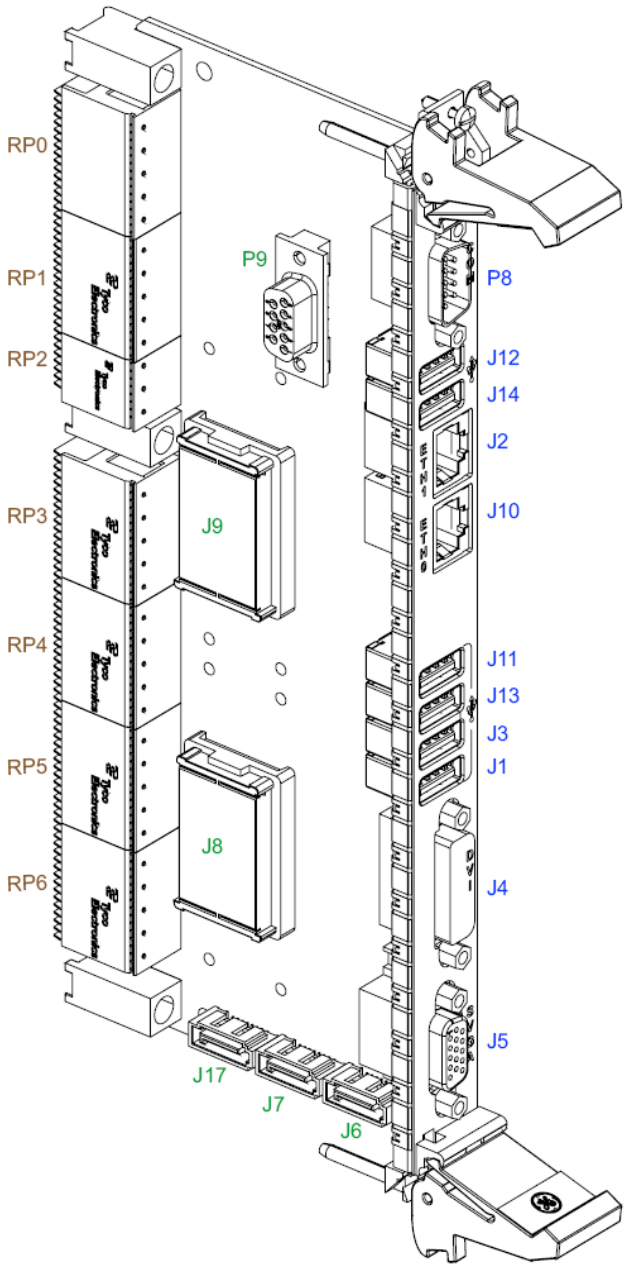
LINKS

VPX6UX604 Hardware Reference Manual, publication number 522-9300527824-000.

MEZZIODVI Hardware Reference Manual, publication number MEZZIODVI-HRM.

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Figure B-1 VPX6UX604 Connector Numbering



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C • Thermal Derating

The processor speed and the temperature are inter-dependent. This means that for a given temperature, a maximum processor speed is achievable before throttling, and conversely for a given processor speed before throttling, a maximum temperature is achievable. This is further affected by the build level, which dictates the maximum ambient temperature at which the board can operate (see the Environmental Specification section).

This appendix shows the measured (unless state otherwise) maximum values for the various processor options.



NOTE

The following data is subject to change as new thermal solutions are developed. Contact your nearest Abaco sales office or agent for the latest thermal derating figures.

C.1 Processor Option 1: ULV Dual Core

Product codes are of the form SBC624-y1xxxxxxx, where y is the build level (see the Product Codes section for details of the other options).

Table C-1 Maximum Processor Speed versus Maximum Temperature for Processor Option 1

Build Level	Maximum Processor Speed at Maximum Operating Temperature		Maximum Operating Temperature at Maximum Processor Speed	
	Temperature (˚C)	Frequency	Frequency (GHz)	Temperature (˚C)
1	55	1.5[a] GHz	1.5	55[a]
2	65	1.5[a] GHz	1.5	65[a]
3	75	1.5[a] GHz	1.5	75[a]
4	75 at card edge	1.5[a] GHz	1.5	75 at card edge[a]
5	85 at card edge	N/A	1.5	N/A

a. These results have been determined by analysis and extrapolation rather than measurement.

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C.2 Processor Option 2: LV Dual Core

Product codes are of the form SBC624-y2xxxxxxx, where y is the build level (see the Product Codes section for details of the other options).

Table C-2 Maximum Processor Speed versus Maximum Temperature for Processor Option 2

Build Level	Maximum Processor Speed at Maximum Operating Temperature		Maximum Operating Temperature at Maximum Processor Speed	
	Temperature (˚C)	Frequency	Frequency (GHz)	Temperature (˚C)
1	55	2.2 GHz	2.2	55[a]
2	65	2.2 GHz	2.2	65[a]
3	75	1.9 GHz[a]	2.2	65[a]
4	75 at card edge	2.0 GHz	2.2	70
5	85 at card edge	900 MHz	2.2	70

a. These results have been determined by analysis and extrapolation rather than measurement.

C.3 Processor Option 4: SV Quad Core

Product codes are of the form SBC624-y4xxxxxxx, where y is the build level (see the Product Codes section for details of the other options).

Table C-3 Maximum Processor Speed versus Maximum Temperature for Processor Option 4

Build Level	Maximum CPU Rating at Maximum Operating Temperature		Maximum Operating Temperature at Maximum CPU Rating	
	Temperature (˚C)	Frequency	Frequency (GHz)	Temperature (˚C)
1	55	2.1[a]	2.1	55[a]
2	65	2.0[a]	2.1	55[a]
3	75	1.1[a]	2.1	55[a]
4	75 at card edge	1.2	2.1	60[a]
5	85 at card edge	< 800 MHz	2.1	60[a]

a. These results have been determined by analysis and extrapolation rather than measurement.

The processor speed can be fixed in the BIOS (see the next section).

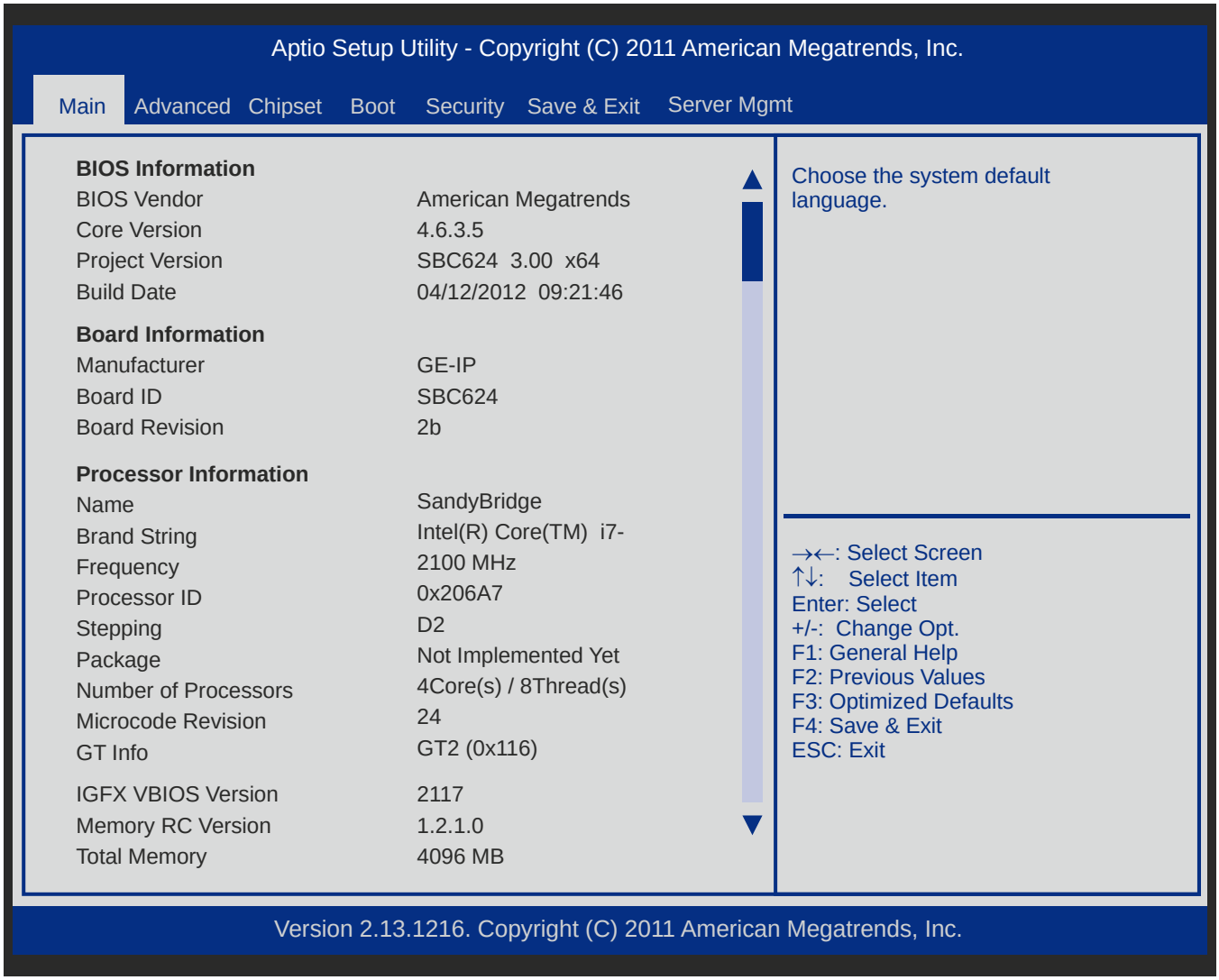
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C.4 Fixing the Processor Operating Frequency

To fix the processor operating frequency requires a custom P-state table to be set up. To do this, follow the steps below:

1. From the Main menu screen, select the Advanced menu screen.

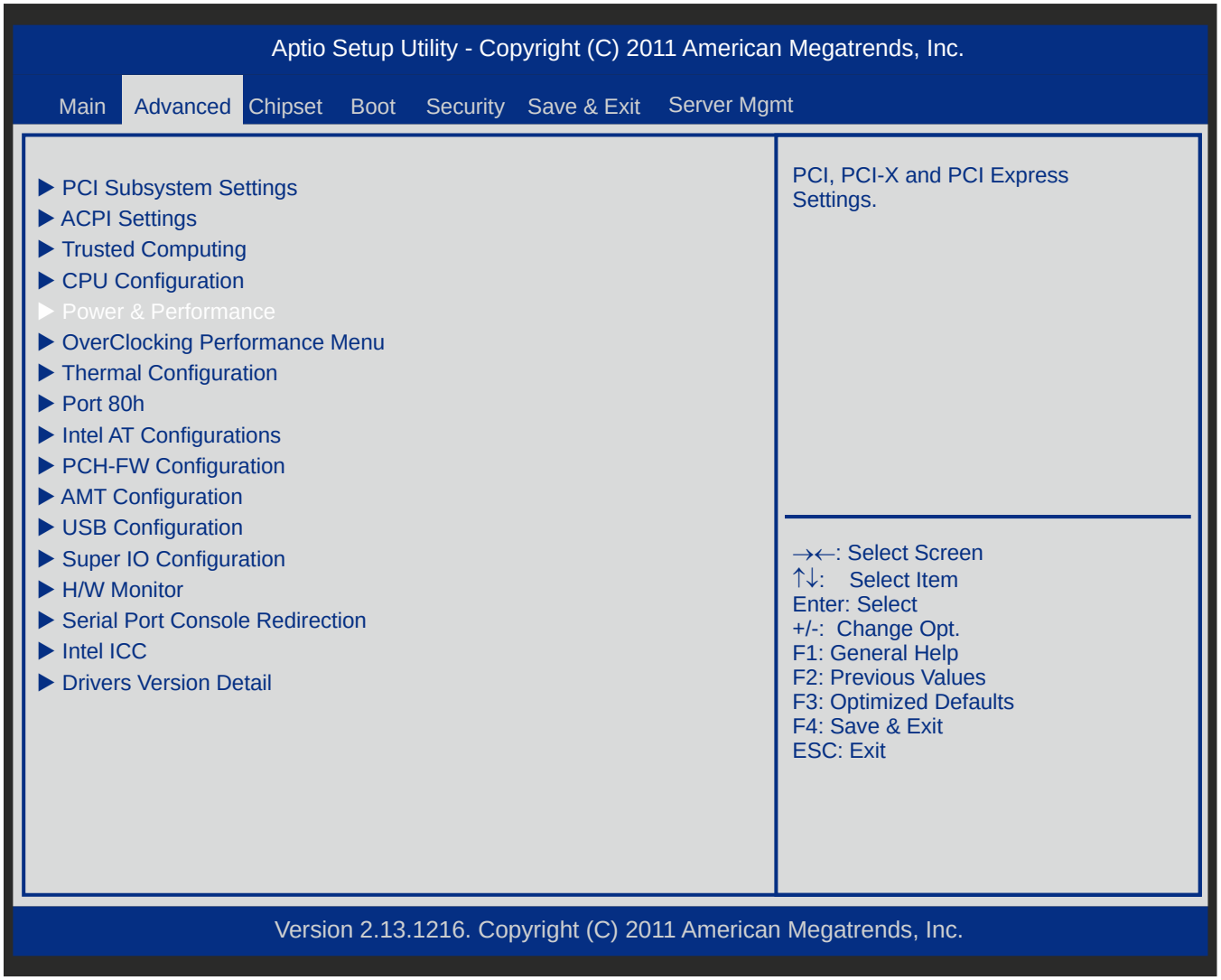
Figure C-1 Main Menu



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2. From the Advanced menu screen, select the Power & Perfomance sub-menu.

Figure C-2 Advanced Menu



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3. From the Power & Perfomance sub-menu, select the CPU – Power Management Control sub-menu.

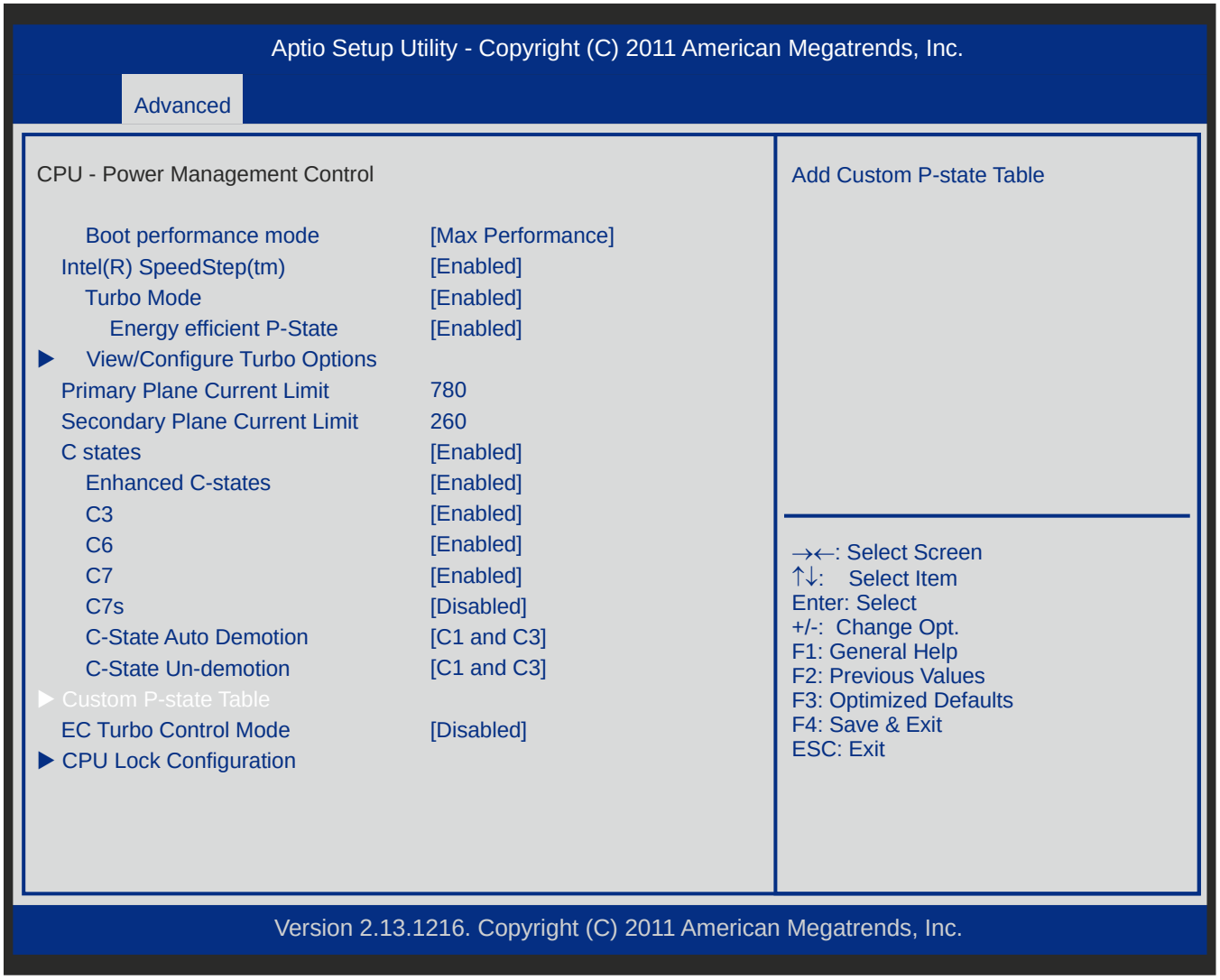
Figure C-3 Power & Performance Sub-menu



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4. From the CPU – Power Management Control sub-menu, select the Custom P-state Table sub-menu.

Figure C-4 CPU – Power Management Control Sub-menu



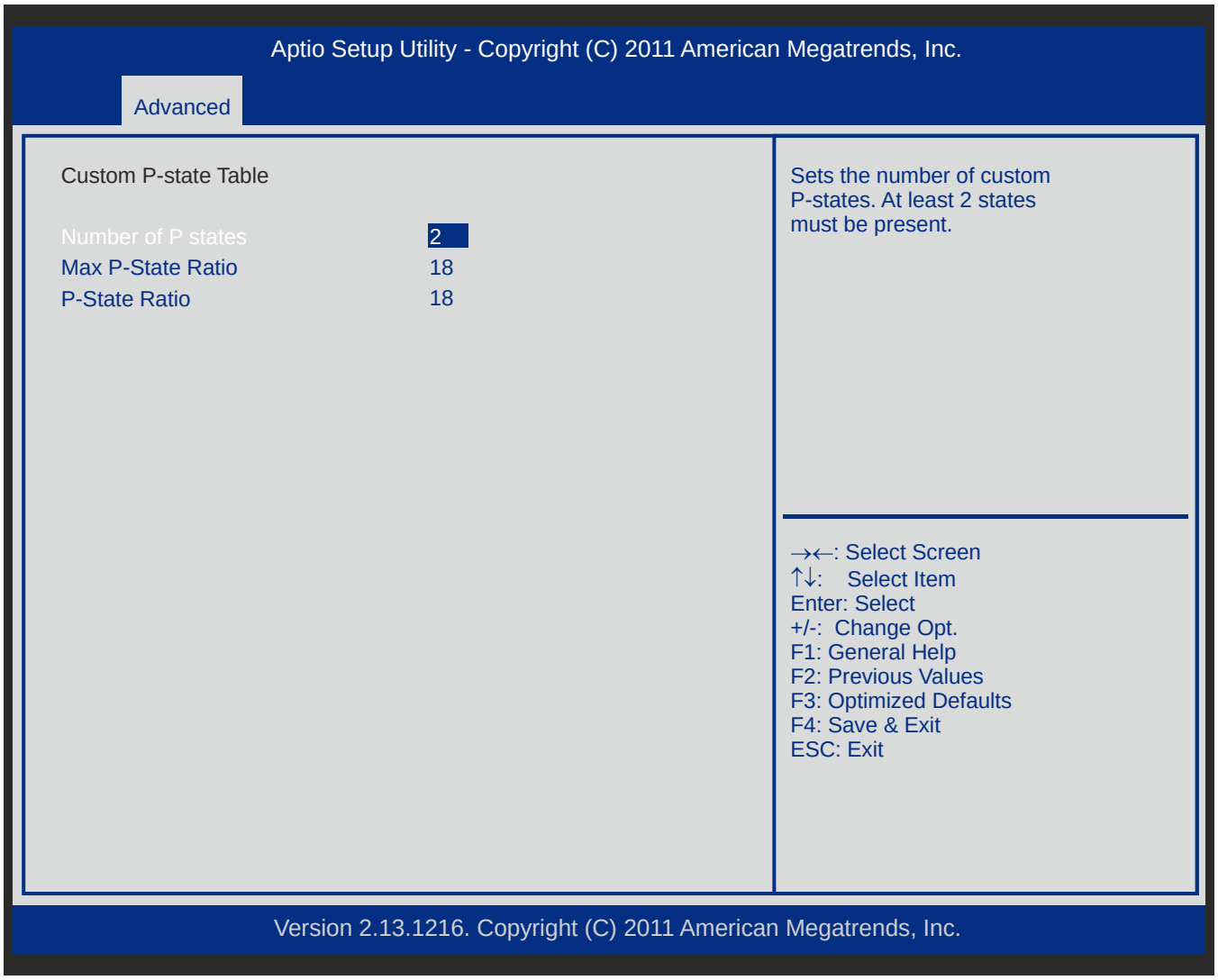
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5. In the Custom P-State Table sub-menu, set the Number of P-states to 2. This opens up two fields, which can be populated with the desired operating frequency divided by 100 MHz. For example, to fix the processor operating frequency to 1800 MHz, enter 18 into both fields.

NOTE

These settings can be overridden by an operating system, so ensure that the OS is configured to use the default settings.

Figure C-5 Custom P-state Table Sub-menu



6. Save these changes and exit, for instance by pressing F4. The BIOS will automatically reboot the SBC624 so that the changes will take effect.

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D • Statement of Volatility

D.1 Volatile Memory

The SBC624 contains volatile memory, i.e. memory in which the contents are lost when power is removed. None of this volatile memory is capable of write protection.

Table D-1 Volatile Memory

Memory Type	Size	User Modifiable?	User Access to Data?	Function	Process to Clear
DDR3 SDRAM	4, 8 or 16 GBytes	Yes	Yes	Contains run-time data	Power-off
On-die processor shared cache	Up to 6 MBytes	No	No	Improved memory performance	Power-off
Chipset CMOS SRAM	256 bytes	No	Yes	Real Time clock data	Power off, including VBAT supply
SRAM	35 Kbit	No	No	Internal FPGA configuration	Power-off
SRAM	40 KBytes	No	No	IPMI BMC program execution and storage	Power-off P3V3_AUX rail

D.2 Non-Volatile Memory

The SBC624 contains non-volatile memory, i.e. memory in which the contents are retained when power is removed.

Table D-2 Non-Volatile Memory

Memory Type	Size	User Modifiable?	User Access to Data?	Write Protectable?	Function	Process to Clear
SATA NAND drive	2 x 4, 8 or 16 GByte devices	Yes	Yes	Yes	Solid State Flash drive stores operating system or user data	Any hard drive formatting utility. Fast Erase facility
Boot (SPI) Flash	3 x 4 Mbyte devices	Yes	Yes	Yes	2 x BIOS code & ME firmware, 1 x BIT code/results	Can be cleared by any utility capable of writing to the PCH SPI bus
NVRAM (MRAM)	2 x 512 KByte devices	Yes	Yes	Yes	User defined parameters	Can be cleared by any utility capable of writing to I/O space
		No	Yes	Yes	BIT and BCS data	
EEPROM	2 x 32 Kbit x 8	No	No	Yes	PCIe bridge setup information	Can be cleared by any utility capable of writing to the Pericom Bridge local I^2C bus
EEPROM	256 Kbit	Yes	Yes	Yes	PCIe Switch configuration	Can be cleared by any utility capable of writing to the Switch local SPI bus
EEPROM	2 x 256 Kbit	No	No	Yes	Ethernet device configuration	Can be cleared by any utility capable of writing to the LAN SPI bus
FPGA/Power Manager	N/A	No	Yes	N/A	Power-up/reset logic, glue logic, LPC registers, timers, Watchdog, NVRAM access	JTAG via VPX connector or TAC

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Memory Type	Size	User Modifiable?	User Access to Data?	Write Protectable?	Function	Process to Clear
EEPROM	40 Kbit	No	Yes	No	TPM key storage and user credential storage	Proprietary software
Flash	32 Mbit	No	No	Yes	Mellanox firmware storage	DOS – Mellanox proprietary software
EEPROM	32 Kbit	No	No	Yes	Mellanox configuration data	DOS – Mellanox proprietary software
EEPROM	2 x 8-bit registers	Yes	Yes	Yes	DIP Switch settings	BIOS set-up utility
EEPROM	2 x 2 Kbit	No	No	Yes	SPD information for on-board SDRAM	Can be cleared by any utility capable of writing to the PCH I^2C bus
EEPROM	10 bytes	No	Yes	Yes	Elapsed Time Indicator	DOS – proprietary software
EEPROM	256 Kbit	No	Yes	Yes	BMC FRU data	DOS – proprietary software
Flash	256 KBytes	No	No	No	BMC boot code storage	Proprietary software

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Glossary



NOTE

The connector signals are explained in Section 7.



LINK

This glossary only features terms special to this manual. Explanations of more general terms can be found in the Glossary, publication number GLOS1.

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