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SBS Technologies, Inc.

4417-DAC16

16 Channel Digital to Analog Converter
With
16 Bit Parallel Port



Technical Manual

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Table of Contents

1 Introduction 1-1
1.1 General 1-1
1.2 Specifications 1-1
1.2.1Electrical Specifications 1-1
1.2.2System Interface Specifications 1-2
1.2.3Mechanical Specifications 1-2
1.2.4Environmental Specifications 1-2
1.2.5Options 1-2

2 Installation 2-1
2.1 Configuration 2-1
2.1.1Port Address Switch SW1 2-1
2.1.2Jumpers 2-1
2.1.3Adjustments 2-1
2.2 Pin-outs 2-2
2.2.1Analog Outputs - P1 2-2
2.2.2Parallel Output of DAC Channel #16 - PL3 2-3
2.2.3APK401 Bus Interface - PL1 2-3
2.2.44422-DA Interface - PL2 2-3
2.3 Card Slot 2-4
2.4 Configuration of Option 401 2-4

3 Programming Information 3-1
3.1 General 3-1
3.2 Registers 3-2
3.2.1Address Register (Base + 0) 3-2
3.2.2Word Table Entry Register (Base + 4) 3-3
3.2.3ISA Bus Channel Select Register (Base + 6) 3-4
3.2.4 ISA Bus Data Register (Base + 8) 3-4
3.2.5 Gain and Offset Adjustment Register (Base +10) 3-4

1 Introduction

1.1 General

The SBS Technologies, Inc. Model 4417-DAC16 is a general purpose 16 channel digital to analog converter. It is designed to work directly with other SBS Technologies, Inc. products to provide a high performance analog output capability. Each channel has its own 12 bit digital to analog converter with the ability of writing the same data to as many of the channels as required simultaneously. Each channel has an 8 bit gain and offset adjustment.

The 4417-DAC16 is a standard ISA card (IBM AT size) which plugs into a single 8 bit IBM PC slot. The 4417-DAC16 is completely configured by software and uses only 16 addresses in the PC I/O address space. The external data to be converted to analog signals can be supplied on two different proprietary 16 bit paths via connectors on the top of the card.

Option 401 provides a plug in daughter board for integration of the 4411-C series decommutator and other third party cards. The second external bus is designed for the SBS Technologies, Inc. 4422-DA decommutator board. Each output DAC channel can also be written to via the PC ISA bus.

Once configured, the 4417-DAC16 operates independently of the PC CPU and does not use any interrupts or bus time unless the PC is writing directly to the card.

1.2 Specifications

1.2.1 Electrical Specifications

Number of channels	16 individual outputs
Resolution	12 bits
Accuracy	1 L.S.B.
Output Range	± 10 volts.
Adjustments	Master reference, Gain, and Offset
Input code	Binary M.S.B. justified in a 16 bit word 2's comp
Output drive capability	programmable
Full power frequency	± 10 volts into 2 k ohm
Slew rate	125 k Hz per channel 3 volts per micro-second per channel
Digital Outputs	16 bit output provided in parallel with Analog channel 16

1.2.2 System Interface Specifications

Interface Type	16 bit ISA I/O mapped for set-up. 16 bit proprietary path for data with 12 bit address or 16 bit path for data with strobes.
Programmable Function	DAC channel source, DAC channel gain and offset.

1.2.3 Mechanical Specifications

Board size	Single ISA full size card
Manufacturing	Six layer board with ground layer.

1.2.4 Environmental Specifications

Temperature (operating)	10 to 45 degrees C
Temperature (non-operating)	-25 to + 70 degrees C
Humidity	0 to 90% non-condensing

1.2.5 Options

-401 Daughter board for the SBS Technologies, Inc. 4411-C/CU PCM decommutator

2 Installation

2.1 Configuration

2.1.1 Port Address Switch SW1

The 4417-DAC16 occupies 16 bytes of I/O address space. The base port address is selected by setting DIP switch SWI. Ones in the address are set by turning the appropriate switch off. The default setting is 210 hex. The switch allocations are:

Switch SW1	Address Bit	Default Settings
1	A9	Off
2	A8	On
3	A7	On
4	A6	On
5	A5	On
6	A4	Off
7		Set On
8		Set On

2.1.2 Jumpers

JP1 none provides a master reference voltage of 10 volts. (Not Supported)
jumper on 1-2 provides a 5 volts master reference (recommended)
jumper on 2-3 provides a 2.5 volt master reference

JP2 off for 2048 word lookup RAMS
on for 4096 word lookup RAMS (Standard)

JP3 off for 2048 word lookup RAMS
on for 4096 word lookup RAMS (Standard)

JP4 off to use PL1 16 bit proprietary bus with APK 401 option (4411C/CU)
on to use PL2 16 bit data bus with strobes (4422DA)

2.1.3 Adjustments

VR1 enables the master reference to be adjusted by approximately 5% down from the maximum voltage set by JP1.

VR2 Adjusts the offset voltage of all channels

VR 3 Adjusts the Gain voltage of all channels

Ordinarily, none of these adjustments will need to be touched in operation.

2.2 Pin-outs

The 4417-DAC16 has four connectors.
P1: A 37 pin D-type connector providing the ANALOG outputs.
PL1: A 34 pin IDC at the top of the board for the 16 bit data and address path.
PL2: A 50 pin IDC at the top of the board for the 16 bit data path with strobes.
PL3: A 26 pin IDC for the 16 bit parallel output port.

2.2.1 Analog Outputs - P1

The analog outputs are single ended.

P1 - 37 Pin D-type Female			
Pin	Signal	Pin	Signal
1	Ground	20	DAC Channel # 1
2	Ground	21	DAC Channel # 2
3	Ground	22	DAC Channel # 3
4	Ground	23	DAC Channel # 4
5	Ground	24	DAC Channel # 5
6	Ground	25	DAC Channel # 6
7	Ground	26	DAC Channel # 7
8	Ground	27	DAC Channel # 8
9	Ground	28	DAC Channel # 9
10	Ground	29	DAC Channel # 10
11	Ground	30	DAC Channel # 11
12	Ground	31	DAC Channel # 12
13	Ground	32	DAC Channel # 13
14	Ground	33	DAC Channel # 14
15	Ground	34	DAC Channel # 15
16	Ground	35	DAC Channel # 16
17	Ground	36	unconnected
18	Ground	37	unconnected
19	Ground		

2.2.2 Parallel Output of DAC Channel #16 - PL3

The parallel port is directly associated with DAC channel #16 of the D/A outputs. This means when data is written to DAC channel #16 it will appear on the parallel port. The connector also provides a major frame strobe and minor frame strobe and a word strobe for each data value directed to the port. The minor frame strobe is consistent with the first word in the frame. The major frame is coincident with the first word in the major frame when data is provided by the SBS Technologies, Inc. 4422-DA board. If used with the SBS Technologies, Inc. 4411-C/CU board the major frame strobe is the same as the minor frame strobe.

PL3 - 26 Pin IDC			
Pin	Signal	Pin	Signal
1	Ground	14	Bit 3
2	Major Strobe	15	Bit 4
3	Ground	16	Bit 5
4	Minor Strobe	17	Bit 6
5	Ground	18	Bit 7
6	Word Strobe	19	Bit 8
7	Ground	20	Bit 9
8	Ground	21	Bit 10
9	Ground	22	Bit 11
10	Ground	23	Bit 12
11	Bit 0	24	Bit 13
12	Bit 1	25	Bit 14
13	Bit 2	26	Bit 15

2.2.3 APK401 Bus Interface - PL1

This proprietary bus uses a 34 pin IDC connection. Its pin definitions are available on request.

2.2.4 4422-DA Interface - PL2

The 50 pin IDC connection is designed to operate with SBS Technologies, Inc. 4422-DA decommutator. Please refer to the 4422-DA manual for pin allocations.

2.3 Card Slot

The 4417-DAC16 card can be installed in any 8 bit PC slot. The connection of the 16 bit proprietary data path by a 34 pin ribbon cable to the -401 daughter card may determine the final slot use.

2.4 Configuration of Option 401

Option -401 is a small daughter board designed to plug into the SBS Technologies, Inc. 4411-C/CU PCM card. The following must be carried out:
Remove the dual port RAM IC's U72 and U80 from the 4411-C. Observe ESD practices.

Insert these RAM IC's into U1 and U2 on the APK 401 daughter board.
Plug the daughter board into the empty sockets of U72 and U80 on 4411-C. Noting that the 34 pin connector should be facing the top of the PC card and therefore pin 1 of all IC's on the daughter board are nearest the top of the PC card and U1,U2 have the same orientation as the original U72 and U80.

There is only one jumper on the APK 401 daughter board. This is a two way jumper which is used to permanently enable the drivers on the daughter board to drive the external bus or to leave control of the drivers to an external signal on the data bus. If an SBS Technologies, Inc. 4422DA or 4411C/CU card is installed and connected to the proprietary bus then the jumper should be set on 1-2 for external control otherwise it should be set to 2-3 to permanently enable.

Jumper 1	Operation
1-2	External Control
2-3	Permanently Enabled

3 Programming Information

3.1 General

The 4417-DAC16 has 16 individual DAC channels. Each DAC channel requires two control signals to go true to load data from the 16 bit data path to any particular DAC channel. Each control signal is a single bit coming from separate dual port RAM's acting as lookup tables. The two tables are 16 bits wide in order to drive the 16 DAC channels. The first table (the Frame Table) has 256 entries. The second table (the Word Table) has 2048 entries (optionally 4096 entries). The tables are filled with the DAC channel select bits that are set by writing to the I/O registers on the board.

Data words arriving on the proprietary 16 bit data path comes in blocks (or frames) and each word within the frame has a corresponding position in the Word Table. The size of the frame (in words) does not have to be known beforehand provided the Word Table has been sufficiently filled.

Frame Table	Address	Word Table
1 1 1 1 1 1 1 1 1 1 1 1 0 1 0 0	00 00 00	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	00 00 01	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	00 00 02	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	00 00 03	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	00 00 04	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 05	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 06	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 07	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 08	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 09	1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 0A	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 0B	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 0C	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 0D	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 0E	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	00 00 0F	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
F E D C B A 9 8 7 6 5 4 3 2 1 0	← Bit Position →	F E D C B A 9 8 7 6 5 4 3 2 1 0
Continues for 256 entries.		Continues for 2048 (optionally 4096) entries.

In the previous example, if a PCM stream with five minor frames per major frame and ten words per minor frame was being received by the 4417-DAC16, then the fourth word of every minor frame would be sent to DAC channel #1, and every word of the first minor frame would be sent to DAC channel #2. Note that the 0 in

position 2 of the first entry of the Word Table would have no effect, because there is no matching 0 in any of the entries of the Frame Table. Likewise, the 0 in position 3 of the Frame Table would also have no effect, because there is no matching 0 in the Word Table. A 0 must be in corresponding positions of both the Frame Table and the Word Table for any word to be sent to any DAC channel.

When Option 401 has been selected, the word with address 0 is special in that it is used as the pointer into the Frame Table. Only the least significant 8 bits are used for the pointer. Once the Frame Table entry is selected the subsequent word addresses are used to point to the Word Table entry.

Each table gives a 16 bit data word and each bit of the 16 bit word selects a DAC channel. When the same bit from both the Frame Table and the Word Table is cleared (logic 0) the appropriate DAC channel is loaded with the incoming data word. By programming the appropriate bits in each table up to 256 frames of 2048 (4096 optional) data words each can be directed to the required single or multiple DAC channel.

Each DAC channel can be written to via the PC bus. The ISA Bus Data Register has each bit assigned to one DAC channel. The least significant bit references DAC channel #1. One or more DAC channels can be written to simultaneously. The DAC channels to be used are first set by writing to the ISA Bus Channel Select Register. Then the data to be outputted is then written to the ISA Bus Data Register. Data must be most significant bits justified with the register. The ISA Bus Channel Select Register does not need to be written to for every output. The data from the PC can be multiplexed with the data from one of the external connectors. All channels are available to both the PC and the external connectors. The timing jitter caused by simultaneous ISA Bus and external connector writes is less than 500 nanoseconds.

Each of the DAC channels have an 8 bit gain and 8 bit offset scaling function. The maximum value of the gain and offset is set by the master reference JP4.

3.2 Registers

The registers on the 4417-DAC16 are all IO mapped and occupy 16 bytes. They can be written to as one 16 bit register or as two 8 bit registers, in subsequent IO address spaces.

3.2.1 Address Register (Base + 0)

3.2.1.1 The bits are assigned as follows:

Bit #	Function
0-3	Select DAC channel to setup with Gain and Offset quantities
0-11	Address of an entry for the Frame Table or Word Table.
12	Serial Data Input bit (only used with the Option 401).
13	Serial Clock Input bit (only used with the Option 401).
14	2's Complement bit.
15	Enable Programming bit.

The Frame Table is 2048 words long but only the first 256 entries are used to control the DAC channels. The remaining space can be used as scratch pad RAM if required.

The Word Table is 2048 words long. A 4096 word long Word Table is optionally available.

3.2.1.2 Frame Table Entry Register (Base +2)

3.2.1.3

After setting the Address Register with the Frame Table entry address (and setting bit 15) the 16 bit DAC channel select word can be written to or read from the Frame Table by accessing this I/O address. The bit assignments are:

DAC Channel #	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Register Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	^ Most significant bit															

A bit in a Frame Table entry must be cleared to select the corresponding DAC channel.

3.2.2 Word Table Entry Register (Base + 4)

3.2.2.1

After setting the Address Register with the Word Table entry address (and setting bit 15) the 16 bit DAC channel select word can be written to or read from the Word Table by accessing this I/O address. The bit assignments are:

DAC Channel #	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Register Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	^ Most significant bit															

A bit in a Frame Table entry must be cleared to select the corresponding DAC channel.

3.2.3 ISA Bus Channel Select Register (Base + 6)

3.2.3.1

This register selects which DAC channels will be loaded when data is written to the ISA Data Register.

DAC Channel #	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Register Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

^ Most significant bit

A bit in ISA Bus Channel Select Register must be cleared to select the corresponding DAC channel.

3.2.4 ISA Bus Data Register (Base + 8)

3.2.4.1

This register is a 16 bit port for writing data from the ISA bus to the selected DAC channels. Data is loaded to the DAC channels on the write of the most significant byte of the data. The data should be justified on the most significant bit of both the data and the register.

Data Value Bit #	11	10	9	8	7	6	5	4	3	2	1	0	Don't Care	12 bit data value
Register Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	16 bit register

^ Most significant bit

3.2.5 Gain and Offset Adjustment Register (Base +10)

3.2.5.1

The SBS Technologies, Inc. 4417-DAC16 can be adjusted on a per channel basis for voltage gain and offset. Output voltage for any given DAC channel is calculated with the following formula:

Voutput = ((12 bit data word) * Gain / (2^12)) + Offset

The most significant byte of this 16 bit register sets the gain of the DAC channel while the least significant byte sets the offset. The DAC channel # to which the value should apply must first be set in the least significant 4 bits of the Address Register. A 0 hex selects DAC channel #1 while an F hex selects DAC channel #16.

The value to program the gain for any channel is given by:
Dgain = 127 – ((127 / 2) * (Vrange / Vref))

where:
Dgain is the 8 bit binary value required.
Vref is the board reference voltage.
Vrange is the total voltage range.

NOTE: Vrange cannot be greater than 2 * Vref.

The value to program the offset for any channel is given by:

Doff = 127 – (127 * Voffset / Vref)

where:
Doff is the 8 bit binary value required.
Vref is the board reference voltage.
Voffset is the starting offset voltage.

NOTE: Voffset cannot be greater then +Vref. Or less then -Vref.

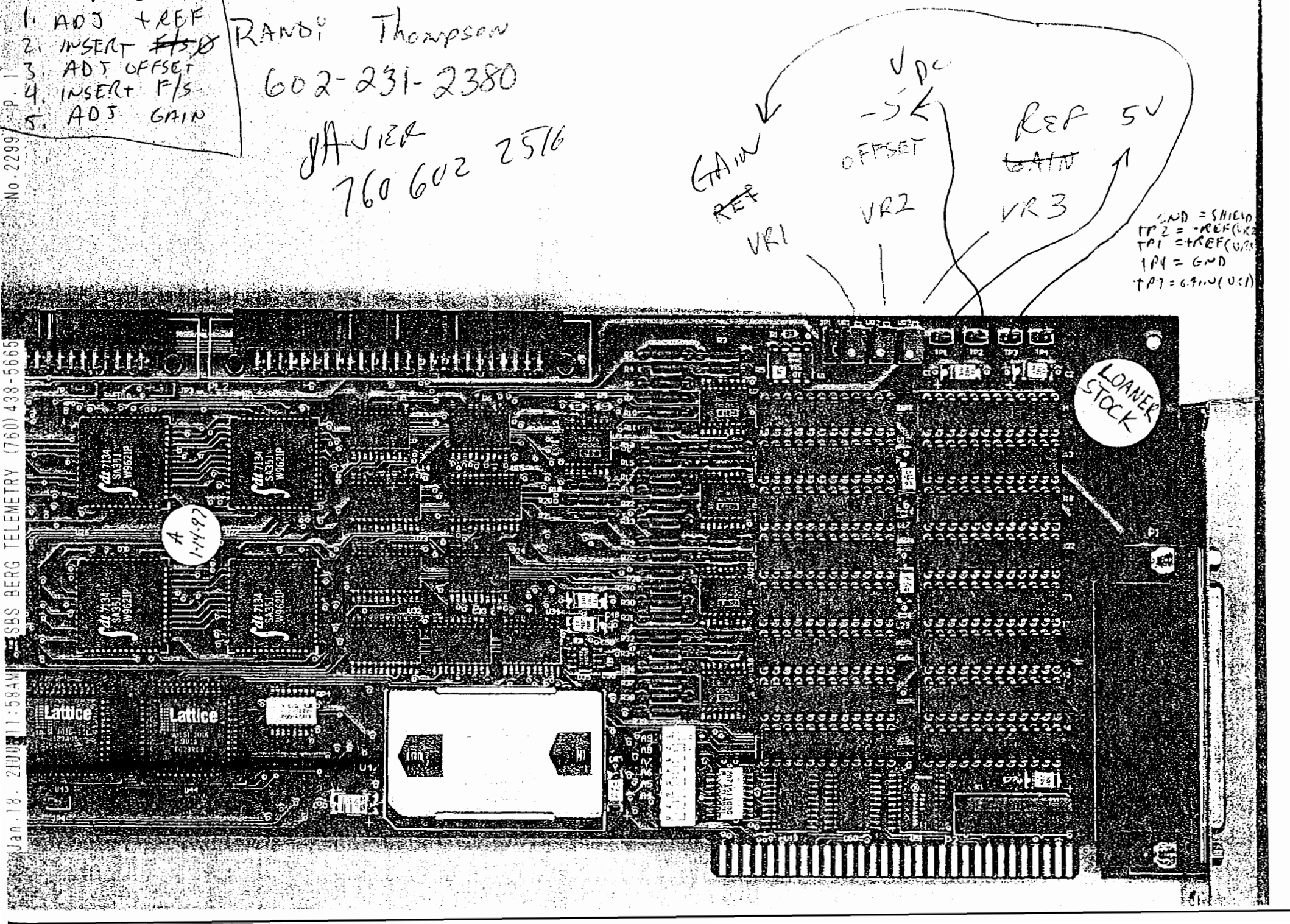
Option 401 Note:
On revision B and later boards the number of words in the frame must be programmed into the board. This has to be sent most significant bit first as a serial 16 bit value. The data bit is bit 12 of the Address Register and the clock is bit 13 of the Address Register. The data is latched on the rising edge of the serial clock. The Enable Programming bit should be set high when programming this information.

For All Programming Options:
When all programming is complete, a final word of 5000 hex should be written to the Address Register. The Serial Clock bit should be cleared, the Serial Data bit should be set high, the 2's Complement bit should be set high and the Enable Programming bit should be cleared. This should be the last programming operation on the board.

Jan. 18. 2000 11:58AM SBS BERG TELEMETRY (760) 438-5665 No. 2299 P. 1

TEST PROC.
1. ADJ +REF
2. INSERT ~~F/S~~
3. ADJ OFFSET
4. INSERT F/S
5. ADJ GAIN

RANDY THOMPSON
602-231-2380
JAVIER
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