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SBS Technologies

CV1

CompactPCI®
3U
Single Board Computer

User's Guide

Rev C

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CV1 User's Guide - Rev. C

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Conventions

The following conventions are used in this user’s guide:

- Signal names are designated with all capital letters (e.g. SYSEN#)
- Signal names followed by the pound sign (#) are active-low (e.g. SYSEN#)
- Data addresses written in hexadecimal are designated with the prefix 0x (e.g. 0xF000_0000)
- Data addresses written in binary are designated with the prefix 0b (e.g. 0b1001100)

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Chapter 1: Introduction

1.1 Overview

The CV1 is a rugged CompactPCI® Single Board Computer (SBC) in 3U form factor, driven by the Freescale MPC7447A G4 PowerPC processor. The CV1 includes significant increases to core processor speeds, bus clock rates and memory array capacities over legacy 3U PowerPC processor boards. The CV1 can be implemented as a system controller or peripheral card.

Processor

The MPC7447A G4 host processor is a high-performance, low-power, 32-bit implementation of the PowerPC RISC architecture with a processor core speed of 1GHz. The MPC7447A processor includes 32kB L1 instruction and data caches and an on-chip 512kB L2 cache. The processor is linked to the MV64460 PowerPC System Controller through a 64-bit 167MHz MPX system bus.

DDR SDRAM

The MV64460 System Controller provides a system memory interface that connects to a total on-board memory of 256MB.

The MV64460 System Controller also provides four independent DMA engines that move large blocks of data between the system bus interface, system memory interface and the PCI bus interface.

Flash Memory

The CV1 includes 128MB of MirrorBit™ flash memory for storing boot code. Flash memory is programmable and the CV1 offers multiple write-protection options.

Serial I/O

The MV64460 includes two MPSC ports that provide one RS-232 serial port (COM1) and one RS-422/485 port (COM2). Both serial ports are routed to the backplane through the cPCI_J2 connector.

Gigabit Ethernet

The MV64460 also includes three Ethernet MACs. The CV1 uses two of these MACs to provide two 10/100/1000 Base-TX Ethernet links to the backplane through the cPCI_J2 connector.

PCI Interface

The MV64460 System Controller includes two PCI local bus interfaces: PCI Bus 0 is a 32-bit 33/66MHz PCI bus dedicated to the PMC site; PCI Bus 1 is a 32-bit 33/66MHz PCI bus to the cPCI backplane through the PCI 6254 cPCI Bridge.

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cPCI Bridge

For PCI transactions, the CV1 employs the PCI 6254 Dual Mode cPCI Bridge. The PCI 6254 manages PCI transactions between PCI Bus 1 and the cPCI backplane. The PCI 6254's dual mode capability allows the CV1 to function as either a system controller or peripheral card.

NVSRAM

The STK17T88 NVRAM/RTC provides 32kB of non-volatile SRAM and a Real-Time Clock (RTC) feature. The RTC provides a programmable timekeeping device driven by a 32.768kHz on-board oscillator that keeps time in increments of seconds up to a century. The CV1 provides the BATT+ line from the cPCI backplane for attaching an external battery backup to the RTC.

Temperature Sensor

The CV1 also includes over-temperature protection with the MAX6658 Temperature Sensor. The MAX6658 uses the MPC7447A's on-die thermal diode to monitor processor temperature. It issues an interrupt to the MV64460 when a threshold value is exceeded. It also monitors ambient board temperature.

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1.2 Features

MPC7447A Processor
- Processor core speed: 1GHz
- 32kB L1 instruction/data caches
- 512kB L2 cache
- 64-bit 167MHz system bus

DDR SDRAM
- 256MB system memory
- Full ECC protection
- 72-bit (with ECC) 167MHz Memory Bus

Flash ROM
- 128MB MirrorBit™ Flash ROM
- Multiple write protection options

PCI Buses
- PCI Bus 0—32-bit, 33/66MHz to PMC site, +3.3V VIO
- PCI Bus 1—32-bit, 33/66MHz to cPCI backplane to PCI 6254 cPCI Bridge

NVRAM/Real-Time Clock
- 32kB non-volatile SRAM
- RTC feature with +3.3V battery backup from system

Warranty
- 2 year warranty

Serial I/O
- COM1:RS-232 (async. operation)
- COM2: RS-422/485 (sync. and async. operation)

PMC site
- Single IEEE 1386/1386.1-2001 compatible extension slot located on 32-bit 33/66MHz PCI bus
- Rear I/O support (+3.3V VIO)

CompactPCI Bridge
- PCI 6254 cPCI Bridge
- Dual-mode operation (transparent and non-transparent mode)

GPIO
- Ten programmable GPIO ports (eight dedicated, two shared)
- Programmable line direction, input polarity, output type, and interrupt masking

Ethernet
- Two 10/100/1000Base-TX Ethernet ports to the backplane
- Onboard Gigabit Ethernet PHYs

1.3 Specifications

Physical Description

Form Factor:	3U per PICMG 2.0
Height:	100 ± 0.15mm (3.9 ± 0.0059 in.)
Width:	160 ± 0.15mm (6.3 ± 0.0059 in.)
Weight:	
Convection-cooled:	15.2oz.
Conduction-cooled:	9.6oz.

Power Requirements

+5V and +3.3V:	Required from the cPCI backplane
±12V:	As required by installed PMC module
+3.3V:	Battery backup from system (BATT+)

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Power Consumption	+5V	+3.3V	Total Power
Peak:*	5.42A	3.26A	37.86W
Typical:*	4.09A	2.50A	28.70W
Idle:**	2.36A	1.80A	17.74W
In-rush:**	2.80A @ 183µs	1.70 @ 860µs	
BATT+		10µA	

* Calculated values
** Measured at JMON prompt

Temperature (operating)

Convection-cooled:*	0° C to 70° C (ambient)
Conduction-cooled:**	-40° C to 85° C

*Min. airflow of 200 LFM required
** Measured at card edge

Temperature (storage)

Convection-cooled:	-40° C to 85° C
Conduction-cooled:	-55° C to 105° C

Relative Humidity (non-condensing)

Convection-cooled:	5% to 95% @ 40° C
Conduction-cooled:	5% to 95% @ 40° C

Shock (half-sine)

Convection-cooled:	20g peak / 6ms, 3 axes, up & down, 3 hits / direction
Conduction-cooled:	40g peak / 11ms, 3 axes, up & down, 3 hits / direction 100g peak / 6ms, 3 axes, up & down, 3 hits / direction

Vibration (random)

Convection-cooled:	$0.04g^2$/Hz @ 5–100Hz (2g rms), 60 minutes / axis
Conduction-cooled:	$0.1g^2$/Hz @ 5–2000Hz (12g rms), 60 minutes / axis

1.4 Compliance

MTBF

Calculations are available in accordance with MIL-HDBK-217. Please contact SBS for latest values.

Safety

Designed to meet standard UL1950/60950

Emissions

Designed to meet FCC Part15, SubPart A

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1.5 Block Diagram

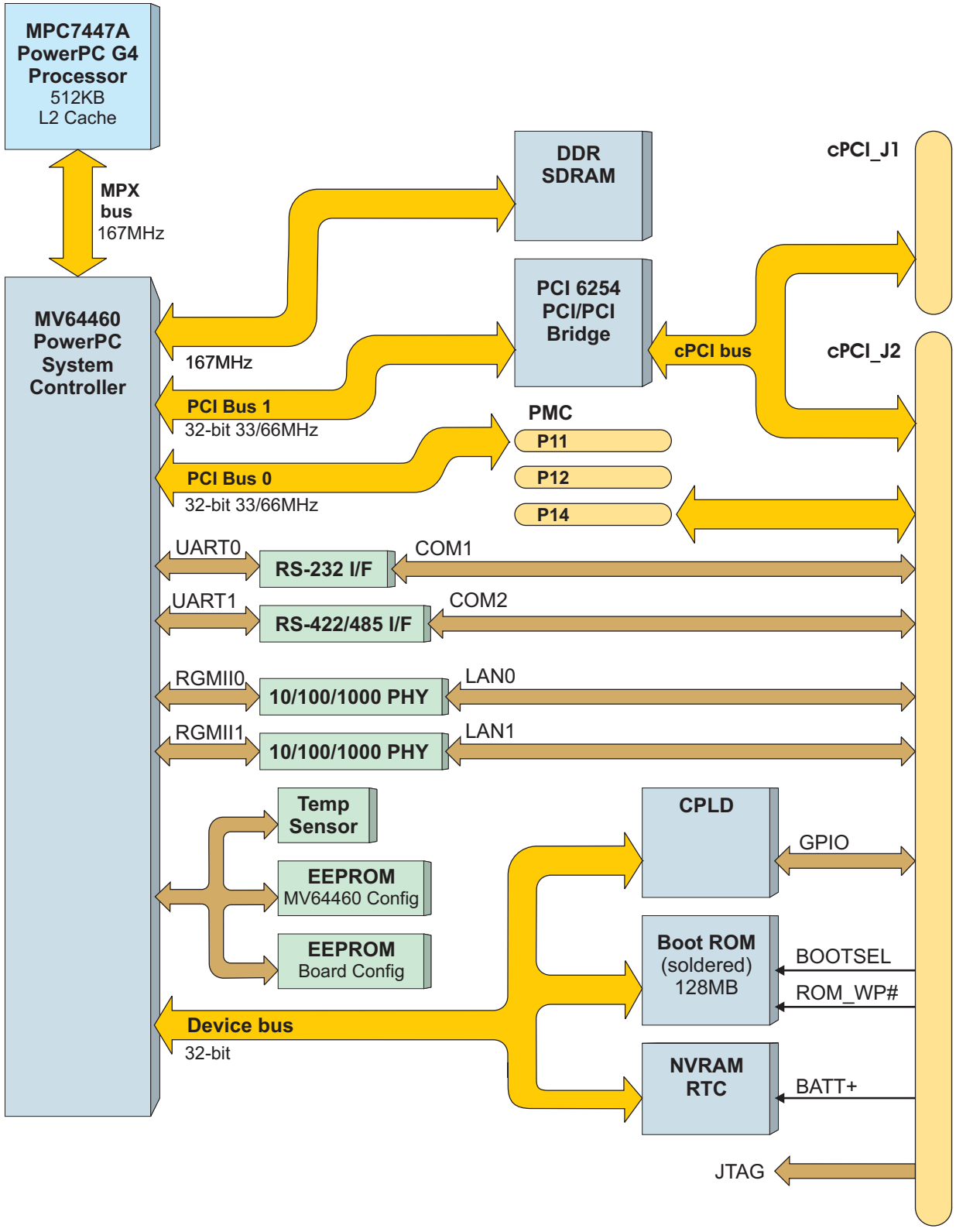


Figure 1-1 CV1 Block diagram

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1.6 Technical Support

Most issues can be resolved by referring to this manual. If any problems cannot be resolved, please contact SBS Technical Support by:

- E-mail: support.sbc@sbs.com
- Telephone: (919) 851-1101 (choose Technical Support option)
- Fax.: (919) 851-2844

For more information, refer to “Customer Service” on page 7-2.

1.7 Related Documents

For more information on CV1 components, refer to the following documents:

Components

- MPC7447A RISC Microprocessor Hardware Specifications—Motorola® Inc., MPC7447AEC Rev. 0, February 2004
- MV64460, MV64461, MV64462 System Controller Hardware Specification - Parts 1 & 2—Marvell Semiconductor, Inc.®, Doc. No. MV-S101286-00(01) Rev B, July 2004
- PCI 6254 (HB6) Dual Mode Universal PCI-to-PCI Bridge DataBook—PLX Technology, Inc., Version 2.1, December 2003
- 512Mb: x4, x8, x16, DDR SDRAM Datasheet—Micron Technology, Inc., July 2004
- XCR3384XL: 384 Macrocell CPLD—Xilinx, Inc., Preliminary Production Specification, February 2004
- S29GLxxxN MirrorBit™ Flash Family S29GL512N, S29GL256N, S29GL128N Data Sheet—AMD Spansion, Publication Number 27631, Revision A, Amendment 5, September 2004
- STK17T88 nvTime Event Data Recorder 32Kx8 AutoStore™ nvSRAM With Real-Time Clock—Simtek Corporation, Document Control #ML0024 Rev 1.0, December 2004
- Maxim MAX6657/MAX6658/MAX6659 ±1°C, SMBus-Compatible Remote/Local Temperature Sensors with Overtemperature Alarms—Maxim Integrated Products, 19-2034; Rev. 2, March 2002

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Specifications

- IEEE Std. 802.3-2002—Part 3: Carrier Sense Multiple Access Collision Detection (CSMA/CD) Access Method and Physical Layer Definitions, March 2002.
- IEEE Std. 1149.1-1990—IEEE Standard Test Access Port and Boundary Scan Architecture, June 1993.
- IEEE Std. 1284-2000—IEEE Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers, September 2000.
- IEEE1386-2001, IEEE Standard for a Common Mezzanine Card (CMC) Family, June, 2001.
- IEEE1386.1-2001, IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), June, 2001.
- Intel, Universal Host Controller Interface (UHCI) Design Guide, Revision 1.1, 297650-002.
- IPC-A-610—Acceptability of Electronic Assemblies, Revision C, January 2000.
- IPC-6012A with Amendment 1—Qualification and Performance Specification for Rigid Printed Boards, July 2000.
- PICMG 2.3, PMC on CompactPCI Specification, R1.0, August, 1998.
- PICMG 2.9, CompactPCI System Management Specification, R1.0, February, 2000.
- PICMG 2.0—CompactPCI Specification, R3.0, October 1999.
- PCI Special Interest Group (SIG)—PCI Local Bus Specification, Revision 2.3, October 2001
- PCI Special Interest Group (SIG)—PCI-X Addendum to the Local PCI Bus Specification, Revision 1.0a, July 2000
- Phillips Semiconductors, The I2C Specification, version 2.1, document 9398-393-40011, January 2000.
- MIL-HDBK-217F, Military Handbook—Reliability Prediction of Electronic Equipment, December 1991
- Telecommunications Industry Association, TIA / EIA-232-F-1997, Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange, October 1997.
- VITA Standards Organization, VITA 20-2001, American National Standard for Conduction Cooled PMC, August, 2001.
- VITA Standards Organization, VITA 30.1-2002, American National Standard for 2mm Connector Practice on Conduction Cooled Euroboards, August, 2002.
- VITA Standards Organization, VITA 32-2002, Processor PMC Standard for Processor PCI Mezzanine Cards, September 2002.
- VITA Standards Organization, VITA 39-2003, PCIX Auxiliary Standard for PMCs and Processor PMCs, August 2003.

1. PICMG Specifications are available to PICMG members only. SBS Technologies is not authorized to distribute copies of these specifications. More information can be found at http://www.picmg.org.
2. Data sheets from hardware components can be downloaded from individual vendors web sites.

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Chapter 2: Installation

2.1 What Is Included

The CV1 Single Board Computer (SBC) is shipped with the following items:

- CV1 SBC Printed Circuit Assembly

2.2 Equipment Needed

The following items are needed to install and operate the CV1:

- 3U Convection-cooled CompactPCI chassis

or

- 3U Conduction-cooled CompactPCI chassis



Caution! Always use proper Electrostatic Discharge (ESD) protection when handling printed circuit boards to avoid seriously damaging components. Product handlers must always be properly grounded.

2.3 Power Requirements

The CV1 requires +5V and +3.3V from the CompactPCI backplane.



Caution! The CV1 is not compatible with a 64-bit backplane.

Because of user I/O routed through cPCI_J2, the CV1 is not pin-compatible with a 64-pin CompactPCI backplane. Therefore, severe damage could result to both the CV1 or other boards installed on the backplane from trying to install the CV1 into a 64-bit backplane.

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2.4 Installation

2.4.1 Convection-cooled CV1 Installation

1. Remove the CV1 from the static-safe envelope (*see "E.S.D. Caution" on page 2-1*).
2. Install a PMC module per manufacturers instructions as shown in Figure 2-2 on page 2-3. Please refer to the Errata concerning PMC component height clearance (*see "Zero Component Height Non-Compliance" on page E-1*).

   NOTE: The PMC site supports 32-bit, 33/66MHz PMC modules with +3.3V VIO.

3. Install the CV1 in a 3U convection-cooled chassis with a 32-bit CompactPCI backplane.
4. Slide the CV1 into the slot guide, applying even pressure to the front panel and lower extraction handles. Be careful not to bend connector pins.
5. Push up on the lower extraction handle to seat the CompactPCI connectors in the backplane connectors. The tab on the extraction handle should "click" when the board is locked into the chassis.
6. Tighten the large screw on the front panel and the small screw embedded in the extraction handle to secure the CV1 to the chassis.
7. Apply power to the chassis.

NOTE: The CV1 can be installed in a system controller or peripheral slot. If the CV1 is not installed in a system slot, a system controller card must be installed in the system slot to supply a PCI reference clock to CV1.

2.4.2 Conduction-cooled CV1 Installation

1. Remove the CV1 from the static-safe envelope (*see "E.S.D. Caution" on page 2-1*).
2. Install a PMC module per manufacturers instructions as shown in Figure 2-1 on page 2-3. Please refer to the Errata concerning PMC component height clearance (*see "Zero Component Height Non-Compliance" on page E-1*).

   NOTE: The PMC site supports 32-bit, 33/66MHz PMC modules with +3.3V VIO.

3. Install the CV1 in a 3U conduction-cooled chassis with a 32-bit CompactPCI backplane.
4. Slide the CV1 into the slot guide, applying even pressure to the upper and lower extraction handles. Be careful not to bend connector pins.
5. Tighten the CardLock™ to 96inch-ounces (6 in-lbs) (max.) using a 3/32-inch hex driver. This secures the CV1 in the system chassis and ensures proper heat conduction. Do not overtighten
6. Apply power to the chassis.

NOTE: The CV1 can be installed in a system controller or peripheral slot. If the CV1 is not installed in a system slot, a system controller card must be installed in the system slot to supply a PCI reference clock to CV1.

NOTE: Since the CV1 does not route any I/O to the front panel, it will be necessary to have either the optional CV1-TM companion board which provides rear-panel serial connectors or a custom serial cable connected to the cPCI backplane. Serial port COM1 pinouts are listed in cPCI_J2 Pin Assignments on page 3-4.

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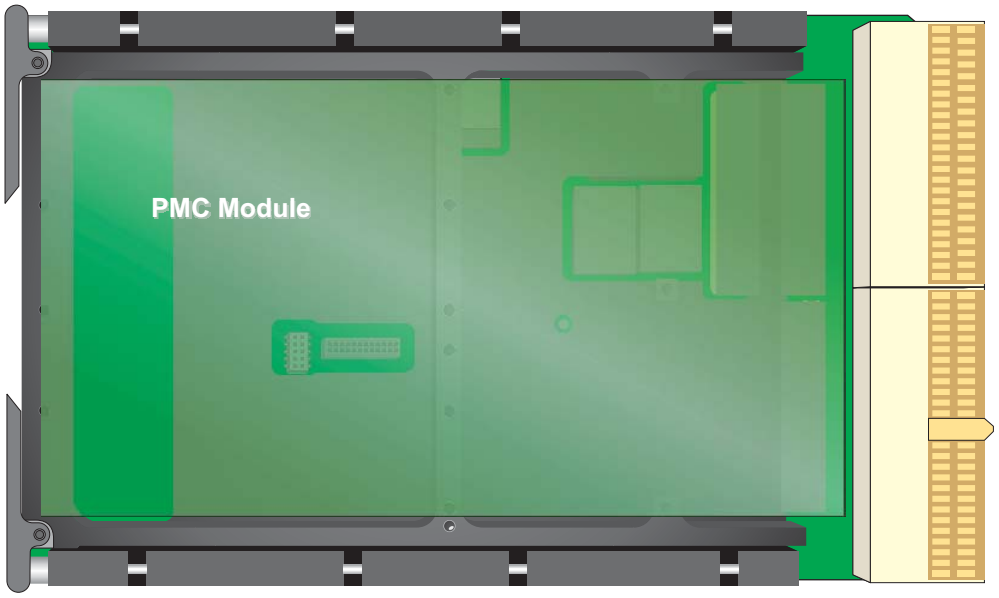


Figure 2-1 CV1 conduction-cooled version with PMC installed

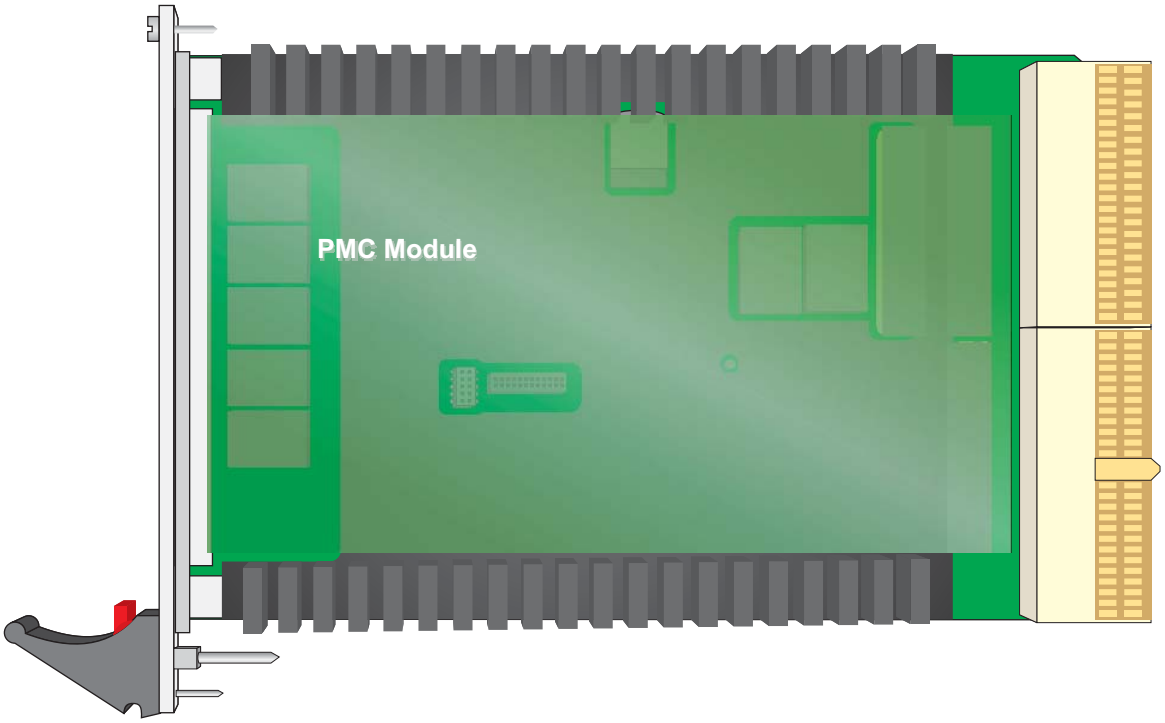


Figure 2-2 CV1 convection-cooled version with PMC installed

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2.5 U-Boot Utility

The CV1 includes a universal boot loader (U-Boot) utility that is pre-installed in Flash ROM. U-Boot is designed to work with any operating system including Linux and VxWorks® and performs the following functions:

- Load the O/S kernel from Ethernet, user flash area
- Program the user flash
- Program the boot flash (self update)
- Load the O/S kernel from user flash
- Set the Real-Time Clock
- Save boot parameters in NVRAM
- Configure the MV64460 Memory Controller

2.5.1 Installation

The CV1 is shipped with U-Boot pre-installed in flash memory.

2.5.2 Initialization

The CV1 has been initialized during production and testing.

2.5.3 Commands

The following is a summary of commands the U-Boot utility uses for the CV1:

`?`	alias for ‘help’
`autoscr`	runs script from memory
`base`	prints or set address offset
`bdinfo`	prints Board Info structure
`boot`	boots default, e.g., run ‘`bootcmd`’
`bootd`	boots default, e.g., run ‘`bootcmd`’
`bootelf`	boots from an ELF image in memory
`bootm`	boots application image from memory
`bootp`	boots image from the network using BootP/TFTP protocol
`bootvx`	boots VxWorks from an ELF image
`cmp`	compares memory
`coninfo`	prints console devices and information
`cp`	copies memory
`crc32`	calculates checksum
`date`	gets / sets / resets date and time
`echo`	echoes arguments to console
`erase`	erases flash memory
`flinfo`	prints flash memory information

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`to`	starts application at address ‘addr’
`help`	prints online help
`iminfo`	prints header information for application image
`imls`	lists all images found in flash
`loadb`	loads binary file over serial line (kermit mode)
`loads`	loads S-Record file over serial line
`loop`	performs infinite loop on address range
`md`	displays memory
`mm`	modifies memory (auto-incrementing)
`mtest`	tests RAM
`mw`	writes memory (fill)
`nm`	modifies memory (constant address)
`ping`	sends ICMP ECHO REQUEST to network host
`printenv`	prints environment variables
`protect`	enables or disable flash write-protect
`rarpboot`	boots image from network using RARP/TFRP protocol
`reset`	performs RESET of the CPU
`run`	runs commands in an environment variable
`saveenv`	saves environment variables to a persistent storage
`setenv`	sets environment variables
`sleep`	delays execution for some time
`tfpboot`	boots image from network using TFTP protocol
`version`	prints monitor version

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2.5.4 Information Commands

The following U-Boot commands provide information

bdinfo

```
CV1=> help bdinfo
```

`bdinfo` – prints board information used by U-Boot, such as memory addresses and sizes, clock frequencies and MAC addresses.

coninfo

```
CV1=> help coninfo
```

`cp [.b, .w, .l] source target count`

– displays console I/O device information.

flinfo

```
CV1=> help flinfo
```

`flinfo`

– prints information for all flash memory banks.

`flinfo N`

– prints information for flash memory bank # N.

iminfo

```
CV1=> help iminfo
```

`iminfo addr [addr ...]`

– prints header information for application image starting at address ‘addr’ in memory; this includes verification of the image contents (magic number, header and payload checksums)

imls

```
CV1=> help imls
```

`imls`

– prints information about all images found at sector boundaries in flash

help

```
CV1=> help
```

`help [command ...]`

– shows help information (for ‘command’)

– ‘help’ prints online help for the monitor commands

– without arguments, it prints a short usage message for all commands

– to get detailed information about specific commands, type ‘help’ with one or more command names as arguments

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2.5.5 Memory Commands

base

```
CV1=> help base
```

`base`	prints address offset from memory commands
`base off`	sets address offset for memory commands to ‘off’

crc32

```
CV1=> help crd32
```

```
crc32 address count [addr]
```

– calculates CRC32 checksum [save at addr]

cmp

```
CV1=> help cmp
```

```
cmp [.b, .w, .l] adder1 addr2 count
```

– compares memory

cp

```
CV1=> help cp
```

```
cp [.b, .w, .l] source target count
```

– copies memory

md

```
CV1=> help md
```

```
md [.b, .w, .l] address [# of objects]
```

– displays memory

mm

```
CV1=> help mm
```

```
mm [.b, .w, .l] address
```

– modifies memory, automatically increments address

mtest

```
CV1=> help mtest
```

```
mtest [start [end [pattern]]]
```

– performs simple RAM read/write test

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mw

```
CV1=> help mw
```

```
mw [.b, .w, .l] address value [count]
```

– perform memory write

nm

```
CV1=> help nm
```

```
nm [.b, .w, .l] address
```

– modifies memory, read and keep address

loop

```
CV1=> help loop
```

```
loop [.b, .w, .l] address number_of_objects
```

– performs loop on a set of addresses

2.5.6 Flash Memory Commands

erase

```
CV1=> help erase
```

```
erase start end
```

– erases flash from addr ‘start’ to addr ‘end’

```
erase N:SF [-SL]
```

– erases sectors SF–SL in flash bank # N

```
erase bank N
```

– erases flash bank # N

```
erase all
```

– erases all flash banks

protect

```
CV1=> help protect
```

```
protect on start end
```

– protects flash from addr ‘start’ to addr ‘end’

```
protect on N:SD [-SL]
```

– protects sectors SF–SL in flash bank # N

```
protect on bank N
```

– protects flash bank N

```
protect on start all
```

– protects all flash banks

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`protect off start end`

– enables writes to flash from addr ‘start’ to addr ‘end’

`protect on N:SD [-SL]`

– enables writes to sectors SF–SL in flash bank # N

`protect on bank N`

– enables writes to flash bank N

`protect on start all`

– enables writes to all flash banks

2.5.7 Execution Control Commands

boot

```
CV1=> help boot
```

bootm

```
CV1=> help bootm
```

`bootm [addr [arg...]]`

– boots application image stored in memory passing argument ‘arg ...’; when booting a Linux kernel, ‘arg’ can be the address of an initrd image

go

```
CV1=> help go
```

`go addr[arg ...]`

– starts application at address ‘addr’ passing ‘arg’ as arguments

2.5.8 Download Commands

bootp

```
CV1=> help bootp
```

`bootp [loadAddress] [bootfilename]`

bootelf

```
CV1=> help bootelf
```

`bootelf [address]`

– loads address of ELF image

bootvx

```
CV1=> help bootvx
```

`bootvx [address]`

– loads address of VxWorks ELF image

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loadb

```
CV1=> help loadb
```

```
loadb [off] [baud]
```

– loads binary file over serial line with offset ‘off’ and baud rate ‘baud’

loads

```
CV1=> help loads
```

```
loads [off] [baud]
```

– loads S-Record fileover serial line with offset ‘off’ and baud rate ‘baud’

rarpboot

```
CV1=> help rarpboot
```

```
rarpboot [loadAddress] [bootfilename]
```

– prints values of all environment variables

tftpboot

```
CV1=> help tftpboot
```

```
tftpboot [loadAddress] [bootfilename]
```

2.5.9 Environment Variables Commands

printenv

```
CV1=> help printenv
```

```
printenv
```

– prints values of all environment variables

```
printenv name ...
```

– print value of environment variable ‘end’

saveenv

```
CV1=> help saveenv
```

```
saveenv
```

– no help available

setenv

```
CV1=> help setenv
```

```
setenv name value ...
```

– sets environment variable ‘name’ to ‘value...’

```
setenv name
```

– deletes environment variable ‘name’

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run

```
CV1=> help run
```

```
run var [...]
```

– runs the commands in the environment variable(s) ‘var’

bootd

```
CV1=> help bootd
```

```
bootd
```

no help available

2.5.10 Miscellaneous Commands

ping

```
CV1=> help ping
```

```
ping pingaddress
```

date

```
CV1=> help date
```

```
date [MMDDhhmm [CC]YY][.ss]
date reset
```

– without arguments: prints data and time
– with arguments: sets the system date and time
– with ‘reset’ argument: resets the Real-Time Clock

reset

```
CV1=> help reset
```

```
reset
```

– no help available

sleep

```
CV1=> help sleep
```

```
sleep N
```

– delays execution for N seconds (N is _decimal_ !!!!)

version

```
CV1=> help version
```

```
version
```

– no help available

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Chapter 3: Interfaces

3.1 Front Panel

The CV1 convection-cooled front panel includes an extraction handle. The conduction-cooled version does not include a front panel but it does includes upper and lower extraction handles.

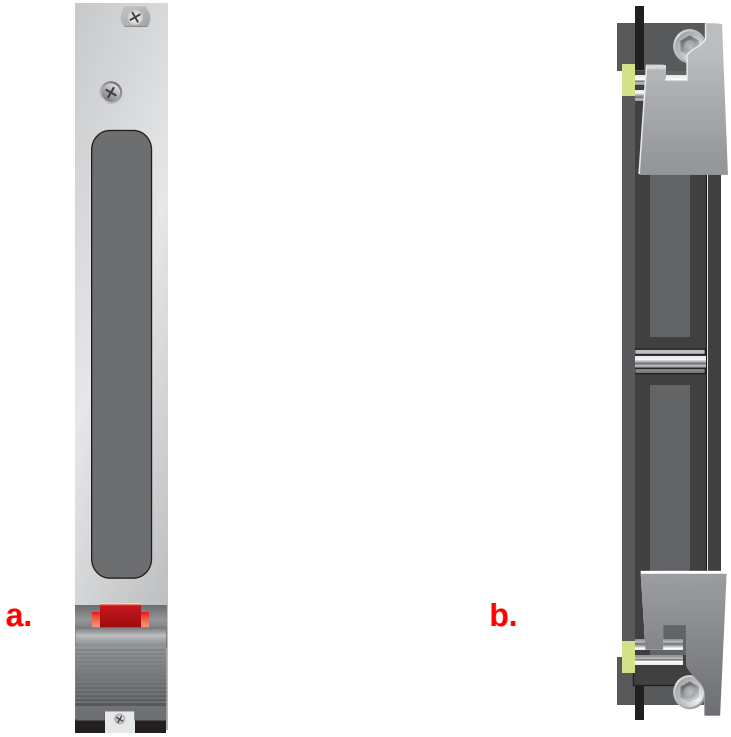


Figure 3-1 Front panels: a. convection-cooled; b. conduction cooled

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3.2 Connectors

3.2.1 Connector Locations

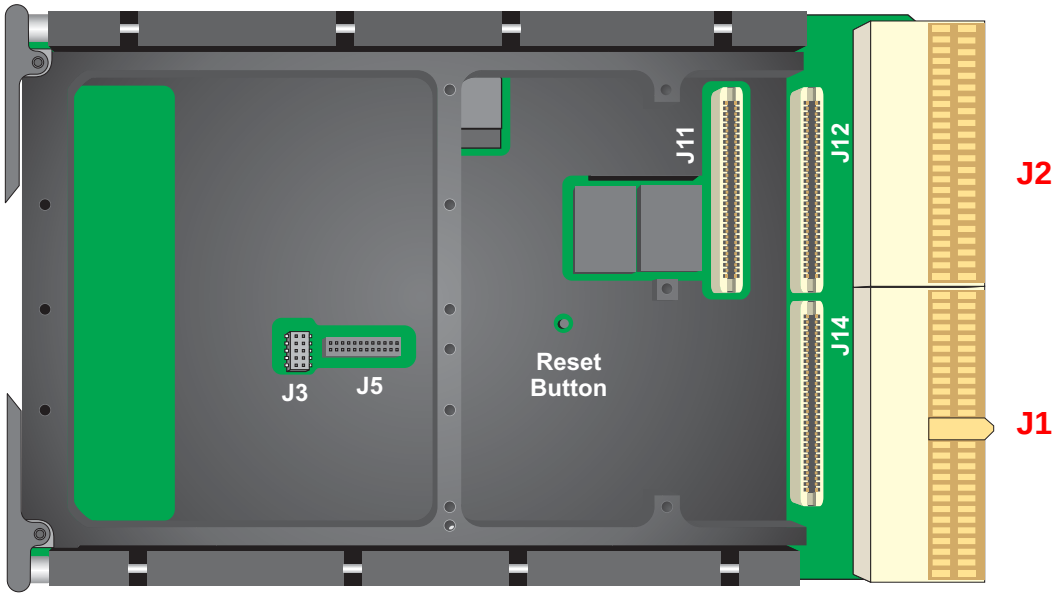


Figure 3-2 CV1 connector locations - conduction-cooled version

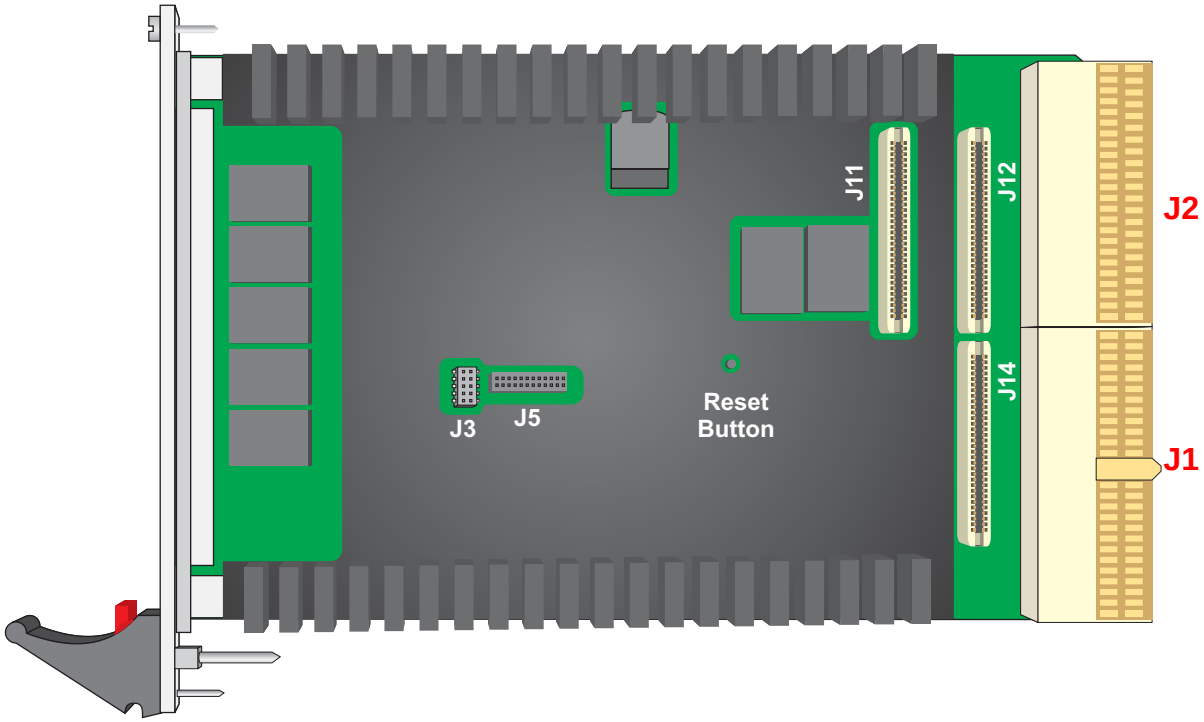


Figure 3-3 CV1 connector locations - convection-cooled version

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Legend

J1, J2 CompactPCI backplane connectors
J3 JTAG connector
J5 COP connector
J11–J14 PMC connectors

3.2.2 CompactPCI Connectors

CPCI_J1 Pin Assignments

Table 3-1 cPCI connector (J1) pin assignments

Pin	A	B	C	D	E	F
J1-25	+5V	REQ64#	ENUM#	+3.3V	+5V	GND
J1-24	AD1	+5V	VIO	AD0	ACK64#	GND
J1-23	+3.3V	AD4	AD3	+5V	AD2	GND
J1-22	AD7	GND	+3.3V	AD6	AD5	GND
J1-21	+3.3V	AD9	AD8	M66EN	C/BE0#	GND
J1-20	AD12	GND	VIO	AD11	AD10	GND
J1-19	+3.3V	AD15	AD14	GND	AD13	GND
J1-18	SERR#	GND	+3.3V	PAR	C/BE1#	GND
J1-17	+3.3V	IPMB_SCL	IPMB_SDA	GND	PERR#	GND
J1-16	DEVSEL#	GND	VIO	STOP#	LOCK#	GND
J1-15	+3.3V	FRAME#	IRDY#	BD_SEL#	TRDY#	GND
J1-14						
J1-13						
J1-12						
J1-11	AD18	AD17	AD16	GND	C/BE2#	GND
J1-10	AD21	GND	+3.3V	AD20	AD19	GND
J1-9	C/BE3#	IDSEL	AD23	GND	AD22	GND
J1-8	AD26	GND	VIO	AD25	AD24	GND
J1-7	AD30	AD29	AD28	GND	AD27	GND
J1-6	CPCI_REQ0#	GND	+3.3V	CPCI_CLK0	AD31	GND
J1-5	n/c	n/c	RST#	GND	CPCI_GNT0#	GND
J1-4	n/c	HEALTHY#	VIO	CPCI_INTP	CPCI_INTS	GND
J1-3	INTA#	INTB#	INTC#	+5V	INTD#	GND
J1-2	J1_TCK	+5V	J1_TMS	J1_TDO	J1_TDI	GND
J1-1	+5V	-12V	J1_TRST#	+12V	+5V	GND

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cPCI_J2 Pin Assignments

Table 3-2 CompactPCI connector (J2) pin assignments

Pin	A	B	C	D	E	F
J2-22	GA4	GA3	GA2	GA1	GA0	GND
J2-21	CPCI_CLK6	GND	COM2_TXD+	COM2_TXD-	COM1_TXD	GND
J2-20	CPCI_CLK5	GND	COM2_TXC+	COM2_TXC-	COM1_RXD	GND
J2-19	GND	GND	COM2_RXD+	COM2_RXD-	EM_BOOTSEL#	GND
J2-18	PMC_1	PMC_2	COM2_RXC+	COM2_RXC-	ROM_WP#	GND
J2-17	PMC_3	PMC_4	CPCI_PRST#	CPCI_REQ6#	CPCI_GNT6#	GND
J2-16	PMC_5	PIMC_6	CPCI_DEG#	GND	BATT+	GND
J2-15	PMC_7	PMC_8	CPCI_FAL#	CPCI_REQ5#	CPCI_GNT5#	GND
J2-14	PMC_9	PMC_10	GPIO 0	GPIO 5	BIT_PASS	GND
J2-13	PMC_11	PMC_12	GPIO 1	GPIO 6	NMI# / GPIO 8	GND
J2-12	PMC_13	PMC_14	GPIO 2	GPIO 7	PROC_FAIL / GPIO 9	GND
J2-11	PMC_15	PMC_16	GPIO 3	ETH1_DA+	ETH1_DC+	GND
J2-10	PMC_17	PMC_18	GPIO 4	ETH1_DA-	ETH1_DC-	GND
J2-9	PMC_19	PMC_20	PMC_30	ETH1_DB+	ETH1_DD+	GND
J2-8	PMC_21	PMC_22	PMC_33	ETH1_DB-	ETH1_DD-	GND
J2-7	PMC_23	PMC_24	PMC_36	ETH0_DA+	ETH0_DC+	GND
J2-6	PMC_25	PMC_26	PMC_38	ETH0_DA-	ETHI0_DC-	GND
J2-5	PMC_27	PMC_28	PMC_50	ETH0_DB+	ETH0_DD+	GND
J2-4	VIO	PMC_29	PMC_52	ETH0_DB-	ETH0_DD-	GND
J2-3	CPCI_CLK4	GND	CPCI_GNT3#	CPCI_REQ4#	CPCI_GNT4#	GND
J2-2	CPCI_CLK2	CPCI_CLK3	CPCI_SYSEN#	CPCI_GNT2#	CPCI_REQ3#	GND
J2-1	CPCI_CLK1	GND	CPCI_REQ1#	CPCI_GNT1#	CPCI_REQ2#	GND

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3.2.3 PMC Connectors

Table 3-3 PMC connectors (PMC_J11/PMC_J12) pin assignments.

PMC_J11				PMC_J12			
Pin	**Assignment**	**Pin**	**Assignment**	**Pin**	**Assignment**	**Pin**	**Assignment**
1	BP_TCK	2	-12V	1	+12V	2	BP_TRST#
3	GND	4	PMC_INTA#	3	BP_TMS	4	PMC_TDO
5	PMC_INTB#	6	PMC_INTC#	5	PMC_TDI	6	GND
7	n/c	8	+5V	7	GND	8	n/c
9	PMC_INTD#	10	n/c	9	n/c	10	n/c
11	GND	12	n/c	11	BUSMODE2# *	12	+3.3V
13	PMC_CLK	14	GND	13	PCI_RST#	14	BUSMODE3# **
15	GND	16	PCI0_GNT0#	15	+3.3V	16	BUSMODE4# **
17	PCI0_REQ0#	18	+5V	17	n/c	18	GND
19	+3.3V (VIO)	20	PCI0_AD31	19	PCI0_AD30	20	PCI0_AD29
21	PCI0_AD28	22	PCI0_AD27	21	GND	22	PCI0_AD26
23	PCI0_AD25	24	GND	23	PCI0_AD24	24	+3.3V
25	GND	26	PCI0_C/BE3#	25	PMC_IDSEL	26	PCI0_AD23
27	PCI0_AD22	28	PCI0_AD21	27	+3.3V	28	PCI0_AD20
29	PCI0_AD19	30	+5V	29	PCI0_AD18	30	GND
31	+3.3V (VIO)	32	PCI0_AD17	31	PCI0_AD16	32	PCI0_C/BE2#
33	PCI0_FRAME#	34	GND	33	GND	34	n/c
35	GND	36	PCI0_IRDY#	35	PCI0_TRDY#	36	+3.3V
37	PCI0_DEVSEL#	38	+5V	37	GND	38	PCI0_STOP#
39	GND	40	PMC_LOCK#	39	PCI0_PERR#	40	GND
41	+3.3V *	42	+3.3V *	41	+3.3V	42	PCI0_SERR#
43	PCI0_PAR	44	GND	43	PCI0_C/BE1#	44	GND
45	+3.3V (VIO)	46	PCI0_AD15	45	PCI0_AD14	46	PCI0_AD13
47	PCI0_AD12	48	PCI0_AD11	47	PCI0_M66EN	48	PCI0_AD10
49	PCI0_AD9	50	+5V	49	PCI0_AD8	50	+3.3V
51	GND	52	PCI0_C/BE0#	51	PCI0_AD7	52	n/c
53	PCI0_AD6	54	PCI0_AD5	53	+3.3V	54	n/c
55	PCI0_AD4	56	GND	55	n/c	56	GND
57	+3.3V (VIO)	58	PCI0_AD3	57	n/c	58	n/c
59	PCI0_AD2	60	PCI0_AD1	59	GND	60	n/c
61	PCI0_AD0	62	+5V	61	PMC_ACK64#	62	+3.3V
63	GND	64	PMC_REQ64#	63	GND	64	+3.3V ***

* Pulled to +3.3V through 1k-ohm resistor.
** Tied directly to ground
*** Pulled to +3.3V through 4.7k-ohm resistor

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Table 3-4 PMC connector (PMC_J14) pin assignments

PMC_J14

Pin	Assignment	Pin	Assignment
1	PMC_1	2	PMC_2
3	PMC_3	4	PMC_4
5	PMC_5	6	PMC_6
7	PMC_7	8	PMC_8
9	PMC_9	10	PMC_10
11	PMC_11	12	PMC_12
13	PMC_13	14	PMC_14
15	PMC_15	16	PMC_16
17	PMC_17	18	PMC_18
19	PMC_19	20	PMC_20
21	PMC_21	22	PMC_22
23	PMC_23	24	PMC_24
25	PMC_25	26	PMC_26
27	PMC_27	28	PMC_28
29	PMC_29	30	PMC_30
31	N/C	32	n/c
33	PMC_33	34	n/c
35	n/c	36	PMC_36
37	n/c	38	PMC_38
39	n/c	40	n/c
41	n/c	42	n/c
43	n/c	44	n/c
45	n/c	46	n/c
47	n/c	48	n/c
49	n/c	50	PMC_50
51	n/c	52	PMC_52
53	n/c	54	n/c
55	n/c	56	n/c
57	n/c	58	n/c
59	n/c	60	n/c
61	n/c	62	n/c
63	n/c	64	n/c

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3.2.4 JTAG Header (J3)

The CV1 includes an on-board 2 x 5 JTAG Scan chain header (J3).

Table 3-5 JTAG header (J3) pin assignment

Pin	Assignment	Pin	Assignment
1	TDO	2	+3.3V
3	TCK	4	TMS
5	GND	6	GND
7	TRST#	8	TDI
9	n/c	10	FLASH_WE#

3.2.5 COP Header (J5)

The CV1 provides a 2 x 10 header (J5) for accessing the MPC7447A Common On-chip Processor (COP) function. This is a +2.5V interface.

Table 3-6 COP port header (J5) pin assignment

Pin	Assignment	Pin	Assignment
1	COP_TDO	2	COP_QACK#
3	COP_TDI	4	COP_TRST#
5	COP_RUN_STOP#	6	VDD_SENSE
7	COP_TCK	8	COP_CKSTP_IN#
9	COP_TMS	10	n/c
11	COP_SRESET#	12	GND
13	COP_HRESET#	14	KEY
15	COP_CKSTP_OUT#	16	GND
17	n/c	18	n/c
19	n/c	20	n/c

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Chapter 4: Functional Blocks

4.1 PowerPC G4 Processor

The CV1 is driven by the MPC7447A G4 PowerPC processor. The MPC7447A is a high-performance, superscaler, low-power, 32-bit processor based on PowerPC RISC architecture. The CV1 offers the MPC7447A with a core processor speed of 1GHz. The MPC7447A includes separate 32kB L1 instruction and data caches and an on-chip 512kB L2 cache.

4.1.1 Processor Interface

The MV64460 System Controller provides a CPU interface to the MPC7447A G4 PowerPC processor through a 64-bit 167MHz MPX system bus. The system bus provides address decoding, data transfer operations, and interrupt signaling.

4.2 DDR SDRAM

The MV64460 System Controller includes a DDR SDRAM Controller that drives a 72-bit (64-bit data with 8-bit ECC) 167MHz Memory Bus. The CV1 is configured for 256MB of system memory.

Full Error Checking and Correction (ECC) is also provided with one-bit error detect and correct; multiple bit error detect and report functions.

4.3 Flash Memory

The CV1 includes one bank of 128MB soldered flash ROM. The flash chips are located on the 32-bit asynchronous parallel Device Bus, mastered by the MV64460 System Controller.

4.3.1 Flash Write Protection

Operating firmware can write and erase data from the flash devices. Each flash device provides ‘chip erase’ functionality as well as separate erase and write protection of sectors. The CV1 provides several write-protect mechanisms to prevent boot code data loss during power cycling and system initialization. Flash write-protection functions are ORed so that any source of write protection can override other functions of that area of flash memory.

The CV1 provides the following write-protection options:

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External Write-Protect: the ROM_WP# signal is provided at the backplane (cPCI_J2 pin E18) to enable write-protection for the entire flash ROM.

If the ROM_WP# signal is asserted (active low), all write/erase functions are disabled.
If the ROM_WP# signal is de-asserted, all write/erase functions are enabled.

SBS Technologies offers an optional CV1-TM companion board that provides a ROM_WP# header/jumper for asserting the ROM_WP# signal.

Device Write-Protect: the CPLD Control register bit—FLASH_WP (bit 7) (*see "Control Register" on page 5-5*) provides an internal mechanism for firmware to configure flash write-protection during hardware reset. The FLASH_WP bit is active (write-protect enabled) during hardware reset, to prevent inadvertent write accesses to the Flash ROM devices until after the CV1 has been initialized. Firmware must disable these bits before performing any write or erase operations.

Boot Area Write-Protect: the CPLD Control register bit—BOOT_FLASH_WP (bit 9) (*see "Control Register" on page 5-5*) provides a mechanism for firmware to configure write-protection for the boot area (upper 8MB) of flash ROM, to protect boot code. Firmware must disable this bit before performing any write or erase operations.

Permanent Write-Protect: a resistor site is provided to permanently enable Flash ROM write-protection.

NOTE: The resistor option is configured during the manufacturing process on a special-order basis. This is not a user-configurable option.

4.3.2 Boot Code Selection

The EM_BOOTSEL# signal provided at the backplane (cPCI_J2 pin E19) selects which boot code is executed on power-up or after reset. If EM_BOOTSEL# is inactive (high) then the code in the user boot area is executed, provided that a boot description header with a valid checksum is detected. If EM_BOOTSEL# is active, the user boot code is not executed. The state of EM_BOOTSEL# can be read from the CPLD Configuration Register bit (bit 9) (*see "Configuration Register" on page 5-3*).

SBS Technologies offers an optional CV1-TM companion board that provides a EM_BOOTSEL# header/jumper for asserting the EM_BOOTSEL# signal.

4.4 PCI Buses

The CV1 includes two PCI buses controlled by the MV64460 System Controller's PCI Bus interface:

PCI Bus 0 is dedicated to the PMC site and is configured for 32-bit 33/66MHz operation.

PCI Bus 1 is dedicated to the PCI 6254 cPCI Bridge and is configured for 32-bit 33/66MHz operation.

4.5 Device Bus

The CV1 provides a 32-bit asynchronous Device Bus mastered by the MV64460 System Controller. The Device Bus provides access to the following devices:

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- CPLD
- NVRAM/RTC
- Flash memory

4.6 SMBus

The MV64460 System Controller includes a SMBus Host Controller to master an on-board IIC serial interface. The SMBus hosts the following slave devices:

- Temperature Sensor
- MV64460 Configuration EEPROM
- Board Configuration EEPROM

4.7 Gigabit Ethernet

The MV64460 System Controller includes three Ethernet Media Access Controllers (MACs). The CV1 uses two of these MACs to provide 10/100/1000 Base-TX Ethernet connectivity. Both ports are routed to the cPCI backplane through the cPCI_J2 connector.

4.8 Serial I/O

The MV64460 System Controller includes two Multi-Protocol Serial Controllers (MPSC) which provide the CV1 with two serial ports: RS-232 (COM1) and RS-422 (COM2) to the cPCI backplane through the cPCI_J2 connector. The MAX3232E Transceiver provides the RS-232 line drivers and receivers with 15KV ESD protection for COM1. The COM1 interface supports only transmit and receive data.

The RS-422 (COM2) interface supports synchronous and asynchronous operation. An external differential receiver and an external differential line-driver provide the interface to the backplane pins for the COM2 port.

4.9 General Purpose I/O

The MV64460 System Controller provides 10 GPIO signals (8 dedicated; two shared) to the cPCI backplane through the cPCI_J2 connector. The CPLD provides GPIO registers to define the GPIO signals (*see “GPIO Registers” on page 5-9*) including register bits to select the function of shared GPIO signals.

The GPIO signals are allocated as follows:.

Dedicated GPIO Signals		Shared GPIO Signals
GPIO 0	GPIO 4	GPIO 8 / NMI#
GPIO 1	GPIO 5	GPIO 9 / PROCFAIL
GPIO 2	GPIO 6	
GPIO 3	GPIO 7	

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4.10 Counter/Timers

The MV64460 System Controller provides four 32-bit general-purpose timers. The 32-bit timers can be cascaded to create two 64-bit timers. The MV64460 includes registers for configuring the timers to a maximum duration of 32.2s for each 32-bit counter.

4.10.1 Watchdog Timer

The MV64460 also includes a 32-bit programmable watchdog timer. It has a maximum interval duration of approximately 32 seconds. The watchdog timer can generate a System Management Interrupt (SMI#) if the timer is allowed to expire.

4.11 CPLD

The CV1 includes a CPLD that provides access to major components on CV1. The CPLD includes configuration, control, and status registers for interrupts, interrupt masking, and flash write-protection as defined in Section 5.4 CPLD Registers on page 5-2. The CPLD also includes registers for GPIO port configuration and control.

4.11.1 System Management Interrupt

The CPLD can assert the System Management Interrupt (SMI) input to the processor. The SMI is a level-sensitive processor input which the CPLD asserts if one or more of the following interrupt sources are asserted:

- Backplane NMI (maskable)
- Backplane DEG (maskable)
- Backplane FAL (maskable)
- MV64460 NMI watchdog timer-expired (maskable)

The SMI receives the NMI#, DEG# and FAL# signals from the backplane as interrupt sources. Each of these signals are maskable through the CPLD Control Register (*see “Control Register” on page 5-5*). These mask bits are set after reset. The MV64460 _WD_NMI# signal is maskable through the CPLD Interrupt Mask Register (*see “Interrupt Mask Register” on page 5-7*).

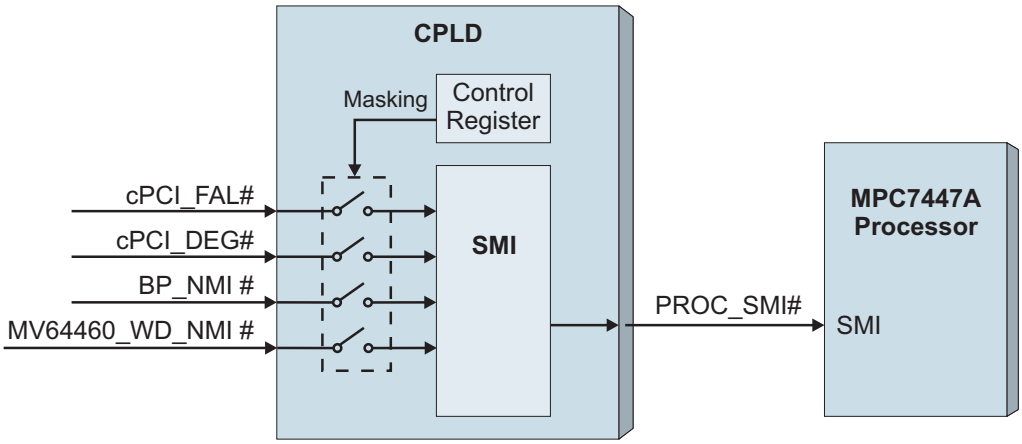


Figure 4-1 SMI processing

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4.12 NVRAM/RTC

The CV1 employs the STK17T88 device to provide 32kB of non-volatile SRAM and a real-time clock feature. The CV1 includes a 32.768kHz crystal oscillator for the RTC. An external +3.3V battery backup can be connected to the RTC through the BATT+ signal from the cPCI backplane on the cPCI_J2 (pin E16) connector.

4.13 CompactPCI Backplane Bridge

The CV1 implements the PCI 6254 Dual Mode cPCI Bridge to transfer PCI data between the cPCI backplane and MV64460 System Controller. The PCI 6254 supports 32-bit-bit data transfers at either 33 or 66MHz bus clocks.

The PCI 6254 is configured to operate in one of two modes: Universal Transparent Mode and Universal Non-transparent Mode. When the CV1 is installed in a system slot, it functions as a system controller and the PCI 6254 operates in the Universal Transparent Mode. In this mode, PCI transactions pass transparently from the primary interface to the secondary interface.

When the CV1 is installed in a peripheral slot, the PCI 6254 operates in the Universal Non-transparent mode. To the PCI host, which would be located on the system controller board, the PCI 6254 appears to be another PCI device. The mode in which the PCI 6254 operates is controlled by the SYSEN# signal from the backplane. SYSEN# is asserted when the CV1 is installed in a system slot and de-asserted when the CV1 is installed in a peripheral slot.

In transparent mode, the PCI 6254 provides bus arbitration logic for seven peripheral slots at the cPCI backplane. The PCI 6254 supports +5V and +3.3 VIO.

4.14 PMC Site

The CV1 hosts one single-wide PMC site that include the following features:

a. PMC site supports standard IEEE 1386.1 PMC modules
b. PMC site is located on dedicated 32-bit 33/66 MHz PCI Bus 0. PCI Bus 0 supports only +3.3V VIO.
c. PMC_P14 I/O signals are routed to cPCI_J2.
d. PMC site is intended for low capacity I/O. It can host a PMC module with power ratings of 7.5W or less.
e. PMC component height may conflict with components in zero component height area (*see “Zero Component Height Non-Compliance” on page E-1*).

4.15 Interrupt Circuitry

The CV1 uses CPLD registers, as reflected in the Interrupt Mask and Status registers, to capture external (cPCI and PMC) interrupts and board interrupts. When one of these interrupts is asserted, the CPLD generates an interrupt to the MV64460 System Controller MPP interface. The Real-Time Clock interrupt is also routed to the MV64460 MPP interface.

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If one of the MV64460 MPP pins assigned as an interrupt is asserted, it sets the corresponding pin in the Interrupt Cause register in the MV64460 Interrupt Controller. This causes the Interrupt Controller to assert the CPU _INT interrupt to the MPC7447A processor.

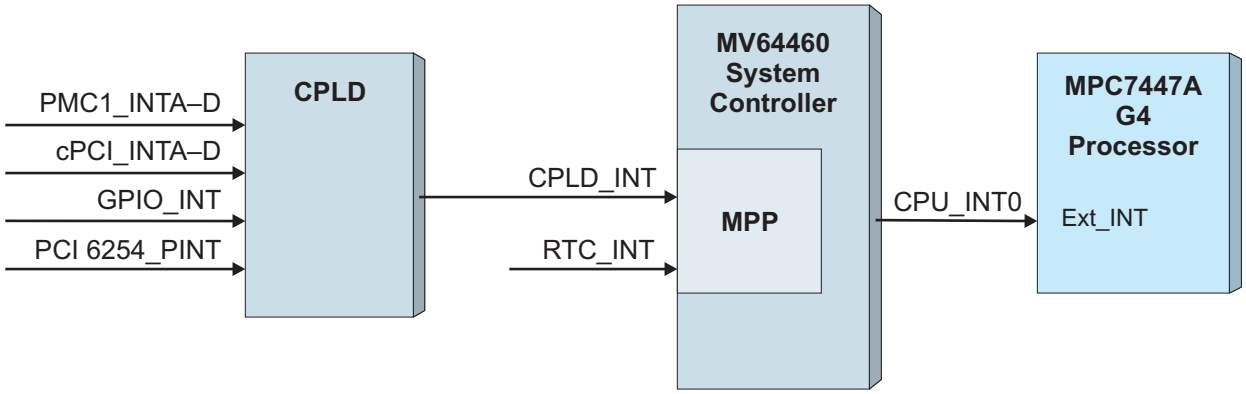


Figure 4-2 Interrupt circuit

4.16 Temperature Sensor

The CV1 includes a MAX6658 Dual Channel Temperature Sensor that monitors the MPC7447A G4 processor temperature through an on-die thermal diode and board temperature through a sensor built into the MAX6658. If the processor exceeds a programmed threshold temperature, the MAX6658 sends an interrupt to the MV64460 System Controller.

4.17 JTAG/COP

4.17.1 JTAG

The CV1 provides an IEEE 1149.1 (JTAG) Scan chain that can be used to check major components included in the chain for open and short circuits, and continuity. The JTAG Scan chain is driven at +3.3V. The Boundary Scan chain for CV1 includes the following components:

- MPC7447A PowerPC G4 processor
- MV64460 System Controller
- VSC8244 Quad Gigabit Ethernet PHY
- PCI 6254 cPCI Bridge
- CPLD

4.17.2 COP

The CV1 provides a COP Port header (J5) for attaching an emulator to step through application software code. The COP is driven at +2.5V and runs up to 4MHz. A bus switch isolates the processor for the COP interface and is controlled by installing a wire between WP3 and WP8 as shown in Figure 4-4 on page 4-8.

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NOTE: The cPCI backplane JTAG signals and JTAG header signals cannot be used simultaneously.

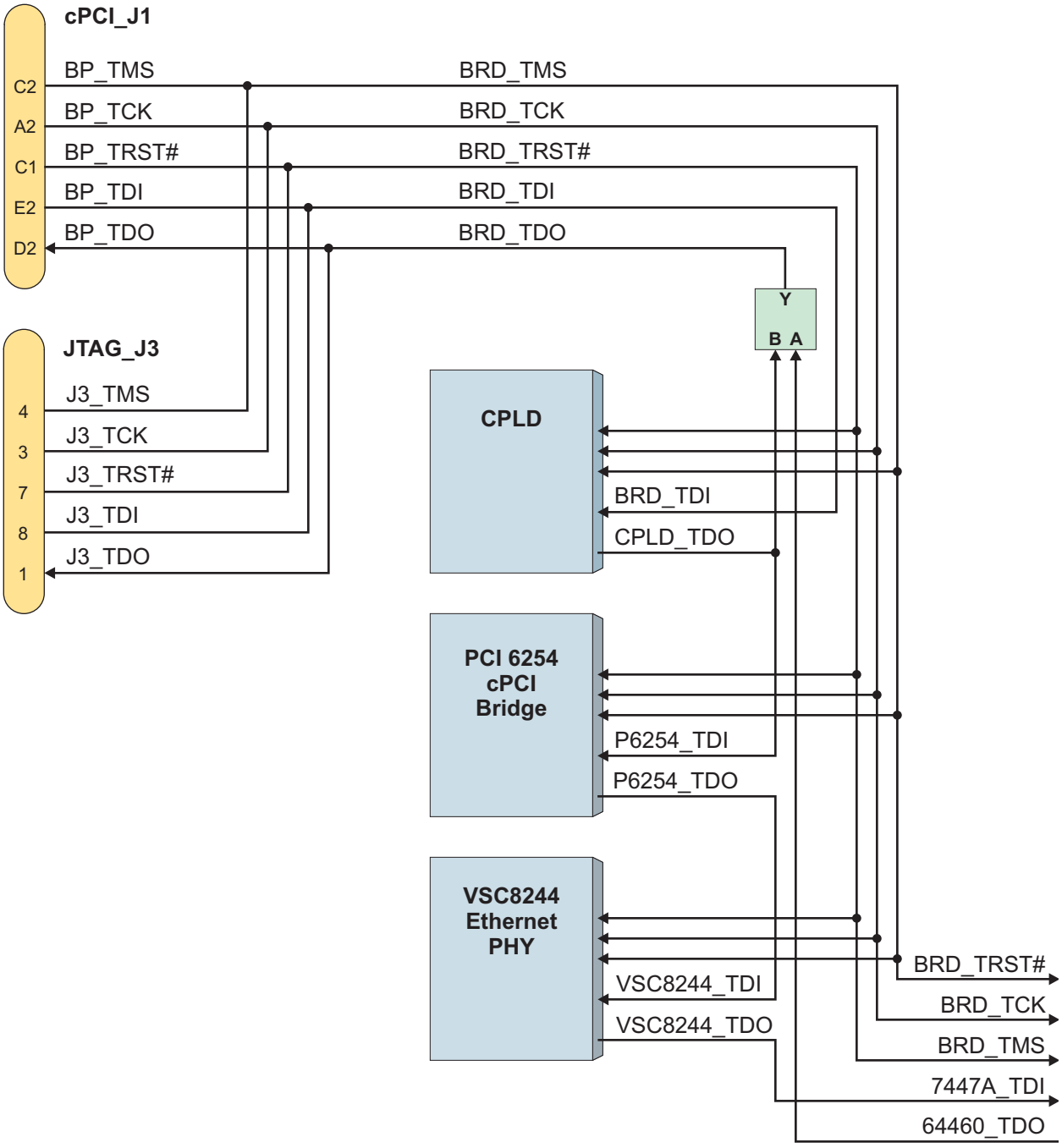


Figure 4-3 JTAG interface configuration

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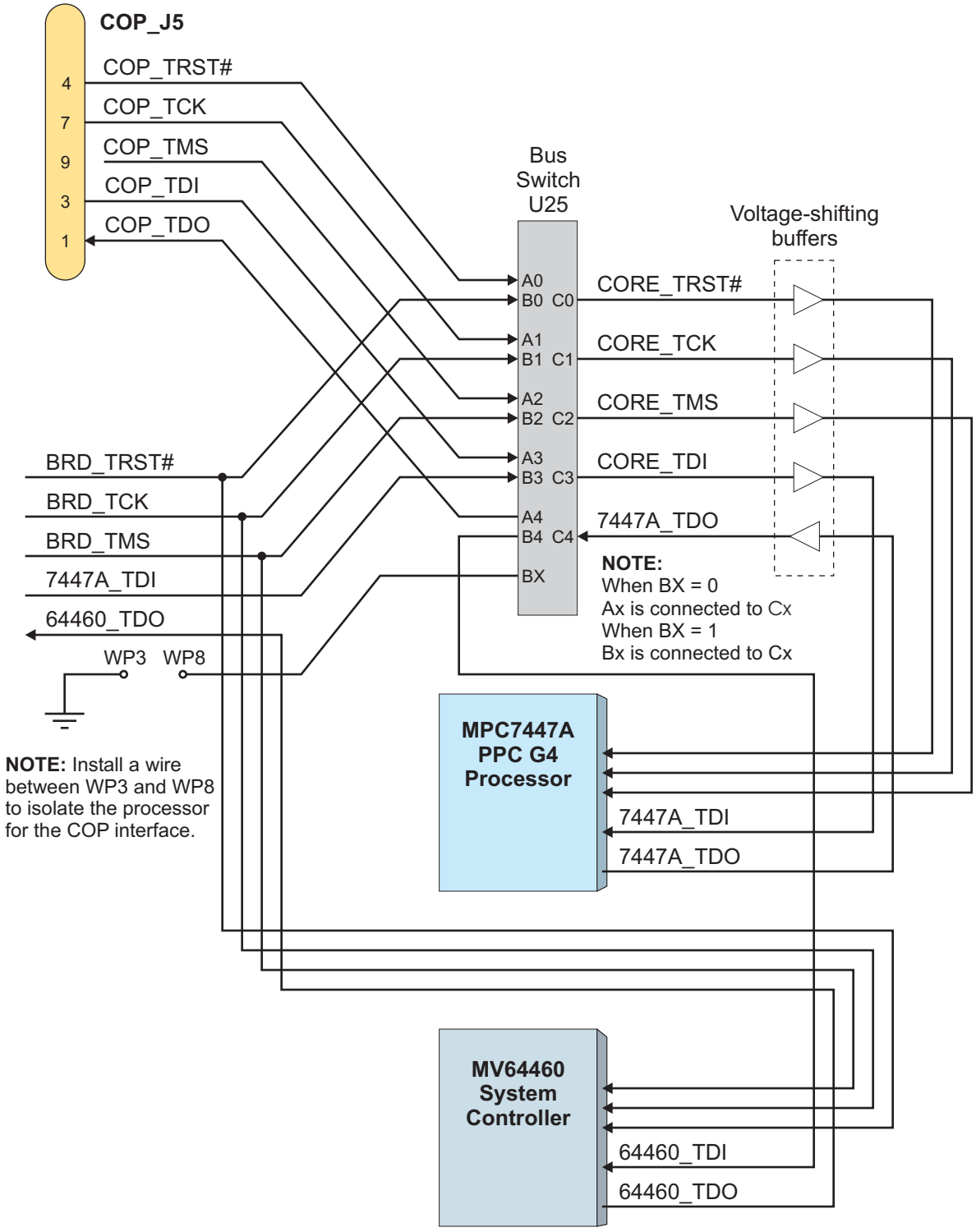


Figure 4-4 COP interface

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Chapter 5: Resources

5.1 PCI Bus Address Assignments

The MV64460 System Controller provides two PCI bus interfaces. PCI Bus 0 is a 32-bit 33MHz bus connected to the PMC site. PCI Bus 1 is 32-bit 33MHz bus connected to the PCI 6254 cPCI Bridge chip.

Table 5-1 summarizes the CV1 PCI bus configurations. The MV64460 System Controller provides arbitration for both buses so they do not require an arbitration number.

Table 5-1 PCI local bus configuration

PCI Bus	Arbitration No.	IDSEL	Device
0	–	AD16	MV64460 PCI I/F 0
0	0	AD17	PMC
1	–	AD16	MV64460 PCI I/F 1
1	0	AD17	PCI 6254 cPCI Bridge

5.2 Device Bus Address Assignments

The CV1 implements an asynchronous 32-bit multiplexed Device Bus, mastered by the MV64460 System Controller with bus control and address decoding provided by the CPLD. Table 5-2 lists the accessible devices and address ranges. Addressing for these devices is according to MV64460 instructions for interfacing 8-bit, 16-bit, and 32-bit devices.

Table 5-2 Device bus devices, access, size and address range

Bank	Device	Access	Size	Address Range
Boot	Flash ROM	32-bit	8MB	0xF800_0000 to 0xFFFF_FFFF
3	Not used	32-bit	8MB	0xF000_0000 to 0xF7FF_FFFF
2	CPLD registers	16-bit	16MB	0xEFFF_0000 to 0xEFFF_FFFF
1	RTC/NVRAM	8-bit	8MB	0xEFFE_0000 to 0xEFFE_FFFF
0	Not used	8-bit	8MB	0xEFFD_0000 to 0xEFFD_FFFF

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5.3 SMBus Address Assignments

The CV1 implements a System Management Bus (SMBus), a two-wire IIC interface that can communicate configuration or status information with other components. The MV64460 System Controller provides the SMBus host controller to three slave ports. Table 5-3 lists the slave devices and their addresses.

Table 5-3 SMBus addressing

Device	Address
MV64460 Configuration Data EEPROM	b1010000
Board Configuration Data EEPROM	b1010001
Temperature sensor	b1001100

5.4 CPLD Registers

The CV1 includes a CPLD to provide programmable logic circuitry for peripheral resources and miscellaneous ‘glue logic’. The CPLD, located on the 32-bit Device Bus, contains 16-bit registers for configuration, status, and control of various functions such as interrupt and interrupt masking, flash write-protection, and GPIO ports status and control. The Default values in the register tables represent values after power-up.

IMPORTANT!: The CPLD must be read as an 8-bit or 16-bit device; 32-bit reads alias the data onto both words of a long word.

5.4.1 Configuration, Status, and Control Registers

CPLD Revision Register

The CPLD Revision Register contains the binary-coded decimal revision number for the current CPLD firmware. It is formatted as a revision number (most significant 8-bits) and version number (least significant 8-bits).

Address offset: 0x00

Access: Read-only

Bits	Field	Description
15 to 8	REV	Revision (major) number
7 to 0	VER	Version (minor) number

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Configuration Register

The Configuration Register provides CV1 configuration information such as system memory size, flash write-protect, and emergency boot select settings.

Address offset: 0x08

Access: Read-only

Bits	Field	Description
15 to 13	Not used	Always read as (0)s
12	BP_ROM_WP	Backplane Flash Write-Protect—indicates whether the flash write-protection signal from the backplane has been asserted. 0 = no backplane write-protection asserted 1 = backplane write-protection asserted
11	PERM_ROM_WP	Permanent Flash ROM Write Protection—indicates whether the permanent flash write-protection option is enabled. 0 = no permanent write-protection enabled 1 = permanent write-protection enabled
10	Not used	Always reads as (0).
9	EMERG_BOOT_SEL	Emergency Boot Select—indicates the state of the emergency boot select signal from the backplane. 0 = emergency boot select signal is inactive 1 = emergency boot select signal is active
8 to 7	MEM_SIZE	SDRAM Memory Size—indicates the installed system memory density. b00 = 256MB b01 = invalid b10 = invalid b11 = invalid
6	Not used	Always read as (0)s
5	SYS_SLOT	System Slot status—indicates whether the CV1 is installed in a system or peripheral slot. 0 = peripheral slot 1 = system slot
4 to 0	GA	cPCI Geographical Address—indicates in which slot the CV1 is installed.

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Status Register

The Status Register provides status information for various subsystems such as reset signal status and PCI local bus speed, as well as flash memory status.

Address offset: 0x0A

Access: Read-only

Bits	Field	Description
15	PROCFAIL	Processor Fail Status—indicates the PROCFAIL signal has been asserted. 0 = no PROCFAIL signal asserted 1 = PROCFAIL signal asserted
14	MV64460_WDOG_NMI	MV64460 Watchdog NMI—indicates the MV64460 watchdog NMI has been asserted. 0 = no MV64460 NMI asserted 1 = MV64460 NMI asserted
13	RTC_HSB	NVRAM Hardware Store Status—indicates whether a hardware data write to the nvSRAM is in progress. 0 = no hardware data write in progress 1 = hardware data write in progress
12	BP_FAL	Backplane cPCI PS Failure—indicates whether a power supply failure signal from the backplane has been asserted. 0 = no FAL signal asserted 1 = FAL signal asserted
11	BP_DEG	Backplane cPCI PS Degradation—indicates whether a power supply degradation signal from the backplane has been asserted. 0 = no DEG signal asserted 1 = DEG signal asserted
10	BP_NMI	Backplane NMI—indicates whether a backplane non-maskable interrupt has been asserted. 0 = no interrupt asserted 1 = interrupt asserted
9	Not used	Always read as (0)s
8	FLASH_BUSY	Flash Busy—indicates whether a program or erase cycle is currently executing in flash. 0 = flash is not busy 1 = flash is busy
7 to 6	Not used	Always read as (0)s
5	PCI0_SPEED	PCI Bus 0 Speed—indicates the PCI Bus 0 clock speed. 0 = 33MHz 1 = 66MHz

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Bits	Field	Description
4	PCI1_SPEED	PCI Bus 1 Speed—indicates the PCI Bus 1 clock speed. 0 = 33MHz 1 = 66MHz
3	Not used	Always read as (0)s
2	PMC_RESET	PMC Reset—indicates whether the installed PMC module has asserted a reset. 0 = no reset asserted 1 = reset asserted
1	CPCI_BRG_PRST	CPCI Bridge Primary-side Reset—indicates a reset from the PCI 6254 Bridge primary interface has been asserted. 0 = no reset asserted 1 = reset asserted
0	CPCI_RESET	CPCI Reset—indicates a backplane PCI reset has been asserted 0 = no reset asserted. 1 = reset asserted

Control Register

The Control Register provides control for various board functions such as resets and flash write-protection settings.

Address offset: 0x10

Access: Read/write

Bits	Field	Default	Description
15	OVR_TEMP_RST_EN	0	Processor Over-temperature Reset Enable—enables the Over-temperature function to reset the CV1. 0 = Over-temperature function not enabled to reset CV1 1 = Over-temperature function enabled to reset CV1
14	BIT_FAIL	1	Built In Test Failure—indicates the status of firmware's Built-In-Test (BIT). 0 = test successful 1 = test has not yet been performed or test failed
13	DISC_WD_NMI_MSK	0	MV64460 Watchdog timer NMI Mask—blocks the NMI interrupt signal triggered by the MV64460's watchdog timer. 0 = enable watchdog NMI signal 1 = disable (mask) watchdog NMI signal

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Bits	Field	Default	Description
12	BP_FAL_MASK	1	Backplane FAL Mask—blocks assertion of SMI by backplane FAL signal. 0 = enable backplane FAL signal 1 = disable (mask) backplane FAL signal
11	BP_DEG_MASK	1	Backplane DEG Mask—blocks assertion of SMI by backplane DEG signal. 0 = enable backplane DEG signal 1 = disable (mask) backplane DEG signal
10	BP_NMI_MASK	1	Backplane NMI Mask—blocks assertion of SMI by backplane NMI signal. 0 = enable backplane NMI 1 = disable (mask) backplane NMI
9	BOOT_FLASH_ WP	1	Boot Flash Write-Protect—asserts write-protection to the emergency boot code area of flash ROM (upper 8MB of flash). 0 = no boot write-protection asserted 1 = boot write-protection asserted
8	Not used	0	Always read as (0)s
7	FLASH_WP	1	Flash Write-protect—asserts flash write-protection. 0 = no flash write-protection asserted 1 = flash write-protection asserted
6	Not used	0	Always read as (0)s
5	ETH_PHY_SOFT RESET	0	Ethernet Soft Reset—asserts a soft reset to the Ethernet PHY. 0 = no soft reset asserted 1 = soft reset asserted to Ethernet PHY
4	ETH_PHY_RESET	0	Ethernet PHY Reset—asserts a reset to the Ethernet PHY. 0 = no reset asserted 1 = reset asserted to Ethernet PHY
3	PCI1_RESET	0	PCI Bus 1 Reset—asserts a reset to PCI Bus 1. 0 = no reset asserted 1 = reset asserted to PCI Bus 1
2	PCI0_RESET	0	PCI Bus 0 Reset—asserts a reset to PCI Bus 0. 0 = no reset asserted 1 = reset asserted to PCI Bus 0
1	Not used	0	Always read as (0)s
0	FLASH_RESET	0	Flash Bank Reset—asserts a reset to flash. 0 = no reset asserted 1 = reset asserted to flash

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5.4.2 Interrupt Registers

The CPLD includes two interrupt registers that provide interrupt status and interrupt blocking (masking).

Interrupt Mask Register

The Interrupt Mask Register provides masking of various interrupt sources.

Address offset: 0x20

Access: Read/write

Bits	Field	Default	Description
15 to 14	Not used	0	Always read as (0)s
13	GPIO_INT_MSK	1	GPIO Line Interrupt Masks (all)—blocks all GPIO line interrupts. 0 = enable interrupts 1 = disable (mask) interrupts
12	Not used (read-only)	0	Always read as 0
11	CPCI_INTD_MSK	1	cPCI INTD Mask—blocks cPCI INTD interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
10	CPCI_INTC_MSK	1	cPCI INTC Mask—blocks cPCI INTC interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
9	CPCI_INTB_MSK	1	cPCI INTB Mask—blocks cPCI INTB interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
8	CPCI_INTA_MSK	1	cPCI INTA Mask—blocks cPCI INTA interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
7 to 4	Not used (read-only)	0	Always read as (0)s
3	PMC_INTD_MSK	1	PMC INTD Mask—blocks PMC INTD interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
2	PMC_INTC_MSK	1	PMC INTC Mask—blocks PMC INTC interrupt. 0 = enable interrupt 1 = disable (mask) interrupt

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Bits	Field	Default	Description
1	PMC_INTB_MSK	1	PMC INTB Mask—blocks PMC INTB interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
0	PMC_INTA_MSK	1	PMC INTA Mask—blocks PMC INTA interrupt. 0 = enable interrupt 1 = disable (mask) interrupt

Interrupt Status Register

The Interrupt Status Register provides current interrupt level (asserted/de-asserted) information.

NOTE: The Interrupt Mask register does not mask the ability to read the interrupt's status in this register.

Address offset: 0x22

Access: Read-only

Bits	Field	Description
15 to 14	Not used	Always reads as (0)s
13	GPIO_INT	GPIO Interrupt 0 = de-asserted 1 = asserted
12	Not used	Always read as 0
11	CPCI_INTD	cPCI INTD (system slot) 0 = de-asserted 1 = asserted
10	CPCI_INTC	cPCI INTC (system slot) 0 = de-asserted 1 = asserted
9	CPCI_INTB	cPCI INTB (system slot) 0 = de-asserted 1 = asserted
8	CPCI_INTA	cPCI INTA (system slot) 0 = de-asserted 1 = asserted
7 to 4	Not used	Always reads as (0)s
3	PMC_INTD	PMC INTD 0 = de-asserted 1 = asserted

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Bits	Field	Description
2	PMC_INTC	PMC INTC 0 = de-asserted 1 = asserted
1	PMC_INTB	PMC INTB 0 = de-asserted 1 = asserted
0	PMC_INTA	PMC INTA 0 = de-asserted 1 = asserted

5.4.3 GPIO Registers

The CPLD provides the GPIO Interrupt Masking, Data, and Control registers for configuring, masking interrupts, and sending/receiving data on the GPIO lines connected to the backplane. The GPIO registers set the following configuration parameters:

- Direction (input or output)
- Output drive type (TTL or open-drain)
- Input polarity (inverted or non-inverted)
- Interrupt masking

When the GPIO lines are configured as outputs, they can be driven as either standard TTL or open-drain (drive-low only). When configured as inputs, the GPIO lines can be treated as positive or negative logic. The selected logic polarity for GPIO inputs affects the value read in the GPIO Data Register and affects which logic level will cause an interrupt assertion.

GPIO Interrupt Mask Register

The GPIO Interrupt Mask Register allows interrupt sources to be masked.

NOTE: GPIO lines configured as outputs in the GPIO Control Register are always masked, regardless of the state of the associated bit in the GPIO Interrupt Mask Register.

Interrupts from GPIO lines go through two levels of masking. Each GPIO line can be individually masked in the GPIO Interrupt Mask Register; the results are logically OR'ed together and routed to the GPIO_INT bit (bit 13) of the Interrupt Status Register, which can be masked by bit 13 in the Interrupt Mask Register.

Address offset: 0x40

Access: Read/write

Bits	Field	Default	Description
15 to 10	Not used	-	Always reads as (0)s
9	GPIO 9_INT_MSK	1	GPIO 9 Interrupt Mask—masks GPIO 9 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt

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Bits	Field	Default	Description
8	GPIO 8_INT_MSK	1	GPIO 8 Interrupt Mask—masks GPIO 8 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
7	GPIO 7_INT_MSK	1	GPIO 7 Interrupt Mask—masks GPIO 7 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
6	GPIO 6_INT_MSK	1	GPIO 6 Interrupt Mask—masks GPIO 6 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
5	GPIO 5_INT_MSK	1	GPIO 5 Interrupt Mask—masks GPIO 5 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
4	GPIO 4_INT_MSK	1	GPIO 4 Interrupt Mask—masks GPIO 4 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
3	GPIO 3_INT_MSK	1	GPIO 3 Interrupt Mask—masks GPIO 3 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
2	GPIO 2_INT_MSK	1	GPIO 2 Interrupt Mask—masks GPIO 2 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
1	GPIO 1_INT_MSK	1	GPIO 1 Interrupt Mask—masks GPIO 1 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt
0	GPIO 0_INT_MSK	1	GPIO 0 Interrupt Mask—masks GPIO 0 interrupt. 0 = enable interrupt 1 = disable (mask) interrupt

GPIO Data Register

Reading the GPIO Data Register provides current state information for the GPIO signals. GPIO lines configured as inverted (active low) inputs in the GPIO Control Register read inverted: (1)s if low; (0)s if high. GPIO lines configured to be outputs in the GPIO Control Register read as (0)s.

Writing to the GPIO Data Register controls the level of GPIO lines configured as outputs by the GPIO Control Register. A logical (1) written to a bit of this register causes the associated GPIO line to be driven high or released to tri-state, depending upon the corresponding bits in the GPIO Control Register. A logical (0) written to a bit of this register causes the corresponding GPIO line to be driven low. Writing a bit associated with a GPIO line configured as an input has no effect unless the GPIO line is subsequently re-configured as an output.

Address offset: 0x42

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Access: Read (input status),
Write (output level)

GPIO Data Register Read Definitions (Input Status)

Bits	Field	Default	Description
15 to 10	Not used	0	Always reads as (0)
9	GPIO 9_VAL	1	GPIO 9 Value—provides data value for GPIO 9 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
8	GPIO 8_VAL	1	GPIO 8 Value—provides data value for GPIO 8 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
7	GPIO 7_VAL	1	GPIO 7 Value—provides data value for GPIO 7 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
6	GPIO 6_VAL	1	GPIO 6 Value—provides data value for GPIO 6 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
5	GPIO 5_VAL	1	GPIO 5 Value—provides data value for GPIO 5 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
4	GPIO 4_VAL	1	GPIO 4 Value—provides data value for GPIO 4 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
3	GPIO 3_VAL	1	GPIO 3 Value—provides data value for GPIO 3 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)

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Bits	Field	Default	Description
2	GPIO 2_VAL	1	GPIO 2 Value—provides data value for GPIO 2 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
1	GPIO 1_VAL	1	GPIO 1 Value—provides data value for GPIO 1 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)
0	GPIO 0_VAL	1	GPIO 0 Value—provides data value for GPIO 0 line. 0 = de-asserted (input - active high) 0 = asserted (input - active low) 1 = asserted (input - active high) 1 = de-asserted (input - active low)

GPIO Data Register Write Definitions (Output Level)

Bits	Field	Default	Description
15 to 10	Not used	0	Always reads as (0)
9	GPIO 9_VAL	1	GPIO 9 Value—provides data value for GPIO 9 line. 0 = low 1 = high or High-Z
8	GPIO 8_VAL	1	GPIO 8 Value—provides data value for GPIO 8 line. 0 = low 1 = high or High-Z
7	GPIO 7_VAL	1	GPIO 7 Value—provides data value for GPIO 7 line. 0 = low 1 = high or High-Z
6	GPIO 6_VAL	1	GPIO 6 Value—provides data value for GPIO 6 line. 0 = low 1 = high or High-Z
5	GPIO 5_VAL	1	GPIO 5 Value—provides data value for GPIO 5 line. 0 = low 1 = high or High-Z
4	GPIO 4_VAL	1	GPIO 4 Value—provides data value for GPIO 4 line. 0 = low 1 = high or High-Z
3	GPIO 3_VAL	1	GPIO 3 Value—provides data value for GPIO 3 line. 0 = low 1 = high or High-Z

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Bits	Field	Default	Description
2	GPIO 2_VAL	1	GPIO 2 Value—provides data value for GPIO 2 line. 0 = low 1 = high or High-Z
1	GPIO 1_VAL	1	GPIO 1 Value—provides data value for GPIO 1 line. 0 = low 1 = high or High-Z
0	GPIO 0_VAL	1	GPIO 0 Value—provides data value for GPIO 0 line. 0 = low 1 = high or High-Z

GPIO Control 1 Register

The GPIO Control 1 Register controls the direction, output drive type, and input polarity of the GPIO lines [7 to 0]. Each line requires two bits. Table 5-4 lists the GPIO Control Register bit pattern definitions.

Table 5-4 GPIO Control register bit pattern definitions

Pattern (msb,lsb)	Definition
0,0	Input—active high
0,1	Input—active low
1,0	Output—TTL
1,1	Output—open drain

Address offset: 0x44

Access: Read/write

Bits	Field	Default	Description
15 to 14	GPIO 7_CTL	0b00	GPIO 7 Control—configures GPIO 7 according to Table 5-4.
13 to 12	GPIO 6_CTL	0b00	GPIO 6 Control—configures GPIO 6 according to Table 5-4.
11 to 10	GPIO 5_CTL	0b00	GPIO 5 Control—configures GPIO 5 according to Table 5-4.
9 to 8	GPIO 4_CTL	0b00	GPIO 4 Control—configures GPIO 4 according to Table 5-4.
7 to 6	GPIO 3_CTL	0b00	GPIO 3 Control—configures GPIO 3 according to Table 5-4.
5 to 4	GPIO 2_CTL	0b00	GPIO 2 Control—configures GPIO 2 according to Table 5-4.

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Bits	Field	Default	Description
3 to 2	GPIO 1_CTL	0b00	GPIO 1 Control—configures GPIO 1 according to Table 5-4.
1 to 0	GPIO 0_CTL	0b00	GPIO 0 Control—configures GPIO 0 according to Table 5-4.

GPIO Control 2 Register

The GPIO Control 2 Register controls the direction, output drive type, and input polarity of the GPIO lines [9 to 8] as defined in Table 5-4 on page 5-13. Each line requires two bits.

The GPIO Control 2 Register can configure GPIO 8 as a GPIO or NMI; GPIO 9 can be configured as a GPIO or watchdog timer status signal.

Address offset: 0x48

Access: Read/write

Bits	Field	Default	Description
15	NMI_SEL	0	NMI Select—defines the GPIO 8 signal. 0 = GPIO 1 = NMI
14	PROCFAIL_SEL	0	PROCFAIL_SEL—defines the GPIO 9 signal. 0 = GPIO 9 1 = watchdog timer status
13 to 4	Not used	0	Always reads as (0)
3 to 2	GPIO 9_CTL	0b00	GPIO 9 Control—configures GPIO 9 according to Table 5-4.
1 to 0	GPIO 8_CTL	0b00	GPIO 8 Control—configures GPIO 8 according to Table 5-4.

5.4.4 Board Reset Register

The Board Reset Register can generate a board reset by receiving a sequence of two writes:

1. First, write: 0xC0DE to the Board Reset Register.
2. Write: 0x8E53 to the Board Reset Register.

After the second write, the CV1 will reset. After a board reset, the Board Reset Register returns to its default state. The board reset sequence must be written again to generate another board reset.

Address offset: 0x50

Access: Read/write

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Bits	Field	Default	Description
15 to 0	BOARD_RST_BIT	0	Board Reset Bits—resets CV1 after two writes in sequence. 1. Write 0xC0DE to Board Reset Register. 2. Write 0x8E53 to Board Reset Regiseter.

5.5 Component Locations

The following diagram shows the location of major components on the CV1.

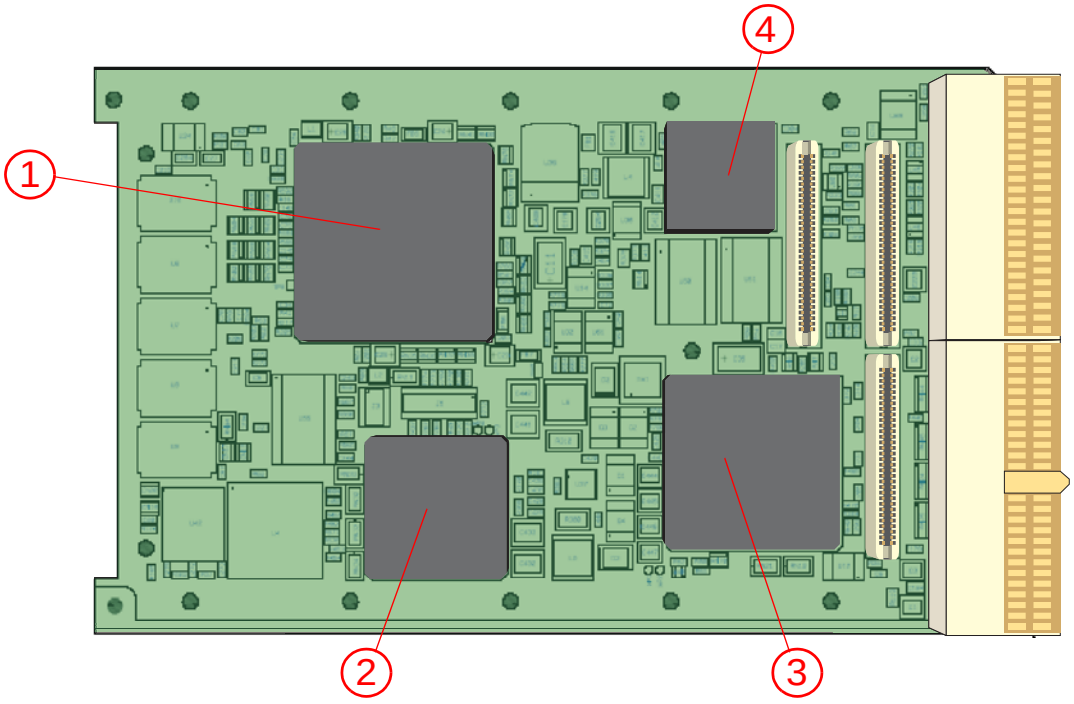


Figure 5-1 Component locations (primary side)

Legend

1. MV64460 System Controller
2. MPC7447A PowerPC G4 processor
3. PCI 6254 cPCI Bridge
4. VSC8244 Ethernet PHY

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Chapter 6: Transition Module CV1-TM

6.1 Overview

SBS Technologies provides the CV1 Rear Transition Module (CV1-TM) as an optional companion board for the convection-cooled CV1 Single Board Computer. The CV1-TM provides the following outboard connectors:

- Serial port COM1 (P1)—rear-panel micro DB9 connector
- Serial port COM2 (P2)—rear-panel micro DB9 connector
- Gigabit Ethernet ETH0 (J11)—rear-panel RJ-45 connector
- Gigabit Ethernet ETH1 (J10)—rear-panel RJ-45 connector
- GPIO (J12)—2 x 13-pin on-board header
- Backup Power (J9)—2 x 5-pin on-board header
- PMC I/O (J6)—2 x 32-pin on-board header

6.2 Physical Description

Form Factor:	3U
Height:	100 ± 0.15mm (3.9 ± 0.0059 in.)
Width:	80 ± 0.15mm (3.15 ± 0.0059 in.)
Weight:	4.16oz.
Temperature	
operating:	0° C to 70° C (ambient)
storage:	-40° C to 85° C
Relative Humidity: (non-condensing)	5% to 95% @ 40° C
Shock (half-sine):	12g peak / 6ms, 3-axes, up & down, 5 hits / direction
Vibration (random):	5–100 Hz, 2g, 60 minutes each axis

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6.3 Block Diagram

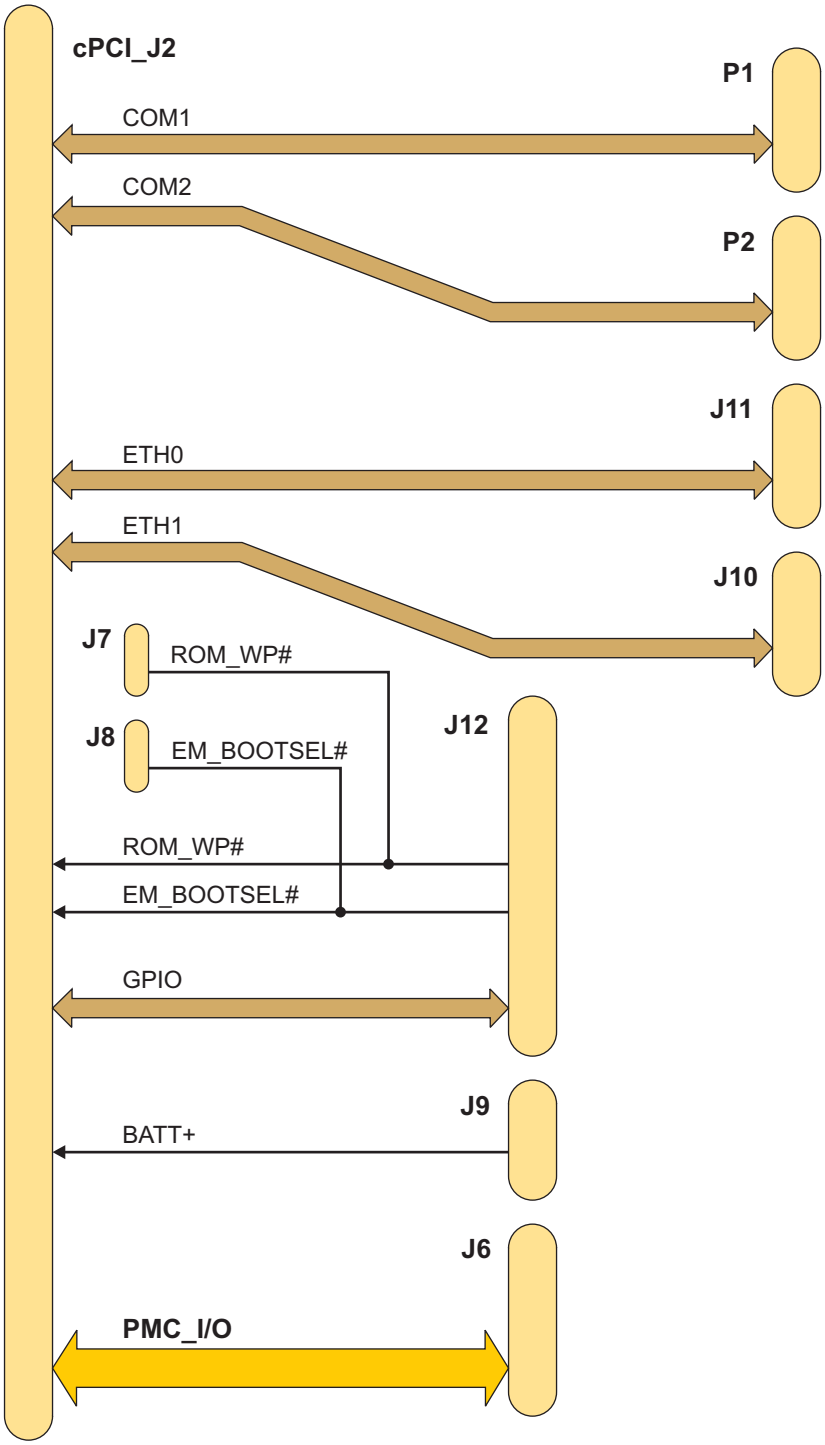


Figure 6-1 CV1-TM block diagram

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6.4 Connectors

6.4.1 CompactPCI Connector (cPCI_J2)

All signals from the CV1 to the CV1-TM are routed through the cPCI_J2 connector.

Table 6-1 CompactPCI connector (J2) pin assignments

Pin	A	B	C	D	E	F
J2-22	n/c	n/c	n/c	n/c	n/c	GND
J2-21	n/c	GND	COM2_TXD+	COM2_TXD-	COM1_TXD	GND
J2-20	n/c	GND	COM2_TXC+	COM2_TXC-	COM1_RXD	GND
J2-19	GND	GND	COM2_RXD+	COM2_RXD-	EM_BOOTSEL#	GND
J2-18	PMC_1	PMC_2	COM2_RXC+	COM2_RXC-	ROM_WP#	GND
J2-17	PMC_3	PMC_4	n/c	n/c	n/c	GND
J2-16	PMC_5	PIMC_6	n/c	GND	BATT+	GND
J2-15	PMC_7	PMC_8	n/c	n/c	n/c	GND
J2-14	PMC_9	PMC_10	GPIO 0	GPIO 5	BIT_PASS#	GND
J2-13	PMC_11	PMC_12	GPIO 1	GPIO 6	NMI# / GPIO 8	GND
J2-12	PMC_13	PMC_14	GPIO 2	GPIO 7	PROCFAIL / GPIO 9	GND
J2-11	PMC_15	PMC_16	GPIO 3	ETH1_DA+	ETH1_DC+	GND
J2-10	PMC_17	PMC_18	GPIO 4	ETH1_DA-	ETH1_DC-	GND
J2-9	PMC_19	PMC_20	PMC_30	ETH1_DB+	ETH1_DD+	GND
J2-8	PMC_21	PMC_22	PMC_33	ETH1_DB-	ETH1_DD-	GND
J2-7	PMC_23	PMC_24	PMC_36	ETH0_DA+	ETH0_DC+	GND
J2-6	PMC_25	PMC_26	PMC_38	ETH0_DA-	ETH0_DC-	GND
J2-5	PMC_27	PMC_28	PMC_50	ETH0_DB+	ETH0_DD+	GND
J2-4	n/c	PMC_29	PMC_52	ETH0_DB-	ETH0_DD-	GND
J2-3	n/c	GND	n/c	n/c	n/c	GND
J2-2	n/c	n/c	n/c	n/c	n/c	GND
J2-1	n/c	GND	n/c	n/c	n/c	GND

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6.4.2 Serial Port Connectors (P1 and P2)

The CV1-TM includes two rear-panel micro-DB9 connectors (P1 and P2) for access to the serial ports COM1 (RS-232) and COM2 (RS-422).

Table 6-2 COM1/COM2 rear-panel micro-DB9 connectors (P1/P2) pin assignments

COM1 (P1)

Pin	Assignment
1	n/c
2	COM1_RXD
3	COM1_TXD
4	n/c
5	GND
6	n/c
7	n/c
8	n/c
9	n/c

COM2 (P2)

Pin	Assignment
1	COM2_TXD-
2	COM2_TXC-
3	COM2_RXC+
4	COM2_RXD+
5	GND
6	COM2_TXD+
7	COM2_TXC+
8	COM2_RXC-
9	COM2_RXD-

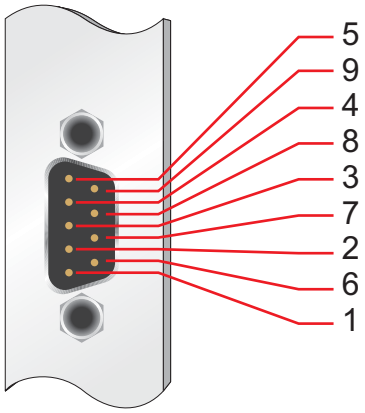


Figure 6-2 Serial port micro-DB9 pin-out

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6.4.3 Ethernet Connectors (J11 and J10)

The CV1-TM includes two rear-panel Ethernet RJ-45 connectors, J11 (ETH0) and J10 (ETH1). The connector shields are connected to chassis ground.

Table 6-3 Ethernet RJ-45 rear-panel connector (J11 and J10) pin assignments

Pin	Assignments (J11)	Assignments (J10)
1	ETH0_DA+	ETH1_DA+
2	ETH0_DA-	ETH1_DA-
3	ETH0_DB+	ETH1_DB+
4	ETH0_DC+	ETH1_DC+
5	ETH0_DC-	ETH1_DC-
6	ETH0_DB-	ETH1_DB-
7	ETH0_DD+	ETH1_DD+
8	ETH0_DD-	ETH1_DD-

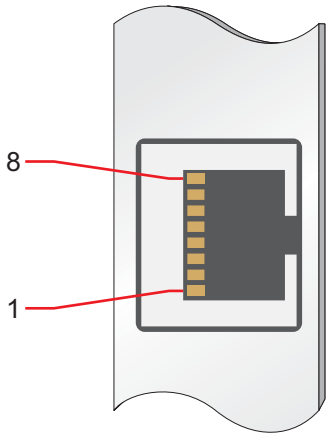


Figure 6-3 Ethernet RJ-45 pinout

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6.4.4 GPIO Connector (J12)

The CV1-TM includes a 2 x 13 header (J12) for access to the GPIO Status and Control signals.

Table 6-4 GPIO on-board header (J12) pin assignments

Pin	Assignment	Pin	Assignment
1	GPIO 1	2	GPIO 0
3	GPIO 3	4	GPIO 2
5	GND	6	GND
7	GPIO 5	8	GPIO 4
9	GPIO 7	10	GPIO 6
11	GND	12	NMI# / GPIO 8
13	PROCFAIL / GPIO 9	14	GND
15	n/c	16	n/c
17	n/c	18	n/c
19	n/c	20	GND
21	GND	22	n/c
23	EM_BOOTSEL#	24	BIT_PASS#
25	GND	26	ROM_WP#

6.4.5 Backup Power Connector (J9)

The CV1-TM provides a 2 x 5 header (J9) for connecting an external +3.3V supply for battery backup to the CV1 Real-Time Clock.

Table 6-5 Backup power header (J9) pin assignments

Pin	Assignment	Pin	Assignment
1	n/c	2	BATT+ (+3.3V)
3	n/c	4	n/c
5	GND	6	n/c
7	n/c	8	n/c
9	n/c	10	n/c

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6.4.6 PMC I/O Connector (J6)

The CV1-TM includes a 2 x 32 connector PMC I/O header (J6) for the PMC I/O lines from the PMC_J14 connector on CV1.

Table 6-6 PMC I/O header (J6) pin assignments

Pin	Assignment	Pin	Assignment
1	PMC_1	2	PMC_2
3	PMC_3	4	PMC_4
5	PMC_5	6	PMC_6
7	PMC_7	8	PMC_8
9	PMC_9	10	PMC_10
11	PMC_11	12	PMC_12
13	PMC_13	14	PMC_14
15	PMC_15	16	PMC_16
17	PMC_17	18	PMC_18
19	PMC_19	20	PMC_20
21	PMC_21	22	PMC_22
23	PMC_23	24	PMC_24
25	PMC_25	26	PMC_26
27	PMC_27	28	PMC_28
29	PMC_29	30	PMC_30
31	n/c	32	n/c
33	PMC_33	34	n/c
35	n/c	36	PMC_36
37	n/c	38	PMC_38
39	n/c	40	n/c
41	n/c	42	n/c
43	n/c	44	n/c
45	n/c	46	n/c
47	n/c	48	n/c
49	n/c	50	PMC_50
51	n/c	52	PMC_52
53	n/c	54	n/c
55	n/c	56	n/c
57	n/c	58	n/c
59	n/c	60	n/c
61	n/c	62	n/c
63	n/c	64	n/c

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6.5 Configuration Jumpers

The CV1-TM includes the following configuration header/jumpers:

- EM_BOOTSEL# (J8)
- ROM_WP# (J7)

6.5.1 EM_BOOTSEL#:

The EM_BOOTSEL# is a two-pin header/jumper (J8) that selects which boot code is executed on power-up or after reset.

If a jumper is installed on J8 (EM_BOOTSEL# = 0), the boot code provided by SBS is executed.

If a jumper is not installed on J8 (EM_BOOTSEL# = 1), the user boot code is executed provided that a boot description header and a valid checksum is detected.

NOTE: A jumper is not typically installed on J8; the EM_BOOTSEL# signal is pulled up.

NOTE: The state of EM_BOOTSEL# can be read from CPLD Configuration Register (bit 9) (*see "Configuration Register" on page 5-3*)

6.5.2 ROM_WP#:

The ROM_WP# is a two-pin header/jumper (J7) that enables flash ROM write-protection.

If a jumper is installed on the J7 (ROM_WP# = 0), the flash ROM write-protection is enabled.

If a jumper is not installed on J7 (ROM_WP# = 1), the flash ROM write-protection is disabled.

NOTE: A jumper is not typically installed on J7; the ROM_WP# signal is pulled up.

NOTE: The state of ROM_WP# can be read from CPLD Configuration Register (bit 12) (*see "Configuration Register" on page 5-3*)

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6.6 Connector Locations

Figure 6-4 shows the location of the connectors on the CV1-TM.

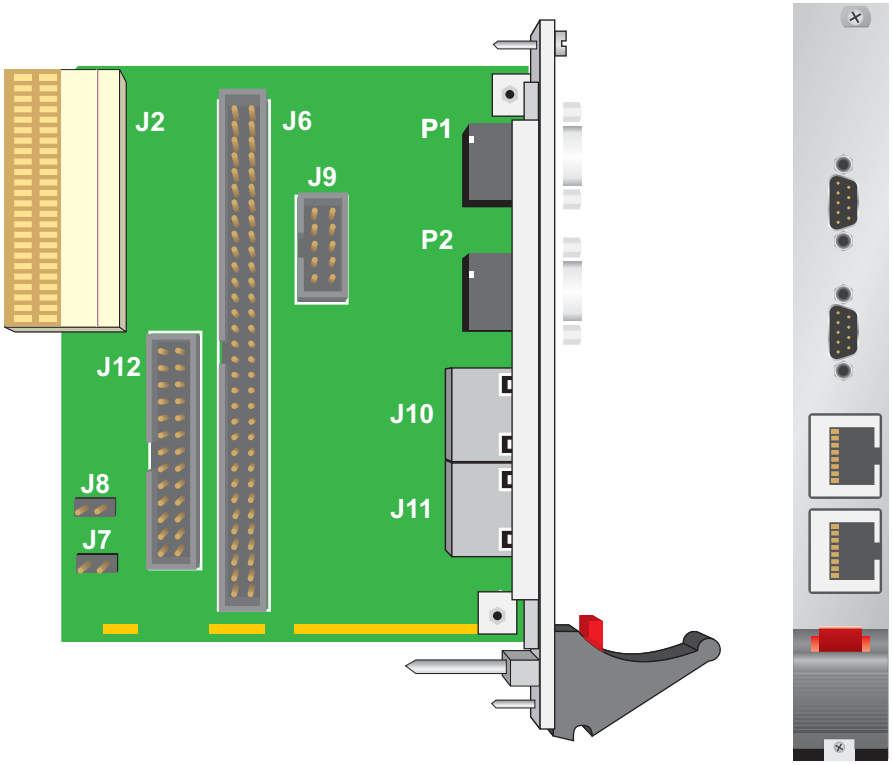


Figure 6-4 CV1-TM connector locations

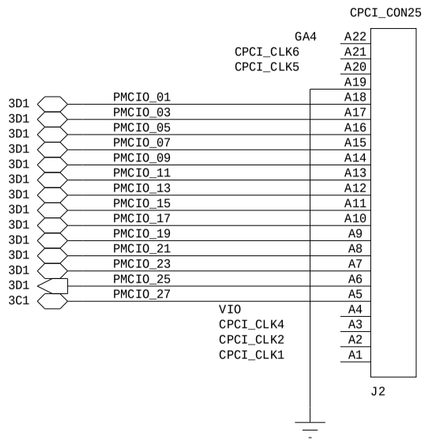
J2	cPCI backplane connector	J11	Ethernet RJ-45 (ETH0)
J6	PMC I/O	J10	Ethernet RJ-45 (ETH1)
P1	Serial I/O port (COM1)	J7	ROM_WP# Select
P2	Serial I/O port (COM2)	J8	EM_BOOT #Select
J12	GPIO	J9	NVRAM/RTC battery backup

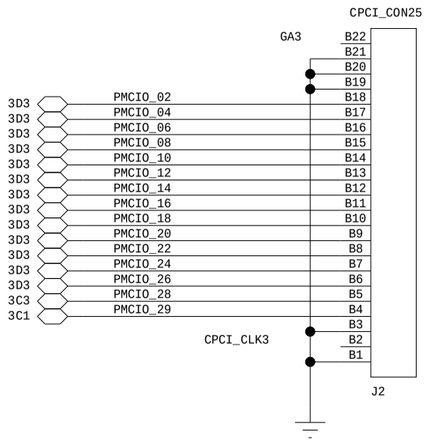
6.7 CV1-TM Schematics

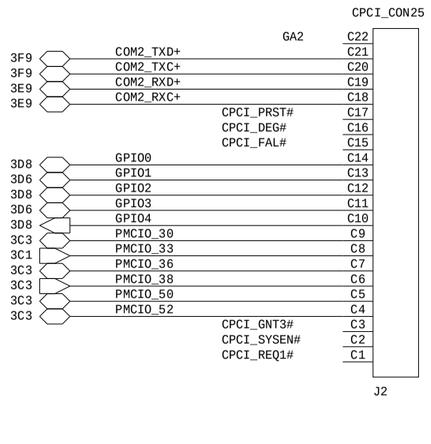
The CV1-TM are provided on the following pages.

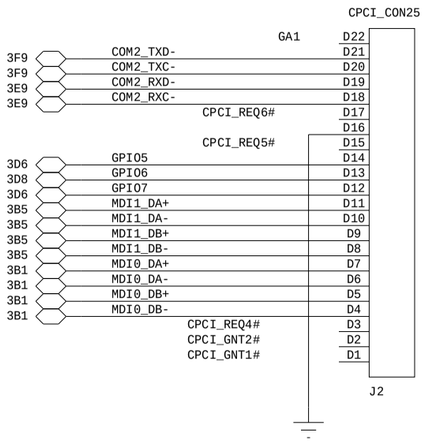
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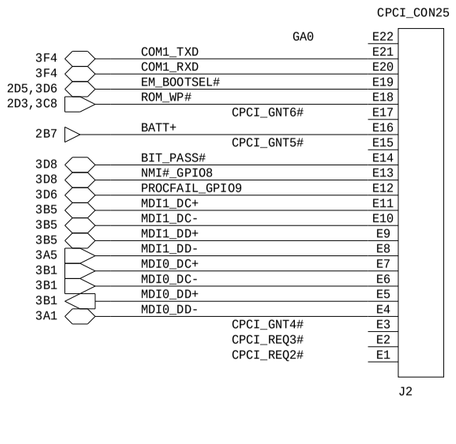
Backplane Connector

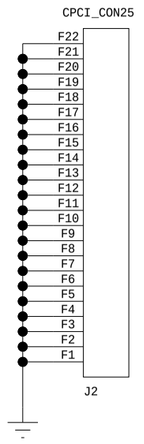


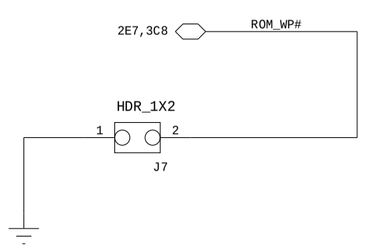












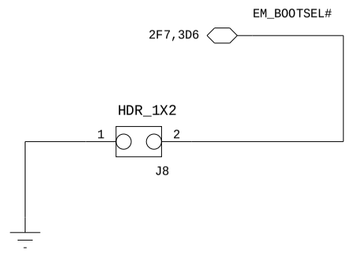
ROM_WP# is used for FLASH write protection

The jumper is normally not installed during user development phase but is received from the factory as installed.

ROM_WP# = 1 normal operation (writes allowed)

ROM_WP# = 0 FLASH write protection enabled

Note: If an external FET device is used to drive this net low it should be an open-drain device.



EM_BOOTSEL# is used as an emergency boot signal.

The jumper is normally not installed.

EM_BOOTSEL# = 1 bootcode execution from customer bootcode segment

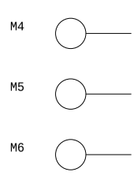
EM_BOOTSEL# = 0 bootcode execution from protected SBS bootcode segment

The jumper is normally not installed during standard operation but is received from the factory as installed.

BATTERY BACKUP HEADER (+3.3V)

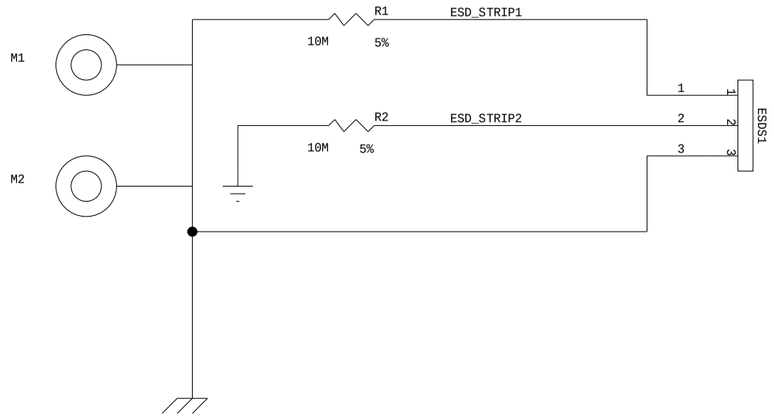


FIDUCIALS



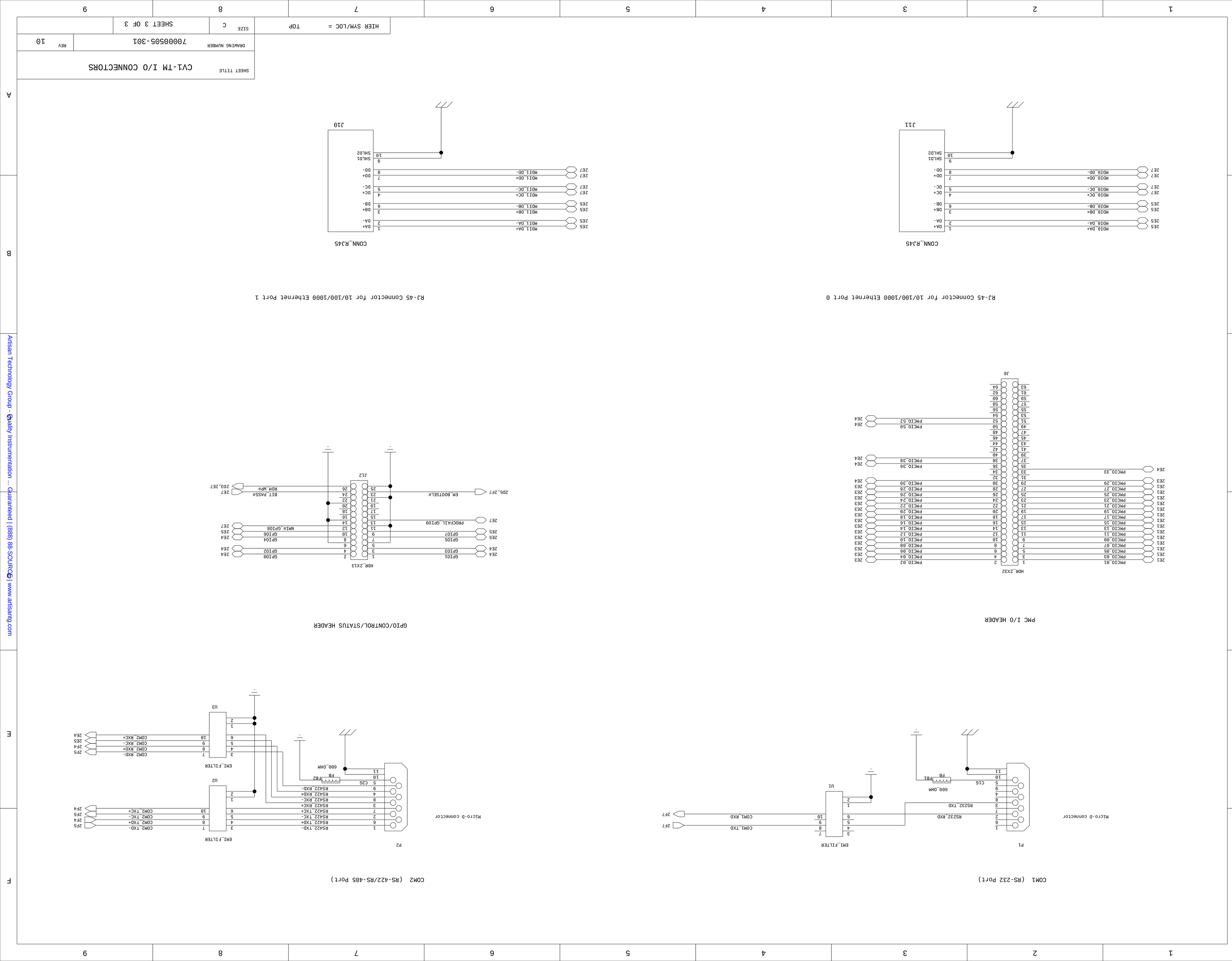
ESD STRIP

BOTTOM EDGE, BOTH SIDES



SHEET TITLE: CV1-TM BACKPLANE CONNECTOR			
DRAWING NUMBER: 70000505-301			REV: 10
HIER SYM/LOC = TOP	SIZE: C	SHEET 2 OF 3	

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J6
PMC I/O HEADER
HDR_2X32
P1
Micro-D connector
COM1 (RS-232 Port)
EMI_FILTER
U1
600_OHM
RS232_TXD
RS232_RXD
COM1_TXD
COM1_RXD
J11
CONN_RJ45
R3-45 Connector for 10/100/1000 Ethernet Port 0
J10
R3-45 Connector for 10/100/1000 Ethernet Port 1
J12
GPIO/CONTROL/STATUS HEADER
P2
COM2 (RS-422/RS-485 Port)
U2
U3
CV1-TM I/O CONNECTORS
7000050S-301
SHEET 3 OF 3
TOP
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Chapter 7: Customer Service

7.1 Introduction

This chapter provides forms and information for requesting product service or repair. The following information is included:

- Contact information for technical support service and repair
- Product warranty information
- Return Material Authorization (RMA) information
- Documentation Feedback form

Returned product will not be accepted without a properly authorized RMA number. An RMA number can be authorized by contacting SBS Technologies Customer Service Department (*see"Customer Service" on page 7-2*). To avoid applicable charges, the customer should make every effort to resolve issues including consulting the technical sections of this manual and contacting Technical Support before securing an RMA.

SBS Technologies makes every effort to include all the information needed to properly install, configure and operate SBS products in the user's guides. However, if information is needed that cannot be found in the manual, please include relevant comments, suggestions and constructive criticisms in the Documentation Feedback Form and return it to SBS Technologies.

7.2 Updated User Guide and Data Sheets

The latest revisions of product documentation including user's guides and data sheets are available in PDF format from the SBS web site at www.sbs.com. PDF documents can be viewed using Adobe® Acrobat Reader, which is available for downloading from the Adobe web site (www.adobe.com) at no charge.

All product documentation can be requested through SBS Technologies Customer Service Department (*see"Customer Service" on page 7-2*).

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7.3 Customer Service

The following is contact information for SBS Technologies Customer Service Department:

E-mail: support.sbc@sbs.com
Telephone: (919) 851-1101 (choose Technical Support option)
Fax.: (919) 851-2844
Mail: SBS Technologies
6301 Chapel Hill Rd.
Raleigh, N.C. 27607-5115

7.4 Warranty Information

SBS Technologies provides a two-year product warranty. Included in the warranty are specific stipulations concerning application and use of the product. Please review the warranty before requesting service.

7.4.1 Warranty

All Single Board Computer (SBC) products manufactured and sold by SBS Technologies, Inc. include a two-year warranty for defects in workmanship and materials for hardware unless otherwise stated in an Original Equipment Manufacturer (OEM) agreement or contract with SBS Technologies. Software is warranted to be readable and functional upon receipt. This warranty shall not apply to equipment that has been repaired or altered outside of SBS facilities in any way as to, in the judgement of SBS, affect its reliability. Nor will it apply: if the equipment has been used in a manner exceeding its specifications, if the serial number has been removed, or if the equipment has been subject to accident, disaster, improper or inadequate maintenance, or electrical or physical misuse, misapplication, or abuse.

SBS will, at its option, repair or replace the defective item at its factory under the terms of this warranty, subject to the provisions and specific exclusions listed herein.

SBS does not assume any liability for consequential damages as a result of the use of its products. Under no circumstances shall the liability of SBS exceed the original selling price of the equipment.

The equipment warranty shall constitute the sole and exclusive remedy of any buyer of SBS equipment and the sole and exclusive liability of SBS, its affiliates, successors or assigns, in connection with equipment purchased and in lieu of all other warranties expressed, implied, or statutory, including, but not limited to, any implied warranty of merchant ability or fitness for a particular purpose and all other obligations or liabilities of SBS, its affiliates, successors, or assigns.

The equipment must be returned securely packaged in anti-static bags and labeled with a Return Material Authorization (RMA) number written on the outside of the package. The package must be insured, and the shipping cost must be paid. SBS will repair or replace failed parts within the limits of the warranty statement referenced above and return the item at no charge. Standard

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repair charges may apply if: there is a lack of proof of the date of purchase, modifications have been performed, the unit has been operated outside its specifications, and /or if the warranty period has expired.

This description of SBS' limited warranty is only a summary; please review the terms of the product warranty for specific coverage and exclusions.

7.4.2 Non-Warranty Terms and Conditions

Payment for all out-of-warranty repairs must be prearranged through a purchase order or credit card information before a RMA number can be issued. SBS Technologies charges a firm, fixed price for repair of non-warranty boards. Third party products purchased through SBS and returned for repair will follow the warranty schedule for that manufacturer. Non-warranty repairs require a purchase order upon receipt of a repair quote and prior to any work being performed.

7.5 Return Material Authorization (RMA)

Important! An RMA number must be issued before product can be returned.

To receive an RMA number:

1. Contact the SBS Single Board Computer Technical Support through the RMA Coordinator.

   Phone: (919) 851-1101 (choose the Technical Support option, then choose RMA option)
   Fax.: (919) 851-2844
   Email: rma.sbc@sbs.com

   Please provide the following information:

   Company name
   Contact person
   Telephone
   Email
   Name of product

2. The RMA Coordinator will contact you and issue an RMA number. The following information will be needed:

   Name of product
   Serial number
   Purchase order number (if out of warranty)
   Description of problem

Important! The RMA Coordinator will determine if warranty applies.

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3. When an RMA number is received, attach the RMA number to the product and ship to:

   SBS Technologies
   Attn.: (*insert RMA number here*)
   6301 Chapel Hill Rd.
   Raleigh, N.C. 27607-5115

4. The product must be securely packaged in an anti-static envelope and placed in a cushioned, corrugated carton (use the original shipping carton if possible).



Caution! Always use proper Electrostatic Discharge (ESD) protection when handling printed circuit boards to avoid seriously damaging components. Product handlers must always be properly grounded.

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7.6 Documentation Feedback Form

The object of a user's guide is to communicate technical information concerning the product's setup and operation from the people who designed the product to the people who will use the product. In our continuous effort to improve the usefulness of the manuals that accompany our products, we provide this form to give customers and end-users the opportunity to feedback comments, suggestions and constructive criticisms to SBS Technologies concerning the accuracy and usability of product manuals.

This feedback should include:

- Additional information that would be helpful to set up and operate the product
- Missing information
- Information that is incomplete, inaccurate, or misleading
- Information that is difficult to understand and needs further clarification
- Information that was beneficial or that made the manual easier to use

Print the form below, fill it out, and fax it to SBS Technologies (919 851-2844).

Section	Page(s)	Comments
Chapter 1: Introduction		
Chapter 2: Installation		
Chapter 3 Interfaces		
Chapter 4 Functional Blocks		
Chapter 5 Resources		
Chapter 6: Transition Module		
Chapter 7: Customer Service		
Other Comments and Suggestions		

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Errata: Zero Component Height Non-Compliance

Due to the design complexity, the CV1 does not comply with the IEEE 1386-2001 and ANSI VITA 20-2001 Host Board Zero Component Height Area requirement. However, a PMC module with front-panel I/O may be installed on the CV1, if component heights in the corresponding area do not exceed 8mm. This non-compliance applies to both convection-cooled and conduction-cooled versions.

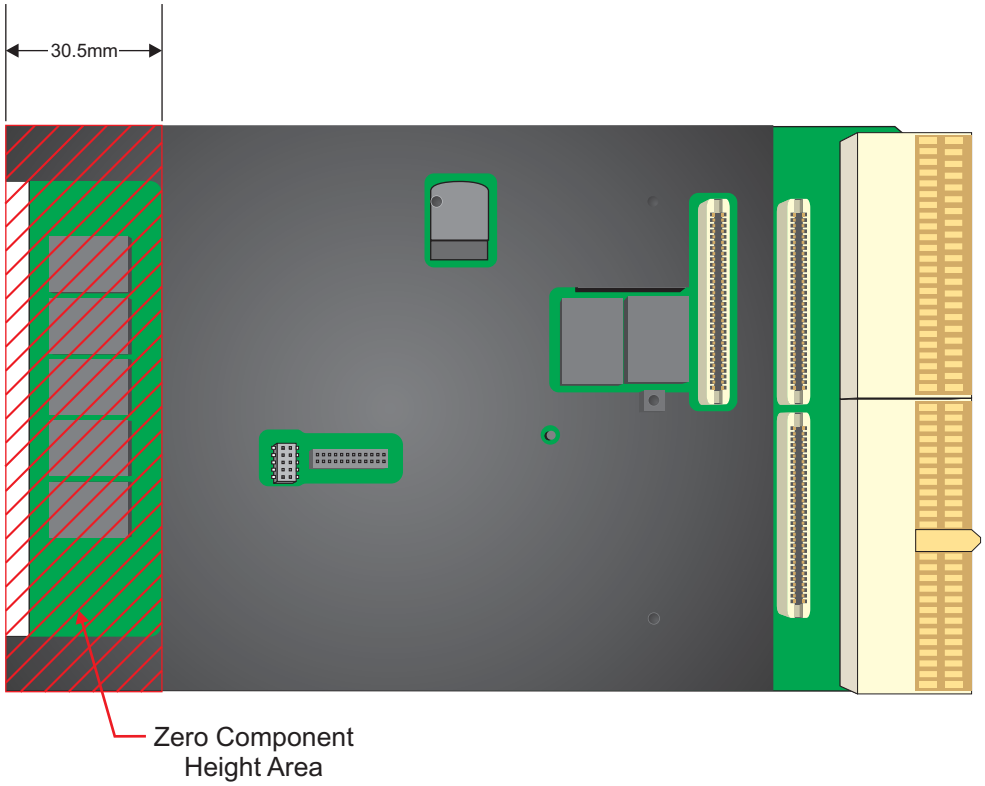


Figure E-1 CV1 zero component height area

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