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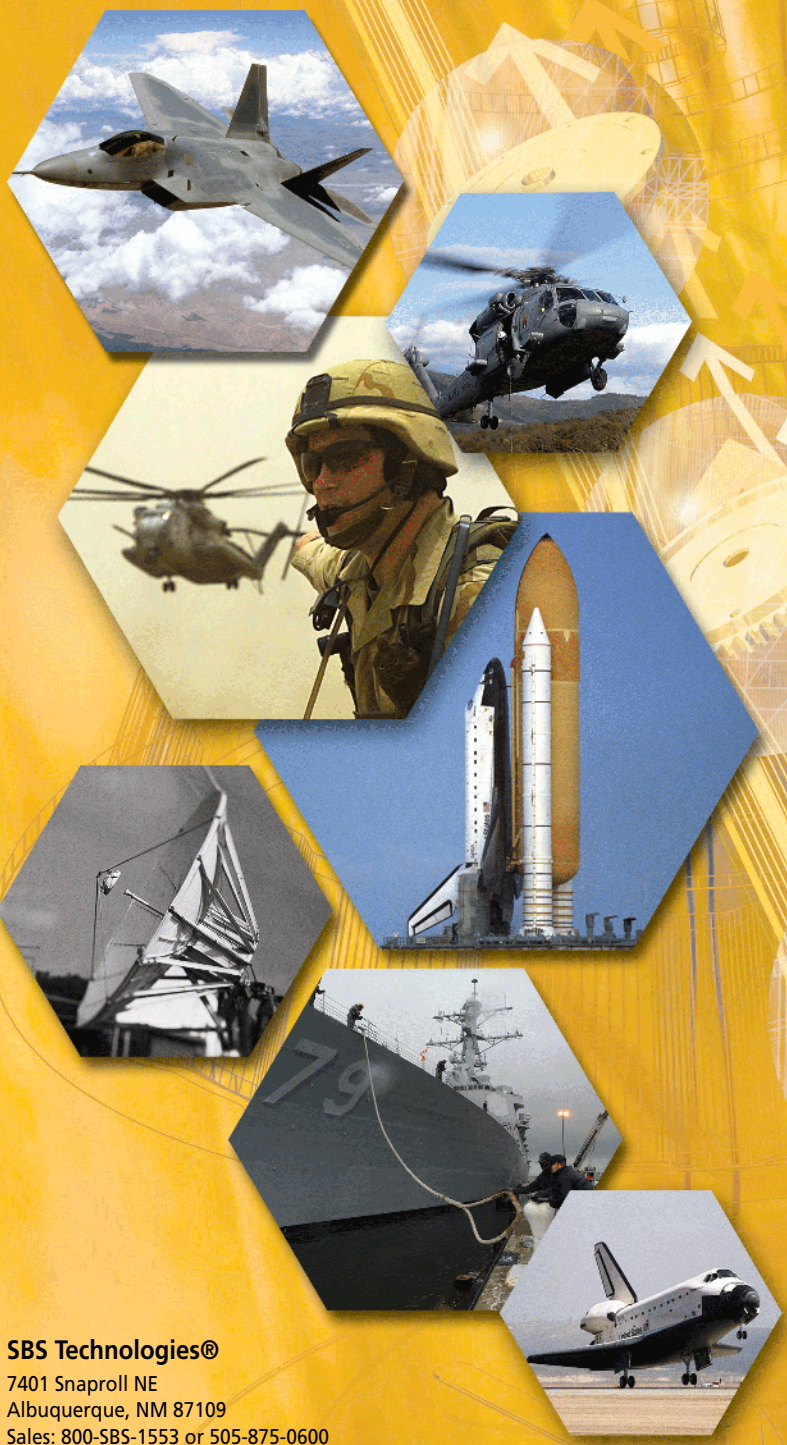
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DIO4-cPCI-CC
User's Manual



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DIO4-cPCI-CC User's Manual

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1: Introduction

This chapter introduces the *DIO4-cPCI-CC User's Manual*. It describes the contents of this manual, and the terminology and conventions used in this manual. The sections are as follows:

- Model Identification
- Contents of the DIO4-cPCI-CC User's Manual
- DIO4-cPCI-CC Description
- Terminology
- Conventions



Cross Reference: Appendix A gives a brief summary of technical revisions made to this manual.

1.1 Model Identification

This manual applies to the model numbers listed in Table 1.1.1.

Table 1.1.1: Model Identification

Model Number	Bus	Form Factor	Generation	Temperature Type C=Comercial R=Rugged, Ext. Temp N=Conduction Cooled	Options
DIO4-cPCI-CCAR0	DIO	3U cPCI	1st	N	00
*Options: 00 = No option installed					

1.2 Contents of the *DIO4-cPCI-CC User's Manual*

Use this manual to familiarize yourself with the DSP-Based Input/Output DIO4-cPCI-CC card. This manual contains the following chapters:

- Introduction (this chapter)
- Before You Begin
- Installing the Software

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- Installing the Hardware
- Installing the Driver
- Hardware Specifications
- Hardware Register Information
- Card Information
- Using the INTEGRITY API

1.3 DIO4-cPCI-CC Description

DSP-Based Input/Output DIO4-cPCI-CC card provides an interface between a cPCI bus and DSP-Based inputs and outputs. DIO4 is a conductive cooled cPCI 3U COTS board that has been ruggedized for military applications. Interfaces are also provided to miscellaneous signals such as the suppression signals. The module also contains a PCI Mezzanine Interface (PMC). Figure 1.3.1 shows a simplified block diagram of the DIO4-cPCI-CC card.

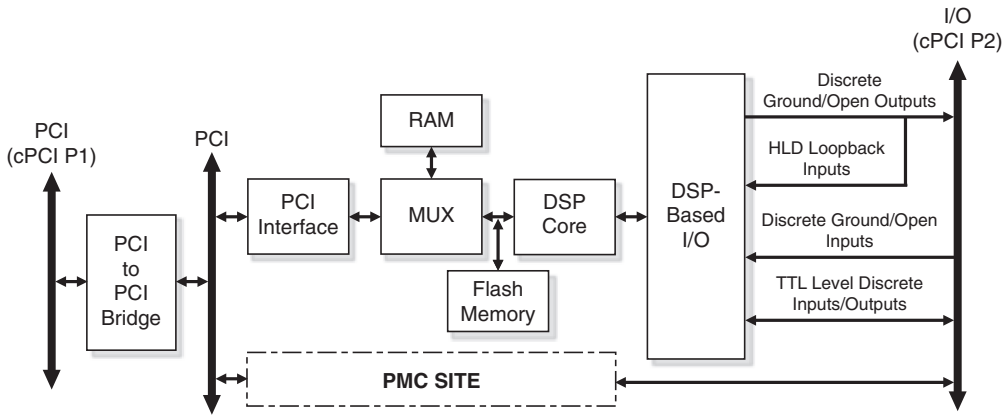


Figure 1.3.1: Simplified Block Diagram of DIO4-cPCI-CC Card

DIO4 provides an interface to a cPCI bus through the PCI to PCI Bridge. PCI Interface provides the interface between the PCI to PCI Bridge and the rest of the module. Mux supplies an interface between the PCI Interface, RAM, Flash Memory, and the DSP Core. DSP processes functions. DIO4 also provides Discrete Ground/Open Outputs, HLD Loopback Inputs, Discrete Ground/Open Inputs, TTL Level Discrete Outputs, TTL Level Discrete Inputs, and a PCI Mezzanine Interface (PMC). Section 6.1 supplies a more detailed description.

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1.4 Terminology

Table 1.4.1 defines some of the basic terms used throughout this manual.

Table 1.4.1: Basic Terminology

Term	Meaning
API	Application Programing Interface
CSR	Control/Status Register
DIO	DSP-Based Input/Output
DSP	Digital Signal Processor
FPGA	Field-Programmable Gate Array

1.5 Conventions

The following conventions appear in this document. These conventions may differ from those used in other SBS publications. The subsections listed below describe each convention in more detail:

- Typographic Conventions
- Words Having Special Meaning
- Compound Keystrokes and Menu Selections
- Symbols

1.5.1 Typographic Conventions

Table 1.5.1 shows the typographic conventions used in this document.

Table 1.5.1: Typographic Conventions

Element	Use in Body Text	Use in Procedures
Italic	➢ Cross references to other SBS publications ➢ Filenames and directory paths ➢ Emphasis	➢ Cross references to other SBS publications ➢ Filenames and directory paths
Bold	➢ (Not used in body text)	➢ Controls, dialogs, menus, and text or numeric fields that appear on the screen ➢ Keys on your keyboard

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Element	Use in Body Text	Use in Procedures
`Courier Roman`	➢ Code examples	➢ Simulating the appearance of screens
`Courier Bold`	➢ Library function calls and syntax ➢ Emphasizing lines of code	➢ Commands and other information that you type as given
Angle brackets, e.g.,< >	➢ Enclosing variable information that you type (without the brackets) in place of a dummy variable	➢ Enclosing variable information that you type (without the brackets) in place of a dummy variable

The point size of the text varies depending on whether it is used in body text, code examples, notes, screens, or procedures.

1.5.2 Words Having Special Meaning

In procedures, the words “Enter” (or “enter”) and “Type” (or “type”) have special meanings that are indicated in Table 1.5.2.

Table 1.5.2: Words with Special Meaning

Word	Meaning
Enter	Key in the specified text or variable information and press the **Return** key.
Type	Key in the specified text. Do not press **Return**.

1.5.3 Compound Keystrokes and Menu Selections

Compound Keystrokes

Whenever a procedure instructs you to press multiple keys, a double angle bracket “»” separates the names of the keys. Table 1.5.3 shows an example.

Menu Selections

Whenever a procedure instructs you to select an item from a pull-down menu, a double angle bracket “»”separates the menu items. Table 1.5.3 shows an example.

Table 1.5.3: Examples of Notation for Compound Keystrokes and Menu Selections

Instruction	Meaning
Press **Ctrl** » **Alt** » **Delete**.	Press the **Ctrl**, **Alt**, and **Delete** keys simultaneously.
Select **File** » **Open**.	Select **Open** from the **File** menu.

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1.5.4 Symbols

The following symbols appear throughout this manual:



Warning: Paragraphs next to this symbol contain information critical to module operation or to your safety.



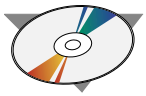
Note: Paragraphs next to this symbol contain information important to module operation.



Tip: Paragraphs next to this symbol contain useful tips.



Cross Reference: Paragraphs next to this symbol contain cross references to the *MIL-STD-1553 FPGA-Based User's Manual*, the *Integrated Avionics Library Reference* , or to a related page in this manual.



Software Reference: Paragraphs next to this symbol contain cross references to software media included with SBS products.

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2: Before You Begin

Sections in this chapter describe what to do after receiving and prior to installing your card. The sections are as follows:

- What You Should Have Received
- Unpacking the Card
- What You Will Need

2.1 What You Should Have Received

- DIO4-cPCI-CC card
- SBS Resource CD containing the following:
  - Device drivers necessary to support the interface between the DIO4-cPCI-CC card and your PC system
  - Product documentation

2.2 Unpacking the Card



Warning: This is an electronic product that is sensitive to electrostatic discharge. Take normal precautions in handling the card to prevent damage.

- Carefully unpack the card and inspect it for physical damage that might have occurred during shipping.
- If you have a damaged card, contact the SBS technical support group that handles maintenance, repairs, and warranties in Albuquerque. When you call us, give us the serial number of your card, and have the card available in case we have questions about its condition. You can find the serial number on a white tag on the card.

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2.3 What You Will Need

DIO4-cPCI-CC product package includes all items required to operate the card on your chassis.

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3: Installing the Software

Sections in this chapter describe the provided software disks and instructions on software installation. The sections are as follows:

- Support Software
- Copying the Software to Your Host System

3.1 Support Software

SBS provides support software for its DIO4 product as part of the Integrated Avionics Library on the following media:

- SBS Resource CD

SBS Resource CD

The SBS Resource CD contains the following:

- Integrated Avionics Library, including C library source files, DLLs, sample applications, and the console mode version of the Unit Test executable
- Device drivers necessary to support the interface between the libraries and your computer system
- SBS PASS demo software
- Product documentation in PDF format (requires Adobe Acrobat Reader)
- Firmware files that have to be downloaded to the cPCI3U card upon initialization.

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3.2 Copying the Software to Your Host System

Use the following instructions to copy the software to the system in which you are installing the DIO4-cPCI-CC card. The following two sections instructions for Windows and INTEGRITY systems.

- Windows Operating Systems
- INTEGRITY Operating Systems (MULTI for Win32)

3.2.1 Windows Operating Systems

Unless otherwise specified, the installation batch files place the Integrated Avionics Library on your system. The *Integrated Avionics Library Reference* provides information on using the library in your own application, and operating system dependent software in the *c:\sbs_ver<x.yz>* folder (directory) in your Windows 95/98/ME/2000 environment, where *<x.yz>* is the version number of the current release.

1. Install the library by completing the following steps:

   - Insert the SBS Resource CD into your CD-ROM drive.
   - Start the Explorer and navigate to the CD.
   - Double-click on the Library folder.
   - Double-click **setup.exe** from the Explorer.
   - Follow the instructions that appear on the screen.

   If you select all of the defaults, the directory structure shown in Figure 3.2.1 is created.

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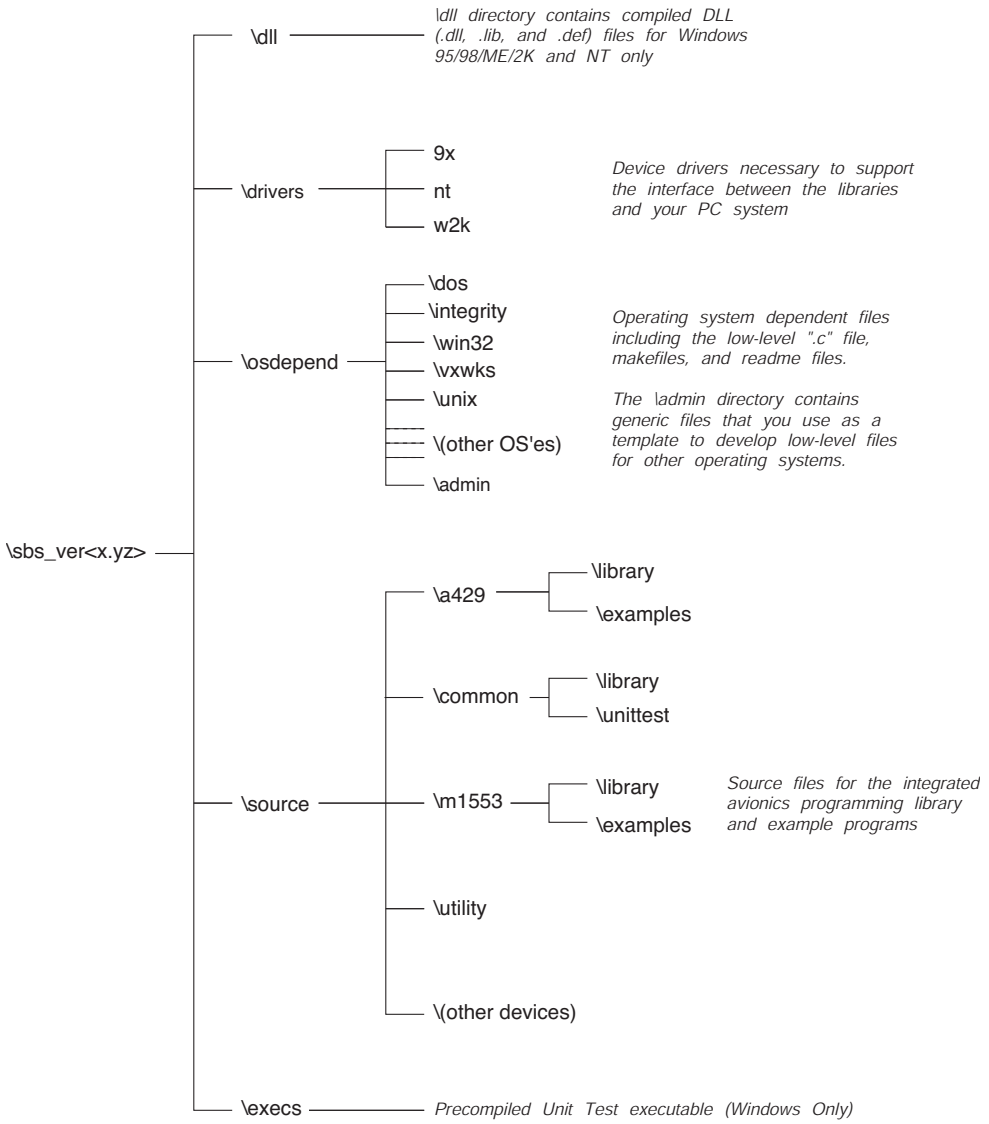


Figure 3.2.1: Default Directory Structure

3.2.2 INTEGRITY Operating Systems (MULTI for Win32)

Use the windows setup as described in Subsection 3.2.1.

➢ Build the project from */osdepend/INTEGRITY/library/default.bld*. This builds the static library for the INTEGRITY Library. Link it with your application.



Note: It may be necessary to modify the *sbs_sys.h* file.

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4: Installing the Hardware

The sections in this chapter provide instructions on how to install the DIO4-cPCI-CC hardware.

4.1 Installing the Card

The section describes installing the DIO4-cPCI-CC card in your system. The subsections are as follows:

- Installing the Card in Your System
- Card Layout

4.1.1 Installing the Card in Your System

To install the DIO4-cPCI-CC card, follow the procedure below.

1. Insert the DIO4-cPCI-CC card into one of the cPCI slots in your system.
2. Power up the host system.



Tip: During card operation, refer to Table 6.2.1 and Table 6.2.2 for information on connector pinouts.

4.1.2 Card Layout

Figure 4.1.1 shows the DIO4-cPCI-CC card layout.

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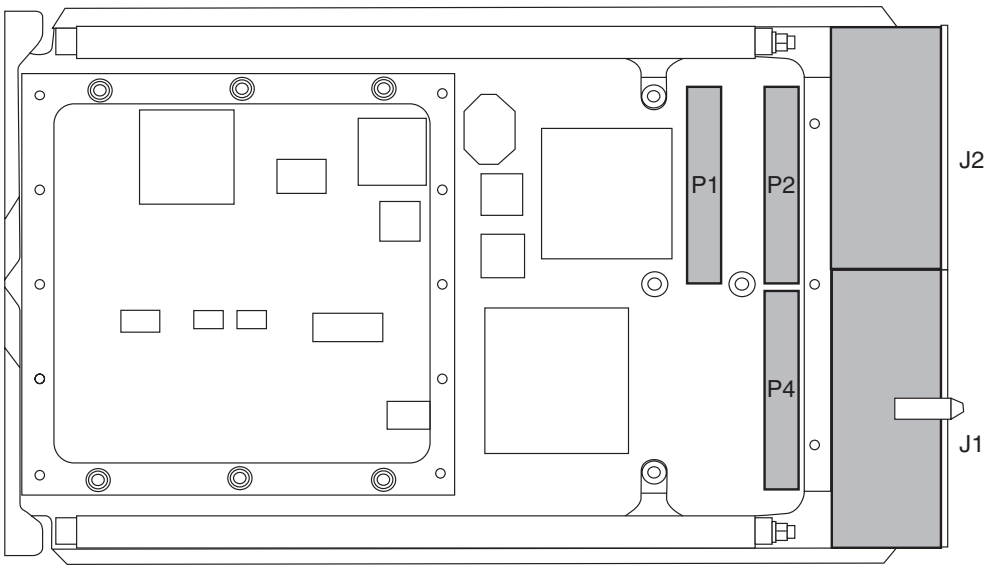


Figure 4.1.1: DIO4-cPCI-CC Layout

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5: Installing the Driver

The following section gives instructions for driver installation.

5.1 Installing the INTEGRITY Driver on Your Host System



Note: This information is for use with the with the CM4 BSP only. Some modification to the driver and/or the BSP may be required to make the driver work on other BSPs.

This section provides information for building and using the DIO4-cPCI-CC board driver for INTEGRITY.

5.1.1 INTEGRITY Driver Setup

To build the DIO4 board INTEGRITY driver, do the following:

- Link the driver to the kernel.
- Initialize the driver's internal structures.

Link the driver to the kernel

This can be achieved by two methods.

- Include the DIO4 driver library project (*cm4_dio4.bld*) into the kernel project.
- Add the *libsbsdio4.a* static library into the kernel project. The DIO4 driver requires the static *libsbspci2050.a* library to be linked with the kernel project.

See Figure 5.1.1 for an example of a kernel project with static libraries linked into the kernel.

Initialize the driver's internal structures

Call the `Dio4IODeviceInit()` routine from kernel's main routine. `DIO4IODeviceInitis` is defined in the *dio4.h* file.

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Example

```
#include "dio4.h"

int main()
{
    // Initialize all DIO4-cPCI3U-CC boards
    Dio4IODeviceInit();

    Exit(0);
}
```

At this point the driver is built into the kernel and ready to use.

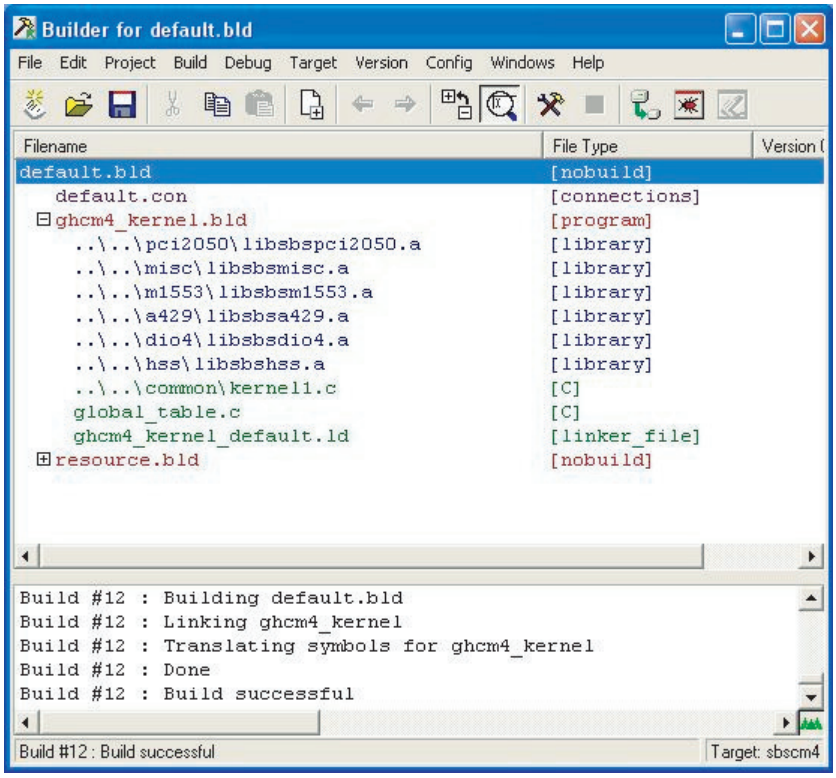


Figure 5.1.1: Example of Kernel Image Project with Static Libraries Linked into the Kernel

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6: Hardware Specifications

This chapter describes the hardware specifications for the DIO4-cPCI-CC card. Sections are as follows:

- Electrical Specifications
- Physical Specifications
- Operational Specifications

6.1 Electrical Specifications

DIO4-cPCI-CC card provides an interface between a cPCI bus and DSP-Based inputs and outputs. The card also provides interfaces to miscellaneous signals such as the suppression signals.

Module contains a TI TMS320VC5402 DSP, a 128 kword RAM buffer, a 512-kword Flash memory, and FPGA's that contain hardware registers and control logic. Access the RAM buffer on the module from the host processor via the VME interface. DIO4 provides Discrete Ground/Open Outputs, HLD Loopback Inputs, Discrete Ground/Open Inputs, TTL Level Discrete Outputs, TTL Level Discrete Inputs, and a PCI Mezzanine Interface (PMC). Figure 6.1.1 shows a functional block diagram of the DIO4-cPCI-CC card. The following paragraphs describe the functional blocks.

6.1.1 DSP

DIO4 uses a TI TMS320VC5402 DSP for processing functions. See Figure 6.1.1. DSP controls Built-In Test (BIT) functions and Input/Output signal processing.

Software Programming

DIO4 stores DSP program code and FPGA configuration data in Flash memory. See Figure 6.1.1. It downloads DSP program code and FPGA configuration data to Flash from host processor via the cPCI bus. DIO4 also uses a JTAG interface for initial programming of the Flash during assembly.

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Built-In Test (BIT) DSP initializes and performs BIT upon power up. BIT ensures proper operation. RAM stores the BIT results. DSP also initiates BIT upon command from the main computer and performs continuous BIT.

Reset When held in a reset state, the DIO4 does not output any spurious signals to any external interface. When reset is released, the DIO4 boots and initializes to a known state. It is then ready to send or receive data under control of the host computer.

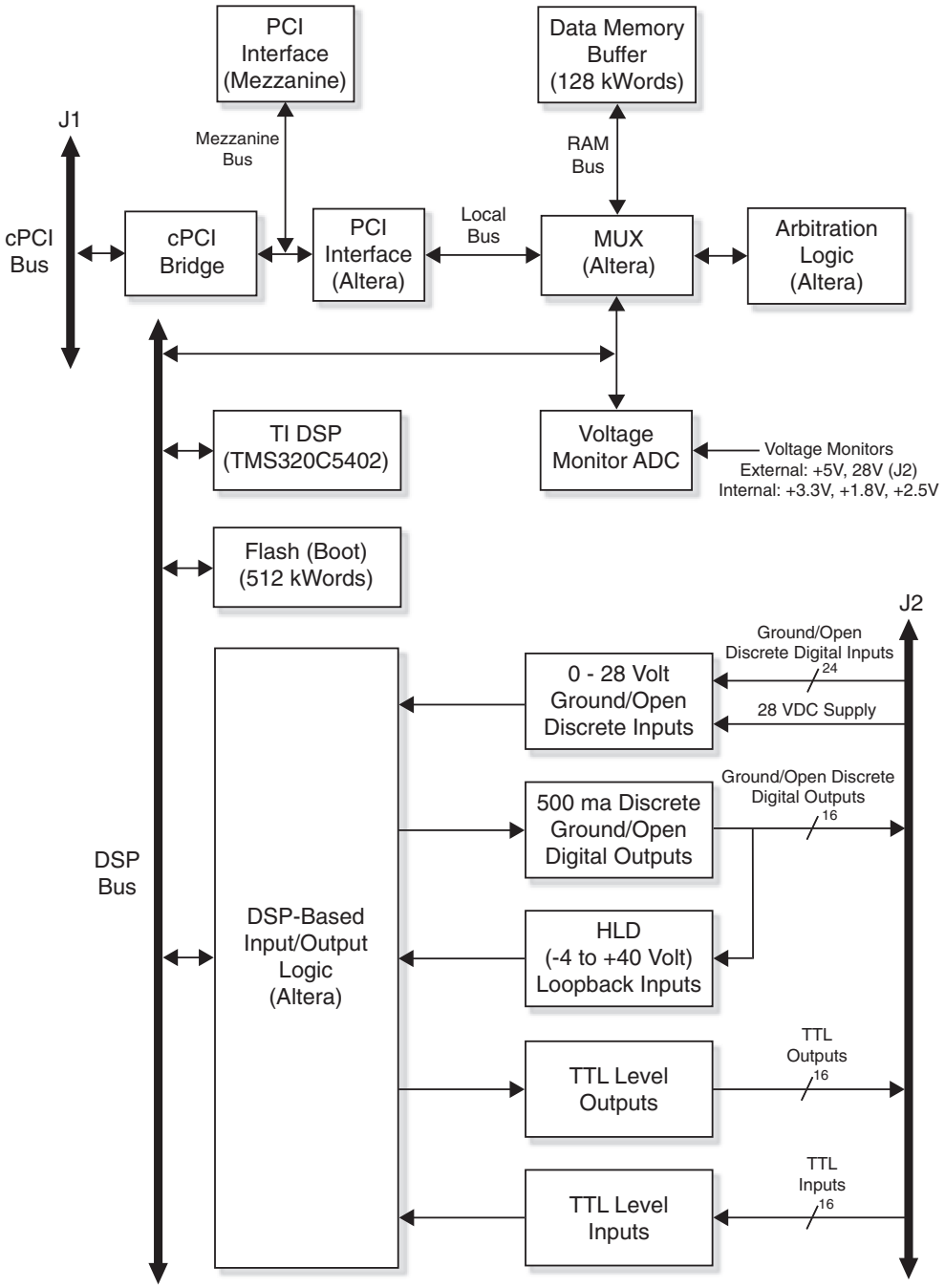


Figure 6.1.1: DIO4-cPCI-CC Functional Block Diagram

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6.1.2 Memory

DIO4 contains RAM and Flash memory. See Figure 6.1.1.

RAM DIO4 has 128k 16-bit words of SRAM for storage of software control, status registers, and data structures. RAM is also a temporary storage buffer for reloading Flash memory with updated DSP code and FPGA configuration data.

Flash DIO4 has 512k 16-bit words of Flash memory for storage of DSP code and FPGA configuration data.

6.1.3 cPCI Bridge

The cPCI Bridge provides an interface between the cPCI bus and the PCI bus.

6.1.4 PCI Mezzanine Interface (PMC)

PCI Mezzanine Interface (PMC) provides an interface between the PCI bus and the PMC bus for an optional PMC card.

6.1.5 Alteras (FPGAs)

DIO4 uses the Alteras (FPGAs) for the PCI Interface, Mux, and the Arbitration Logic. See Figure 6.1.1.

PCI Interface DIO4 PCI Interface Altera (FPGA) provides the interface between the cPCI Bridge and the rest of the module.

Mux Mux Altera (FPGA) provides the interface between the Local Bus, RAM Bus, DSP Bus, and the Arbitration Logic.

Arbitration Logic Altera (FPGA) Arbitration Logic Altera (FPGA) arbitrates between PCI Interface access and DSP access to memory.

6.1.6 Voltage Monitor ADC

Voltage Monitor ADC monitors the following power supply voltages:

- External: +5 V and 28 V
- Internal: +1.8 V, +2.5 V, and +3.3 V

Voltage Monitor ADC sends the results to the DSP.

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6.1.7 Input Signal Processing

DIO4 receives input signals consisting of Discrete Ground/Open Inputs, TTL Level Discrete Inputs, and HLD Loopback Inputs. See Figure 6.1.1. DSP determines the state of each incoming signal. DSP formats and stores this information in the RAM software registers. All inputs have programmable main processor interrupt capability.

Discrete Ground/Open Inputs

DIO4 has twenty-four 0 to 28 V Discrete Ground/Open Inputs. See Figure 6.1.1. The circuits are shown in Figure 6.1.2.

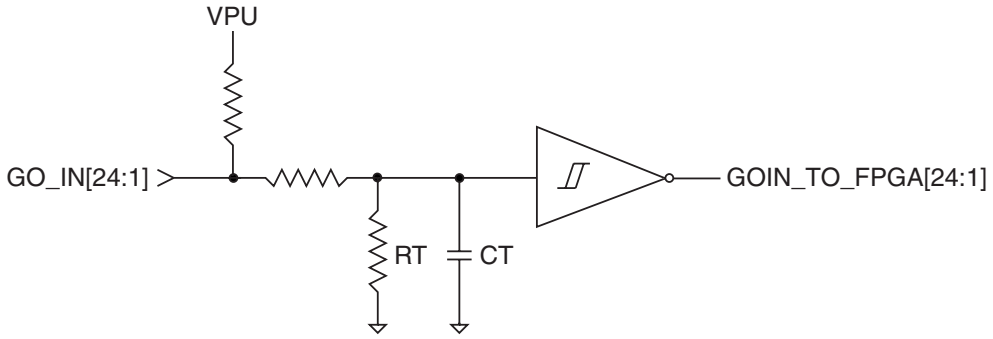


Figure 6.1.2: 0-28 Volt Discrete Ground/Open Input Circuits

TTL Level Discrete Inputs

DIO4 has 16 TTL level discrete input lines each with pull-up resistors (4.7K ohms). See Figure 6.1.1. Figure 6.1.3 shows the circuit.

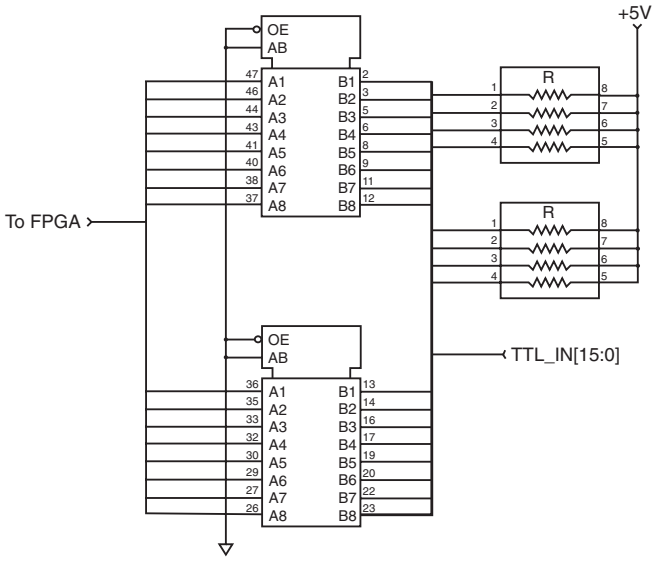


Figure 6.1.3: TTL Level Discrete Inputs Circuit

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HLD Loopback Inputs

DIO4 has 16 HLD Loopback Inputs lines. See Figure 6.1.1. Each of these loopback signals comes from Discrete Ground/Open Output line. Figure 6.1.4 shows the circuit.

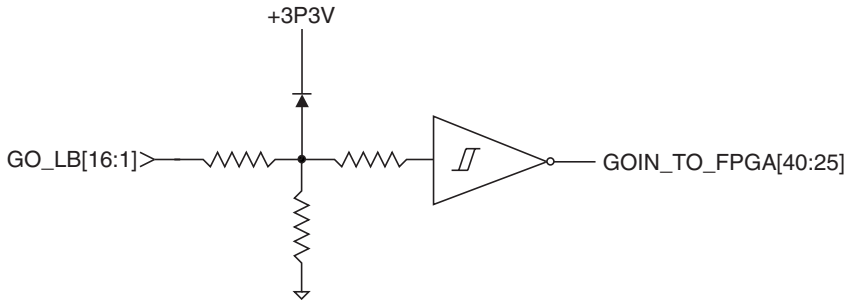


Figure 6.1.4: HLD Loopback Input Circuit

6.1.8 Output Signal Processing

DIO4 generates output signals consisting of Discrete Ground/Open Outputs and TTL Level Discrete Outputs. See Figure 6.1.1. DSP reads the RAM data structures and uses this information to generate discrete outputs on command.

Discrete Ground/Open Outputs

DIO4 has 16 Discrete Ground/Open Outputs. See Figure 6.1.1. Figure 6.1.5 shows the circuit.

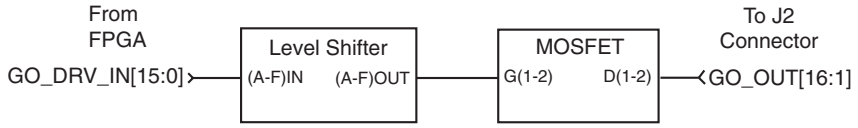


Figure 6.1.5: Discrete Ground/Open Output Circuit

TTL Level Discrete Outputs

DIO4 has 16 TTL Level Discrete Outputs. See Figure 6.1.1. Figure 6.1.6 shows the circuit.

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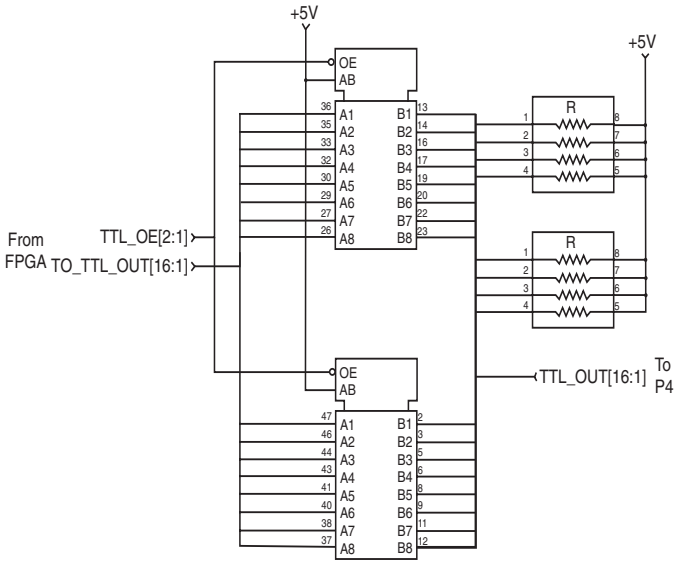


Figure 6.1.6: TTL Level Discrete Output Circuit

6.2 Physical Specifications

6.2.1 Layout and Connectors

DIO4-cPCI-CC card has two cPCI connectors and three PMC connectors. Figure 6.2.1 shows the J1 and J2 and P1, P2, and P4 connectors.

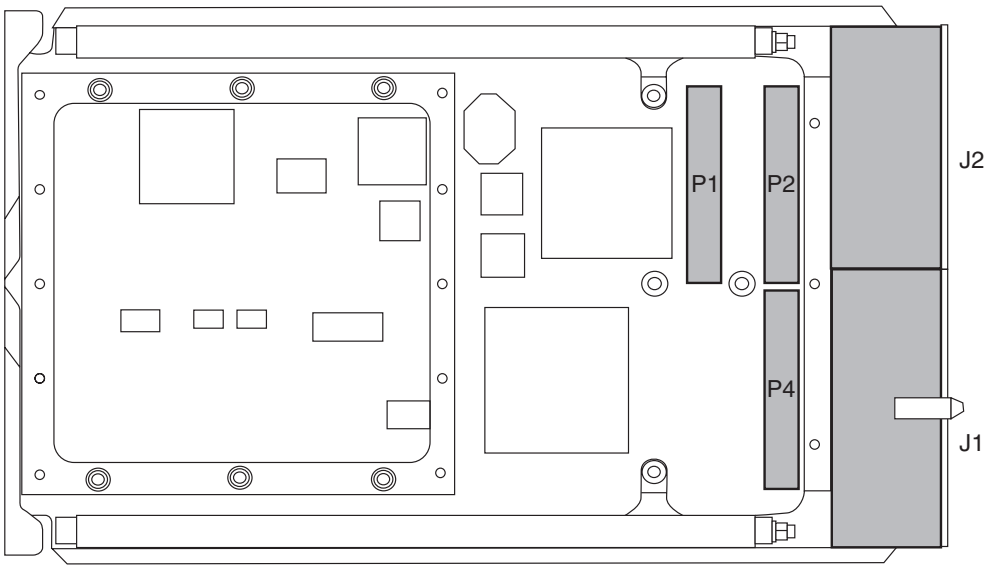


Figure 6.2.1: DIO4-cPCI-CC Layout

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6.2.2 J1 Pin and Signal Assignments

Table 6.2.1 shows the pin and signal assignments for J1.

Table 6.2.1: J1 Pin and Signal Assignments

		Connector Row					
		A	B	C	D	E	F
Connector Column	1	5V	-12V	TRST#	+12V	5V	GND
	2	TCK	5V	TMS	TDO	TDI	GND
	3	INTA#	INTB#	INTC#	5V	INTD#	GND
	4	BRSVP1A4	GND	V(I/O)	INTP	INTS	GND
	5	BRSVP1A5	BRSVP1B5	RST#	GND	GNT#	GND
	6	REQ#	GND	3.3V	CLK	AD31	GND
	7	AD30	AD29	AD28	GND	AD27	GND
	8	AD26	GND	V(I/O)	AD25	AD24	GND
	9	C/BE3#	IDSEL	AD23	GND	AD22	GND
	10	AD21	GND	3.3V	AD20	AD19	GND
	11	AD18	AD17	AD16	GND	C/BE2#	GND
	12	KEY	KEY	KEY	KEY	KEY	KEY
	13	KEY	KEY	KEY	KEY	KEY	KEY
	14	KEY	KEY	KEY	KEY	KEY	KEY
	15	3.3V	FRAME#	IRDY#	GND	TRDY#	GND
	16	DEVSEL#	GND	V(I/O)	STOP#	LOCK#	GND
	17	3.3V	SDONE	SBO#	GND	PERR#	GND
	18	SERR#	GND	3.3V	PAR	C/BE1#	GND
	19	3.3V	AD15	AD14	GND	AD13	GND
	20	AD12	GND	V(I/O)	AD11	AD10	GND
	21	3.3V	AD09	AD08	M66EN	C/BE0#	GND
	22	AD07	GND	3.3V	AD06	AD05	GND
	23	3.3V	AD04	AD03	5V	AD02	GND
	24	AD01	5V	V(I/O)	AD00	ACK64#	GND
	25	5V	REQ64#	ENUM#	3.3V	5V	GND

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6.2.3 J2 Pin and Signal Assignments

Table 6.2.2 shows the pin and signal assignments for the J2 connector. J2 signals are the I/O (user defined) signals.

Table 6.2.2: J2 Pin and Signal Assignments

		Connector Row					
		A	B	C	D	E	F
Connector Column	1	TTL_IN1	TTL_IN9	GO_OUT13	GO_IN1	GO_IN19	GND
	2	TTL_IN2	TTL_IN10	GO_OUT14	GO_IN2	GO_IN20	GND
	3	TTL_IN3	TTL_IN11	GO_OUT15	GO_IN3	GO_IN21	GND
	4	TTL_IN4	TTL_IN12	GO_OUT16	GO_IN4	GO_IN22	GND
	5	TTL_IN5	TTL_IN13	MEZZ9	GO_IN5	GO_IN23	GND
	6	TTL_IN6	TTL_IN14	MEZZ10	GO_IN6	GO_IN24	GND
	7	TTL_IN7	TTL_IN15	MEZZ11	GO_IN7	GND	GND
	8	TTL_IN8	TTL_IN16	+28V	GO_IN8	MEZZ12	GND
	9	TTL_OUT1	TTL_OUT9	GND	GO_IN9	MEZZ13	GND
	10	TTL_OUT2	TTL_OUT10	GO_OUT1	GO_IN10	MEZZ14	GND
	11	TTL_OUT3	TTL_OUT11	GO_OUT2	GO_IN11	MEZZ15	GND
	12	TTL_OUT4	TTL_OUT12	GO_OUT3	GO_IN12	MEZZ16	GND
	13	TTL_OUT5	TTL_OUT13	GO_OUT4	GO_IN13	MEZZ17	GND
	14	TTL_OUT6	TTL_OUT14	GO_OUT5	GO_IN14	MEZZ18	GND
	15	TTL_OUT7	TTL_OUT15	GO_OUT6	GO_IN15	MEZZ19	GND
	16	TTL_OUT8	TTL_OUT16	GO_OUT7	GO_IN16	MEZZ20	GND
	17	GND	MEZZ5	GO_OUT8	GO_IN17	MEZZ21	GND
	18	MEZZ1	MEZZ6	GO_OUT9	GO_IN18	MEZZ22	GND
	19	MEZZ2	MEZZ7	GO_OUT10	+12V	MEZZ23	GND
	20	MEZZ3	MEZZ8	GO_OUT11	GND	MEZZ24	GND
	21	MEZZ4	GND	GO_OUT12	3.3V	5V	GND
	22	GA4	GA3	GA2	GA1	GA0	GND

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6.2.4 Mezzanine Connectors

DIO4 provides two mezzanine connectors (P1 and P2) for PMC Bus Extension into the mezzanine and one mezzanine connector (P4) for user-defined signals. See Figure 6.2.2, Figure 6.2.3, and Figure 6.2.2 for the signal identifications P1, P2 and P4, respectively.

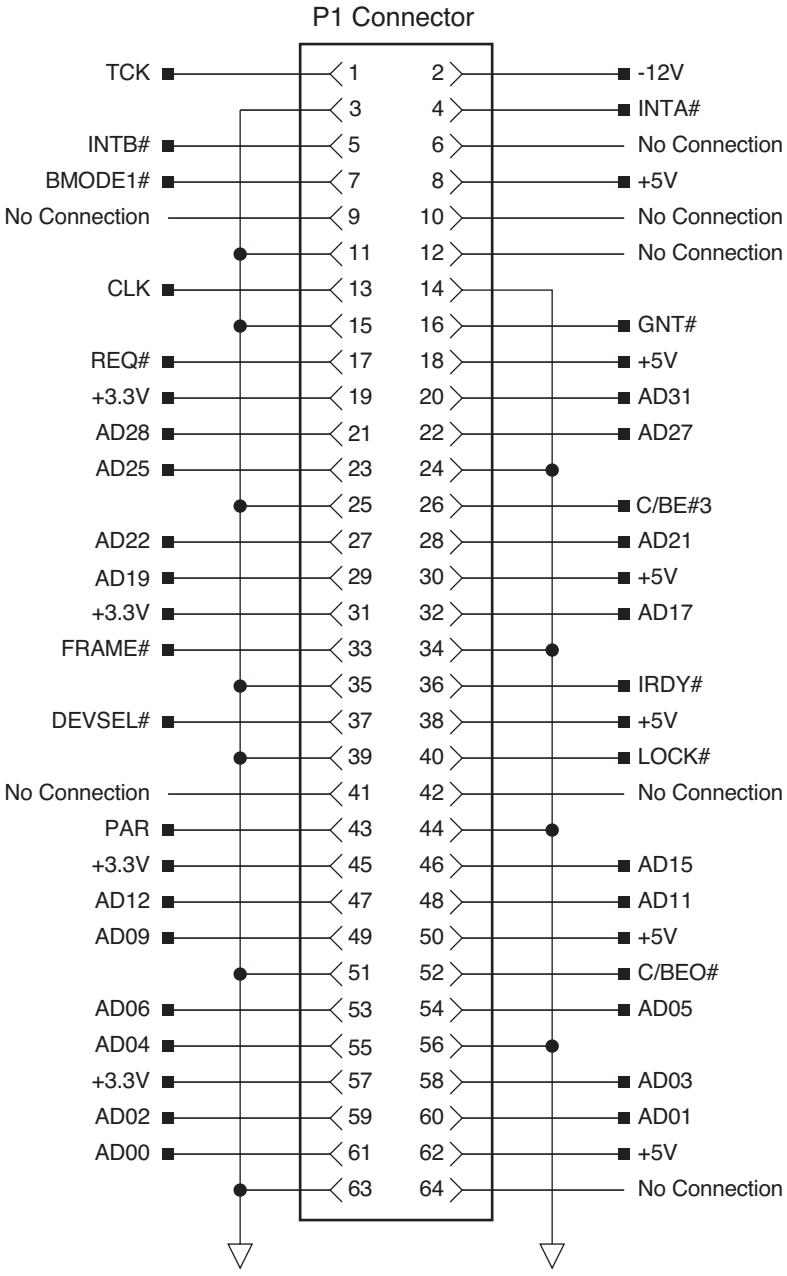


Figure 6.2.2: Mezzanine Connector P1

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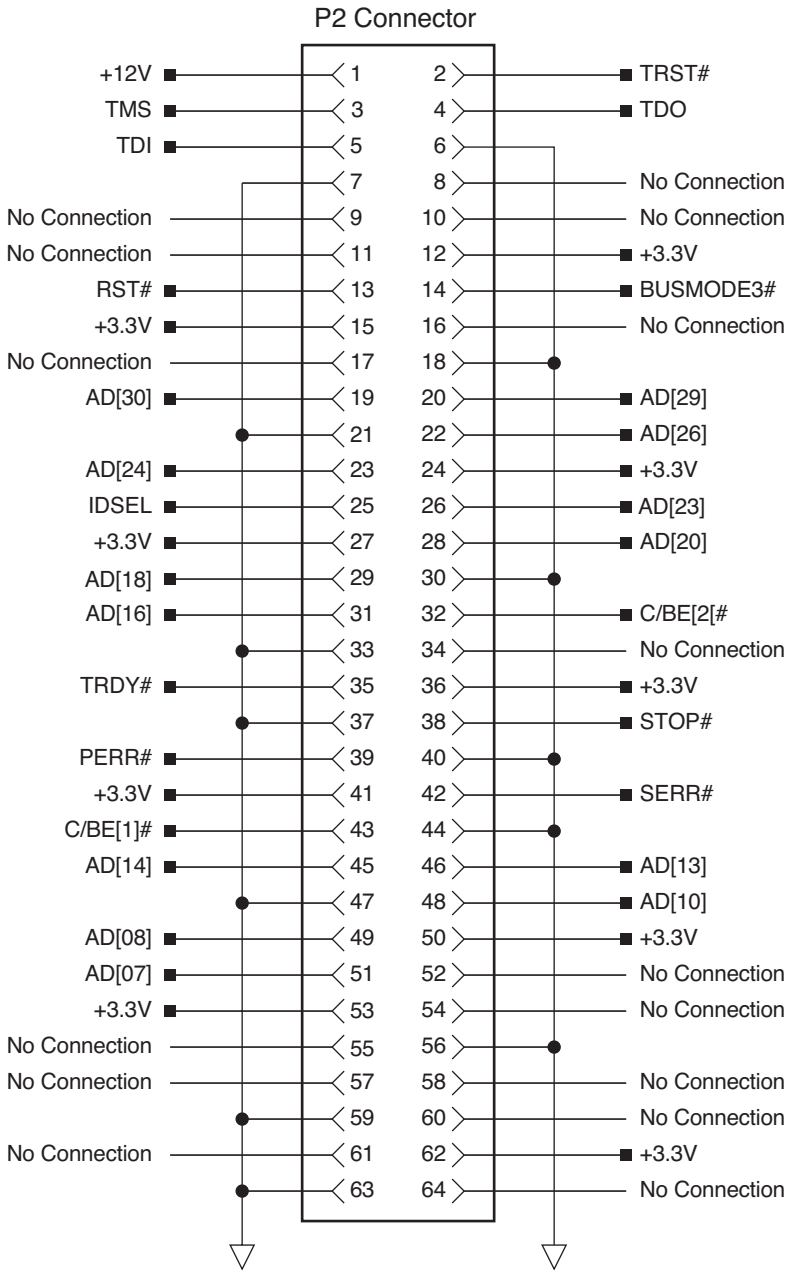


Figure 6.2.3: Mezzanine Connector P2

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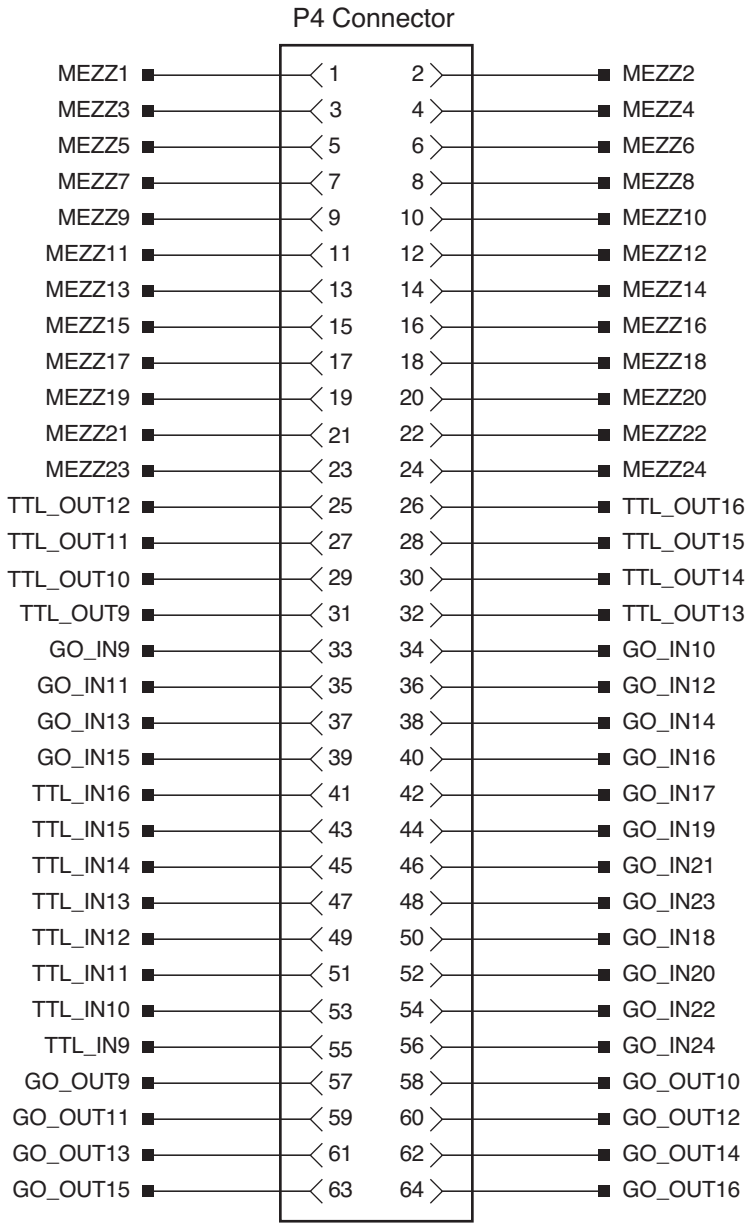


Figure 6.2.4: Mezzanine Connector P4

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6.3 Operational Specifications

6.3.1 Specifications

Table 6.3.1 lists the specifications for the DIO4-cPCI-CC card.

Table 6.3.1: Specifications

Specification	Description
Form Factor	cPCI 3U
I/O Connector	J1, J2
Dimensions	3U Euroboard, 100.0 mm x 160.0 mm
Weight	Will not exceed 0.159 kg (0.35 lb.)
Power Requirements	+5.0 VDC
Environmental	Operating temperature: -40 to +85°C Humidity: 5 to 95% non-condensing Storage: -55 to +105°C

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7: Hardware Register Information

This chapter describes hardware operation for the DIO4-cPCI-CC card. The sections are as follows:

- Introduction
- Hardware Control Registers

7.1 Introduction

DIO4-cPCI-CC card provides an interface between the cPCI bus and DSP-Based inputs and outputs. Figure 7.1.1 shows a data flow diagram of the DIO4. DIO4 card contains a DSP, a 128-kword RAM buffer, a 512-kword Flash memory, and FPGA's containing hardware registers and control logic. Host processor accesses the RAM buffer via the cPCI interface. Various hardware and software registers control the operation of the board. Chapter 8: Card Information discusses the software registers. This chapter describes the hardware registers (Hardware Control Registers).

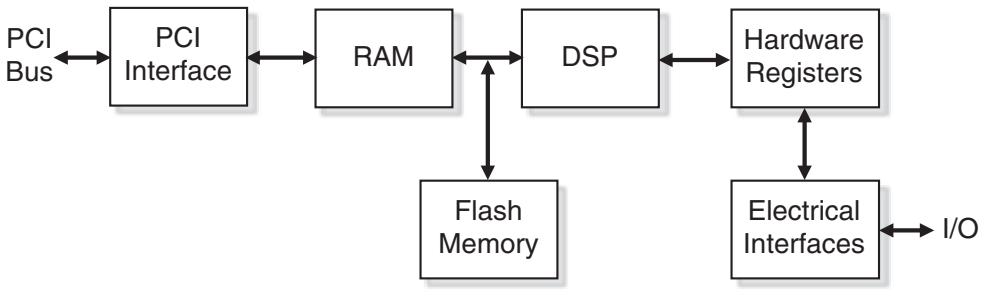


Figure 7.1.1: DIO4 Data Flow Diagram

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7.2 Hardware Control Registers

Hardware control registers divide into three categories: PCI configuration registers, main device Control/Status Register (CSR), and secondary device registers. PCI configuration registers configure the PCI bus interface. Main module CSR controls activation of the module and configures host interrupts. Generally you refer to the main module CSR as the CSR. The module also has reserved space for 16 secondary registers which control detailed configuration and operation of the module. Secondary registers access and control the DSP-Based I/O signals.

7.2.1 DIO4 PCI Configuration Registers

PCI interface uses an Altera core function. PCI register data compiles into the FPGA hardware. Host computer requires the following information to identify the DIO4-cPCI-CC module in PCI Configuration space.

Table 7.2.1: Host Computer ID Requirements

Name	Address	Description
Device ID	0003	Altera device ID
Vendor ID	1172	Altera vendor ID
Subdevice ID	0011	SBS DIO4-cPCI-CC module device ID
Subvendor ID	12DF	SBS vendor ID

Other Requirements

- ➢ Class Code is “Network Controller” (02).
- ➢ Sub-Class Code is “Other” (80).
- ➢ Board memory requirement is one megabyte.
- ➢ PCI interrupt pin INTA# is enabled.

7.2.2 DIO4-cPCI-CC CSR

DIO4-cPCI-CC provides a CSR that is asymmetrical with slightly different read and write definitions. Only the Host computer can access the CSR. Table 7.2.2 defines the CSR for the DIO4-cPCI-CC.

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Table 7.2.2: Device 1 CSR Definition (40000h Wd)

Bit	Function	Description
D0	DSP Reset	0=DSP (Firmware) Run 1=DSP (Firmware) Reset
D1	Flash/RAM	0=RAM 1=Flash
D2	Master interrupt to generate interrupt	0=Blocked 1=Enabled
D3	DSP Interrupt Enable to generate interrupt	0=Blocked 1=Enabled
D4	Altera Reload	0=No Reload 1=Reload
D5	Reserved	-
D6	Clear Master Interrupt (WO)	0=N/A 1=Clear
	Master Interrupt Status (RO)	0=No Interrupt 1=Interrupt Pending
D7	Clear DSP Interrupt(W0)	0=N/A 1=Clear
	DSP Interrupt Status	0=No Interrupt 1=Interrupt Pending
D8-D15	Reserved	-

(RO) = Read Only
(W0) = Write Only

7.2.3 DIO4-cPCI-CC Secondary Registers

Secondary hardware registers provide a means of configuring and controlling DIO4 specific functions. Secondary registers are only accessible via the DSP. While secondary registers are not directly accessible by the host computer, some of the registers are indirectly accessible via the DSP and software registers located in device RAM. Location of Registers 0 through B are in the 10KE100 (PCI) array. Location of Registers C-F are in the 7256 (Mux) array. Access the 16 secondary hardware registers via the DSP I/O port. Table 7.2.3 lists each secondary hardware register and its DSP I/O port address. Table 7.2.3 shows the secondary hardware register definitions and bit mappings.

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Table 7.2.3: Secondary Hardware Registers

Address	Mnemonic	Name	Function
0	GCSR	General CSR	General Control Status Register (See Table 7.2.4)
1	HCSR	Host CSR	Host Control Status Register (See Table 7.2.5)
2	GPIO	General Purpose I/O	GPIO to PCI Bridge Chip & Geographical Address (See Table 7.2.6)
3	ADCC	ADC Control	Analog to Digital Control Register (See Table 7.2.7)
4	SPAREIO	Spare Inputs & Outputs	Spare Inputs & Outputs Register (See Table 7.2.8)
5	TTLOUT	TTL Outputs	TTL Output Register (See Table 7.2.9)
6	TTLIN	TTL Inputs	TTL Input Register (See Table 7.2.10)
7	GOOUT	Ground/Open 28V Output	Ground/Open Output Register (See Table 7.2.11)
8	GOOCF	Current Fault Registers	Current Fault Register for Ground/Open Outputs (See Table 7.2.12)
9	GOINV1	Inversion Selection for GOIN #1	Ground/Open Inverted Inputs #1 Register (See Table 7.2.13)
A	GOIN1	Ground/Open Inputs #1	Ground/Open Inputs #1 Register (See Table 7.2.14)
B	GOIN2	Ground/Open Inputs #2	Ground/Open Inputs #2 Register (See Table 7.2.15)
C	GOOLB	Loopback Inputs for GOOUT	Ground/Open Output Loopback Input Register (See Table 7.2.16)
D	BSP1	DSP BSP1	Future use – Not implemented (See Table 7.2.17)
E	ALTRG	10KE CSR	Altera 10KE Configuration (4 BITS) (See Table 7.2.18)
F	MEMCSR	Memory Page CSR	DSP Status and Memory Page Control & Device ID (4 bits) (See Table 7.2.19)

DSP I/O Address 0h General CSR (Read/Write)

Table 7.2.4: DSP I/O Address 0h

Bit	Definition
D0	Reset of specific functions (Read = 0)
D1	Unused (Read = 0
D2	Clear Interrupt Host Bit 7 in Main CSR (Routed through CSR & PCI to Host) (Read = 0)
D3	Read Interrupt Host Bit 7 in Main CSR (Routed through CSR & PCI to Host) (No Write)

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Bit	Definition
D4	Set Interrupt Host Bit 7 in Main CSR (Routed through CSR & PCI to Host) (Read = 0)
D5	Timer Control Bit Enable (Read =Write)
D6	Ready Timer Output Active (Read =Write)
D7-D11	Unused (Read = 0)
D12	Test Bit Enable (Enables changing of Bits D13-D15) (Read = 0)
D13	Write = DSP Test Bit 1
D14	Write = DSP Test Bit 2
D15	Write = DSP Test Bit 3 (Route to Test Points)

DSP I/O Address 1h Host CSR read by DSP (Read Only)

Table 7.2.5: DSP I/O Address 1h

Bit	Definition
D0-D7	Host CSR (Read only)
D8-D15	Unused, reads 45h

DSP I/O Address 2h GPIO to PCI Bridge Chip and Geographical Address (Read/Write)

Table 7.2.6: DSP I/O Address 2h

Bit	Definition
D0	PCI_GPIO Bit 0
D1	PCI_GPIO Bit 1
D2	PCI_GPIO Bit 2
D3	PCI_GPIO Bit 3
D4	Output bit - Not assigned
D5	Data Direction of GPIO Bits 0-3, 0 = In, 1 = Out
D6-D7	Unused (Read = 0)
D8	GA0
D9	GA1
D10	GA2
D11	GA3
D12	GA4
D13-D15	Unused (Read = 0)

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DSP I/O Address 3h ADC Control and MUX TPs (Read/Write) and Enables

Table 7.2.7: DSP I/O Address 3h

Bit	Definition
D0	ADC Enable
D1	End of Conversion (Status - Read Only)
D2	ADC Interrupt Enable to DSP (1 = Enable)
D3	Interrupt Acknowledge from DSP
D4	MUX_TP1 Input from 7256 TP2 (Can be read back)
D5	MUX_TP2 Input from 7256 TP3 (Can be read back)
D6	MUX_TP3 Input from 7256 TP3 (Can be read back)
D7	MUX_TP4 Input from 7256 TP4 (Can be read back)
D8	MUX_TP5 Output to 7256 TP5 (Can be read back)
D9	MUX_TP6 Output to 7256 TP6 (Can be read back)
D10	Reserved for future use (Read = 0)
D11	TTL Output (Bits 0-7) Enable (1 = Enable, Can be read back)
D12	TTL Output (Bits 8-15) Enable (1 = Enable, Can be read back)
D13	Reserved for future use (Read = 0)
D14	12V Gate Drive Power Supply Enable (1 = Enable, Can be read back)
D15	Low 28 Volt Supply (0 = Undervoltage on 28V, 1= Normal)

DSP I/O Address 4h Spare Inputs and Outputs

Table 7.2.8: DSP I/O Address 4h

Bit	Definition
D0	Spare Output 0 (Reads back value written)
D1	Spare Output 1 (Reads back value written)
D2	Spare Output 2 (Reads back value written)
D3	Spare Output 3 (Reads back value written)
D4	Spare Output 4 (Reads back value written)
D5	Spare Output 5 (Reads back value written)
D6	Spare Output 6 (Reads back value written)
D7	Spare Output 7 (Reads back value written)
D8	Spare Input 0 (Read Only)
D9	Spare Input 1 (Read Only)

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Bit	Definition
D10	Spare Input 2 (Read Only)
D11	Spare Input 3 (Read Only)
D12	Spare Input 4 (Read Only)
D13	Spare Input 5 (Read Only)
D14	Spare Input 6 (Read Only)
D15	Spare Input 7 (Read Only)

DSP I/O Address 5h TTL Output Control (Read/Write)

Table 7.2.9: DSP I/O Address 5h

Bit	Definition
D0	TTL Output 0 (Reads back value written)
D1	TTL Output 1 (Reads back value written)
D2	TTL Output 2 (Reads back value written)
D3	TTL Output 3 (Reads back value written)
D4	TTL Output 4 (Reads back value written)
D5	TTL Output 5 (Reads back value written)
D6	TTL Output 6 (Reads back value written)
D7	TTL Output 7 (Reads back value written)
D8	TTL Output 8 (Reads back value written)
D9	TTL Output 9 (Reads back value written)
D10	TTL Output10 (Reads back value written)
D11	TTL Output 11 (Reads back value written)
D12	TTL Output 12 (Reads back value written)
D13	TTL Output 13 (Reads back value written)
D14	TTL Output 14 (Reads back value written)
D15	TTL Output 15 (Reads back value written)

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DSP I/O Address 6h TTL Inputs (Read Only)

Table 7.2.10: DSP I/O Address 6h

Bit	Definition
D0	TTL Input 0 (Read only)
D1	TTL Input 1 (Read only)
D2	TTL Input 2 (Read only)
D3	TTL Input 3 (Read only)
D4	TTL Input 4 (Read only)
D5	TTL Input 5 (Read only)
D6	TTL Input 6 (Read only)
D7	TTL Input 7 (Read only)
D8	TTL Input 8 (Read only)
D9	TTL Input 9 (Read only)
D10	TTL Input 10 (Read only)
D11	TTL Input 11 (Read only)
D12	TTL Input 12 (Read only)
D13	TTL Input 13 (Read only)
D14	TTL Input 14 (Read only)
D15	TTL Input 15 (Read only)

DSP I/O Address 7h Ground/Open Discrete Output Control (Read/Write)

Table 7.2.11: DSP I/O Address 7h

Bit	Definition
D0	Ground/Open Discrete Output 1 (Write a 1 to turn on (Sink), Reads back value written)
D1	Ground/Open Discrete Output 2 (Write a 1 to turn on (Sink), Reads back value written)
D2	Ground/Open Discrete Output 3 (Write a 1 to turn on (Sink), Reads back value written)
D3	Ground/Open Discrete Output 4 (Write a 1 to turn on (Sink), Reads back value written)
D4	Ground/Open Discrete Output 5 (Write a 1 to turn on (Sink), Reads back value written)
D5	Ground/Open Discrete Output 6 (Write a 1 to turn on (Sink), Reads back value written)
D6	Ground/Open Discrete Output 7 (Write a 1 to turn on (Sink), Reads back value written)
D7	Ground/Open Discrete Output 8 (Write a 1 to turn on (Sink), Reads back value written)
D8	Ground/Open Discrete Output 9 (Write a 1 to turn on (Sink), Reads back value written)
D9	Ground/Open Discrete Output 10 (Write a 1 to turn on (Sink), Reads back value written)

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Bit	Definition
D10	Ground/Open Discrete Output 11 (Write a 1 to turn on (Sink), Reads back value written)
D11	Ground/Open Discrete Output 12 (Write a 1 to turn on (Sink), Reads back value written)
D12	Ground/Open Discrete Output 13 (Write a 1 to turn on (Sink), Reads back value written)
D13	Ground/Open Discrete Output 14 (Write a 1 to turn on (Sink), Reads back value written)
D14	Ground/Open Discrete Output 15 (Write a 1 to turn on (Sink), Reads back value written)
D15	Ground/Open Discrete Output 16 (Write a 1 to turn on (Sink), Reads back value written)

DSP I/O Address 8h

Ground/Open Discrete Output Current Fault (Write to Clear)

Table 7.2.12: DSP I/O Address 8h

Bit	Definition
D0	Ground/Open Discrete Output 1 (Over Current Fault Detected)
D1	Ground/Open Discrete Output 2 (Over Current Fault Detected)
D2	Ground/Open Discrete Output 3 (Over Current Fault Detected)
D3	Ground/Open Discrete Output 4 (Over Current Fault Detected)
D4	Ground/Open Discrete Output 5 (Over Current Fault Detected)
D5	Ground/Open Discrete Output 6 (Over Current Fault Detected)
D6	Ground/Open Discrete Output 7 (Over Current Fault Detected)
D7	Ground/Open Discrete Output 8 (Over Current Fault Detected)
D8	Ground/Open Discrete Output 9 (Over Current Fault Detected)
D9	Ground/Open Discrete Output 10 (Over Current Fault Detected)
D10	Ground/Open Discrete Output 11 (Over Current Fault Detected)
D11	Ground/Open Discrete Output 12 (Over Current Fault Detected)
D12	Ground/Open Discrete Output 13 (Over Current Fault Detected)
D13	Ground/Open Discrete Output 14 (Over Current Fault Detected)
D14	Ground/Open Discrete Output 15 (Over Current Fault Detected)
D15	Ground/Open Discrete Output 16 (Over Current Fault Detected)
	Note: Write anything to this register to clear it.

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DSP I/O Address 9h Bipolar Ground/Open Input Polarity Select #1 (Read/Write)

Table 7.2.13: DSP I/O Address 9h

Bit	Definition
D0	Ground/Open (HLD Discrete) # 1 Input Polarity (Write a 1 to Invert, Reads back value written)
D1	Ground/Open (HLD Discrete) # 2 Input Polarity (Write a 1 to Invert, Reads back value written)
D2	Ground/Open (HLD Discrete) # 3 Input Polarity (Write a 1 to Invert, Reads back value written)
D3	Ground/Open (HLD Discrete) # 4 Input Polarity (Write a 1 to Invert, Reads back value written)
D4	Ground/Open (HLD Discrete) # 5 Input Polarity (Write a 1 to Invert, Reads back value written)
D5	Ground/Open (HLD Discrete) # 6 Input Polarity (Write a 1 to Invert, Reads back value written)
D6	Ground/Open (HLD Discrete) # 7 Input Polarity (Write a 1 to Invert, Reads back value written)
D7	Ground/Open (HLD Discrete) # 8 Input Polarity (Write a 1 to Invert, Reads back value written)
D8	Ground/Open (HLD Discrete) # 9 Input Polarity (Write a 1 to Invert, Reads back value written)
D9	Ground/Open (HLD Discrete) # 10 Input Polarity (Write a 1 to Invert, Reads back value written)
D10	Ground/Open (HLD Discrete) # 11 Input Polarity (Write a 1 to Invert, Reads back value written)
D11	Ground/Open (HLD Discrete) # 12 Input Polarity (Write a 1 to Invert, Reads back value written)
D12	Ground/Open (HLD Discrete) # 13 Input Polarity (Write a 1 to Invert, Reads back value written)
D13	Ground/Open (HLD Discrete) # 14 Input Polarity (Write a 1 to Invert, Reads back value written)
D14	Ground/Open (HLD Discrete) # 15 Input Polarity (Write a 1 to Invert, Reads back value written)
D15	Ground/Open (HLD Discrete) # 16 Input Polarity (Write a 1 to Invert, Reads back value written)

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DSP I/O Address Ah Ground/ Open Input Register #1 (Read Only)

Table 7.2.14: DSP I/O Address Ah

Bit	Definition
D0	Ground/Open Discrete Input # 1 (Reads value on input)
D1	Ground/Open Discrete Input # 2 (Reads value on input)
D2	Ground/Open Discrete Input # 3 (Reads value on input)
D3	Ground/Open Discrete Input # 4 (Reads value on input)
D4	Ground/Open Discrete Input # 5 (Reads value on input)
D5	Ground/Open Discrete Input # 6 (Reads value on input)
D6	Ground/Open Discrete Input # 7 (Reads value on input)
D7	Ground/Open Discrete Input # 8 (Reads value on input)
D8	Ground/Open Discrete Input # 9 (Reads value on input)
D9	Ground/Open Discrete Input # 10 (Reads value on input)
D10	Ground/Open Discrete Input # 11 (Reads value on input)
D11	Ground/Open Discrete Input # 12 (Reads value on input)
D12	Ground/Open Discrete Input # 13 (Reads value on input)
D13	Ground/Open Discrete Input # 14 (Reads value on input)
D14	Ground/Open Discrete Input # 15 (Reads value on input)
D15	Ground/Open Discrete Input # 16 (Reads value on input)

DSP I/O Address Bh Ground/Open Input Register #2

Table 7.2.15: DSP I/O Address Bh

Bit	Definition
D0	Ground/Open Discrete Input # 17 (Reads value on input)
D1	Ground/Open Discrete Input # 18 (Reads value on input)
D2	Ground/Open Discrete Input # 19 (Reads value on input)
D3	Ground/Open Discrete Input # 20 (Reads value on input)
D4	Ground/Open Discrete Input # 21 (Reads value on input)
D5	Ground/Open Discrete Input # 22 (Reads value on input)
D6	Ground/Open Discrete Input # 23 (Reads value on input)
D7	Ground/Open Discrete Input # 24 (Reads value on input)
D8	Ground/Open (HLD Discrete) # 17 Input Polarity (Write a 1 to Invert, Reads back value written)

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Bit	Definition
D9	Ground/Open (HLD Discrete) # 18 Input Polarity (Write a 1 to Invert, Reads back value written)
D10	Ground/Open (HLD Discrete) # 19 Input Polarity (Write a 1 to Invert, Reads back value written)
D11	Ground/Open (HLD Discrete) # 20 Input Polarity (Write a 1 to Invert, Reads back value written)
D12	Ground/Open (HLD Discrete) # 21 Input Polarity (Write a 1 to Invert, Reads back value written)
D13	Ground/Open (HLD Discrete) # 22 Input Polarity (Write a 1 to Invert, Reads back value written)
D14	Ground/Open (HLD Discrete) # 23 Input Polarity (Write a 1 to Invert, Reads back value written)
D15	Ground/Open (HLD Discrete) # 24 Input Polarity (Write a 1 to Invert, Reads back value written)

DSP I/O Address Ch Ground/Open Output Feedback Register

Table 7.2.16: DSP I/O Address Ch

Bit	Definition
D0	Ground/Open Discrete Output 1 (Read only)
D1	Ground/Open Discrete Output 2 (Read only)
D2	Ground/Open Discrete Output 3(Read only)
D3	Ground/Open Discrete Output 4 (Read only)
D4	Ground/Open Discrete Output 5 (Read only)
D5	Ground/Open Discrete Output 6 (Read only)
D6	Ground/Open Discrete Output 7 (Read only)
D7	Ground/Open Discrete Output 8 (Read only)
D8	Ground/Open Discrete Output 9 (Read only)
D9	Ground/Open Discrete Output 10 (Read only)
D10	Ground/Open Discrete Output 11 (Read only)
D11	Ground/Open Discrete Output 12 (Read only)
D12	Ground/Open Discrete Output 13 (Read only)
D13	Ground/Open Discrete Output 14 (Read only)
D14	Ground/Open Discrete Output 15 (Read only)
D15	Ground/Open Discrete Output 16 (Read only)

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DSP I/O Address Dh DSP Serial I/F BSP 1 (Future Use)

Table 7.2.17: DSP I/O Address Dh

Bit	Definition
D0	BFSX1 (Transmit Data Synchronization) (Read/Write)
D1	BDX1 (Transmit Data) (Read)
D2	BCLKX1 (Transmit Reference Clock) (Read/Write)
D3	BFSR1 (Receive Frame Synchronization) (Read/Write)
D4	BDR1 (Receive Data) (Write)
D5	BCLKR1 (Receive Reference Clock) (Read/Write)
D6-D15	Unused (Read = 0)

DSP I/O Address Eh 10KE CSR Bit Definition (Read/Write)

Table 7.2.18: DSP I/O Address Eh

Bit	Definition
D0	Altera Clock (ALTCLK = 1h)
D1	Altera Data (Read = zero) (ALTDATA = 2h)
D2	Altera Configuration (ALTCFG = 4h)
D3	Altera Done (Read Only) (ALTDONE = 8h)
D4-D7	(Reads Back same as Register F)
D8-D15	Unused (Read = 0)

DSP I/O Address Fh Memory Page Register Bit Definition (Read/Write)

Table 7.2.19: DSP I/O Address Fh

Bit	Definition
D0	Memory Address Bit A0 (See Figure 7.2.1)
D1	Memory Address Bit A1 (See Figure 7.2.1)
D2	Memory Address Bit A2 (See Figure 7.2.1)
D3	Memory Address Bit A3 (See Figure 7.2.1)
D4	Memory Address Bit A4 (See Figure 7.2.1)
D5	Memory Address Bit A5 (Reserved for Future Expansion)
D6	Altera Status. (Read Only)

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Bit	Definition
D7	Status from Flash Memory
D8-D12	Unused (Read = 0)
D13	DSP_TOUT0 (Read)
D14	DSP_BIO (Read)
D15	DSP_XF (Read)

Bits					Selection
D4	D3	D2	D1	D0	
0	0	0	0	0	Memory Page 1
0	0	0	0	1	Memory Page 2
0	0	0	1	0	Memory Page 3
1	1	1	1	1	Memory Page 32

Figure 7.2.1: Memory Page Selection

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8: Card Information

This Sections in this chapter describes firmware operation for the DIO4-cPCI-CC card.

- Firmware Information
- Control/Status Register
- Starting the DIO4-cPCI-CC Firmware
- Downloading the Firmware File
- Interrupt Registers
- Address Map Reference
- BIT Status Registers Definitions and BIT Test Descriptions
- Application Code Register Definitions

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8.1 Firmware Information

DSP firmware consists of two modes of operation: BIT Mode and Application Mode. See Figure 8.1.1. Following the power up cycle, the DSP initiates the bootload sequence. This sequence programs and configures both the DSP and FPGA. When the DSP finishes the bootload process, it initializes the card and performs Power-Up Tests. (Not all BIT tests are performed at this time). After the BIT tests are complete, 3Ch contains an error count (if there is an error) and the firmware remains in an idle loop waiting for the Host command. At this time, the user can perform any or all of the BIT Routine or enter the Application Mode.

Refer to Section 8.7 on page 8-15 for further explanation of each BIT Test.



Note: The firmware will write the BIT Product Code and Version Number (Offsets 38h and 39h) after the Power-Up Tests are complete.

8.1.1 Memory Map Registers

DIO4 contains 128 kWords of memory. DIO4 controls key segments of main memory containing the program pointer tables for both BIT and Application Modes of operation. See Figure 8.1.2. Each mode resides in separate areas of main memory as follows:

- Status Register resides in memory from 0h – 4Fh and 80h – FFh
- Flash Status Registers resides in memory from 50h – 7Fh
- Status and BIT mode registers resides in memory from 100h –17Fh
- Application mode registers resides in memory from 180h to FFFFh

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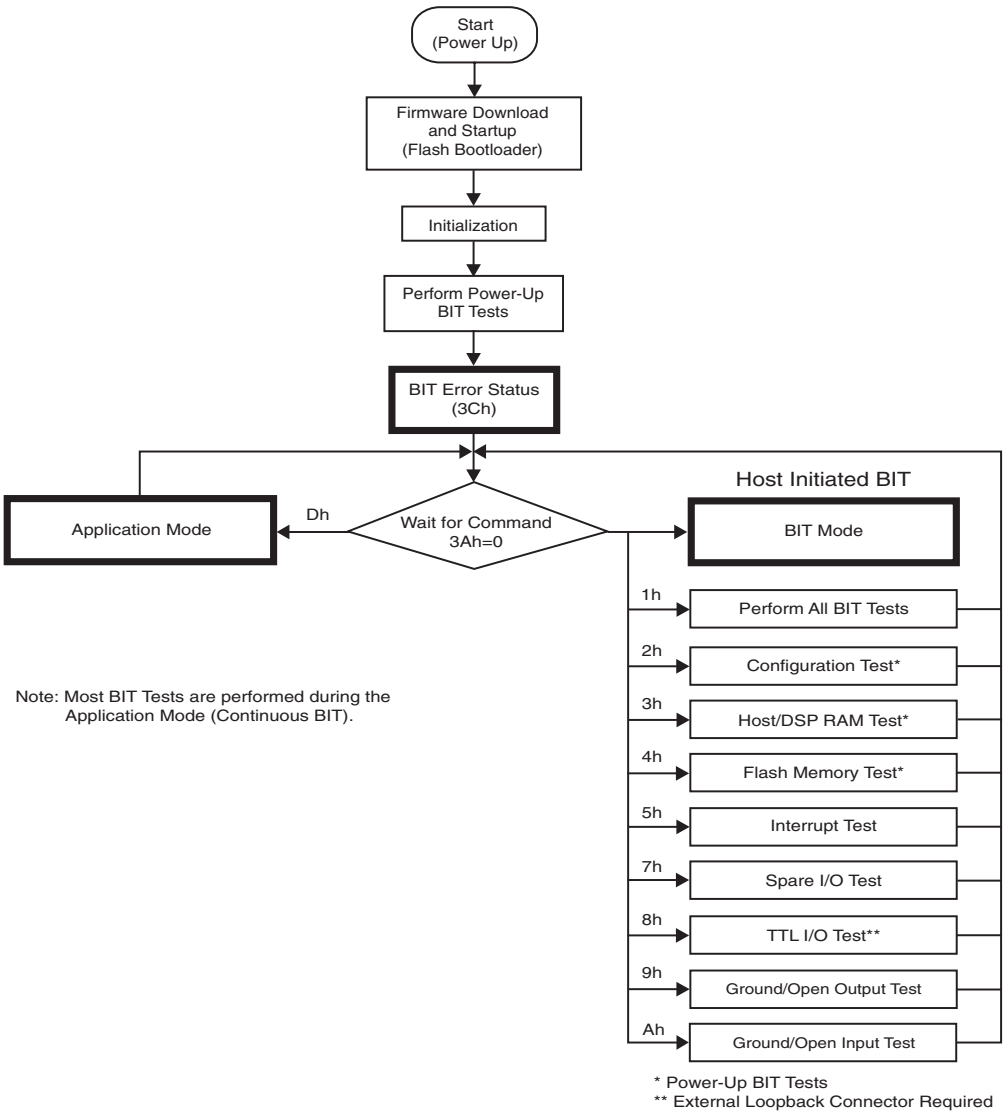


Figure 8.1.1: Top Level Firmware Flow Chart

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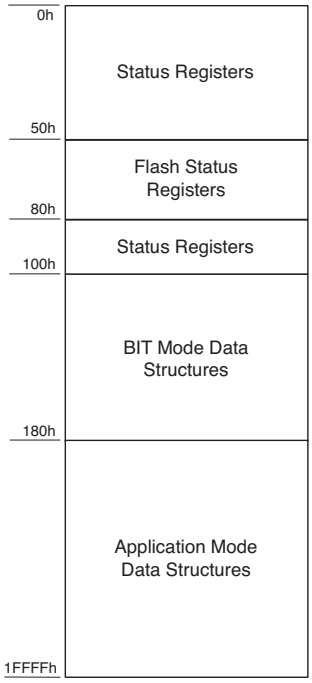


Figure 8.1.2: DIO4 Memory Map

8.1.2 Application Mode Operation

When the firmware enters the application mode, memory clears and internal data structures initialize. See Figure 8.1.3. Once the FW writes the Application Product Code (value of 3278h at offset 40h) and Version Number (value 0001h at offset 41h), it initializes the external data structures and begins I/O processing. At any time during idle processing, the Host can stop the I/O and re-enter the BIT Mode.

- Re-entering the BIT Mode after the Application Mode has started:
  - Stop I/O (write a 0 to 80h).
  - Wait for 81h to clear to be sure I/O stopped.
  - 3Ah and 3Bh clear.
  - Firmware is in the BIT mode waiting for command.

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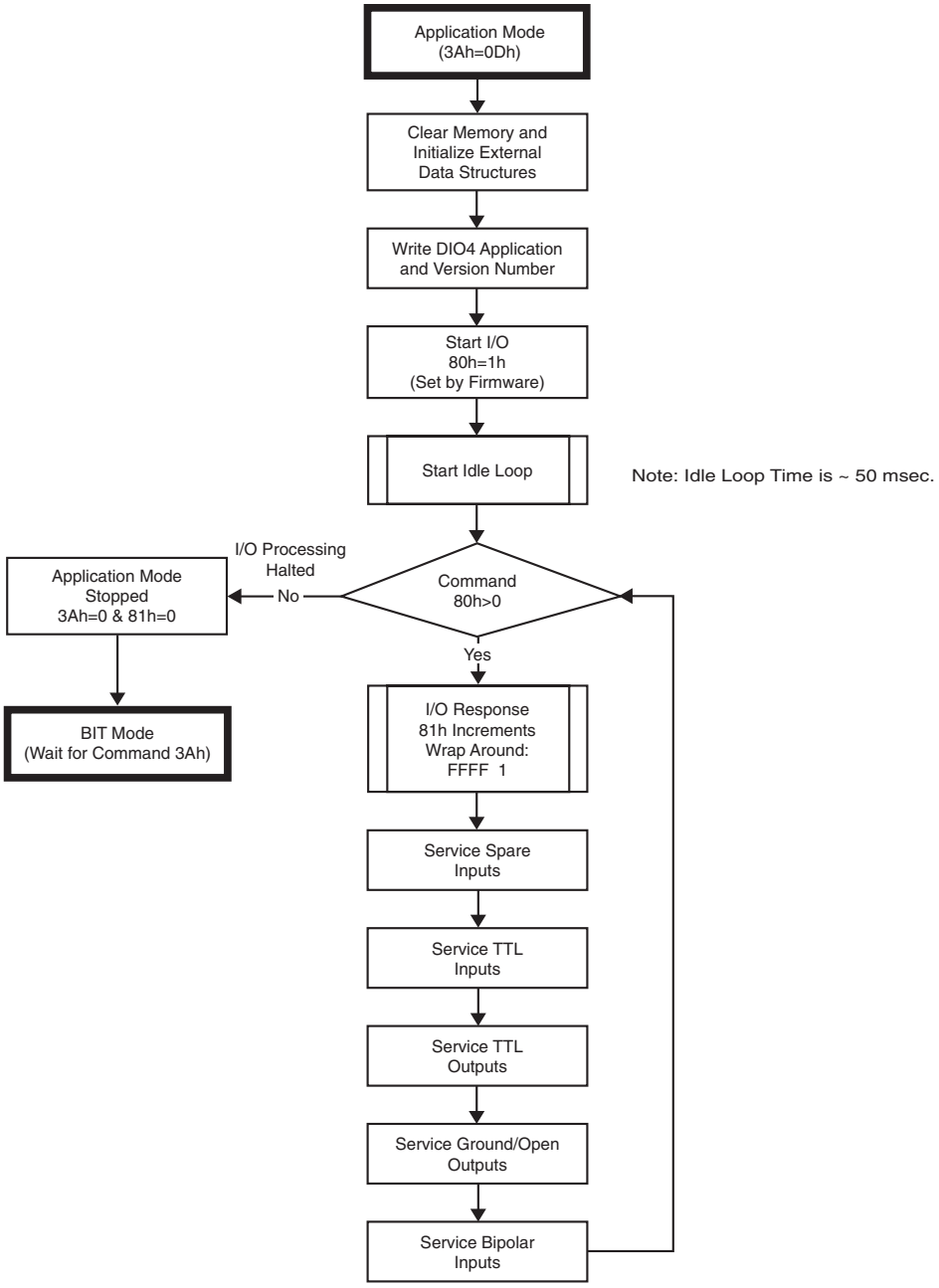


Figure 8.1.3: Application Mode Firmware Flow Chart

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8.2 Control/Status Register

Control/Status Register (CSR) is a key register for proper initialization and operation of the DIO4-cPCI. Only the Host computer can access the CSR. Table 8.2.1 describes the bits in the Control/Status Register of the DIO4-cPCI card. These registers provide the following module functions to the host:

- ➢ Module reset and operation control
- ➢ PCI interrupt control

Table 8.2.1: Device 1 CSR Definition (40000h Wd)

Bit	Function	Description
D0	DSP Reset	0=DSP (Firmware) Run 1=DSP (Firmware) Reset
D1	Flash/RAM	0=RAM 1=Flash
D2	Master interrupt to generate interrupt	0=Blocked 1=Enabled
D3	DSP Interrupt Enable to generate interrupt	0=Blocked 1=Enabled
D4	Altera Reload	0=No Reload 1=Reload
D5	Reserved	-
D6	Clear Master Interrupt (WO)	0=N/A 1=Clear
	Master Interrupt Status (RO)	0=No Interrupt 1=Interrupt Pending
D7	Clear DSP Interrupt(W0)	0=N/A 1=Clear
	DSP Interrupt Status	0=No Interrupt 1=Interrupt Pending
D8-D15	Reserved	-

(RO) = Read Only
(W0) = Write Only

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8.3 Starting the DIO4-cPCI-CC Firmware

To start the firmware, follow the procedure below.

1. Write a value of `1h` to the CSR

   This resets the DSP.

2. Write a value of `0h` to the CSR

   This starts the DSP and downloads the DSP section of the firmware from flash.

3. Read offset 3Bh and wait for the value to equal `0h`.

   This indicates the power-up tests are complete.

4. Read offset 3Ch. Contact SBS Technologies if a nonzero value is detected.

   A nonzero value indicates errors were detected during power up.

5. The firmware is initialized and waiting for a BIT control register (Offset 3Ah) command.

6. To start the application code, write a `0Dh` to the BIT control register.

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8.4 Downloading the Firmware File

DIO4-cPCI-CC uses flash memory to store the firmware code. Prior to shipping the board, SBS loads the latest firmware into flash. Normally, the firmware loads automatically when power is applied to the board.

- SBS provides a download file that contains the firmware code.
- Download file data structure contains 16-bit words. The first sixteen words makeup the file header, containing product and version information.

If you need to load new firmware into flash memory, follow the procedure below.

1. Write a value of 00003h to the CSR.

   This resets the DSP and selects host flash access.

2. Read the first 16 words from the firmware file. The first 16 words are header information and can be skipped.

3. Read the next 2 words from the firmware file, convert the two 16-bit words to a 32-bit word count (N). The first word is the 16 MSBs and the second word is the 16 LSBs. The 32-bit word count are the number of words (N) in the DSP section of the firmware file.

4. Read the next N number of words from the firmware file AND write each word to flash starting at offset 00000h. This is the DSP portion of the firmware file. Each sector in flash is 8000h words long and sector 0 must be cleared before the DSP portion of the firmware file can be written.

5. Read the next 2 words from the firmware file, convert the two 16-bit words to a 32-bit word count (M). The first word is the 16 MSBs and the second word is the 16 LSBs. The 32-bit word count are the number of words (M) in the Altera section of the firmware file.

6. Read the next M number of words from the firmware file writing each word to flash starting at offset 08000h. This is the Altera portion of the firmware file. Each sector in flash is 8000h words long and must be cleared before the Altera portion of the firmware can be file written.

7. Power off the computer and restart it.

   The new Altera will be loaded when the computer is powered up.

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8.5 Interrupt Registers

DIO4 uses interrupts to notify the host processor that input and monitoring events have occurred.

DIO4 utilizes a doubled buffered queue structure to store detected or generated events for the host system interrupt service routines. Control registers manage the queue addresses and event counters for this data structure. Host system reads these control registers during an interrupt service procedure to determine which interrupt queue is currently active and how many interrupt events are stored in the active queue. Host system may handle interrupt events in one of two ways:

- By polling the interrupt control registers with host software with the hardware interrupts disabled
- By using an Interrupt Service Routine (ISR) written for the specific device with the hardware interrupts enabled

DIO4 fills the interrupt queues and updates interrupt control register regardless of which method is used. If the host system does not require hardware interrupts, the interrupt enable bit in the CSR is set to "0" at startup. Interrupt queue data structures and control registers allow the host system to easily determine what type of event occurred.

Table 8.5.1 describes the various DIO4 interrupt conditions. The "Code" column lists the numbers assigned to each interrupt condition. Each entry in an interrupt queue consists of four words with the first word representing the code type. Host system uses this code to determine how to handle each interrupt.

Table 8.5.1: Interrupt Types

Type	Code (HEX)	Description
Error Detected	1	This interrupt occurs when an error is detected and bit 1 of INTCTRL (1E2h) is set.
Interrupt Overflow	2	This interrupt indicates that the interrupt queue has overflowed. The host system neglected to service the first interrupt of the queue before the entire queue filled with data. This interrupt type is enabled by setting bit 2 of INTCTRL (1E2h)
Spare Input Detected	3	This interrupt occurs when an SPARE input has changed for at least one of the channels of interest. This interrupt type is enabled by setting SPAREIE register (190h). The second word of the interrupt structure will have corresponding bits set to 1 for enabled channels that were changed.

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Type	Code (HEX)	Description
TTL Input Detected	4	This interrupt occurs when an TTL input has changed for at least one of the channels of interest. This interrupt type is enabled by setting TTLIE register (195h). The second word of the interrupt structure will have corresponding bits set to 1 for the enabled channels that were changed.
Ground/Open Fault Threshold Reached	5	If an over current condition occurs, the firmware tries resetting outputs for as many as times as specified in the GODTHRESHOLD (19Dh) register. When that number is reached, an interrupt to the host is generated and all processing is stopped. If the value in the GODTHRESHOLD (19Dh) register is 0, the processing never stops and the interrupt is never generated.
Bipolar Input Detected	6	This interrupt occurs when an Bipolar input has changed for at least one of the channels of interest. This interrupt type is enabled by setting BGOIE16 and BGOIE24 registers (offsets 1B1h and 1B2h). The second and third word of the interrupt structure will have corresponding bits set to 1 for enabled channels that were changed. The second word will contain information for channels 0-15 and third word for channels 16-23.

8.5.1 Interrupt Queue Data Structures and Control Registers

DIO4 manages interrupts using double buffered queues and counter control registers. When an interrupt event occurs, the DIO4 stores four words in the current interrupt queue. These four words consist of an interrupt code and three information words. The host reads these words to determine what type of interrupt occurred and to obtain related information. Figure 8.5.1 show the Interrupt queues and control registers.

The firmware defines where the interrupt resides in memory.

- 1EBh – (IQRSP) Interrupt Queue Response Flag Word
- 1ECh – (IQPTR1) Interrupt Queue Pointer 1 (Firmware set to A00h)
- 1EDh – (IQPTR2) Interrupt Queue Pointer 2 (Firmware set to B00h)
- 1EEh – (IQCNT1) Interrupt Queue Count 1
- 1EFh – (IQCNT2) Interrupt Queue Count 2
- 1F0h – (IQNUM) Interrupt Queue Max Number (Firmware set to 4)

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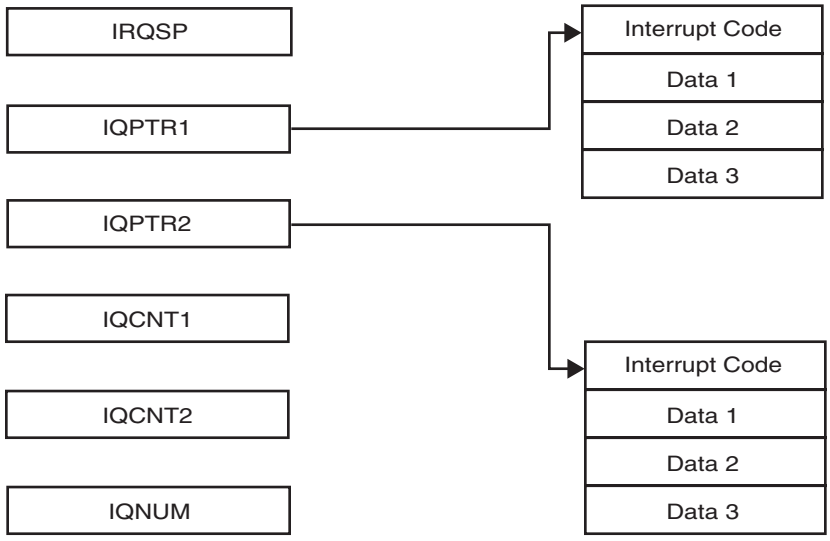


Figure 8.5.1: Interrupt Queues and Control Registers

When an interrupt event occurs, the firmware sets the interrupt pending bit of the CSR control register (bit 7). If bit 3 of the CSR is set to 1, the DIO4 generates a hardware interrupt. The host ISR writes the value FFFFh to IQRSP when starting the service routine and writes 0001h to IQRSP when the routine is complete. Control register IQCNT1 and IQCNT2 provide an event count for each buffer (there are four words per event).

After startup, the firmware writes interrupt events to the queue indicated by IQPTR1. When an interrupt occurs, the host ISR sets IQRSP to FFFFh. The host must then wait two microseconds for the firmware to finish processing any partially completed asynchronous interrupt events. If there is a partial interrupt pending, the firmware finishes processing, places the event information in the queue indicated by IQPTR1, and increments IQCNT1. If a new interrupt occurs during the host service (after FFFFh is written to IQRSP), the new interrupt event information goes in the queue indicated by IQPTR2. After servicing the interrupts, the host ISR writes a 1 to IQRSP and the firmware swaps the values from IQPTR2 to IQPTR1 and from IQCNT2 to IQCNT1. If an interrupt event was placed in IQPTR2, the firmware generates a new hardware interrupt.



Note: If the host has programmed the DIO4 for interrupt events that are known to be synchronous, and these events occur more than 10 microseconds apart, the host ISR does not need to wait two microseconds before servicing the interrupts.

When the host services an interrupt, it reads the code word from the interrupt entry to determine the interrupt type.

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Hardware Interrupt Service Routine

1. Host receives hardware interrupt and starts ISR.
2. Host ISR reads IQRSP in a loop until IQRSP is equal to `0`.
3. Host ISR writes `FFFFh` to IQRSP.
4. Host ISR waits 2 microseconds for the firmware to complete any partial interrupts.
5. Host ISR reads IQCNT1 to determine the number of interrupt events to process.
6. Host ISR reads IQPTR1 to get the address of the interrupt queue to process.
7. The host reads each interrupt event, beginning at the address indicated by IQPTR1. The host reads each interrupt event in the queue, deciphering the code word to determine if data words are present. The host ISR may either process the interrupt data at this point or after execution has returned to the host software.
8. Clear the pending interrupt bit.
9. Host ISR writes `0001h` to IQRSP, and the IQPTRs and IQCNTs swap.

Software Polling Interrupt Service Routine

1. Host polls (reads) bit 7 of the host CSR until it detects a value of `1`. A `1` indicates an interrupt event occurred on the board.
2. Host ISR reads IQRSP in a loop until IQRSP is equal to `0`.
3. Host ISR writes `FFFFh` to IQRSP.
4. Host ISR waits 2 microseconds for the firmware to complete any partial interrupts.
5. Host ISR reads IQCNT1 to determine the number of interrupt events to process.
6. Host ISR reads IQPTR1 to get the address of the interrupt queue to process.
7. The host reads each interrupt event, beginning at the address indicated by IQPTR1. The host reads each interrupt event in the queue, deciphering the code word to determine if data words are present. The host ISR may either process the interrupt data at this point or after execution has returned to the host software.
8. Host ISR writes a `1` to bit 7 of the Host CSR control register to clear the interrupt request.
9. Host ISR writes `0001h` to IQRSP, and the IQPTRs and IQCNTs swap.

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8.6 Address Map Reference

This section describes the DIO4 Address Map in detail. See Table 8.6.1.

Table 8.6.1: DIO4 Address Map

Offset	Command	Description
0-37h	–	Reserved
		Board Status Registers
38h		BIT Product Code
39h		BIT Version Number
3Ah		BIT Control Word
	0	Wait for command
	1	BIT Select Test
	2	Configuration Test
	3	RAM Test
	4	Flash Test
	5	Interrupt Test
	7	Spare I/O Test
	8	TTL I/O Test
	9	Ground/Open Discrete Test
	A	Bipolar Input Test
3Bh		BIT Status Word
	0	Wait for command
	1	BIT Select Test
	2	Configuration Test
	3	RAM Test
	4	Flash Test
	5	Interrupt Test
	7	Spare I/O Test
	8	TTL I/O Test
	9	Ground/Open Discrete Test
	A	Bipolar Input Test
3Ch		BIT Total Error Count

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Offset	Command	Description
3Dh	Selected Test Word	Each bit selects the BIT test to run. Example: If bit 3 is set, BIT Test 3 will be executed once. If bits 3 and 6 are set, BIT Tests 3 and 6 will be executed. (Only applies to performing selected BIT tests - BIT 1)
3Eh	Firmware Product Code	
3Fh	Firmware Version	
40h	Application Product Code	
41h	Application Version	
Flash Configuration Registers		
50h – 7Fh	–	–
Application Code I/O Registers		
80h	I/O Command Word	
81h	I/O Response Word	
BIT Status Registers		
100h –17Fh	See Section 8.7 on page 8-15 for a detailed description.	
Application Code Registers		
180h – 1FFFh	See Section 8.8 on page 8-30 for a detailed description.	

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8.7 BIT Status Registers Definitions and BIT Test Descriptions

This section describes the BIT Status Registers in detail and breaks down each BIT test. The BIT Status Register range is from 100h to 17Fh.

8.7.1 BIT Test 1

Table 8.7.1 shows the BIT Selected Test Control Register.

Table 8.7.1: BIT Selected (BIT 1) Test Control Register

Offset	Description
3Dh	Selected Test Word

BIT Select Test

Purpose of this test is to perform selected BIT tests. To Start BIT 1 testing, set the bits of the select test register (offset 3Dh) for each test of interest.

➢ Example: If bit 3 is set, BIT Test 3 executes once (offset 3Dh = `0008h`). See Table 8.6.1. If bits 3 and 6 are set, BIT Tests 3 and 6 executes once (offset 3Dh = `0048h`). Then, write a 1 to the BIT Control Status Register (offset 3Ah). This test performs one loop of the selected BIT tests, and executes in sequential order. If there is an error with any one of these tests, the BIT total error count (offset 3Ch) increments for every error that occurs. Registers for each individual test performed show the status of these errors (refer to the register definitions for each test).

8.7.2 BIT Test 2

Table 8.7.2 shows the Configuration Test Control Registers.

Table 8.7.2: Configuration (BIT 2) Test Control Registers

Offset	Description
100h	FPGA Download Product Code
101h	FPGA Download Version Number
102h	FPGA Download Status BADDh – FPGA(s) Download Fail CODEh – FPGA(s) Download Pass

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Configuration Test

This test determines if the FPGA downloads correctly and the firmware starts successfully. To start BIT 2 testing, write a 2 to the BIT control register (offset 3Ah). See Table 8.6.1. This command initiates the test automatically and updates the offsets as shown in Table 8.7.2. If test is successful, the DSP returns a valid Product Code, Version Number, and Status for the FPGA design being loaded. If the test fails, offsets 100h through 102h contain `BADDh` in each offset.

8.7.3 BIT Test 3

Table 8.7.3 shows the Host/DSP RAM Test Control Registers.

Table 8.7.3: Host/DSP RAM (BIT 3) Test Control Registers

Offset	Command	Description
105h		RAM Test Control Word
	0	Stop
	1	Loop once and wait
	2	Loop until error
	3	Loop continuously
	4	Return to main (Return control to BIT control register)
	5	Loop once and return to main
106h		RAM Test Status Word
	0	Waiting for command
	1	Zeros test in progress
	2	Ones test in progress
	3	Counter test in progress
	4	Invalid address range
107h	RAM Test Starting Address (180h)	
108h	RAM Test Ending Address (FFFFh)	
109h	RAM Test Loop Count	
10Ah	RAM Test Error Count	
10Bh	RAM Test Error Address	
10Ch	RAM Test Good Data	
10Dh	RAM Test Error Data	
10Eh	RAM Test Error Data 2nd Read	
10Fh	Echo Read Location (Default **DEADh**)	
110h	Echo Write Location	

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Host/DSP RAM and Echo Test

This test verifies that the Host/DSP RAM is addressing and operating properly. To start BIT 3 testing, write a 3 to the BIT control register (offset 3Ah). See Table 8.6.1. This clears locations 105h to 110h. Control word (offset 105h) controls BIT 3 testing. Table 8.7.4 shows a list of valid commands with their descriptions.

Table 8.7.4: Offset 105h Valid Commands

Command	Action	Description
0	Stop	This option stops the test after it completes the current loop.
1	Loop once and wait	This option causes the test to loop one time, then wait for the next command in BIT 3.
2	Loop until error	This option causes the test to loop continuously until an error occurs.
3	Loop continuously	This option causes the test to loop continuously.
4	Return to main	Returns control to BIT control register. This option exits from BIT 3 and returns control to BIT Main.
5	Loop once and return to main	Test executes BIT 3 one time, exits from BIT 3, and returns to BIT Main.
8000	Run automatically once and return to main	Tests both upper and lower memory windows. Test executes one time with default values and returns to BIT Main.

BIT 3 tests three patterns that are written and then read from a range of memory. The three patterns are zeroes, ones, and address. Memory is tested starting at the address in offset 107h and ending at the address in offset 108h. Valid address range is from 180h to 1FFFFh in both memory windows. One loop tests both memory windows with the three patterns. If an invalid address is specified, the status word indicates an address range error (4h at offset 106h). Status word (offset 106h) indicates the state of the test. Table 8.7.5 shows a list of possible states.

Table 8.7.5: List of Possible States for Offset 106h

State	Description
0	Waiting for command
X001	Zeroes test in progress
X002	Ones test in progress
X003	Address test in progress
X004	Invalid address range
X = Memory window (1 or 2)	

If an error occurs during testing, locations 10Ah through 10Eh contain the information, with the memory window and type of test stored at 106h, as follows:

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- An error count increments at offset 10Ah for each error that occurs.
- Location 10Bh stores the last error address.
- Location 10Ch stores the last “should be” data.
- Location 10Dh stores the last “bad” data.
- Location 10Eh stores the last “bad” 2nd read data.

Locations 10Fh and 110h are Echo read and write locations. What ever is stored at the Echo read location (10Fh) echoes to the Echo write location (110h) while testing is in progress. Default echo read location is DEADh.

8.7.4 BIT Test 4

Table 8.7.6 shows the Flash Memory Test Control Registers.

Table 8.7.6: Flash Memory (BIT 4) Test Control Registers

Offset	Command	Description
115h		Flash Test Control Word
	0	Stop
	1	Loop once and wait
	2	Loop until error
	3	Loop continuously
	4	Return to main
	5	Loop once and return to main
116h		Flash Test Status Word
	0	Waiting for command
	1	Zeros test in progress
	2	Ones test in progress
	3	Address test in progress
117h	Flash Test Starting Address (38000h)	
118h	Flash Test Ending Address (3FFFFh)	
119h	Flash Test Loop Count	
11Ah	Flash Test Error Count	
11Bh	Flash Test Error Address	
11Ch	Flash Test Good Data	
11Dh	Flash Test Error Data	
11Eh	Flash Test Error Data 2nd read	

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Flash Memory Test

This test verifies that the Flash device is addressing and operating properly. To start BIT 4 testing, write a 4 to the BIT control register (offset 3Ah). See Table 8.6.1. This clears locations 115h through 11Eh. Control word (offset 115h) controls BIT 4 testing. Table 8.7.7 shows a list of valid commands with their descriptions.

Table 8.7.7: Offset 115h Valid Commands

Command	Action	Description
0	Stop	This option stops the test after it completes the current loop.
1	Loop once and wait	This option causes the test to loop one time, then wait for the next command in BIT 4.
2	Loop until error	This option causes the test to loop continuously until an error occurs.
3	Loop continuously	This option causes the test to loop continuously.
4	Return to main	Returns control to BIT control register. This option exits from BIT 4 and returns control to BIT Main.
5	Loop once and return to main	Test executes BIT 4 one time, exits from BIT 4, and returns to BIT Main.
8000	Run automatically once and return to main	Test executes one time with default values.

BIT 4 tests three patterns that are written and then read from a designated range in Flash memory. The three patterns are zeroes, ones, and address. Flash memory test starts at the address in offset 117h and ends at the address in offset 118h. Valid address range is from 38000h to 3FFFFh. Flash memory range that is tested is not changeable. Status word (offset 116h) indicates the state of the test. Table 8.7.8 shows a list of the possible states.

Table 8.7.8: List of Possible States for Offset 116h

State	Description
0	Waiting for command
1	Zeros test in progress
2	Ones test in progress
3	Address test in progress

If an error occurs during testing, locations 11Ah through 11Eh contain the information, with the type of test stored at 116h, as follows:

- An error count increments at offset 11Ah for each error that occurs
- Location 11Bh stores the last error address
- Location 11Ch stores the last “should be” data
- Location 11Dh stores the last “bad” data
- Location 11Eh stores the last “bad” 2nd read data

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8.7.5 BIT Test 5

Table 8.7.9 shows the Interrupt Test Control Registers.

Table 8.7.9: Interrupt (BIT 5) Test Control Registers

Offset	Description
120h	Interrupt Test Count
121h	Interrupt Test Time Interval (1 µs resolution, default - 1000 µs)
122h	Interrupt Error Count
123h	Interrupt Type Control

Interrupt Test

To start BIT 5 testing, write a 5 to the BIT control register (offset 3Ah). See Table 8.6.1. This clears locations 120h through 123h. First, enter the Interrupt Interval; this is the time between each interval (default is 1000 µs). Second, enter the Interrupt Count; this is the total number of interrupts to be generated. Once this value is entered, the test starts. With each loop through the test, the interrupt count decrements until finished.

- If bit 1 of the Interrupt Type Control Word (123h) is not set (default), the firmware generates an interrupt to the host, checks interrupt pending in the HCSR, then clears the interrupt (1 loop).
- If bit 1 is set in the Interrupt Type Control Word register, the firmware generates an interrupt in the specified time. Firmware does not check or clear the pending bit in the host CSR. If an error occurs, the total bit error count (122h) increments.

8.7.6 BIT Test 7

Table 8.7.10 shows the Spare I/O Test Control Registers. A Loopback w/External Circuitry is required for proper operation.

Table 8.7.10: Spare I/O (BIT 7) Test Control Registers

Offset	Command	Description
140h		Spare I/O Test Control Word
	0	Wait for control word
	1	Loop once and wait
	2	Loop until error
	3	Loop continuously
	4	Return to main
	5	Loop once and return to main
141h	Loop Count	
142h	Error Count	
143h	Spare Output Control/Input Status Register - See Table 8.7.11 for bit positions.	

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Table 8.7.11: Spare Output Control/Input Status Register (Offset 143h)

Bit	Description
0	Spare Output 0 Control
1	Spare Output 1 Control
2	Spare Output 2 Control
3	Spare Output 3 Control
4	Spare Output 4 Control
5	Spare Output 5 Control
6	Spare Output 6 Control
7	Spare Output 7 Control
8	Spare Input 0 Status
9	Spare Input 1 Status
10	Spare Input 2 Status
11	Spare Input 3 Status
12	Spare Input 4 Status
13	Spare Input 5 Status
14	Spare Input 6 Status
15	Spare Input 7 Status

Spare I/O Test

This test verifies that the Spare Inputs and Outputs are working correctly (8 inputs and 8 outputs). It requires a loopback for proper operation. Connect the loopback from the outputs to the corresponding inputs. To start BIT 7 testing, write a 7 to the BIT control register (offset 3Ah). See Table 8.6.1. Control word (offset 140h) controls BIT 7 testing. Table 8.7.12 shows a list of valid commands with their descriptions.

Table 8.7.12: Offset 140h Valid Commands

Command	Action	Description
0	Wait for control word	This option stops the test after it completes the current loop, then waits for the next control word.
1	Loop once and wait	This option causes the test to loop one time, then wait for the next command in BIT 7.
2	Loop until error	This option causes the test to loop continuously until an error occurs.
3	Loop continuously	This option causes the test to loop continuously.
4	Return to main	Returns control to BIT control register. This option exits from BIT 7 and returns control to BIT Main.
5	Loop once and return to main	Test executes one time and then exits from BIT 7 and returns to BIT Main.
8000	Run automatically once and return to main	Test executes one time with default values.

This test verifies that the inputs are set for the corresponding outputs selected in offset 143h. If an error occurs, the error count increments (offset 142h).

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8.7.7 BIT Test 8

Table 8.7.13 shows the TTL I/O Test Control Registers. A Loopback w/External Circuitry is required for proper operation.

Table 8.7.13: TTL I/O (BIT 8) Test Control Registers

Offset	Command	Description
150h		TTL I/O Test Control Word
	0	Wait for control word
	1	Loop once and wait
	2	Loop until error
	3	Loop continuously
	4	Return to main
	5	Loop once and return to main
151h	Loop Count	
152h	Error Count	
153h	TTL Output Control Register - See Table 8.7.14 for bit positions.	
154h	TTL Input Status Register - See Table 8.7.15 for bit positions.	

Table 8.7.14: TTL Output Control Register (Offset 153h)

Bit	Description
0	TTL Output 0 Control
1	TTL Output 1 Control
2	TTL Output 2 Control
3	TTL Output 3 Control
4	TTL Output 4 Control
5	TTL Output 5 Control
6	TTL Output 6 Control
7	TTL Output 7 Control
8	TTL Output 8 Control
9	TTL Output 9 Control
10	TTL Output 10 Control
11	TTL Output 11 Control
12	TTL Output 12 Control
13	TTL Output 13 Control
14	TTL Output 14 Control
15	TTL Output 15 Control

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Table 8.7.15: TTL Input Status Register (Offset 154h)

Bit	Description
0	TTL Input 0 Status
1	TTL Input 1 Status
2	TTL Input 2 Status
3	TTL Input 3 Status
4	TTL Input 4 Status
5	TTL Input 5 Status
6	TTL Input 6 Status
7	TTL Input 7 Status
8	TTL Input 8 Status
9	TTL Input 9 Status
10	TTL Input 10 Status
11	TTL Input 11 Status
12	TTL Input 12 Status
13	TTL Input 13 Status
14	TTL Input 14 Status
15	TTL Input 15 Status

TTL I/O Test

This test verifies that the TTL Inputs and Outputs are working correctly (16 inputs and 16 outputs). It requires a external loopback for proper operation. Connect the loopback from the outputs to the corresponding inputs. To start BIT 8 testing, write an 8 to the BIT control register (offset 3Ah). See Table 8.6.1. Control word (offset 150h) controls BIT 8 testing. Table 8.7.16 shows a list of valid commands with their descriptions.

Table 8.7.16: Offset 145h Valid Commands

Command	Action	Description
0	Wait for control word	This option stops the test after it completes the current loop, then waits for the next control word.
1	Loop once and wait	This option causes the test to loop one time, then wait for the next command in BIT 8.
2	Loop until error	This option causes the test to loop continuously until an error occurs.
3	Loop continuously	This option causes the test to loop continuously.
4	Return to main	Returns control to BIT control register. This option exits from BIT 8 and returns control to BIT Main.
5	Loop once and return to main	Test executes one time and then exits from BIT 8 then returns to BIT Main.

This test verifies that the inputs are set for the corresponding outputs selected in offset 153h. If an error occurs, the error count increments (offset 152h - Table 8.7.13). Inputs are written to offset 154h.

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8.7.8 BIT Test 9

Table 8.7.17 shows the Ground/Open Discrete Output Test Control Registers. A Loopback is required for proper operation.

Table 8.7.17: Ground/Open Discrete Output I/O (BIT 9) Test Control Registers

Offset	Command	Description
160h		Ground/Open Discrete Output Test Control Word
	0	Wait for control word
	1	Loop once and wait
	2	Loop until error
	3	Loop continuously
	4	Return to main
	5	Loop once and return to main
161h	Ground/Open Discrete Loop Count	
162h	Ground/Open Discrete Error Count	
163h	Ground/Open Discrete Output Data Register - See Table 8.7.18 for bit positions.	
164h	Ground/Open Discrete Feedback Register - See Table 8.7.19 for bit positions.	
165h	Ground/Open Discrete Over Current Register - See Table 8.7.20 for bit positions.	

Table 8.7.18: Ground/Open Discrete Output Data Register (Offset 163h)

Bit	Description
0	Ground/Open Discrete Output 0 Control
1	Ground/Open Discrete Output 1 Control
2	Ground/Open Discrete Output 2 Control
3	Ground/Open Discrete Output 3 Control
4	Ground/Open Discrete Output 4 Control
5	Ground/Open Discrete Output 5 Control
6	Ground/Open Discrete Output 6 Control
7	Ground/Open Discrete Output 7 Control
8	Ground/Open Discrete Output 8 Control
9	Ground/Open Discrete Output 9 Control
10	Ground/Open Discrete Output 10 Control
11	Ground/Open Discrete Output 11 Control
12	Ground/Open Discrete Output 12 Control
13	Ground/Open Discrete Output 13 Control
14	Ground/Open Discrete Output 14 Control
15	Ground/Open Discrete Output 15 Control

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Table 8.7.19: Ground/Open Discrete Feedback Register (Offset 164h)

Bit	Description
0	Ground/Open Discrete Feedback 0
1	Ground/Open Discrete Feedback 1
2	Ground/Open Discrete Feedback 2
3	Ground/Open Discrete Feedback 3
4	Ground/Open Discrete Feedback 4
5	Ground/Open Discrete Feedback 5
6	Ground/Open Discrete Feedback 6
7	Ground/Open Discrete Feedback 7
8	Ground/Open Discrete Feedback 8
9	Ground/Open Discrete Feedback 9
10	Ground/Open Discrete Feedback 10
11	Ground/Open Discrete Feedback 11
12	Ground/Open Discrete Feedback 12
13	Ground/Open Discrete Feedback 13
14	Ground/Open Discrete Feedback 14
15	Ground/Open Discrete Feedback 15

Table 8.7.20: Ground/Open Discrete Over Current Register (Offset 165h)

Bit	Description
0	Ground/Open Discrete Over Current 0
1	Ground/Open Discrete Over Current 1
2	Ground/Open Discrete Over Current 2
3	Ground/Open Discrete Over Current 3
4	Ground/Open Discrete Over Current 4
5	Ground/Open Discrete Over Current 5
6	Ground/Open Discrete Over Current 6
7	Ground/Open Discrete Over Current 7
8	Ground/Open Discrete Over Current 8
9	Ground/Open Discrete Over Current 9
10	Ground/Open Discrete Over Current 10
11	Ground/Open Discrete Over Current 11
12	Ground/Open Discrete Over Current 12
13	Ground/Open Discrete Over Current 13
14	Ground/Open Discrete Over Current 14
15	Ground/Open Discrete Over Current 15

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Ground/Open Discrete Output Test

This test verifies that the Ground/Open Discrete Outputs are working correctly. To start BIT 9 testing, write a 9 to the BIT control register (offset 3Ah). See Table 8.6.1. This clears locations 160h through 165h. Control word (offset 160h) controls BIT 9 testing. Table 8.7.21 shows a list of valid commands with their descriptions.

Table 8.7.21: Offset 160h Valid Commands

Command	Action	Description
0	Wait for control word	This option stops the test after it completes the current loop, then waits for the next control word.
1	Loop once and wait	This option causes the test to loop one time, then wait for the next command in BIT 9.
2	Loop until error	This option causes the test to loop continuously until an error occurs.
3	Loop continuously	This option causes the test to loop continuously.
4	Return to main	Returns control to BIT control register. This option exits from BIT 9 and returns control to BIT Main.
5	Loop once and return to main	Test executes one time and then exits from BIT 9 then returns to BIT Main.
8000	Run automatically once and return to main	Test executes one time with default values.

This test verifies the Ground/Open Discrete Output operation. To run this test, set data registers first and proceed as follows:

- ➢ Set the value in control register to select the appropriate test
- ➢ Read register 164h to obtain latched data
- ➢ Read register 165h to obtain over current information

If an error occurs, the error count increments (offset 162h - Table 8.7.17).

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8.7.9 BIT Test A

Table 8.7.22 shows the Bipolar Ground/Open Input Test Control Registers.

Table 8.7.22: Bipolar Ground/Open Input (BIT A) Test Control Registers

Offset	Command	Description
170h		Bipolar Ground/Open Input Test Control Word
	0	Wait for control word
	1	Loop once and wait
	2	Loop until error
	3	Loop continuously
	4	Return to main
	5	Loop once and return to main
171h	Loop Count	
172h	Bipolar Ground/Open Polarity for Inputs 0-15 Register - See Table 8.7.18 for bit positions.	
173h	Bipolar Ground/Open Polarity for Inputs 16-23 Register - See Table 8.7.18 for bit positions.	
174h	Bipolar Ground/Open Input Data for Inputs 0-15 Register - See Table 8.7.18 for bit positions.	
175h	Bipolar Ground/Open Input Data for Inputs 16-23 Register - See Table 8.7.18 for bit positions.	

Table 8.7.23: Bipolar Ground/Open Polarity for Inputs 0-15 Register (Offset 172h)

Bit	Description
0	Bipolar Ground/Open Polarity 0
1	Bipolar Ground/Open Polarity 1
2	Bipolar Ground/Open Polarity 2
3	Bipolar Ground/Open Polarity 3
4	Bipolar Ground/Open Polarity 4
5	Bipolar Ground/Open Polarity 5
6	Bipolar Ground/Open Polarity 6
7	Bipolar Ground/Open Polarity 7
8	Bipolar Ground/Open Polarity 8
9	Bipolar Ground/Open Polarity 9
10	Bipolar Ground/Open Polarity 10

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Bit	Description
11	Bipolar Ground/Open Polarity 11
12	Bipolar Ground/Open Polarity 12
13	Bipolar Ground/Open Polarity 13
14	Bipolar Ground/Open Polarity 14
15	Bipolar Ground/Open Polarity 15

Table 8.7.24: Bipolar Ground/Open Polarity for Inputs 16-23 Register (Offset 173h)

Bit	Description
0	Bipolar Ground/Open Polarity 16
1	Bipolar Ground/Open Polarity 17
2	Bipolar Ground/Open Polarity 18
3	Bipolar Ground/Open Polarity 19
4	Bipolar Ground/Open Polarity 20
5	Bipolar Ground/Open Polarity 21
6	Bipolar Ground/Open Polarity 22
7	Bipolar Ground/Open Polarity 23
8-15	Unused

Table 8.7.25: Bipolar Ground/Open Input Data for Inputs 0-15 Register (Offset 174h)

Bit	Description
0	Bipolar Ground/Open Input Data 0
1	Bipolar Ground/Open Input Data 1
2	Bipolar Ground/Open Input Data 2
3	Bipolar Ground/Open Input Data 3
4	Bipolar Ground/Open Input Data 4
5	Bipolar Ground/Open Input Data 5
6	Bipolar Ground/Open Input Data 6
7	Bipolar Ground/Open Input Data 7
8	Bipolar Ground/Open Input Data 8
9	Bipolar Ground/Open Input Data 9
10	Bipolar Ground/Open Input Data 10
11	Bipolar Ground/Open Input Data 11
12	Bipolar Ground/Open Input Data 12
13	Bipolar Ground/Open Input Data 13
14	Bipolar Ground/Open Input Data 14
15	Bipolar Ground/Open Input Data 15

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Table 8.7.26: Bipolar Ground/Open Input Data for Inputs 16-23 Register (Offset 175h)

Bit	Description
0	Bipolar Ground/Open Input Data 16
1	Bipolar Ground/Open Input Data 17
2	Bipolar Ground/Open Input Data 18
3	Bipolar Ground/Open Input Data 19
4	Bipolar Ground/Open Input Data 20
5	Bipolar Ground/Open Input Data 21
6	Bipolar Ground/Open Input Data 22
7	Bipolar Ground/Open Input Data 23
8-15	Unused

Bipolar Ground/ Open Input Test

This test verifies that the Bipolar Ground/Open Inputs working correctly. To start BIT A testing, write a A to the BIT control register (offset 3Ah). See Table 8.6.1. This clears locations 170h through 175h. Control word (offset 170h) controls BIT A testing. Table 8.7.27 shows a list of valid commands with their descriptions.

Table 8.7.27: Offset 160h Valid Commands

Command	Action	Description
0	Wait for control word	This option stops the test after it completes the current loop, then waits for the next control word.
1	Loop once and wait	This option causes the test to loop one time, then wait for the next command in BIT A.
2	Loop until error	This option causes the test to loop continuously until an error occurs.
3	Loop continuously	This option causes the test to loop continuously.
4	Return to main	Returns control to BIT control register. This option exits from BIT A and returns control to BIT Main.
5	Loop once and return to main	Test executes one time, exits from BIT A, and then returns to BIT Main.
8000	Run automatically once and return to main	Test executes one time with default values.

This test verifies the Bipolar Inputs operation. To run this test, set data registers first and proceed as follows:

- ➢ Set the value in control register to select the appropriate test.
- ➢ Set the polarity in registers 172h and 173h.
- ➢ Read input data at registers 174h and 175h.

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8.8 Application Code Register Definitions

This section describes the Application Code Registers in detail and breaks down each register. Application Code Registers reside in memory from 180h to 1FFFh.

8.8.1 Spare Input/Output Registers

Table 8.8.1 shows the Spare Input/Output Registers.

Table 8.8.1: Spare I/O Registers

Offset	Description
190h	Spare Input Interrupt Register (SPAREIE)
191h	Spare Inputs Data Register (SPAREIND)
192h	Spare Outputs Control Register (SPAREOC)
193h	Spare Output Control Data Register (SPAREOD)

Spare Input Interrupt Register

Spare Input Interrupt Register (SPAREIE) at offset 190h enables an interrupt to be generated for detection of each input in offset 191h. Table 8.8.2 shows the bit positions for offset 190h.

Table 8.8.2: Spare Input Interrupt Register (Offset 190h)

Bit	Description
0	Detection Interrupt Enable Input 0 (0 = Disable, 1 = Enable)
1	Detection Interrupt Enable Input 1 (0 = Disable, 1 = Enable)
2	Detection Interrupt Enable Input 2 (0 = Disable, 1 = Enable)
3	Detection Interrupt Enable Input 3 (0 = Disable, 1 = Enable)
4	Detection Interrupt Enable Input 4 (0 = Disable, 1 = Enable)
5	Detection Interrupt Enable Input 5 (0 = Disable, 1 = Enable)
6	Detection Interrupt Enable Input 6 (0 = Disable, 1 = Enable)
7	Detection Interrupt Enable Input 7 (0 = Disable, 1 = Enable)
8-15	Unused

Detection of a valid input generates an interrupt (Hardware/Software). SPAREIE sets for the SPARE Input of interest. A valid signal is any transition from 1 to 0 or 0 to 1.

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Spare Inputs Data Register

Spare Inputs Data Register (SPAREIND) at offset 191h provides the host with the Spare Inputs Data. Firmware updates this register continuously. Table 8.8.3 shows the bit positions for offset 191h.

Table 8.8.3: Spare Inputs Data Register (Offset 191h)

Bit	Description
0	Spare Input Data 0
1	Spare Input Data 1
2	Spare Input Data 2
3	Spare Input Data 3
4	Spare Input Data 4
5	Spare Input Data 5
6	Spare Input Data 6
7	Spare Input Data 7
8-15	Unused

Spare Outputs Control Register

Spare Outputs Control Register (SPAREOC) at offset 192h controls Spare Output Operations. Table 8.8.4 shows the bit positions for offset 192h.

Table 8.8.4: Spare Outputs Control Register (Offset 192h)

Bit	Description
0	Enable Outputs = 1
1-15	Unused

Spare Output Control Data Register

Spare Output Control Data Register (SPAREOD) at offset 193h configures the output data and provides the latched readback data. Table 8.8.5 shows the bit positions for offset 193h.

Table 8.8.5: Spare Output Control Data Register (Offset 193h)

Bit	Description
0	Channel 0 Output Control
1	Channel 1 Output Control
2	Channel 2 Output Control
3	Channel 3 Output Control
4	Channel 4 Output Control
5	Channel 5 Output Control
6	Channel 6 Output Control
7	Channel 7 Output Control
8-15	Unused

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To set Spare Outputs, do the following:

- ➢ Set the state of the outputs which are controlled by SPAREOD (offset 193h).
- ➢ Set bit 0 of SPAREOC (offset 192h).

When firmware sets the Spare Outputs, bit 0 of SPAREOC (offset 192h) clears.

8.8.2 TTL Input/Output Registers

Table 8.8.6 shows the TTL Input/Output Registers.

Table 8.8.6: TTL Input/Output Registers

Offset	Description
195h	TTL Inputs Interrupt Enable Register (TTLIE)
196h	TTL Inputs Data Register (TTLIND)
197h	TTL Outputs Control Register (TTLOC)
198h	TTL Output Control Data Register (TTLOD)
199h	TTL Feedback Register (TTLOF)

TTL Inputs Interrupt Enable Register

TTL Inputs Interrupt Enable Register (TTLIE) at offset 195h enables an interrupt to be generated for detection of each input in offset 196h. Detection of a valid input generates an interrupt (Hardware/Software). TTLIE sets for the TTL Input of interest. A valid signal is any transition from 1 to 0 or 0 to 1. Table 8.8.6 shows the bit positions for offset 195h.

Table 8.8.7: TTL Inputs Interrupt Enable Register (Offset 195h)

Bit	Description
0	Detection Interrupt Enable Input 0 (0 = Disable, 1= Enable)
1	Detection Interrupt Enable Input 1 (0 = Disable, 1= Enable)
2	Detection Interrupt Enable Input 2 (0 = Disable, 1= Enable)
3	Detection Interrupt Enable Input 3 (0 = Disable, 1= Enable)
4	Detection Interrupt Enable Input 4 (0 = Disable, 1= Enable)
5	Detection Interrupt Enable Input 5 (0 = Disable, 1= Enable)
6	Detection Interrupt Enable Input 6 (0 = Disable, 1= Enable)
7	Detection Interrupt Enable Input 7 (0 = Disable, 1= Enable)
8	Detection Interrupt Enable Input 8 (0 = Disable, 1= Enable)
9	Detection Interrupt Enable Input 9 (0 = Disable, 1= Enable)

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Bit	Description
10	Detection Interrupt Enable Input 10 (0 = Disable, 1= Enable)
11	Detection Interrupt Enable Input 11 (0 = Disable, 1= Enable)
12	Detection Interrupt Enable Input 12 (0 = Disable, 1= Enable)
13	Detection Interrupt Enable Input 13 (0 = Disable, 1= Enable)
14	Detection Interrupt Enable Input 14 (0 = Disable, 1= Enable)
15	Detection Interrupt Enable Input 15 (0 = Disable, 1= Enable)

TTL Inputs Data Register

TTL Inputs Data Register (TTLIND) at offset 196h provides the host with the TTL Inputs Data. Firmware updates this register continuously. Table 8.8.8 shows the bit positions for offset 196h.

Table 8.8.8: TTL Inputs Data Register (Offset 196h)

Bit	Description
0	TTL Input Data 0
1	TTL Input Data 1
2	TTL Input Data 2
3	TTL Input Data 3
4	TTL Input Data 4
5	TTL Input Data 5
6	TTL Input Data 6
7	TTL Input Data 7
8	TTL Input Data 8
9	TTL Input Data 9
10	TTL Input Data 10
11	TTL Input Data 11
12	TTL Input Data 12
13	TTL Input Data 13
14	TTL Input Data 14
15	TTL Input Data 15

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TTL Outputs Control Register

TTL Outputs Control Register (TTLOC) at offset 197h controls TTL Output operations. Table 8.8.9 shows the bit positions for offset 197h.

Table 8.8.9: TTL Outputs Control Register (Offset 197h)

Bit	Description
0	Enable Outputs = 1
1 - 15	Unused

TTL Output Control Data Register

TTL Output Control Data Register (TTLOD) at offset 198h configures the Output Data. Table 8.8.10 shows the bit positions for offset 198h.

Table 8.8.10: TTL Output Control Data Register (Offset 198h)

Bit	Description
0	Channel 0 Output Control
1	Channel 1 Output Control
2	Channel 2 Output Control
3	Channel 3 Output Control
4	Channel 4 Output Control
5	Channel 5 Output Control
6	Channel 6 Output Control
7	Channel 7 Output Control
8	Channel 8 Output Control
9	Channel 9 Output Control
10	Channel 10 Output Control
11	Channel 11 Output Control
12	Channel 12 Output Control
13	Channel 13 Output Control
14	Channel 14 Output Control
15	Channel 15 Output Control

To set TTL Outputs, do the following:

- Set the state of the outputs which are controlled by TTLOD (offset 198h- Table 8.8.10).
- Set bit 0 of TTLOC (offset 197h - Table 8.8.9).
- When the firmware sets the TTL Outputs, bit 0 of TTLOC clears. Feedback data writes to TTLOF register (Table 8.8.11).

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TTL Feedback Register

TTL Feedback Register (TTLOF) at offset 199h verifies that the output data was written correctly. Table 8.8.11 shows the bit positions for offset 199h.

Table 8.8.11: TTL Feedback Register (Offset 199h)

Bit	Description
0	Channel 0 Feedback Data
1	Channel 1 Feedback Data
2	Channel 2 Feedback Data
3	Channel 3 Feedback Data
4	Channel 4 Feedback Data
5	Channel 5 Feedback Data
6	Channel 6 Feedback Data
7	Channel 7 Feedback Data
8	Channel 8 Feedback Data
9	Channel 9 Feedback Data
10	Channel 10 Feedback Data
11	Channel 11 Feedback Data
12	Channel 12 Feedback Data
13	Channel 13 Feedback Data
14	Channel 14 Feedback Data
15	Channel 15 Feedback Data

8.8.3 0-28V Ground/Open Discrete Output Registers

Table 8.8.12 shows the 0-28V Ground/Open Discrete Output Registers.

Table 8.8.12: 0-28V Ground/Open Discrete Output Registers

Offset	Description
19Ah	Ground/Open Discrete Output Control Register (GODOC)
19Bh	Ground/Open Discrete Output Data Register (GODOD)
19Ch	Ground/Open Discrete Data Feedback Register (GODFB)
19Dh	Ground/Open Discrete Fault Threshold Register (GODTHRESHOLD)
19Eh – 1ADh	Ground/Open Discrete Fault Count Register (GODFAULT0-15)

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Ground/Open Discrete Output Control Register

Ground/Open Discrete Output Control Register (GODOC) at offset 19Ah controls Ground/Open Discrete Output Operations. Table 8.8.13 shows the bit positions for offset 19Ah.

Table 8.8.13: Ground/Open Discrete Output Control Register (Offset 19Ah)

Bit	Description
0	1 = Set Single Ended Outputs
1	1 = Clear Fault Overflow
2 - 15	Unused

Ground/Open Discrete Output Data Register

Ground/Open Discrete Output Data Register (GODOD) at offset 19Bh contols the data for Ground/Open Discrete Outputs. Table 8.8.14 shows the bit positions for offset 19Bh.

Table 8.8.14: Ground/Open Discrete Output Data Register (Offset 19Bh)

Bit	Description
0	Ground/Open Discrete Output 0, 0 = Open, 1 = Ground
1	Ground/Open Discrete Output 1, 0 = Open, 1 = Ground
2	Ground/Open Discrete Output 2, 0 = Open, 1 = Ground
3	Ground/Open Discrete Output 3, 0 = Open, 1 = Ground
4	Ground/Open Discrete Output 4, 0 = Open, 1 = Ground
5	Ground/Open Discrete Output 5, 0 = Open, 1 = Ground
6	Ground/Open Discrete Output 6, 0 = Open, 1 = Ground
7	Ground/Open Discrete Output 7, 0 = Open, 1 = Ground
8	Ground/Open Discrete Output 8, 0 = Open, 1 = Ground
9	Ground/Open Discrete Output 9, 0 = Open, 1 = Ground
10	Ground/Open Discrete Output 10, 0 = Open, 1 = Ground
11	Ground/Open Discrete Output 11, 0 = Open, 1 = Ground
12	Ground/Open Discrete Output 12, 0 = Open, 1 = Ground
13	Ground/Open Discrete Output 13, 0 = Open, 1 = Ground
14	Ground/Open Discrete Output 14, 0 = Open, 1 = Ground
15	Ground/Open Discrete Output 15, 0 = Open, 1 = Ground

To set the Ground/Open Discrete outputs, do the following:

- ➢ Set the Ground/Open Discrete data controlled by GODOD (offset 19Bh - Table 8.8.14)
- ➢ Set bit 0 of GODOC (offset 19Ah- Table 8.8.13)
- ➢ When the firmware sets all Ground/Open Discrete outputs, bit 0 of GODOC clears (Table 8.8.13)

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Ground/Open Discrete Data Feedback Register

Ground/Open Discrete Data Feedback Register (GODFB) at offset 19Ch verifies that the data was written correctly. It compares the contents of the GODFB register at offset 19Ch to the GODOD register at offset 19Bh. If a bit of the GODFB register is set to 0 for an output of the GODOD register that is a 1, the firmware registers a fault for that channel. Table 8.8.15 shows the bit positions for offset 19Ch.

Table 8.8.15: Ground/Open Discrete Data Feedback Register (Offset 19Ch)

Bit	Description
0	Ground/Open Discrete Feedback 0
1	Ground/Open Discrete Feedback 1
2	Ground/Open Discrete Feedback 2
3	Ground/Open Discrete Feedback 3
4	Ground/Open Discrete Feedback 4
5	Ground/Open Discrete Feedback 5
6	Ground/Open Discrete Feedback 6
7	Ground/Open Discrete Feedback 7
8	Ground/Open Discrete Feedback 8
9	Ground/Open Discrete Feedback 9
10	Ground/Open Discrete Feedback 10
11	Ground/Open Discrete Feedback 11
12	Ground/Open Discrete Feedback 12
13	Ground/Open Discrete Feedback 13
14	Ground/Open Discrete Feedback 14
15	Ground/Open Discrete Feedback 15

Ground/Open Discrete Fault Threshold Register

Ground/Open Discrete Fault Threshold Register (GODTHRESHOLD) at offset 19Dh sets a limit on the maximum number of faults per output channel which firmware can read before generating an overrun condition to the host and stops processing.

Ground/Open Discrete Fault Count Registers

Ground/Open Discrete Fault Count Registers (GODFAULT0-15) at offsets 19Eh through 1ADh hold the number of fault counts for each output. A fault generates each time an over current condition is detected.

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8.8.4 Bipolar Ground/Open Input Registers

Table 8.8.16 shows the Bipolar Ground/Open Input Registers.

Table 8.8.16: Bipolar Ground/Open Input Registers

Offset	Description
1B0h	Bipolar Input Control Register (BGOC)
1B1h	Bipolar Inputs Interrupt Enable for Channels 0-15 Register (BGOIE16)
1B2h	Bipolar Inputs Interrupt Enable for Channels 16-23 Register (BGOIE24)
1B3h	Bipolar Input Data for Channels 0-15 Register (BGOIND16)
1B4h	Bipolar Input Data for Channels 16-23 Register (BGOIND24)
1B5h	Bipolar Input Polarity for Bipolar Inputs 0-15 Register (BGOIP16)
1B6h	Bipolar Input Polarity for Bipolar Inputs 16-23 Register (BGOIP24)

Bipolar Input Control Register

Bipolar Input Control Register (BGOC) at offset 1B0h controls the polarity for bipolar inputs. Table 8.8.17 shows the bit positions for offset 1B0h.

Table 8.8.17: Bipolar Input Control Register (Offset 1B0h)

Bit	Description
0	1 = Set Input Polarity
1 - 15	Not Used

Bipolar Inputs Interrupt Enable for Channels 0-15 Register

Bipolar Inputs Interrupt Enable for Channels 0-15 Register (BGOIE16) at offset 1B1h enables an interrupt to be generated for detection of each input in offset 1B3h. Detection of a valid input generates an interrupt (Hardware/Software). BGOIE16 sets for the Bipolar Input of interest. A valid signal is any transition from 1 to 0 or 0 to 1. Table 8.8.18 shows the bit positions for offset 1B1h.

Table 8.8.18: Bipolar Inputs Interrupt Enable for Channels 0-15 Register (Offset 1B1h)

Bit	Description
0	Detection Interrupt Enable Input 0, 0 = Disable, 1 = Enable
1	Detection Interrupt Enable Input 1, 0 = Disable, 1 = Enable
2	Detection Interrupt Enable Input 2, 0 = Disable, 1 = Enable
3	Detection Interrupt Enable Input 3, 0 = Disable, 1 = Enable
4	Detection Interrupt Enable Input 4, 0 = Disable, 1 = Enable
5	Detection Interrupt Enable Input 5, 0 = Disable, 1 = Enable
6	Detection Interrupt Enable Input 6, 0 = Disable, 1 = Enable
7	Detection Interrupt Enable Input 7, 0 = Disable, 1 = Enable
8	Detection Interrupt Enable Input 8, 0 = Disable, 1 = Enable

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Bit	Description
9	Detection Interrupt Enable Input 9, 0 = Disable, 1 = Enable
10	Detection Interrupt Enable Input 10, 0 = Disable, 1 = Enable
11	Detection Interrupt Enable Input 11, 0 = Disable, 1 = Enable
12	Detection Interrupt Enable Input 12, 0 = Disable, 1 = Enable
13	Detection Interrupt Enable Input 13, 0 = Disable, 1 = Enable
14	Detection Interrupt Enable Input 14, 0 = Disable, 1 = Enable
15	Detection Interrupt Enable Input 15, 0 = Disable, 1 = Enable

Bipolar Inputs Interrupt Enable for Channels 16-23 Register

Bipolar Inputs Interrupt Enable for Channels 16-23 Register (BGOIE24) at offset 1B2h enables an interrupt to be generated for detection of each input in offset 1B4h. Detection of a valid input generates an interrupt (Hardware/Software). BGOIE24 sets for the Bipolar Input of interest. A valid signal is any transition from 1 to 0 or 0 to 1. Table 8.8.19 shows the bit positions for offset 1B2h.

Table 8.8.19: Bipolar Inputs Interrupt Enable for Channels 16-23 Register (Offset 1B2h)

Bit	Description
0	Detection Interrupt Enable Input 16, 0 = Disable, 1 = Enable
1	Detection Interrupt Enable Input 17, 0 = Disable, 1 = Enable
2	Detection Interrupt Enable Input 18, 0 = Disable, 1 = Enable
3	Detection Interrupt Enable Input 19, 0 = Disable, 1 = Enable
4	Detection Interrupt Enable Input 20, 0 = Disable, 1 = Enable
5	Detection Interrupt Enable Input 21, 0 = Disable, 1 = Enable
6	Detection Interrupt Enable Input 22, 0 = Disable, 1 = Enable
7	Detection Interrupt Enable Input 23, 0 = Disable, 1 = Enable
8-15	Unused

Bipolar Input Data for Channels 0-15 Register

Bipolar Input Data for Channels 0-15 Register (BGOIND16) at offset 1B3h contains input data for channels 0-15. Table 8.8.20 shows the bit positions for offset 1B3h.

Table 8.8.20: Bipolar Input Data for Channels 0-15 Register (Offset 1B3h)

Bit	Description
0	Bipolar Data Input 0
1	Bipolar Data Input 1
2	Bipolar Data Input 2
3	Bipolar Data Input 3
4	Bipolar Data Input 4
5	Bipolar Data Input 5
6	Bipolar Data Input 6
7	Bipolar Data Input 7

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Bit	Description
8	Bipolar Data Input 8
9	Bipolar Data Input 9
10	Bipolar Data Input 10
11	Bipolar Data Input 11
12	Bipolar Data Input 12
13	Bipolar Data Input 13
14	Bipolar Data Input 14
15	Bipolar Data Input 15

Bipolar Input Data for Channels 16-23 Register

Bipolar Input Data for Channels 16-23 Register (BGOIND24) at offset 1B4h contains input data for channels 16-23. Table 8.8.21 shows the bit positions for offset 1B4h.

Table 8.8.21: Bipolar Input Data for Channels 16-23 Register (Offset 1B4h)

Bit	Description
0	Bipolar Data Input 16
1	Bipolar Data Input 17
2	Bipolar Data Input 18
3	Bipolar Data Input 19
4	Bipolar Data Input 20
5	Bipolar Data Input 21
6	Bipolar Data Input 22
7	Bipolar Data Input 23
8-15	Unused

Bipolar Input Polarity for Bipolar Inputs 0-15 Register

Bipolar Input Polarity for Bipolar Inputs 0-15 Register (BGOIP16) at offset 1B5h contains polarity information for inputs 0-15. Table 8.8.22 shows the bit positions for offset 1B5h.

Table 8.8.22: Bipolar Input Polarity for Bipolar Inputs 0-15 Register (Offset 1B5h)

Bit	Description
0	Input Polarity for Channel 0
1	Input Polarity for Channel 1
2	Input Polarity for Channel 2
3	Input Polarity for Channel 3
4	Input Polarity for Channel 4
5	Input Polarity for Channel 5
6	Input Polarity for Channel 6
7	Input Polarity for Channel 7

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Bit	Description
8	Input Polarity for Channel 8
9	Input Polarity for Channel 9
10	Input Polarity for Channel 10
11	Input Polarity for Channel 11
12	Input Polarity for Channel 12
13	Input Polarity for Channel 13
14	Input Polarity for Channel 14
15	Input Polarity for Channel 15

Bipolar Input Polarity for Bipolar Inputs 16-23 Register

Bipolar Input Polarity for Bipolar Inputs 16-23 Register (BGOIP24) at offset 1B6h contains polarity information for inputs 16-23. Table 8.8.21 shows the bit positions for offset 1B6h.

Table 8.8.23: Bipolar Input Data for Channels 16-23 Register (Offset 1B6h)

Bit	Description
0	Input Polarity for Channel 16
1	Input Polarity for Channel 17
2	Input Polarity for Channel 18
3	Input Polarity for Channel 19
4	Input Polarity for Channel 20
5	Input Polarity for Channel 21
6	Input Polarity for Channel 22
7	Input Polarity for Channel 23
8-15	Unused

To set Input Polarity, do the following:

- ➢ Configure Polarity registers (BGOIP16/ BGOIP24 offsets 1B5h, 1B6h).
- ➢ Set bit 0 of BGOC (offset 1B0h).
- ➢ Once the polarity is set, bit 0 of BGOC clears.

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8.8.5 Data Output Option Registers

If you purchased the Data Output option, this Subsection describes how the firmware operates, and provides descriptions of the appropriate registers.

Firmware Operation Overview

You can provide up to 3 buffers filled with data. Buffers are indexed from 1 to 3 and can have sizes up to 8000h words.

The buffers should start at RAM offsets of 8000h, 10000h, and 18000h. Buffer lengths should be written to registers BDO_BUFF1_LENGTH, BDO_BUFF2_LENGTH, and BDO_BUFF3_LENGTH.

Once the firmware detects a nonzero value in the one of those offsets, it copies the length, and the buffer index, into its internal variables and starts writing the buffer data out to the FIFO. For each Rising/Falling Edge of the strobe signal the FIFO sends a word of data. Once all the data is written to the FIFO, the firmware clears the corresponding buffer length register and attempts to locate another non empty buffer. If the firmware succeeds in locating another non-empty buffer, and Bit 0 of BDO_INT_CTRL register is set, the firmware will generate an interrupt to the host with information about which buffer was processed. If the firmware does not find a non empty buffer, and Bit 1 of the BDO_INT_CTRL is set, the firmware generates an "All Buffers Empty" interrupt.

At any moment, you can read BDO_WORDS_IN_FIFO offset to determine how many words are currently loaded into the FIFO. If Bit 2 of BDO_INT_CTRL register is set and the FIFO becomes empty, the firmware generates an "Empty FIFO" interrupt.

The remaining topics describe the register structure bit definitions.

BDO_CTRL (200h)

This is the general Control Register for Data Generation. The bit settings in this register determine the general operation of the data output option registers.

Table 8.8.24: BDO_CTRL Bit Definitions

Bit	Function	Description
0	Run Enable State	To enable the Run Enable State, set this bit to 1. Before writing to this bit make sure to specify the state in Bit 0 of BDO_MISC register. Bit will clear when the operation is completed by the firmware.
1	Strobe De-bounce/ Bypass	To enable the Strobe De-bounce/Bypass, set this bit to 1. Make sure that the state is specified in Bit 1 of BDO_MISC register. Bit will clear when the operation is completed by the firmware.

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Bit	Function	Description
2	Strobe Rising/Falling Edge Mode	To enable the Strobe Rising/Falling Edge Modes, set this bit to 1. Make sure that the mode is specified in Bit 2 of BDO_MISC register. The firmware clears the bit when the operation is complete.
3	Strobe Input Select	To enable the Strobe Input Select, set this bit to 1. Make sure that the input TTL is specified in BDO_IN_SEL register. The firmware clears the bit when the operation is complete.
4	Reset Interface	To reset the interface, set this bit to 1. This clears the FIFO and all of the internal registers. The firmware clears the bit when the operation is complete.

BDO_MISC (201h) Miscellaneous Setup Register

Table 8.8.25: Miscellaneous Setup information Bit Definitions

Bit	Function	Description
0	Buffer Run Enable	0=Disable the interface 1=Allow Buffers to Run when strobe is generated to the specified TTL input pin
1	Strobe De-bounce/ Bypass	1=Bypass 0=Enable Strobe De-bounce
2	Strobe Edge	0=Use rising edge 1=Use falling edge

BDO_IN_SEL (202h) Specifies TTL Input where firmware expects the strobe. (4 Lower Bits).

BDO_INT_CTRL (0x203) Interrupt Control Register

Table 8.8.26: Interrupt Control Register Bit Definitions

Bit	Description
0	Setting this bit to 1 causes the DSP to generate an interrupt when it completes sending a buffer of data, and detects another buffer waiting to be sent. The interrupt information will be sent to the user via standard DIO interface specified in the manual and the 4 elements of the interrupt structure will contain the following information: ➢ Offset 0 - Value of 7 ➢ Offset 1 - Contains a 1 based index of the buffer that the firmware just finished sending out to the FIFO. ➢ Offset 2 - 0 ➢ Offset 3 - 0

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Bit	Description
1	Setting this bit to 1 causes the DSP to generate an interrupt when it completes sending a buffer of data, *but did not detect* another buffer waiting to be sent. The 4 elements of the interrupt structure will contain the following information: ➢ Offset 0 - Value of 7 ➢ Offset 1 - 0 ➢ Offset 2 - 0 ➢ Offset 3 - 0
2	If this bit is set, and the DSP detected an empty FIFO, it generates an interrupt with the 4 elements of the interrupt structure containing the following information: ➢ Offset 0 - Value of 7 ➢ Offset 1 - Value of 4 ➢ Offset 2 - 0 ➢ Offset 3 - 0

BDO_BUFF1_LENGTH (204h) Write a non-zero value to indicate how many words are in the buffer. When the value equals 0, the buffer is not used. The buffer starts at offset 8000h.

BDO_BUFF2_LENGTH (205h) Write a non-zero value to indicate how many words are in the buffer. When the value equals 0, the buffer is not used. The buffer starts at offset 10000h.

BDO_BUFF3_LENGTH (206h) Write a non-zero value to indicate how many words are in the buffer. When the value equals 0, the buffer is not used. The buffer starts at offset 18000h.

BDO_WORDS_IN_FIFO (207h) The 9 lower bits contain the number of words currently in the FIFO.

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9: Using the INTEGRITY API



Note: The INTEGRITY IODevice API calls that are supported by the DIO4-cPCI-CC driver are described in this chapter.

DIO4-cPCI-CC INTEGRITY driver doesn't have a specialized Application Programing Interface (API). Instead, it facilitates various INTEGRITY IODevice API calls. The following sections describe the IODevice API calls that are supported by the DIO4 INTEGRITY driver and can be used in a user application. See the list below:

- `RequestResource()`
- `CloseIODevice()`
- `ReadIODeviceRegister()`

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9.1 RequestResource

Description `RequestResource` call opens a given DIO4 device. A zero-based index identifies each device. Concatenating strings `SBSDIO4_NAME_ROOT` and <`device index`> creates the device full name. For example, `SBSDIO4_NAME_ROOT "1"` creates a name for the second DIO4 device. `SBSDIO4_NAME_ROOT` is defined in the *dio4.h* file.

Syntax

```
Error  RequestResource(Object      *TheObject,
                       const char  *name,
                       const char  *password);
```

Parameters `TheObject` parameter is the DIO4 device's IODevice object to be created.

The `name` parameter is the name of the DIO4 device registered with the Resource Manager.

The `password` parameter uses the default Resource manager password `"!password"`.

Comments None

Example

```
#include "dio4.h"

Error e;
IODevice ioDev;

// open first device (0)
e = RequestResource((Object*)&ioDev, SBSDIO4_NAME_ROOT "0", "!systempassword);
```

See Also None

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9.2 CloseIODevice

Description `CloseIODevice` closes the given device. The device must be successfully opened by a previous call to `RequestResource`.

Syntax **`Error CloseIODevice(IODevice TheIODevice)`**

Parameters `TheIODevice` parameter is the DIO4 device's IODevice object created by `RequestResource`.

Comments None

Example

```
#include "dio4.h"

Error e;
IODevice ioDev;

// open device here
...

// done, close the device
e = CloseIODevice(ioDev);
```

See Also `RequestResource()`

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9.3 ReadIODeviceRegister

Description `ReadIODeviceRegister` has only one register numbers defined as follows:

- `DIO4_BASE_ADDR_REG` reads the PCI memory base address assigned to the device's onboard registers.

Status number is defined in the *dio4.h* file.

Syntax

```
Error  ReadIODeviceRegister(IODevice   TheIODevice,
                            Value      RegisterNumber,
                            Value      *RegisterValue)
```

Parameters `TheIODevice` parameter is the DIO4 device's IODevice object created by `RequestResource`.

`RegisterNumber` parameter is the register number to be read from.

`RegisterValue` parameter is the register value read.

Comments None

Example

```
#include "dio4.h"

IODevice ioDev;
Error e;
Value bar;

// open device here
...

// get BAR register from PCI configuration space
e = ReadIODeviceRegister(ioDev, DIO4_BASE_ADDR_REG, &bar);
```

See Also `RequestResource()`

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A: Revisions

The table in this appendix gives a brief summary of any technical revisions made to this manual. When reading this manual online, you can jump to the first citation of a revision by clicking the links in blue.



Note: Only technical revisions appear in the table. Most even numbered pages contain a date stamp in the footer. If the footer date is more recent then the latest revision date given in the table, then the newest revision of this manual contains only *non-technical* revisions.

Revision Number	Revision Date	Description
1	21 May 2004	This is the initial release of this manual.
1.01	14 Mar 2005	Changed the card name from DIO4-cPCI3U-CC to DIO4-3CP beginning at the Front Cover.
1.02	2 Jun 2004	This revision changes Configuration and Storage Register (CSR) to Control/Status Register (CSR) beginning at Table 1.4.1. Added Section 1.1 Model Identification.
1.03	13 Dec 2005	Changed the card name from DIO4-3CP to DIO4-cPCI-CC beginning at the Front Cover.
1.04	11 May 2006	Added Subsection 8.8.5, Data Output Option Registers to Chapter 8.

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