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GREEN SPRING COMPUTERS

User Manual

IP-BSDI

Buffered Serial Data Input IndustryPack®

Manual Revision: ii

Hardware Revision: A

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IP-BSDI

Buffered Serial Data Input
IndustryPack

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Product Description

General

IP-BSDI is part of the IndustryPack family of modular I/O components. It provides two protocols of serial reception. The reception protocols currently implemented include Synchronous mode and SCAR mode. The Synchronous mode depends on software protocol for transmission integrity and the SCAR mode utilizes a hardware handshake line. Both protocols are implemented within a Xilinx FPGA for maximum flexibility. Please contact GreenSpring Computers with your custom application.

Both single ended and differential I/O are available on the serial reception signals. The differential drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signals are terminated with 180Ω. The single ended driver signal is characterized as an open drain driver with 48 mA of sink. The pull-up is to be supplied by the receiving circuit.

All configuration registers support read and write operations for maximum software convenience. Word or byte operations are supported (please refer to the memory map).

The IP-BSDI conforms to the IndustryPack Interface Specification revision .6. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module, with final system implementation on a different one.

The serial channel is supported with a 1K x 16 FIFO. The FIFO supports byte and word reads. A byte wide write path exists for loopback testing. The serial channel writes the first byte of data received into FIFO_0. The second byte will be written into FIFO_1. The FIFOs are alternated until the strobe signal is deactivated.

The IP-BSDI can create an external reference clock. Several rate divisors are selectable. The base rate for the generator is the IPCLK divided by 4.

Interrupts are supported by the IP-BSDI. An interrupt is supported in the SCAR protocol. The interrupt occurs at the end of the transmission. The Synchronous protocol interrupt occurs at the start of the reception when STB is first activated. The vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The FIFO status is available for FIFO_0 making it possible to operate in a polled mode. A status bit is set if the reception was successful.

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Memory Map

All addresses shown are offsets from the base established by the carrier board.

Function		Offset	Width	Type
BSDI_STAT	EQU	$00	byte on word boundary	read
BSDI_CNTL	EQU	$02	word	read/write
BSDI_VECTOR	EQU	$04	byte on word boundary	read/write
BSDI_FIFO_0_W	EQU	$07	byte	write
BSDI_FIFO_1_W	EQU	$09	byte	write
BSDI_FIFO_0_R	EQU	$06	word or byte	read
BSDI_FIFO_1_R	EQU	$07	byte	read
BSDI_RESET	EQU	$0E	word	write
BSDI_IDPROM	EQU	$80	byte on word boundary	read

Figure 1 BSDI Memory Map

Bitmaps

BSDI_STAT [$00] BSDI Status Port [read only]

Data Bit	Status
0	FIFO_0_EMPTY 0 = MT
1	FIFO_0_HF 0 = HALF FULL +
2	FIFO_0_FULL 0 = FULL
3	TX_ST, 1 = Good Reception, auto cleared when read
4	ISTB strobe status 0 = active

Figure 2 BSDI Status Bitmap

BSDI_Vector [$04] BSDI Interrupt Vector Port
The Interrupt vector for the BSDI is stored in this register. The register is a byte wide read/write register which is initialized to 'xx00' upon power-on reset or software reset. The odd byte location [D7..0] is used for the vector. The vector should be initialized before the interrupt is enabled or the mask lowered. The interrupt is autocleared when the CPU reads the vector.

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BSDI_FIFO_0_W [$07] BSDI FIFO byte 0 write
The BSDI supports byte writes to the data FIFOs. By writing a byte to this address only byte_0 is affected. This path is provided for test purposes. This feature competes with the receiver section and should not be used when a message is in process.

BSDI_FIFO_1_W [$09] BSDI FIFO byte 1 write
The lower byte can be written to through this port.

BSDI_FIFO_0_R [$07] BSDI FIFO byte 0 read
The data stored into FIFO_0 can be accessed through this port. Byte and word accesses are available. A word access will fetch data from both FIFO 0 and FIFO 1. Data is received MSB first.

BSDI_FIFO_1_R [$09] BSDI FIFO byte 1 read
The data stored into FIFO 1 can be accessed through this port. Byte wide accesses only.

BSDI_RESET [$0E] BSDI Reset Port
The user can, by accessing this port, cause the BSDI to reset all major functions. The Control register, Interrupt Vector, and FIFO's are cleared by this port. Any data pattern can be written.

BSDI_CNTL [$02] BSDI Control Register Port read/write

CONTROL RESISTER

DATA BIT	DESCRIPTION
15	UNUSED
14	UNUSED
13	UNUSED
12	UNUSED
11	FBUSEN
10	FIFOEN/FIFORST
9	INTEN
8	Spare
7	B2
6	B1
5	B0
4	Spare
3	NORMAL/TEST
2	START/ABORT
1	PROTO1
0	PROTO0

Figure 3 BSDI Control Register Bit Map

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1. PROTO1,0 select SCAR and SYNC protocols. 00 corresponds to SCAR, and 01 to Synchronous mode respectively.

2. All bits are active high and are reset on power-up or reset command.

3. Start/Abort when set high will set RDY high. This bit is auto cleared in SCAR mode

4. Normal/Test selects which version of Data, Clock, and Strobe to use, the RS-422 or the TTL loopback version. Test = TTL Loop-back, and is the default.

5. B2B1B0 are the encoded baud rate selection for generating the external reference clock.

bit pattern	**divisor**	
000	1	default = 2 mhz
001	2	
010	4	
011	8	
100	16	
101	32	
110	64	
111	128	

6. The spare bits are functional for loopback, and reserved for future use as Width control.

7. INTEN is the Interrupt enable bit. Default to off. Interrupt is reset on power-up initialization. Interrupt is cleared by CPU vector fetch. Vector from vector port.

8. FIFO Enable should be high to use the FIFO. When bit 10 is low [default] the FIFOs are held in reset.

9. FBUSEN Enable is used to select the parallel or serial input paths. When low [default] the serial path is chosen. [code as 0].

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Interrupts

The state machine is used to create an interrupt request when in the SCAR Protocol, the INTEN bit in the control register is set, and the transmission completes. The transmission is considered complete when the strobe line is deactivated. This means that an interrupt is generated when a transmission in the SCAR mode completes with or without error conditions. The status register should be checked as a part of the interrupt service routine to determine if the transmission completed properly. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector and clear the request when accessed by the CPU.

In the Synchronous mode the interrupt is generated when the strobe is activated. The hardware handshake line RDY is ignored in this mode, and transmissions of any length are possible. The software will use an embedded protocol to control the data transfer length. The software will after reception of the initial interrupt be responsible to poll the status bits to determine when data is available to read.
IDPROM

BSDI_IDPROM [$80] Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-BSDI is shown below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

Address	Data
01	Ascii "I" ($49)
03	Ascii "P" ($50)
05	Ascii "A" ($41)
07	Ascii "C" ($43)
09	Manufacturer ID (F0)
0B	Model Number (31)
0D	Revision (A1)
0F	reserved (00)
11	Driver ID, low byte (00)
13	Driver ID, high byte (00)
15	No of extra bytes used (0C)
17	CRC (35)
19-3F	available for user

Figure 4 ID PROM

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ID PROM

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived by multiplying the address by two and then subtracting one. RM1270 addresses may be derived by multiplying the addresses by two and then adding one.

I/O Pin Wiring

This section gives the pin assignments and wiring recommendation for the IP-BSDI.

The pin numbers below correspond to the 50 pin IndustryPack I/O connector, to the wires on a 50 pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP Terminal block.

GND		GND		1		26	
	RDY422+		PD0+		2		27
RDY422-		PD0-		3		28	
	GND		GND		4		29
RDYTTL		PD1+		5		30	
	GND		PD1-		6		31
EXTREF+		GND		7		32	
	EXTREF-		PD2+		8		33
GND		PD2-		9		34	
	STB+		GND		10		35
STB-	PD3+		11		36		
	GND		PD3-		12		37
CLK+	GND		13		38		
	CLK-		PD4		14		39
GND		PD4-		15		40	
	DATA+		GND		16		41
DATA-		PD5+		17		42	
	GND		PD5-		18		43
STBTTL		GND		19		44	
	GND		PD6+		20		45
CLKTTL		PD6-		21		46	
	GND		GND		22		47
DATATTL		PD7+		23		48	
	GND		PD7-		24		49
N/C		GND		25		50	

Figure 5 BSDO I/O Interface Pin Assignment

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IndustryPack Logic Interface Pin Assignment

The figure below gives the pin assignments for the IndustryPack Logic Interface on the IP-BSDI. Pins marked n/c below are defined by the specification, but not used on the IP-BSDI. See also the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*	R/W*		3		28		
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		IntSel*		8		33
D5		n/c		9		34	
	D6		IOSel*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		IntReq0*		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		n/c		20		45
BS1*		n/c		21		46	
	n/c		n/c		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		Gnd		25		50	

NOTE 1: The no-connect signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 6 IP-BSDI Logic Interface P1

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J1 Pin Assignments

+5V	1	
GND	2	
M00, M01, M02	3	tied to pullup
CCLK	4	
D/P	5	
DIN	6	

Figure 7 Xilinx Programming Connector

To download, the standard download cable is connected between the parallel port on your PC and the J1 connector on the BSDI. The M00, M01, M02 bits are pulled high to select cable download. Once development is complete pins 2 and 3 should be shorted to select PROM mode. The BSDI is supplied from the factory with pins 2 and 3 connected with a shorting plug.

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Programming

Programming the IP-BSDI requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Support Module. This documentation refers to this address as base.

In order to receive data the software is only required to enable the receivers and select the appropriate protocol. If desired the interrupt can be enabled. If in the SCAR protocol the RDY line must be asserted by selecting the Start bit. If the Start bit is rewritten low during a SCAR protocol reception then the message will be aborted and the TX_ST bit on the BSDO board will not be set and the RX_ST on the BSDI will also not be set. Data will be loaded into the FIFOs as it is received. FIFO_0 is written to first with the MSB of data then FIFO_1. The FIFOs are loaded with alternate bytes until the transmission is completed.

A typical sequence would be to first write to the vector register with the desired vector. For example $40 is a valid user vector for the Motorola 680x0 family. The interrupt service routine and mask should be loaded and set . Next the software can select SCAR mode, Serial (FBUSEN low), Normal, Interrupt Enabled by writing to the control register with $060C. By setting the Start bit the RDY signal will be activated and if the output channel is waiting to transmit a transmission will immediately begin. After the interrupt is received the data pattern can be retrieved. If the data pattern contains an embedded length then the software can read the count and set-up a loop counter to efficiently read the data from the FIFOs. If the data pattern does not contain a message length then the status register will be polled to determine when the FIFOs go empty. FIFO_1 is not represented by the status register which will restrict the protocol to a known even or odd length.

The end of transmission interrupt will indicate to the software that the message has been started and that the message has terminated. The software needs to look at the RX_ST bit in the BSDI_STAT register to determine if all of the bits were transferred. Reading the status register autoclears the RX_ST bit. It is a good idea to read the status register to force the RX_ST to 0 before Start is enabled to insure that the RX=1 value the interrupt service routine reads came from the current transmission.

The Synchronous mode is very similar to the SCAR mode in set-up and execution. The key differences is that the interrupt associated with the Synchronous mode occurs at the beginning of the message, the transmitter does not wait for the RDY signal, and the RX_ST bit is set as transmission begins.

Please refer to the Memory Map, Bit Map, and Theory of Operation for more information regarding exact sequencing and interrupt definitions.

Contact GreenSpring Computers for additional assistance.

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Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail safe common ground that is large enough to handle all current loads without impacting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common source.

Power all system power supplies from one switch. Connecting external voltage to the IP-BSDI when it is unpowered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels should be used.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-BSDI does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practise. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within .7 volts of ground potential.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cable, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

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Theory of Operation

The IP-BSDI is designed for the purpose of transferring data from one point to another in either a serial or parallel protocol. The parallel protocol is not currently implemented within the FPGA.

The BSDI features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BSDI design. Only the drivers, receivers, boot PROM and FIFOs are external to the Xilinx device.
IndustryPack Standards

The IP BSDI is a part of the IndustryPack family of modular I/O products. It meets the IndustryPack Logic Specification revision .6. Contact GreenSpring Computers for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

Control Logic

The bus interface to the host CPU is controlled by a logic block within the Xilinx device. The IP_IF contains the decoding and timing elements required to interface to the IP bus interface. The timing is referenced to the 8 MHz. IP logic clock. The IP responds to the ID, INTSEL, IO, and MEM selects. It does not respond to DMA selects.

The IP data bus is brought into the Xilinx device to interface with the registers etc. The Xilinx device doesn't support bidirectional tristate devices. The IO_12 block is used to separate the incoming from the outgoing signals. The IP data bus writes are channeled onto the IDx lines and the IP Data bus reads use the ODx data bus. The IP_IF controls the interface with the OBUFZ signal which controls the output buffer tristate controls.

The BSDI design does not require wait states for read or write cycles to any address. The control PAL generates ACK on the clock cycle following any select. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host remove the SEL line. Local timing terminates a write cycle prior to the SEL being deasserted. If no hold cycles are requested by the host, the IP-BSDI is capable of supporting the full 8 MB per second data transfer rate of the IP Logic Interface Specification.

ID PROM

The ID PROM is implemented as a pseudo PROM inside the FPGA by programming CLBs with Boolean equations. The IDPROM is controlled via the ID space select and the IP_IF logic block.

For the contents of the ID PROM, see figure ID PROM in the main text. For more information on ID PROMs in general, see the IndustryPack Logic Interface Specification.

Parallel I/O

The Parallel Output port is supported by a pair of differential receivers directly connected to the FIFO bus. The concept is for the serial lines to be used as control for the parallel data. The serial signals are grouped with three dedicated inputs, one dedicated output and one bidirectional device. The directional control and tristate control originate within the gate array. The Xilinx load map can be modified to implement the protocol in the future without changing the PC board.

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Serial I/O

The serial IO supports the SCAR and Synchronous protocols. The protocols are named for the devices the channels were initially interfaced to.

The SCAR interface utilizes the RDY signal as a handshake line for the receiver to hold off transmissions or to abort them in the middle. The timing of the control signals is as shown in the following diagram. The clock is bursted, the data is valid on the rising edge of the clock, the strobe frames the data. The Xilinx device utilizes a logic block to control the timing.

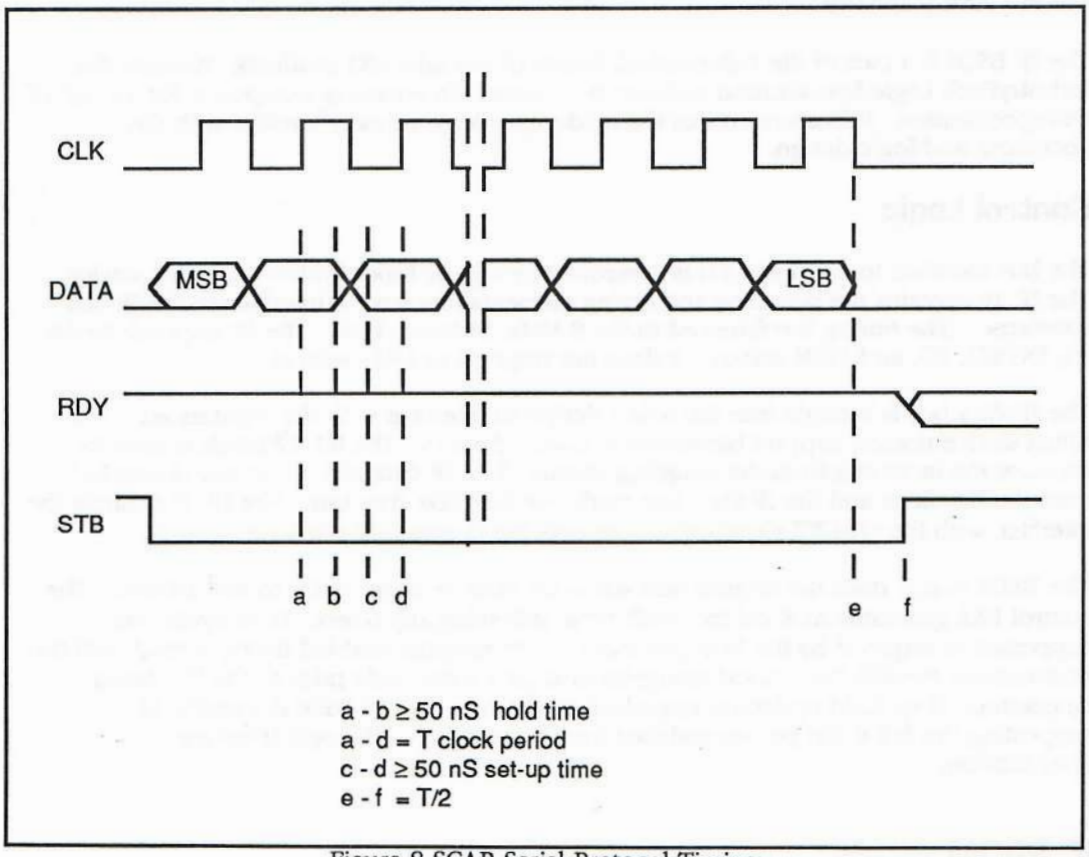


Figure 8 SCAR Serial Protocol Timing

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The state machine which controls the transfer takes care of moving data from the shift register into the FIFO at the appropriate times. The state machine uses a 4 bit counter to determine which FIFO should be loaded and when. The counter starts at 0 and counts to F before rolling over. The MSB determines which FIFO to load from, and the lower three bits determine when to load the shift register.

The counter counts the data clock on the rising edge. When the count reaches $7 or $F then [referring to the Xilinx schematics] the second flip-flop in the chain latches in a high condition representing a full shift register. The counter counts from 0 but transitions on the first clock. The second latch uses the data clock as well to capture the condition on the 8th clock to form the load signal. The IPCLK (8Mhz.) is used to delay the load signal one to two periods to insure that the data bus to the FIFO is stable with the new data. One period later the load pulse is removed. The upper counter bit is used to point to the FIFO to load. The counter will be pointed at the next FIFO in sequence because it is one period ahead of the data. When Q3 is high FIFO_0 is enabled to be loaded.

In the Synchronous mode the hardware allows the clock to be free running, ignores the ready signal, doesn't create an interrupt, and creates the RX_ST signal at the start rather than the end of the transmission. The strobe is terminated after the last data hold time which is 1/2 T before the SCAR mode deassertion.

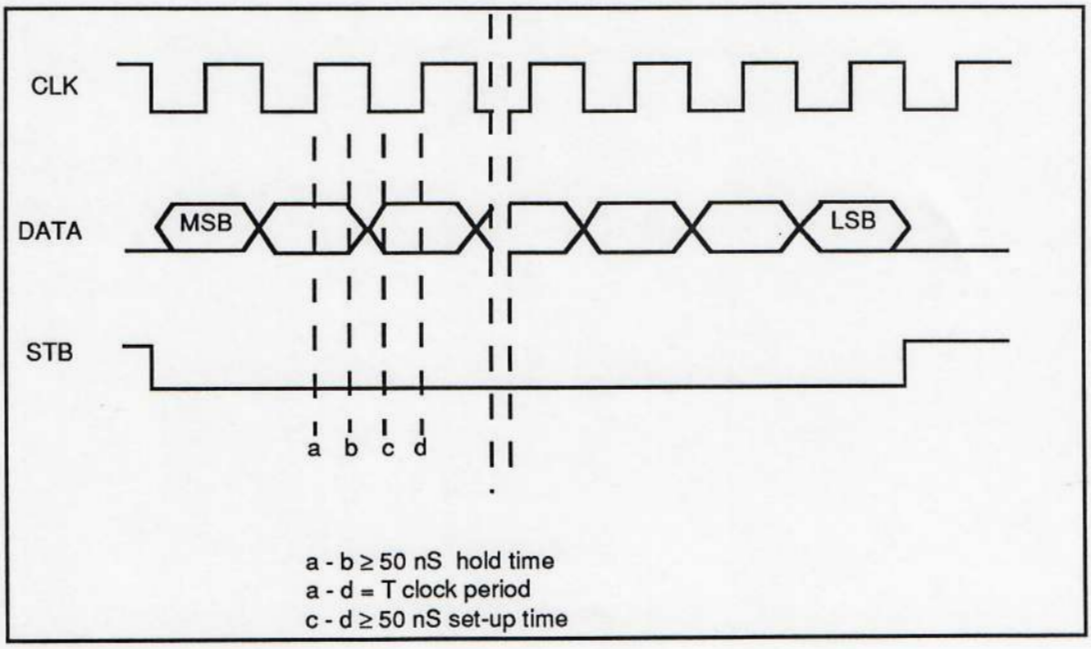


Figure 9 Synchronous Serial Protocol Timing

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Interrupts

All IndustryPack interrupts use a vector. The vector from the IP-BSDI comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $00 which is usually not a valid user vector. The software is responsible for choosing a valid user vector.

In the SCAR mode the interrupt request will be driven on IntReq0 when the strobe is deactivated. The CPU will respond by reading the vector to determine the source of the interrupt. The interrupt mask, interrupt vector, and interrupt service routine all need to be coordinated properly. The interrupt level that the CPU will "see" is determined by the IP Carrier board being used. The interrupt can be disabled or enabled via the BSDI_CNTL register. The enable operates before the holding latch which stores the request for the CPU. If the interrupt request is set then the only method of clearing the request is to reset the board or to service the request with the CPU. Power on initialization will provide a cleared interrupt request register, interrupts disabled, and vector of $00.

The Synchronous mode asserts the interrupt request when STB is activated. The same vector register is used in both protocols.

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-BSDO is constructed out of .062 inch thick FR4 material. The four layers consist of 2 power planes and two signal layers.

Through hole and surface mounting of components is used. IC sockets are screw machined pins, gold plated. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and Gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of .89 W/^{O}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of .31 W/m-^{O}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts is applied uniformly on the component side, that the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

The BSDO design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

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Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to GreenSpring Computers. All replaced products become the sole property of GreenSpring Computers.

GreenSpring Computer's warranty of and liability for defective products is limited to that set forth herein. GreenSpring Computers disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from GreenSpring Computers contact your reseller. Products returned to GreenSpring Computers for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
GreenSpring Computers
1204 O'Brien Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax

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Specifications

Logic Interface:	IndustryPack Logic Interface
Serial Interface:	RS-485 RDY, Data, CLK, STB
ExtCLK rates	generated 2 Mhz., 1 Mhz, 500 Khz, 250 Khz., 125 Khz., 62.5 Khz., 31.25 Khz., and 15.625 Khz.
Parallel Interface:	RS-485 8 parallel data lines plus serial control defined above.
Software Interface:	Control Register ID PROM Vector Register Status Port FIFO
Initialization:	Hardware Reset forces all registers to 0. Software Reset Command Resets the vector, control register, and shift register to 0. Note: The Controlregister being reset causes the interrupt to be disabled, and FIFOs to be reset.
Access Modes:	Word or Byte in I/O Space (see memory map) Word in ID Space Vectored interrupt
Access Time:	125 nanoseconds
Wait States:	Zero
Transfer Time:	8 Mbyte/second continuous
Interrupt:	SCAR mode interrupt at end of transmission Synchronous mode interrupt at start of transmission
DMA:	No Logic Interface DMA Support
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Documentation:	User Manual includes Schematics, PROM Listing, PAL Listings, Theory of Operation, Applications Guide
Dimensions:	Standard Single IndustryPack. 1.8 x 3.9 x .344 (max) inches
Construction:	Conformal Coated FR4 4 Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	.89 W/^{O}C for uniform heat across IP
Power:	Max 220 mA @ 5V

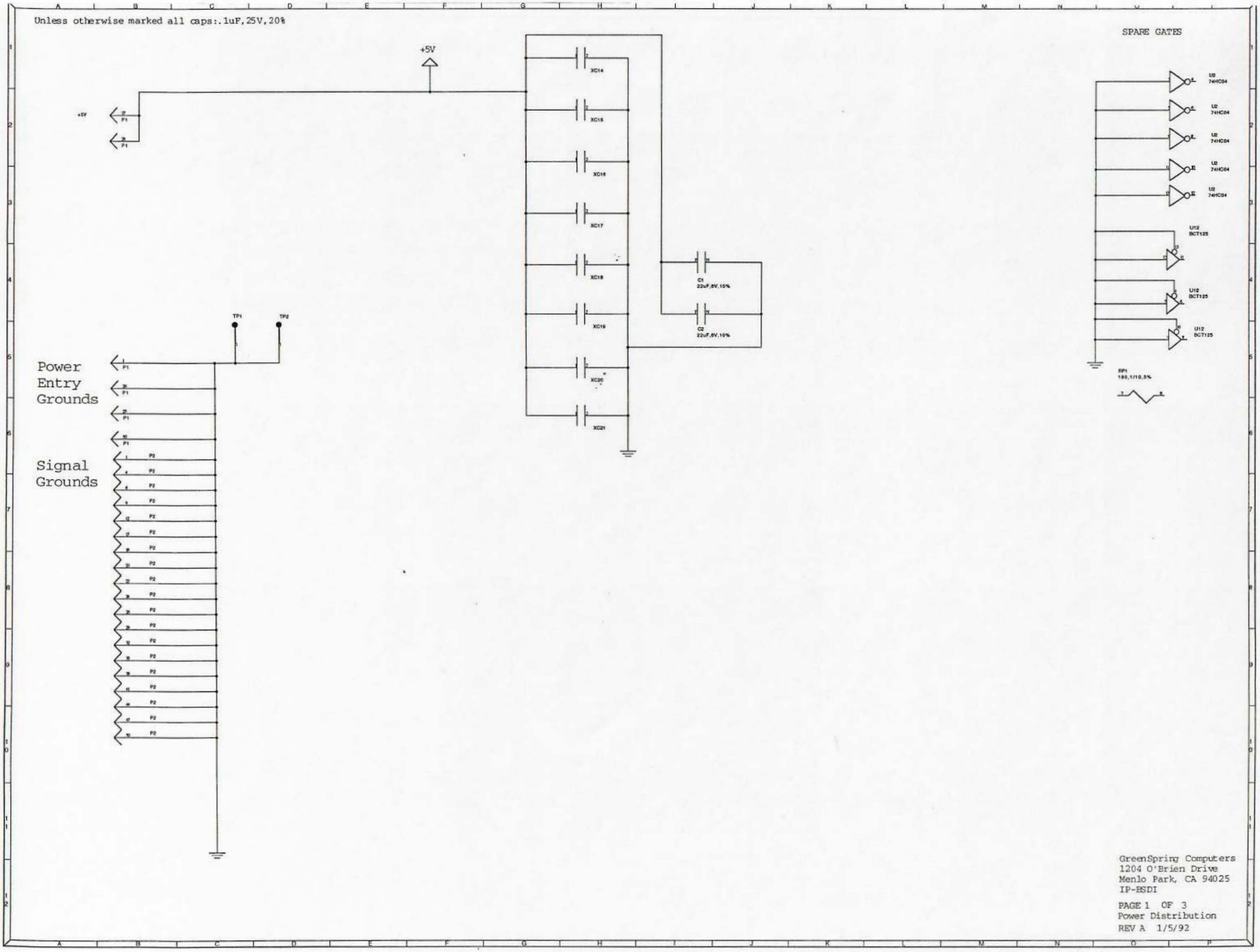
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Schematics

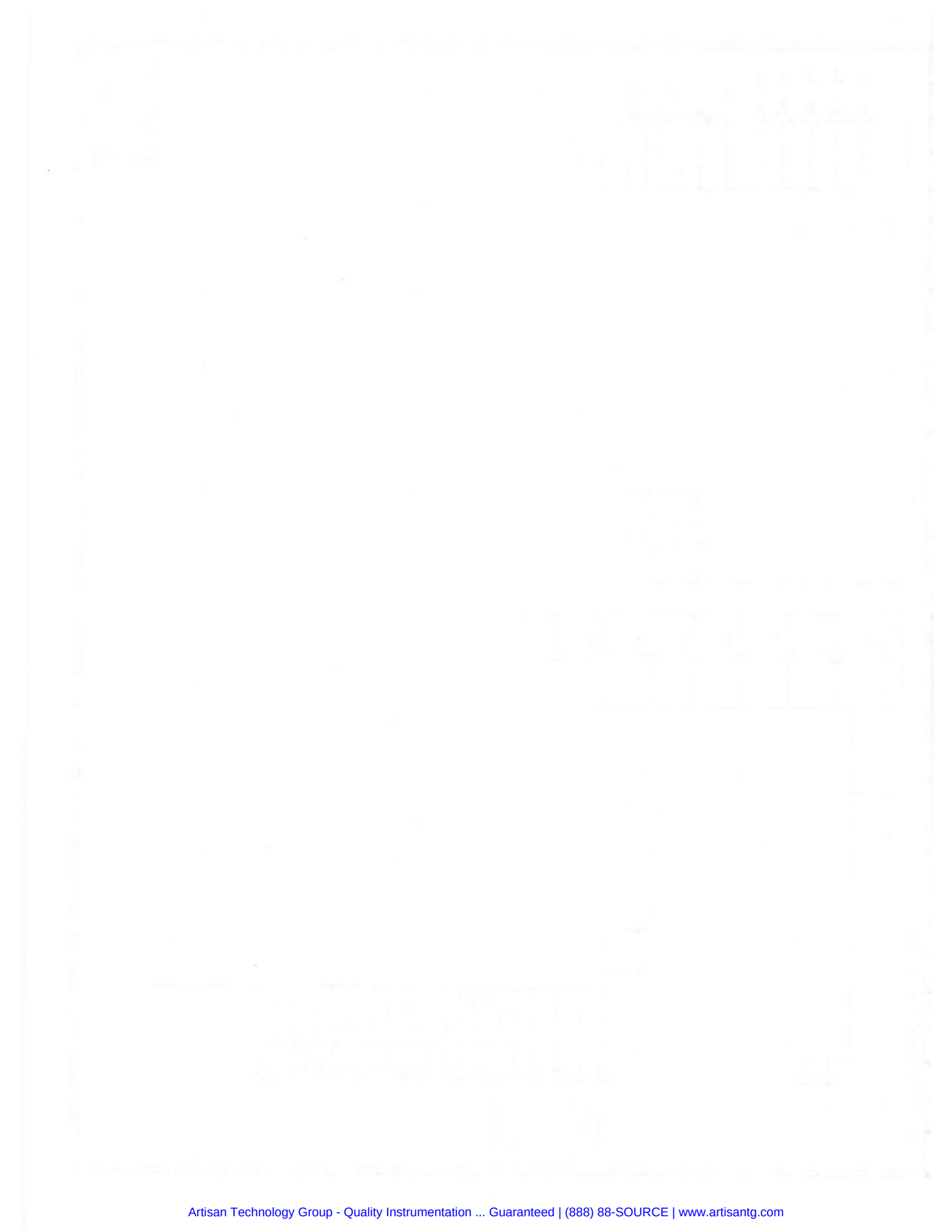
Schematics are provided here for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessary current or complete manufacturing data, nor is it part of the product specification. All information following is Copyright GreenSpring Computers, Inc.

Current manufacturing information, including schematics, programmed device listings, bills-of-material, and assembly diagrams are available from GreenSpring Computers as part of the Engineering Kit option or from your international distributor.

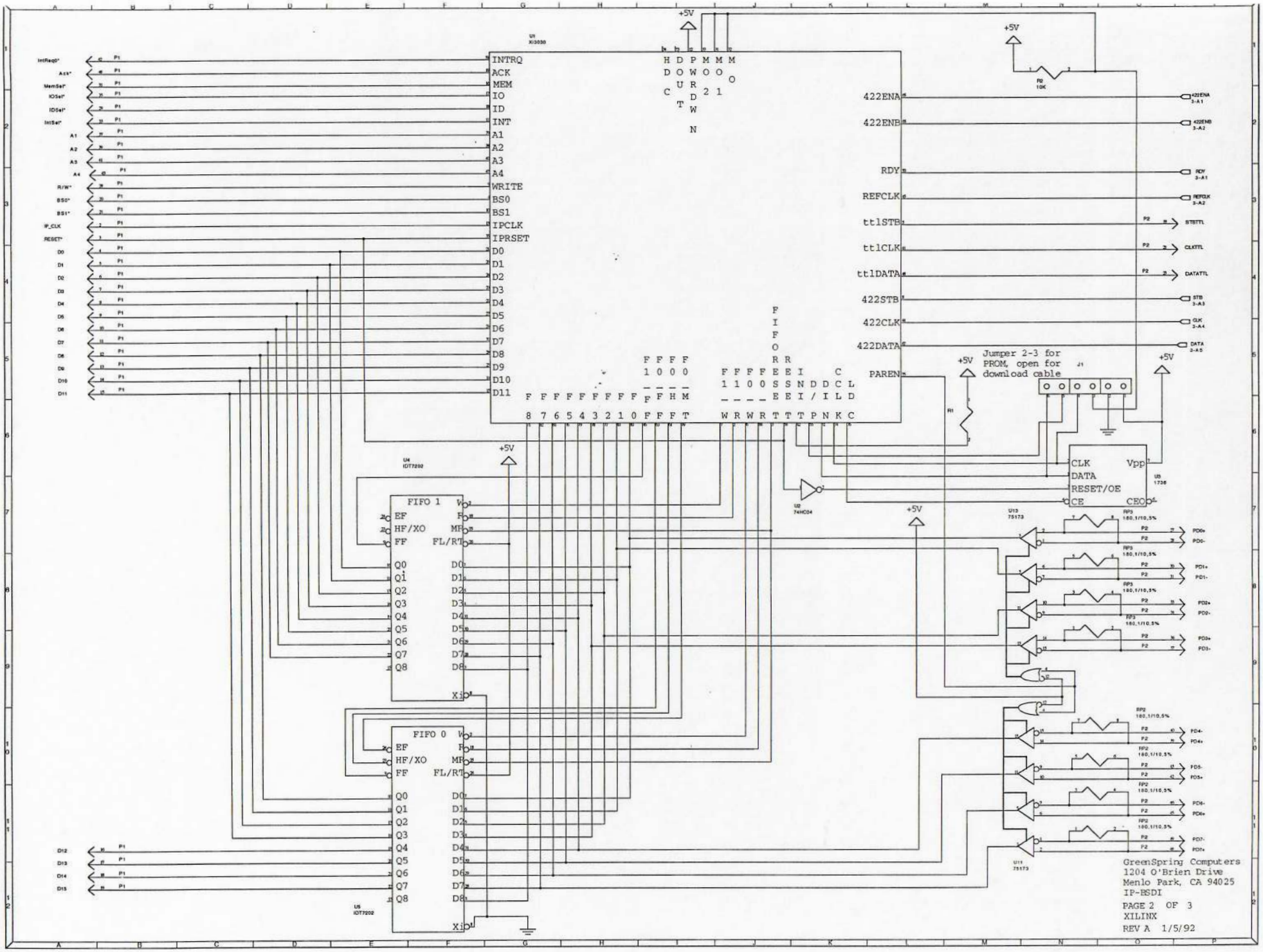
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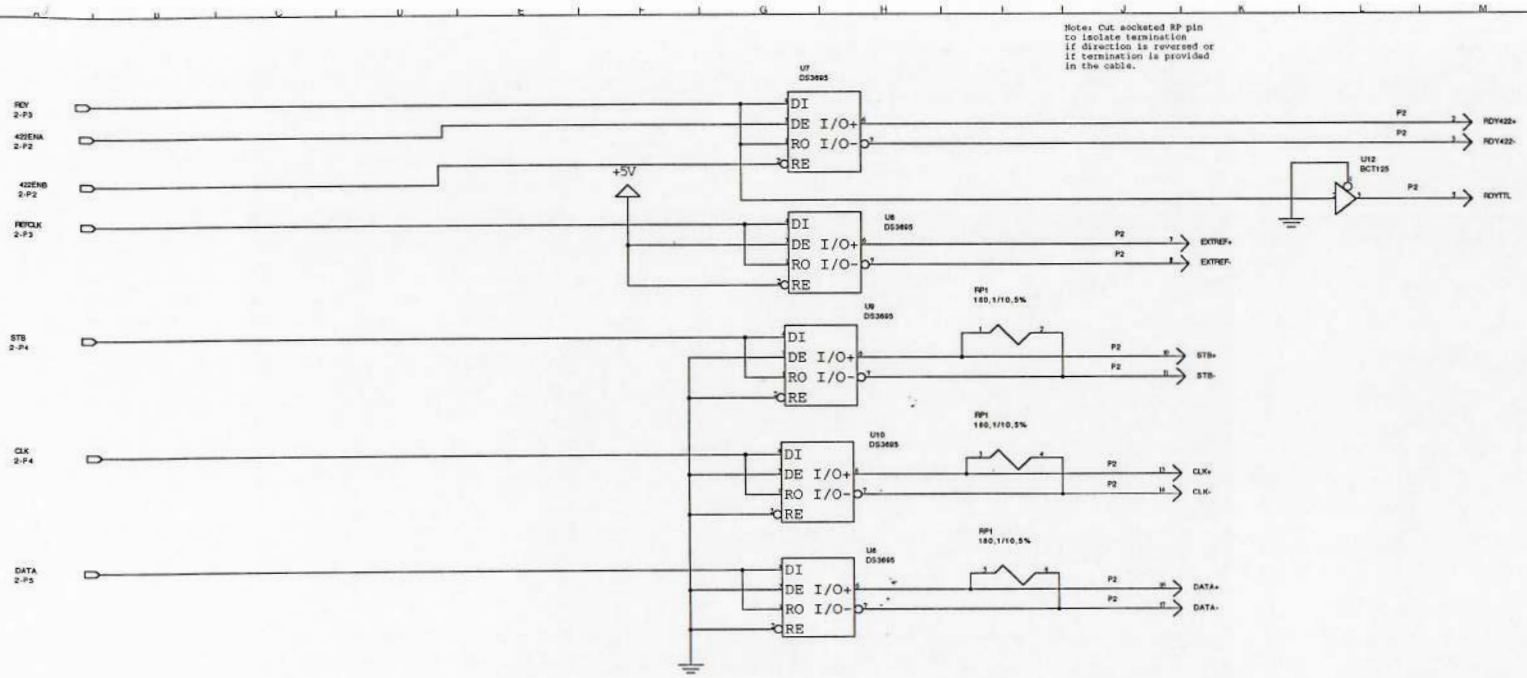
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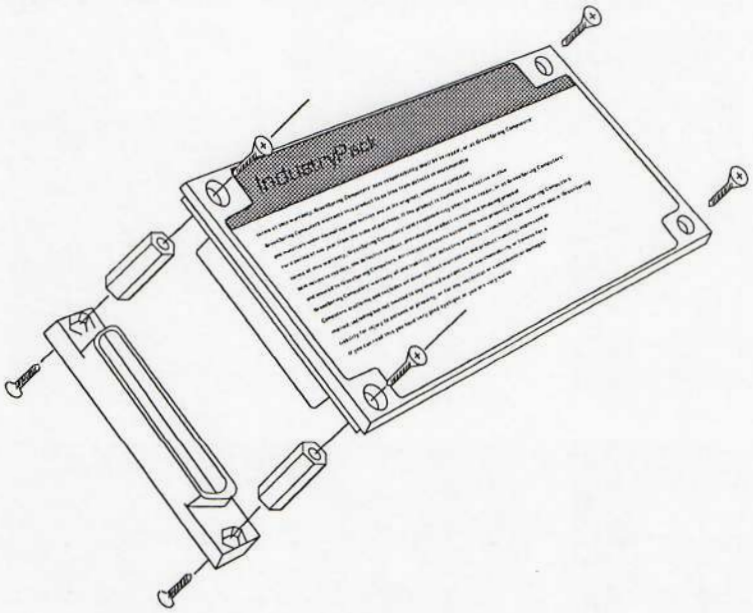
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IndustryPack Hardware Mounting Information



IndustryPack installation instructions

Install the four hex standoffs onto the IndustryPack Connectors. Fasten the standoffs to the IndustryPacks with four M2 x 5mm flat head machine screws. Install the IndustryPack onto the carrier board. Fasten the IndustryPack to the carrier with four M2 x 5mm pan head machine screws.

Please use a thread locking compound on all screws.

IndustryPack installation for non-compliant carriers

Some carrier boards use non-compliant 50 pin connectors. These connectors mate with IndustryPacks but cannot use the standard mounting hardware. A hardware kit for non-compliant carriers is available. The order number is EK-NCC. This must be ordered separately. Contact your local GreenSpring Representative or the factory for price and delivery.

Install the IndustryPack onto the carrier board. Fasten the IndustryPack to the carrier with four M2 x 16mm flat head machine screws and four M2 hex nuts. Use caution when tightening the screws. Too much force may damage the IndustryPack.

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