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GREEN SPRING COMPUTERS

User Manual

IP-BSDO

Buffered Serial Data Output IndustryPack®

Manual Revision: i

Hardware Revision: A

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IP-BSDO

Buffered Serial Data Output
IndustryPack

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Caution:

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Product Description

General

IP-BSDO is part of the IndustryPack family of modular I/O components. It provides two protocols of serial transmission. The transmission protocols currently implemented include Synchronous mode and SCAR mode. The Synchronous mode depends on software protocol for transmission integrity and the SCAR mode utilizes a hardware handshake line. Both protocols are implemented within a Xilinx FPGA for maximum flexibility. Please contact GreenSpring Computers with your custom application.

Both single ended and differential I/O are available on the serial transmission signals. The differential drivers and receivers conform to the RS-485 specification (exceeds RS-422 specification). The RS-485 input signal is terminated with 180Ω. The single ended signals are characterized as open drain drivers with 48 mA of sink. The pull-ups are supplied by the receiving circuit.

All configuration registers support read and write operations for maximum software convenience. Word or byte operations are supported (please refer to the memory map).

The IP-BSDO conforms to the IndustryPack Interface Specification revision .6. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module, with final system implementation on a different one.

The serial channel is supported with a 1K x 16 FIFO. The FIFO supports byte and word writes. A byte wide read back path exists for loopback testing. The Serial channel expects the first byte of data for transmission to be loaded into FIFO_0. The second byte will be read from FIFO_1. When the next FIFO to read from is empty the transmission will terminate.

Several baud rate divisors are selectable. The base rate for the baud rate generator is selectable between the IPCLK and an external source.

An interrupt is supported in the SCAR protocol. The interrupt occurs at the end of the transmission. The vector is user programmable by a read/write register. The interrupt occurs on IntReq0. The FIFO status is available for FIFO_0 making it possible to operate in a polled mode. A status bit is set if the transmission was successful.

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Memory Map

All addresses shown are offsets from the base established by the carrier board.

Function		Offset	width	type
BSDO_STAT	EQU	$00	byte on word boundary	read
BSDO_CNTL	EQU	$02	word	read/write
BSDO_VECTOR	EQU	$04	byte on word boundary	read/write
BSDO_FIFO_0_W	EQU	$06	word or byte	write
BSDO_FIFO_1_W	EQU	$07	byte	write
BSDO_FIFO_0_R	EQU	$07	byte	read
BSDO_FIFO_1_R	EQU	$09	byte	read
BSDO_RESET	EQU	$0E	word	write
BSDO_IDPROM	EQU	$80	byte on word boundary	read

Figure 1 Memory Map

Bitmaps

BSDO_STAT [$00] BSDO Status Port [read only]

Data Bit	Status
0	FIFO_0 EMPTY, 0 = MT
1	FIFO_0 HALF FULL, 0 = HALF FULL +
2	FIFO_0 FULL, 0 = FULL
3	TX_ST, 1 = Good Transmission, auto cleared when read
4	422RDY

Figure 2 BSDO Status Bitmap

BSDO_Vector [$04] BSDO Interrupt Vector Port

The Interrupt vector for the BSDO is stored in this register. The register is a byte wide read/write register which is initialized to 'xx00' upon power-on reset or software reset. The odd byte location [D7..0] is used for the vector. The vector should be initialized before the interrupt is enabled or the mask lowered. The interrupt is autocleared when the CPU reads the vector.

BSDO_FIFO_0_W [$06] BSDO FIFO byte 0 write

The BSDO supports byte and word writes to the data FIFOs. By writing a byte to this address only byte_0 is affected. By writing a word to this address both bytes are loaded. Data is read from FIFO 0 first when transmitting. Data is transmitted MSBit first.

BSDO_FIFO_1_W [$07] BSDO FIFO byte 1 write

The lower byte can be written to through this port.

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BSDO_FIFO_0_R [$07] BSDO FIFO byte 0 read

The data stored into FIFO_0 can be accessed through this port for loop back purposes. The read function competes with the transmission process. This port should not be accessed while a transmission is underway.

BSDO_FIFO_1_R [$09] BSDO FIFO byte 1 read

The data stored into FIFO 1 can be accessed through this port for loop back purposes. The read function competes with the transmission process. This port should not be accessed while a transmission is underway.

BSDO_RESET [$0E] BSDO Reset Port

The user can, by accessing this port, cause the BSDO to reset all major functions. The Control register, Interrupt Vector, FIFO's, and shift register are cleared by this port. Any data pattern can be written.

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BSDO_CNTL [$02] BSDO Control Register Port read/write

DATA BIT	DESCRIPTION
15	UNUSED
14	UNUSED
13	PAREN
12	FIFOEN/FIFORST
11	UNUSED
10	INTEN
9	WID1
8	WID0
7	B2
6	B1
5	B0
4	Ext/Int CLK
3	NORMAL/TEST
2	START/ABORT
1	PROTO1
0	PROTO0

Figure 3 BSDO Control Register Bitmap

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BSDO Control Bitmap

1. PROTO1,0 select SCAR and SYNC protocols. 00 corresponds to SCAR, and 01 to Synchronous mode respectively.

2. All bits are active high and are reset on power-up or reset command.

3. Start/Abort when set high will start a transfer out the serial port. In SCAR mode the transfer is also dependent on RDY being in the correct state.

4. Normal/Test selects which version of RDY to use, the RS422 or the TTL loopback version. Test = TTL Loop-back, and is the power-up condition.

5. INTCLK selects the internally generated baud rate or an external clock divided down. Default is to internal [derived from IPCLK].

6. B2B1B0 are the encoded baud rate selection.

bit pattern	**divisor**
000	1 default = 2 MHz
001	2
010	4
011	8
100	16
101	32
110	64
111	128

7. The WID bits currently serve no function, and are read-writeable.

8. INTEN is the Interrupt enable bit. Default to off. Interrupt is reset on power-up initialization. Interrupt is cleared by CPU vector fetch. Vector from vector port.

9. Bit 11 is unused, and is provided for loopback.

10. FIFO Enable should be high to use the FIFO. When bit 12 is low [default] the FIFOs are held in reset.

11. Parallel Enable is used to enable the parallel port data path, default is to the serial path. [code as 0].

Interrupts

The state machine is used to create an interrupt request when in the SCAR Protocol, the INTEN bit in the control register is set, and the transmission completes. The transmission is considered complete when the strobe line is deactivated. This means that an interrupt is generated when a transmission in the SCAR mode completes with or without error conditions. The status register should be checked as a part of the interrupt service routine to determine if the transmission completed properly. The interrupt is mapped to interrupt request 0. The CPU will respond by asserting INT. The hardware will automatically supply the appropriate interrupt vector and clear the request when accessed by the CPU.

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ID PROM

BSDO_ID_PROM [$80] Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-BSDO is shown below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally the ID PROM space is directly above the IPs I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived by multiplying the address by two and then subtracting one. RM1270 addresses may be derived by multiplying the addresses by two and then adding one.

Address	Data
01	ASCII "I" ($49)
03	ASCII "P" ($50)
05	ASCII "A" ($41)
07	ASCII "C" ($43)
09	Manufacturer ID (F0)
0B	Model Number (30)
0D	Revision (A1)
0F	reserved (00)
11	Driver ID, low byte (00)
13	Driver ID, high byte (00)
15	No of extra bytes used (0C)
17	CRC (54)
19-3F	available for user

Figure 4 ID PROM

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I/O Pin Wiring

This section gives the pin assignments and wiring recommendation for the IP-BSDO.

The pin numbers below correspond to the 50 pin IndustryPack I/O connector, to the wires on a 50 pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP Terminal block.

GND	GND		1	26	
RDY422+	PD0+		2	27	
RDY422-	PD0-		3	28	
GND	GND		4	29	
RDYTTL	PD1+		5	30	
GND	PD1-		6	31	
EXTREF+	GND		7	32	
EXTREF-	PD2+		8	33	
GND	PD2-		9	34	
STB+	GND		10	35	
STB-	PD3+		11	36	
GND	PD3-		12	37	
CLK+	GND		13	38	
CLK-	PD4+		14	39	
GND	PD4-		15	40	
DATA+	GND		16	41	
DATA-	PD5+		17	42	
GND	PD5-		18	43	
STBTTL	GND		19	44	
GND	PD6+		20	45	
CLKTTL	PD6-		21	46	
GND	GND		22	47	
DATATTL	PD7+		23	48	
GND	PD7-		24	49	
N/C	GND		25	50	

Figure 5 BSDO I/O Interface Pin Assignment

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IndustryPack Logic Interface Pin Assignment

The figure below gives the pin assignments for the IndustryPack Logic Interface on the IP-BSDO. Pins marked n/c below are defined by the specification, but not used on the IP-BSDO. See also the User Manual for your carrier board for more information.

GND		GND		1		26	
	CLK		+5V		2		27
Reset*		R/W*		3		28	
	D0		IDSEL*		4		29
D1		n/c		5		30	
	D2		MEMSEL*		6		31
D3		n/c		7		32	
	D4		IntSel*		8		33
D5		n/c		9		34	
	D6		IOSel*		10		35
D7		n/c		11		36	
	D8		A1		12		37
D9		n/c		13		38	
	D10		A2		14		39
D11		n/c		15		40	
	D12		A3		16		41
D13		IntReq0*		17		42	
	D14		A4		18		43
D15		n/c		19		44	
	BS0*		n/c		20		45
BS1*		n/c		21		46	
	n/c		n/c		22		47
n/c		Ack*		23		48	
	+5V		n/c		24		49
GND		Gnd		25		50	

NOTE 1: The no-connect signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

NOTE 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 6 BSDO Logic Interface Pin Assignment

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J1 Pin Assignments

+5V	1	
GND	2	
M00, M01, M02	3	tied to pullup
CCLK	4	
D/P	5	
DIN	6	

Figure 7 Xilinx Programming Connector

To down load, the standard download cable is connected between the parallel port on your PC and the J1 connector on the BSDO. The M00, M01, M02 bits are pulled high to select cable download. Once development is complete pins 2 and 3 should be shorted to select PROM mode. The BSDO is supplied from the factory with pins 2 and 3 connected with a shorting plug.

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Programming

Programming the IP-BSDO requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Support Module. This documentation refers to this address as base.

In order to start a transmission the software is required to first: select the appropriate control register settings, second: load the data and third: begin the transmission. If interrupts are desired then the vector register should also be written to with the desired interrupt vector.

A typical sequence would be to select SCAR mode, Normal Mode, Internal Clock, 2 MHz., Interrupt Enabled, and Serial Drivers by writing to the control register with $1408. Next the software should write to the vector register with the desired vector. For example $40 is a valid user vector for the Motorola 680x0 family. Next the software should load the data pattern to transmit into the FIFO space. For example to send $0123456789, one could MOVE.W $0123 to BSDO_FIFO_0_W, MOVE.W $4567 to BSDO_FIFO_0_W, and MOVE.B $89 to BSDO_FIFO_0_W. The interrupt service routine and mask should be loaded and set. The transmission is now ready to be started by writing $140C to BSDO_CNTL. The transmission will begin immediately if the RDY signal is indicating that the receiver is ready for data. If the ready signal is not indicating that the receiver is ready then the hardware will wait until RDY is asserted before starting.

The end of transmission interrupt will indicate to the software that the message has been started and that the message has terminated. The software needs to look at the TX_ST bit in the BSDO_STAT register to determine if all of the bits were transferred. Reading the status register autoclears the TX_ST bit. It is a good idea to read the status register to force the TX_ST to 0 before a transmission to insure that the TX=1 value the interrupt service routine reads came from the current transmission.

The Synchronous mode is very similar to the SCAR mode in set-up and execution. The key differences are that there is no interrupt associated with the Synchronous mode, the transmitter does not wait for the RDY signal, and the TX_ST bit is set as transmission begins.

Please refer to the Memory Map, Bit Map, and Theory of Operation for more information regarding exact sequencing and interrupt definitions.

Contact GreenSpring Computers for additional assistance.

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Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Watch the system grounds. All electrically connected equipment should have a fail safe common ground that is large enough to handle all current loads without impacting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common source.

Power all system power supplies from one switch. Connecting external voltage to the IP-BSDO when it is unpowered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. Alternatively, the use of OPTO-22 isolation panels should be used.

Keep cables short. Flat cables, even with alternate ground lines, are not suitable for long distances. IP-BSDO does not contain special input protection.

We provide the components. You provide the system. Safety and reliability can be achieved only by careful planning and practice. Inputs can be damaged by static discharge, by applying voltage less than ground or more than +5 volts with the IP powered. With the IP unpowered, driven input voltages should be kept within .7 volts of ground potential.

Terminal Block. We offer a high quality 50 screw terminal block that directly connects to the flat cable. The terminal block mounts on standard DIN rails.

Many flat cable interface products are available from third party vendors to assist you in your system integration and debugging. These include connectors, cable, test points, 'Y's, 50 pin in-line switches, breakout boxes, etc.

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Theory of Operation

Please refer to the board and Xilinx level schematics in the Appendix.

The IP-BSDO is designed for the purpose of transferring data from one point to another in either a serial or parallel protocol. The parallel protocol is not currently implemented within the FPGA.

The BSDO features a Xilinx FPGA. The FPGA contains all of the registers and protocol controlling elements of the BSDO design. Only the drivers, receivers, boot PROM and FIFOs are external to the Xilinx device.

IndustryPack Standards

The IP BSDO is a part of the IndustryPack family of modular I/O products. It meets the IndustryPack Logic Specification revision .6. Contact GreenSpring Computers for a copy of this specification. It is assumed that the reader is at least casually familiar with this document and logic design.

Control Logic

The bus interface to the host CPU is controlled by a logic block within the Xilinx device. The IP_IF contains the decoding and timing elements required to interface to the IP bus interface. The timing is referenced to the 8 MHz. IP logic clock. The IP responds to the ID, INTSEL, IO, and MEM selects. It does not respond to DMA selects.

The IP data bus is brought into the Xilinx device to interface with the registers etc. The Xilinx device doesn't support bidirectional tristate devices. The IO_14 block is used to separate the incoming from the outgoing signals. The IP data bus writes are channeled onto the IDx lines and the IP Data bus reads use the ODx data bus. The IP_IF controls the interface with the OBUFZ signal which controls the output buffer tristate controls.

The BSDO design does not require wait states for read or write cycles to any address. The control PAL generates ACK on the clock cycle following any select. Hold cycles are supported as required by the host processor. Data remains enabled during a read until the host remove the SEL line. Local timing terminates a write cycle prior to the SEL being deasserted. If no hold cycles are requested by the host, the IP-BSDO is capable of supporting the full 8 MB per second data transfer rate of the IP Logic Interface Specification.

ID PROM

The ID PROM is implemented as a pseudo PROM inside the FPGA by programming CLBs with Boolean equations. The IDPROM is controlled via the ID space select and the IP_IF logic block.

For the contents of the ID PROM, see figure ID PROM in the main text. For more information on ID PROMs in general, see the IndustryPack Logic Interface Specification.

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Parallel I/O

The Parallel Output port is supported by a pair of differential drivers directly connected to the FIFO bus. The concept is for the serial lines to be used as control for the parallel data. The serial signals are grouped with three dedicated outputs, one dedicated input and one bi-directional device. The directional control and tristate control originate within the gate array. The Xilinx load map can be modified to implement the protocol in the future without changing the PC board.

Serial I/O

The serial IO supports the SCAR and Synchronous protocols. The protocols are named for the devices the channels were initially interfaced to.

The SCAR interface utilizes the RDY signal as a handshake line for the receiver to hold off transmissions or to abort them in the middle. The timing of the control signals is as shown in the following diagram. The clock is bursted, the data is valid on the rising edge of the clock, the strobe frames the data. The Xilinx device utilizes a logic block to control the timing. A pseudo PAL22V10 is used to allow equation input to the FPGA and to allow ease of modification to the protocol. A listing for the pseudo PAL can be found in the appendix.

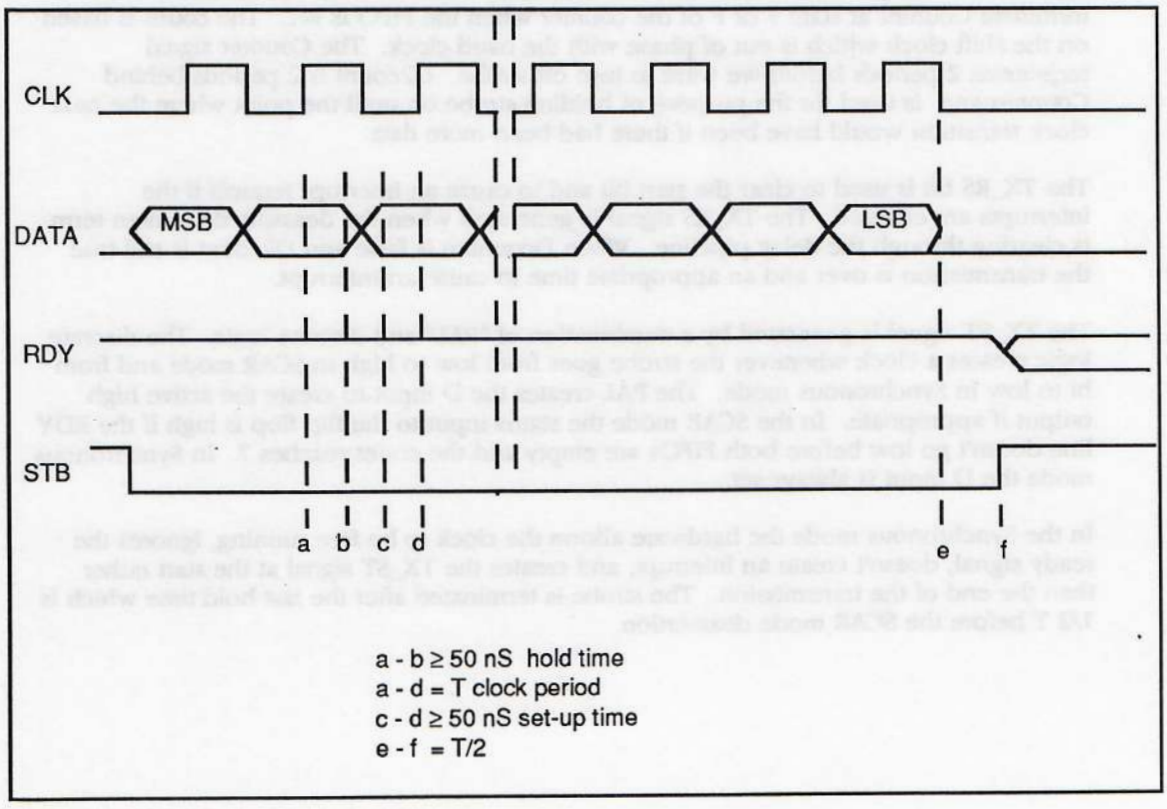


Figure 8 SCAR Serial Protocol Timing

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The state machine which controls the transfer takes care of moving data from the FIFO storage into the shift register at the appropriate times. The state machine uses a 4 bit counter to determine which FIFO should be loaded from, and when. The counter starts at 0 and counts to F before rolling over. The MSB determines which FIFO to load from, and the lower three bits determine when to load the shift register. A special case exists when the start command is issued because the counter is not yet enabled, and the control terms are in transition. The term "start & !counten & !prot1 & !prot0 & rdy & mt_0" provides the initial loading of the shift register by loading when the start signal has been received but the counters are not yet enabled. One clock later the Counten term will turn the special case term off to change from load mode to shift mode. The counters then count the shift clock. The shift clock leads the data clock by one half period. When the lower 3 counter bits reach 0 then it is time to reload the shift register. The FIFO to load from is determined by the counter bit C3. After the initial load the counter is counting from 0 -> 8 -> F ->0. The second load point corresponds to a count of 8. The MSB is set when we point at FIFO_1. The bits are continued to be transmitted and the counters count shift clocks until the counters roll over to 0. Now C3 is pointed at FIFO_0. The process repeats until the FIFO to be read next becomes empty. The Counter signal tests the FIFO MT signal one clock before the SH_LD signal is activated and checks the next FIFO to be used. If the next FIFO is MT then the Counter signal is deasserted and the termination sequence begins.

The strobe is held on for one half clock beyond the last data transition by a delayed version of Counter. Because we do not want to have extra accesses to the FIFOs we terminate Counter at state 7 or F of the counter when the FIFO is MT. The count is based on the shift clock which is out of phase with the baud clock. The Counter signal terminates 2 periods before we want to turn off strobe. D2count is 2 periods behind Counten and is used for the purpose of holding strobe on until the point where the next clock transition would have been if there had been more data.

The TX_RS bit is used to clear the start bit and to cause an interrupt request if the interrupts are enabled. The TX_RS signal is generated when the deasserted counten term is clearing through the delay pipeline. When Dcounten is false and D2count is still true the transmission is over and an appropriate time to cause an interrupt.

The TX_ST signal is generated by a combination of "PAL" and discrete logic. The discrete logic creates a clock whenever the strobe goes from low to high in SCAR mode and from hi to low in Synchronous mode. The PAL creates the D input to create the active high output if appropriate. In the SCAR mode the status input to the flip flop is high if the RDY line doesn't go low before both FIFOs are empty and the count reaches 7. In Synchronous mode the D input is always set.

In the Synchronous mode the hardware allows the clock to be free running, ignores the ready signal, doesn't create an interrupt, and creates the TX_ST signal at the start rather than the end of the transmission. The strobe is terminated after the last hold time which is 1/2 T before the SCAR mode deassertion.

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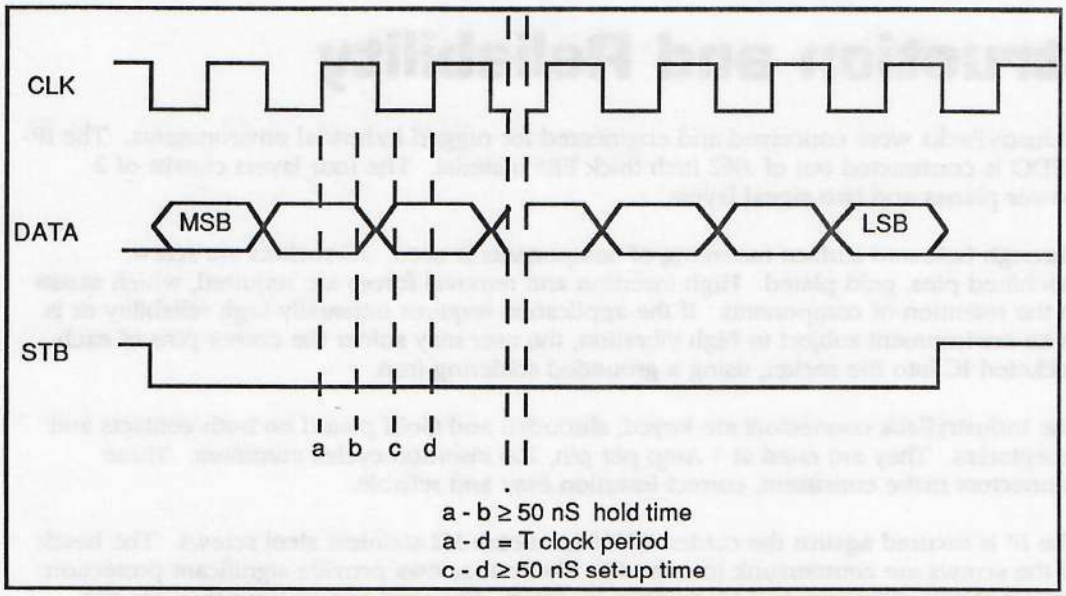


Figure 9 Synchronous Serial Protocol Timing

Interrupts

All IndustryPack interrupts use a vector. The vector from the IP-BSDO comes from a vector register loaded as part of the initialization process. The vector register can be programmed to any 8 bit value. The default value is $00 which is usually not a valid user vector. The software is responsible for choosing a valid user vector.

In the SCAR mode the interrupt request will be driven on IntReq0 when the strobe is deactivated. The CPU will respond by reading the vector to determine the source of the interrupt. The interrupt mask, interrupt vector, and interrupt service routine all need to be coordinated properly. The interrupt level that the CPU will "see" is determined by the IP Carrier board being used. The interrupt can be disabled or enabled via the BSDO_CNTL register. The enable operates before the holding latch which stores the request for the CPU. If the interrupt request is set then the only method of clearing the request is to reset the board or to service the request with the CPU. Power on initialization will provide a cleared interrupt request register, interrupts disabled, and vector of $00.

The Synchronous mode does not have an interrupt capability.

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-BSDO is constructed out of .062 inch thick FR4 material. The four layers consist of 2 power planes and two signal layers.

Through hole and surface mounting of components is used. IC sockets are screw machined pins, gold plated. High insertion and removal forces are required, which assists in the retention of components. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and Gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured against the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of .89 W/^{O}C for uniform heat. This is based upon the temperature coefficient of the base FR4 material of .31 W/m-^{O}C, and taking into account the thickness and area of the IP. The coefficient means that if .89 Watts is applied uniformly on the component side, that the temperature difference between the component side and solder side is one degree Celsius.

Thermal Considerations

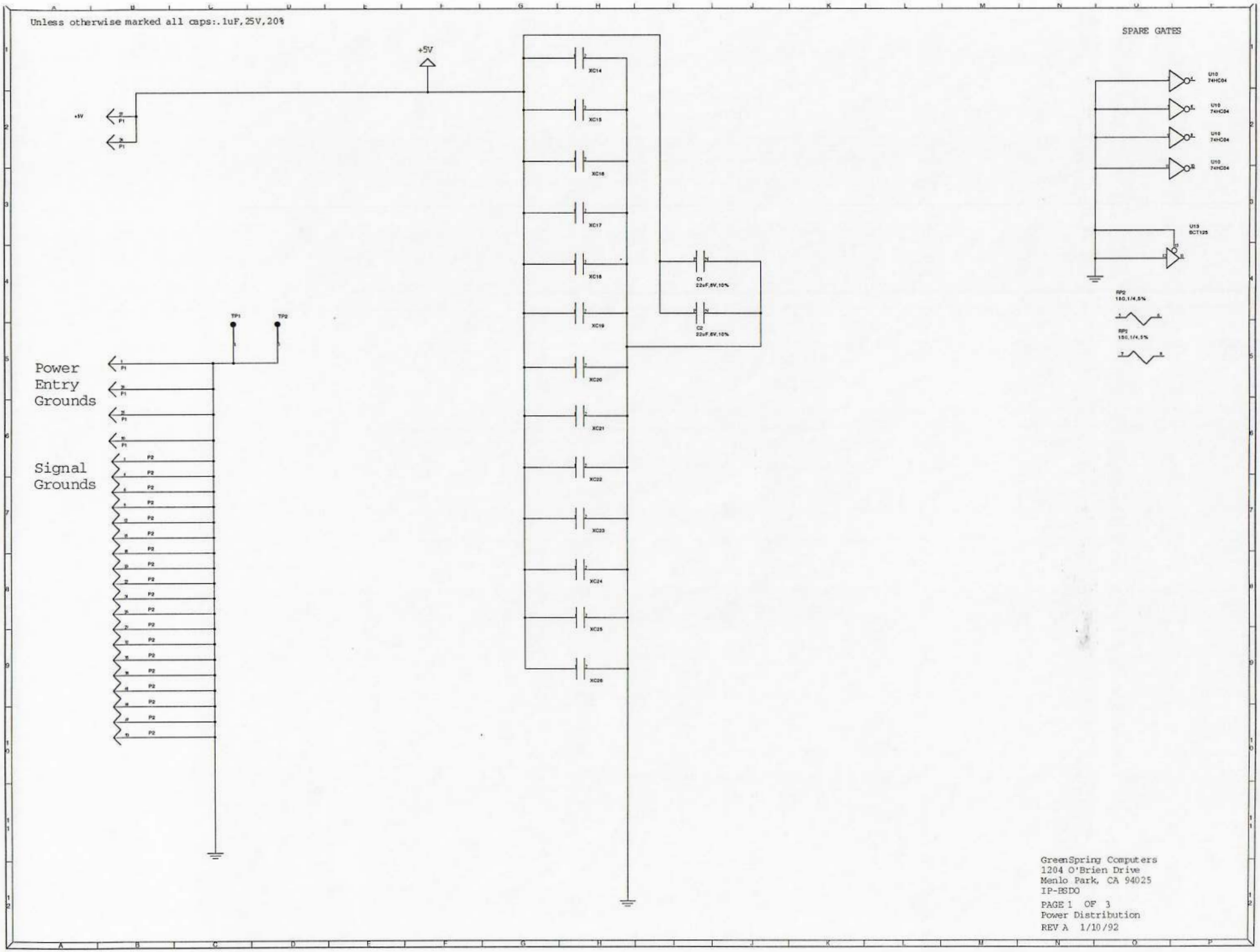
The BSDO design consists of CMOS circuits. The power dissipation due to internal circuitry is very low. It is possible to create a higher power dissipation with the externally connected logic. If more than one a Watt is required to be dissipated due to external loading then forced air cooling is recommended. With the one degree differential temperature to the solder side of the board external cooling is easily accomplished.

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Specifications

Logic Interface:	IndustryPack Logic Interface
Serial Interface:	RS-485 RDY, Data, Clk, Stb, ExtClk 2 Mhz., 1 Mhz, 500 Khz, 250 Khz., 125 Khz., 62.5 Khz., 31.25 Khz., and 15.625 Khz. transmission frequencies are internally generated. User supplied ExtClk can be selected for other transmission rates.
Parallel Interface:	RS-485 8 parallel data lines plus serial control defined above.
Software Interface:	Control Register ID PROM Vector Register Status Port FIFO
Initialization:	Hardware Reset forces all registers to 0. Software Reset Command Resets the vector, control register, and shift register to 0. Note: The Control register being reset causes the interrupt to be disabled, and FIFOs to be reset.
Access Modes:	Word or Byte in I/O Space (see memory map) Word in ID Space Vectored interrupt
Access Time:	125 nanoseconds
Wait States:	Zero
Transfer Time:	8 Mbyte/second continuous
Interrupt:	SCAR mode interrupt at end of transmission Synchronous mode has no interrupt
DMA:	No Logic Interface DMA Support
Onboard Options:	All Options are Software Programmable
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Documentation:	User Manual includes Schematics, PROM Listing, PAL Listings, Theory of Operation, Applications Guide
Dimensions:	Standard Single IndustryPack: 1.8 x 3.9 x .344 (max) inches
Construction:	Conformal Coated FR4 4 Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	.89 W/^{o}C for uniform heat across IP
Power:	Max 300 mA @ 5V

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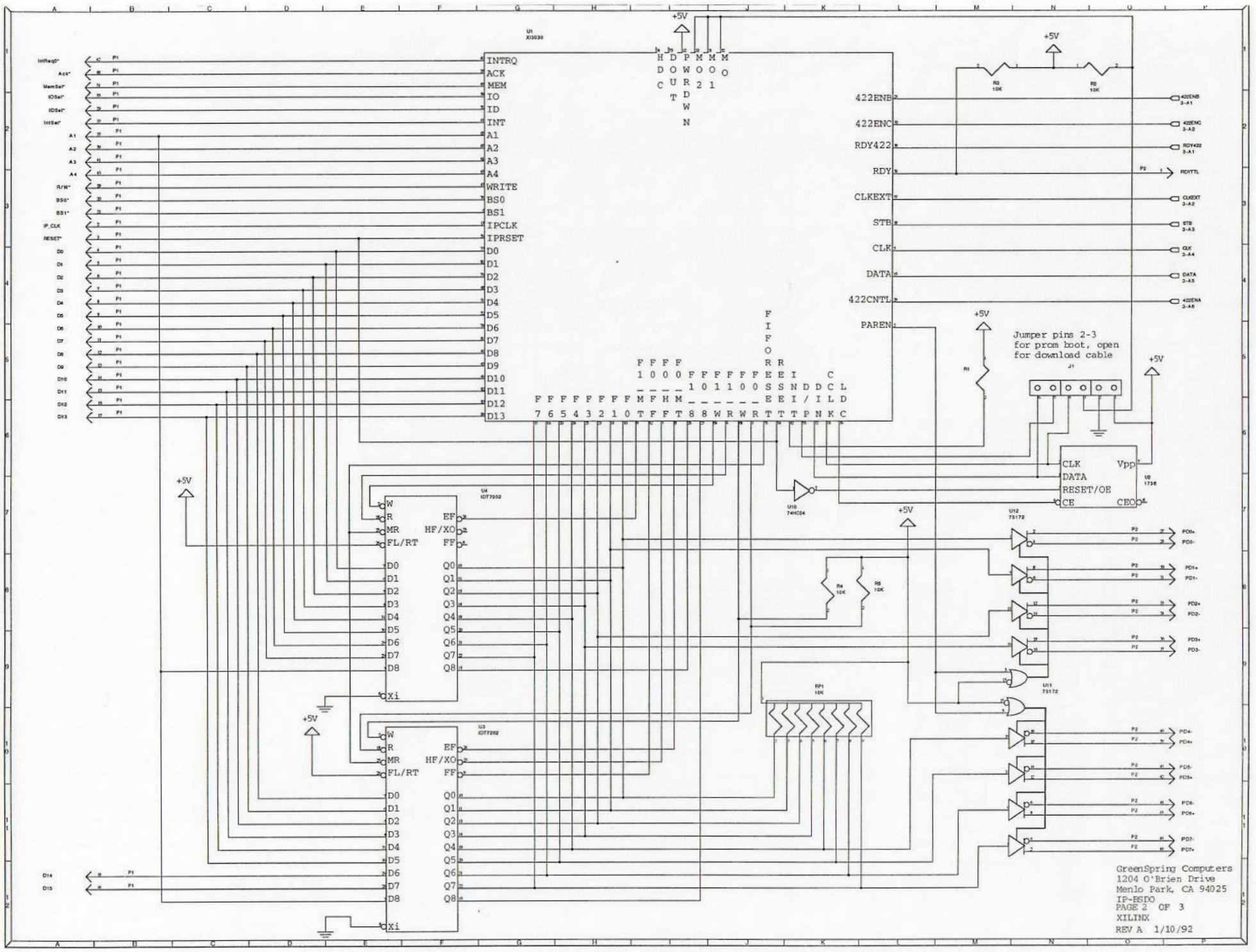


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IP-BSDO

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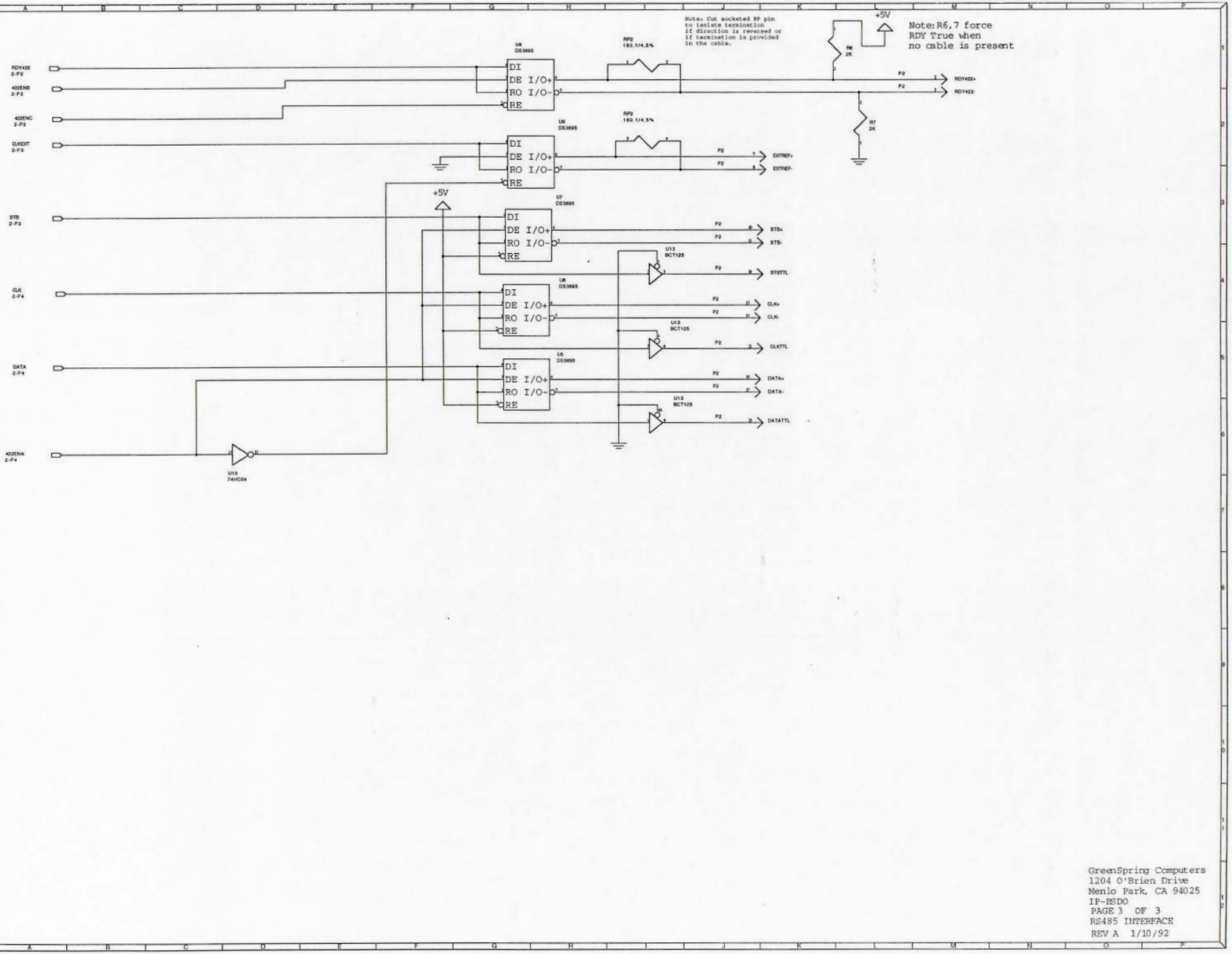
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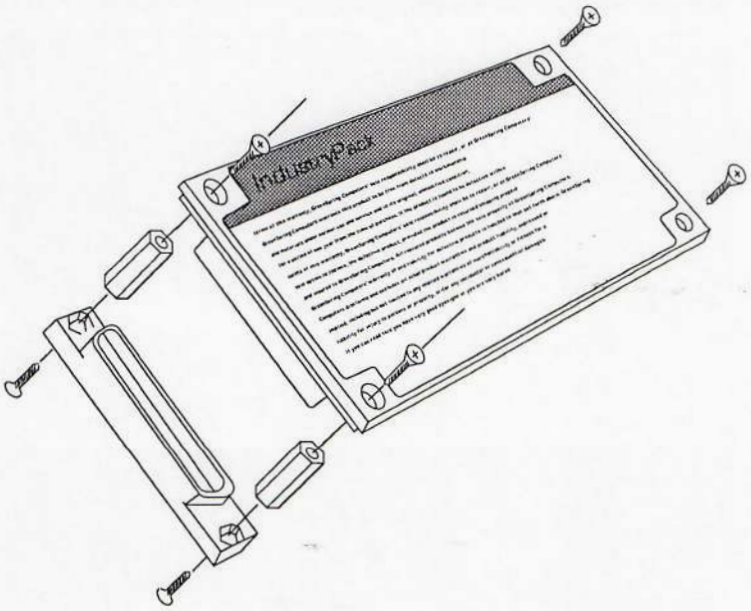


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IndustryPack Hardware Mounting Information



IndustryPack installation instructions

Install the four hex standoffs onto the IndustryPack Connectors. Fasten the standoffs to the IndustryPacks with four M2 x 5mm flat head machine screws. Install the IndustryPack onto the carrier board. Fasten the IndustryPack to the carrier with four M2 x 5mm pan head machine screws.

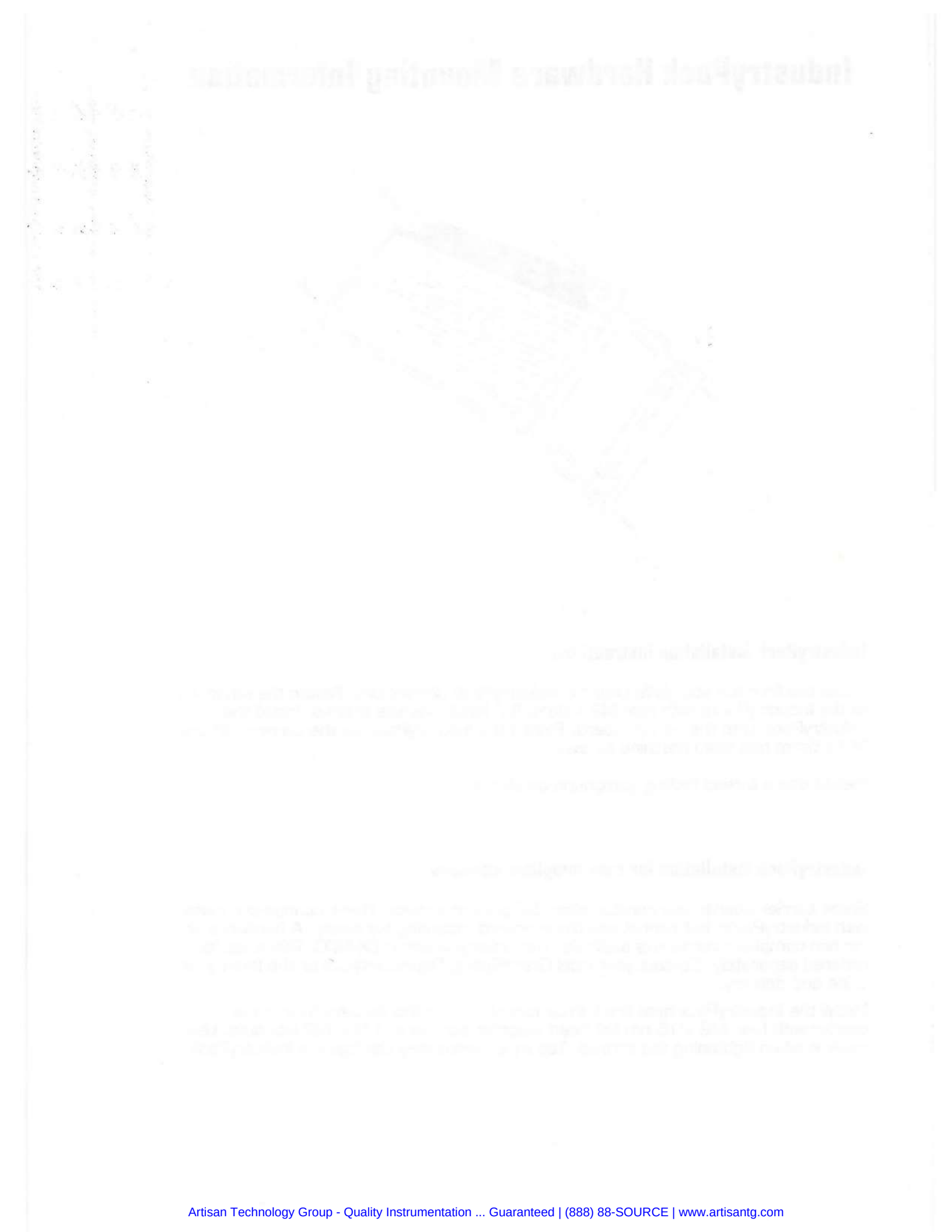
Please use a thread locking compound on all screws.

IndustryPack installation for non-compliant carriers

Some carrier boards use non-compliant 50 pin connectors. These connectors mate with IndustryPacks but cannot use the standard mounting hardware. A hardware kit for non-compliant carriers is available. The order number is EK-NCC. This must be ordered separately. Contact your local GreenSpring Representative or the factory for price and delivery.

Install the IndustryPack onto the carrier board. Fasten the IndustryPack to the carrier with four M2 x 16mm flat head machine screws and four M2 hex nuts. Use caution when tightening the screws. Too much force may damage the IndustryPack.

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