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IP-Dual PI/T
IP-Digital 48

Dual Programmable Interface/Timer
48 Line Digital Interface
IndustryPacks®

User's Manual

Revision x
Corresponding Hardware: Revision A2

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This product has been designed to operate with IndustryPack carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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ICs. These popular interface components often go by the acronym PI/T, pronounced “pit.”

The PI/T has many programmable features, such as double buffered input or output, hardware handshake lines, 8 or 16-bit wide external data transfer, edge or level sensitive interrupt generation, and a 24-bit timer. In the simplest case, the part provides up to 24 lines of bit I/O.

The IP-Dual PI/T is configured to take advantage of the more sophisticated features of the PI/Ts. Timer I/O, interrupts, DMA, and hardware mediated double-buffered data transfer are supported. 32 general purpose digital I/O lines are available in several programmable modes.

The IP-Digital 48 is configured to maximize the number of digital I/O lines. Multiple modes are available via programming.

Users may reconfigure either IndustryPack to implement desired features, while maximizing the number of available I/O lines.

Each 68230 provides up to three 8-bit I/O ports, one 24-bit timer, five separate interrupt vectors, and independent DMA capability. Ports may be software configured for bit I/O, unidirectional 8-bit and 16-bit I/O, or bi-directional 8-bit and 16-bit I/O. Port modes include single and double buffering, with strobe and handshake options. Due to pin limitations, not all options are available simultaneously.

The IP-Dual PI/T and IP-Digital 48, like all IndustryPacks, use a 50-pin flat ribbon cable connected to the carrier board for I/O. The IP-Dual PI/T configuration uses 32 lines for bit I/O, 8-bit or 16-bit (unidirectional, bi-directional, single or double buffered) plus 8 lines as programmable handshake lines or timer I/O with alternate ground wires.

IP-Digital 48 is configured for 48 general purpose lines of bit I/O. These lines may also be used for 8-bit and 16-bit I/O with handshake lines. Timer I/O is also available. In this configuration 48 of the 50 cable lines are I/O, with 2 ground lines. User provided cabling with additional grounds may be required for high speed operation in this configuration. Interrupts and DMA are unavailable if all 48 lines are used for I/O.

IP-Dual PI/T and IP-Digital 48 connect user I/O lines directly to the NMOS 68230. Inputs and outputs are TTL and CMOS compatible. Source current is 100 μA @ 2.4 V. Sink current is 2.4 mA. Input and leakage current is 10 μA.

Each of the two 68230s has a 24-bit programmable timer. Timer clock source is a 250 KHz internal clock or a user provided external clock. Using the internal clock, a resolution of 4 μS with a maximum time of 64 seconds is available. The timer may be used as a counter, watchdog, or square wave generator. It may generate single or periodic interrupts. An external gate signal as well as an external timer output are available. In general, it is easier to use the timers starting from an IP-Digital 48 configuration than from an IP-Dual PI/T configuration.

20 pin-programmable on-board jumper-wire groups provide a wide range of configurations. Most common configuration changes, such as port modes, loading interrupt vectors, and setting I/O direction are done by programming the 68230s.

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which is standard for 68000 family peripheral chips. Figure 1 shows the base address of the X and Y 68230. See the next sections for Nubus and ISA bus addressing.

Address	68230
base + $00	X 68230
base + $40	Y 68230

Note: All accesses are byte wide, using odd address.

Figure 1 VMEbus Address Map

Complete register addresses consist of the sum of the carrier board's base address, any offset due to the Pack location on the carrier board, the X or Y offset shown in Figure 1, and the register address. Register Address for the VMEbus are shown in Figure 2. See the next section for Nubus addressing. More information on programming the 68230 is given in the MC68230 Parallel Interface Timer Data Sheet available in GreenSpring's Engineering Kit or from Motorola.

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0F	X	Port B Control Register
11	X	Port A Data Register
13	X	Port B Data Register
15	X	Port A Alternate Register
17	X	Port B Alternate Register
19	X	Port C Data Register
1B	X	Port Status Register
21	X	Timer Control Register
23	X	Timer Interrupt Vector Register
27	X	Counter Preload Register (High)
29	X	Counter Preload Register (Med)
2B	X	Counter Preload Register (Low)
2F	X	Count Register (High)
31	X	Count Register (Med)
33	X	Count Register (Low)
35	X	Timer Status Register
41	Y	Port General Control Register
43	Y	Port Service Request Register
45	Y	Port A Data Direction Register
47	Y	Port B Data Direction Register
49	Y	Port C Data Direction Register
4B	Y	Port Interrupt Vector Register
4D	Y	Port A Control Register
4F	Y	Port B Control Register
51	Y	Port A Data Register
53	Y	Port B Data Register
55	Y	Port A Alternate Register
57	Y	Port B Alternate Register
59	Y	Port C Data Register
5B	Y	Port Status Register
61	Y	Timer Control Register
63	Y	Timer Interrupt Vector Register
67	Y	Counter Preload Register (High)
69	Y	Counter Preload Register (Med)
6B	Y	Counter Preload Register (Low)
6F	Y	Count Register (High)
71	Y	Count Register (Med)
73	Y	Count Register (Low)
75	Y	Timer Status Register

Figure 2 VMEbus Register Map

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the Nubus. Since the Nubus uses only 32-bit wide accesses, byte peripherals such as the 68230 appear in the host address space every four bytes. See the previous section for VMEbus addressing and the next section for ISA bus addressing.

Address	68230
base + $00	X 68230
base + $80	Y 68230

Note: All accesses are byte wide, using odd address.

Figure 3 NuBus Address Map

Complete register addresses consist of the sum of the carrier board's base address, any offset due to the Pack location on the carrier board, the X or Y offset shown in Figure 3, and the register address. Register Address for the NuBus are shown in Figure 4. See the previous section for VMEbus addressing. More information on programming the 68230 is given in the MC68230 Parallel Interface Timer Data Sheet available in GreenSpring's Engineering Kit or from Motorola.

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19	1B	X	Port A Control Register
1D	1F	X	Port B Control Register
21	23	X	Port A Data Register
25	27	X	Port B Data Register
29	2B	X	Port A Alternate Register
2D	2F	X	Port B Alternate Register
31	33	X	Port C Data Register
35	37	X	Port Status Register
41	43	X	Timer Control Register
45	47	X	Timer Interrupt Vector Register
4D	4F	X	Counter Preload Register (High)
51	53	X	Counter Preload Register (Med)
55	57	X	Counter Preload Register (Low)
5D	5F	X	Count Register (High)
61	63	X	Count Register (Med)
65	67	X	Count Register (Low)
69	6B	X	Timer Status Register
81	83	Y	Port General Control Register
85	87	Y	Port Service Request Register
89	8B	Y	Port A Data Direction Register
8D	8F	Y	Port B Data Direction Register
91	93	Y	Port C Data Direction Register
95	97	Y	Port Interrupt Vector Register
99	9B	Y	Port A Control Register
9D	9F	Y	Port B Control Register
A1	A3	Y	Port A Data Register
A5	A7	Y	Port B Data Register
A9	AB	Y	Port A Alternate Register
AD	AF	Y	Port B Alternate Register
B1	B3	Y	Port C Data Register
B5	B7	Y	Port Status Register
C1	C3	Y	Timer Control Register
C5	C7	Y	Timer Interrupt Vector Register
C9	CB	Y	Counter Preload Register (High)
CD	CF	Y	Counter Preload Register (Med)
D1	D3	Y	Counter Preload Register (Low)
DD	DF	Y	Count Register (High)
E1	E3	Y	Count Register (Med)
E5	E7	Y	Count Register (Low)
E9	EB	Y	Timer Status Register

Figure 4 NuBus Register Map

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host architectures, and odd for Motorola 68K host architectures. Figure 5 shows the base address of the X and Y 68230. See the previous sections for VMEbus and Nubus addressing.

Address	68230
base + $00	X 68230
base + $40	Y 68230

Note: All accesses are byte wide, using odd address.

Figure 5 ISA bus Address Map

Complete register addresses consist of the sum of the carrier board's base address, any offset due to the Pack location on the carrier board, the X or Y offset shown in Figure 5, and the register address. Even Register Address for Intel family host architectures using the ISA bus are shown in Figure 6. See the previous sections for VMEbus and Nubus addressing. More information on programming the 68230 is given in the MC68230 Parallel Interface Timer Data Sheet available in GreenSpring's Engineering Kit or from Motorola.

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0E	X	Port B Control Register
10	X	Port A Data Register
12	X	Port B Data Register
14	X	Port A Alternate Register
16	X	Port B Alternate Register
18	X	Port C Data Register
1A	X	Port Status Register
20	X	Timer Control Register
22	X	Timer Interrupt Vector Register
26	X	Counter Preload Register (High)
28	X	Counter Preload Register (Med)
2A	X	Counter Preload Register (Low)
2E	X	Count Register (High)
30	X	Count Register (Med)
32	X	Count Register (Low)
34	X	Timer Status Register
40	Y	Port General Control Register
42	Y	Port Service Request Register
44	Y	Port A Data Direction Register
46	Y	Port B Data Direction Register
48	Y	Port C Data Direction Register
4A	Y	Port Interrupt Vector Register
4C	Y	Port A Control Register
4E	Y	Port B Control Register
50	Y	Port A Data Register
52	Y	Port B Data Register
54	Y	Port A Alternate Register
56	Y	Port B Alternate Register
58	Y	Port C Data Register
5A	Y	Port Status Register
60	Y	Timer Control Register
62	Y	Timer Interrupt Vector Register
66	Y	Counter Preload Register (High)
68	Y	Counter Preload Register (Med)
6A	Y	Counter Preload Register (Low)
6E	Y	Count Register (High)
70	Y	Count Register (Med)
72	Y	Count Register (Low)
74	Y	Timer Status Register

Figure 6 ISA bus Register Map

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Standard data in the ID PROM on the IP-Dual PI/T and IP-Digital 48 is shown in Figure 7 below. Note that the Product ID is $23 for IP-Dual PI/T and $24 for IP-Digital 48. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 7 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

The ID PROM used is an AMD 27LS19A. or equivalent

3F 19	(available for user)	
17	CRC IP-Dual PI/T CRC IP-Digital 48	(4D) (09)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(A2)
0B	Model No IP-Dual PI/T Model No IP-Digital 48	(23) (24)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 7 ID PROM Data (hex)

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Note that the X and Y 68230s are wired nearly symmetrically. That is, the X PI/T uses the first 25 lines of the I/O cable, and the Y PI/T uses the last 25 lines. Within each group of 25 lines the pin usage is almost the same (factory default). The X PI/T has some shunt options involving its timer. See the User Options section below for more details.

Note that special customer configurations may change this default wiring symmetry.

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8	X	PA7	PA7
9	X	PB0	PB0
10	X	PB1	PB1
11	X	PB2	PB2
12	X	PB3	PB3
13	X	PB4	PB4
14	X	PB5	PB5
15	X	PB6	PB6
16	X	PB7	PB7
17	X	GND	PC0
18	X	H1	PC4
19	X	GND	PC1
20	X	H2	PC5
21	X	GND	PC2/TIN
22	X	H3	PC6
23	X	GND	PC3/TOUT
24	X	H4	PC7
25		GND	GND
26	Y	PA0	PA0
27	Y	PA1	PA1
28	Y	PA2	PA2
29	Y	PA3	PA3
30	Y	PA4	PA4
31	Y	PA5	PA5
32	Y	PA6	PA6
33	Y	PA7	PA7
34	Y	PB0	PB0
35	Y	PB1	PB1
36	Y	PB2	PB2
37	Y	PB3	PB3
38	Y	PB4	PB4
39	Y	PB5	PB5
40	Y	PB6	PB6
41	Y	PB7	PB7
42	Y	GND	PC0
43	Y	H1	PC4
44	Y	GND	PC1
45	Y	H2	PC5
46	Y	GND	PC2/TIN
47	Y	H3	PC6
48	Y	GND	PC3/TOUT
49	Y	H4	PC7
50		GND	GND

Figure 8 I/O Pin Numbering

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The 68230 is an NMOS device. As such it should never have a voltage applied to any pin outside the range of its own power pins. Note that if the IndustryPack is unpowered, then no input should have a driven voltage on it. NMOS devices should not, in general, have any inputs left floating. Unused inputs should either be programmed as outputs or connected to GND. Unused input will not float to a known level.

NMOS output have minimal current drive. See the Specification section or the 68230 data sheet for details. Since there are typically few ground lines on the IP-Digital 48 I/O cable, this low current drive is an advantage, since it reduces cross talk on output lines. (It is the resulting slow rise and fall times that reduces cross talk..)

Flat cables have surprisingly large capacitance and hence crosstalk. Systems integrators should note that unless the flat cable portion of the system wiring is kept very short, that fast edges (either input or output) are likely to show up on adjacent lines.

When moving data between systems it is common to have a group of data lines—usually eight or 16—and a clock line. The IP-Dual PI/T supports this mode effectively. The 68230 has programmable modes for double buffered input and output, eight or 16 bits wide, with hardware handshake clock lines of programmable polarity. The default IP-Dual PI/T cabling has alternate ground lines next to all the handshake and clock lines. This wiring allows flat cable to be used for high speed data transfer at reasonable distances. The systems integrator should connect the ground lines at the external end of the cable for best noise immunity.

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this document. Wire jumpers E5 through E12 are located under the Y 68230 (closest to the edge of the IP). Wire jumpers E13 through E20 are located under the X 68230 (closest to the center of the IP).

Pin one on all shunt headers and wire jumpers is marked on the board, top and bottom, with a square pad.

Changing wire jumpers requires removing the 68230 from its socket. Work on a grounded, static free work surface. Place the 68230 in conductive foam when it is not installed in the IndustryPack. Changing wire jumpers requires 28 gauge tinned solid wire, cutters, fine nose pliers and a grounded soldering iron. Removing the label on the rear of the IP is not required. If it is removed, replacement labels are available from GreenSpring Computers.

Special configurations of shunts and jumpers are available from GreenSpring Computers at no change for orders of 25 or more IndustryPacks. A customer configuration number is assigned and a drawing generated. Use of this configuration number on future orders assures consistent product configuration and minimum user handling. GreenSpring computers encourages all customers who change the configuration from the factory default on any IndustryPacks to ask for a customer configuration number.

Interrupts

Each IndustryPack can generate up to two interrupt requests. These are called IRQ0 and IRQ1. The carrier board maps these IP interrupt requests into the available interrupt levels on the host bus. See your carrier board User Manual for more information.

The X 68230 uses the IRQ0 line. The Y 68230 uses the IRQ1 line. This can be changed, if necessary, by reprogramming the PAL at location U3 on the IndustryPack.

Two shunts are used to assist in interrupt configuration. The interrupt vector and most interrupt options are programmed in the 68230s

In each 68230, the data transfer section (the “interface” portion) is distinct from the timer section. Shunt E1 determines which of these two sections has priority if both are requesting service. Note that the two sections typically have distinct vectors, but share an interrupt level. See Figure 9 below.

Timer highest priority	E1 IN	**Default**
Interface highest priority	E1 OUT	

Figure 9 Interrupt Priority

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Strobe

The IndustryPack Logic Specification defines a pin on the interface called Strobe (pin 46). The Strobe line is used to input or output special clocks, for example to set the sample rate on the IP-Precision ADC. Some carrier board provide for shunt or programmable Strobe functions.

The IP-Dual PI/T and IP-Digital 48 may use the Strobe as clock input or output. The Timer in the X 68230 is used for Strobe functions. See Figure 11 below for configuration options. TIN is Timer IN. TOUT is Timer OUT. See Jumper Options, later in this section for E19 and E20 usage.

Shunts	Function	Default
E3-1 to E3-2 E3-2 to E3-3	X–PC3/TOUT to E19 Strobe to X–TOUT	**Default**
E4-1 to E4-2 E4-2 to E4-3	X–PC2/TIN to E20 Strobe to X–TIN	**Default**

Figure 11 Strobe Usage

Jumper Options

The two charts below, Figures 12 and 13, show wire jumper connections. Note that the IP-Dual PI/T connects pin 1 to pin 2 for all wire jumpers. Note that the IP-Digital 48 connects pin 2 to pin 3 for all wire jumpers.

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E8-1 to E8-2	Pin 43 to Y–H1	Y	Dual PI/T
E8-2 to E8-3	Pin 43 to Y–PC4	Y	Digital 48
E9-1 to E9-2	Pin 48 to GND	Y	Dual PI/T
E9-2 to E9-3	Pin 48 to Y–PC3/TOUT	Y	Digital 48
E10-1 to E10-2	Pin 46 to GND	Y	Dual PI/T
E10-2 to E10-3	Pin 46 to Y–PC2/TIN	Y	Digital 48
E11-1 to E11-2	Pin 44 to GND	Y	Dual PI/T
E11-2 to E11-3	Pin 44 to Y-PC1	Y	Digital 48
E12-1 to E12-2	Pin 42 to GND	Y	Dual PI/T
E12-2 to E12-3	Pin 42 to Y–PC0	Y	Digital 48

Figure 12 Wire Jumper Usage for Y 68230

Jumper	I/O Connection	68230	Default
E13-1 to E13-2	Pin 24 to X–H4	X	Dual PI/T
E13-2 to E13-3	Pin 24 to X-PC7	X	Digital 48
E14-1 to E14-2	Pin 22 to X–H3	X	Dual PI/T
E14-2 to E14-3	Pin 22 to X–PC6	X	Digital 48
E15-1 to E15-2	Pin 20 to X–H2	X	Dual PI/T
E15-2 to E15-3	Pin 20 to X-PC5	X	Digital 48
E16-1 to E16-2	Pin 18 to X–H1	X	Dual PI/T
E16-2 to E16-3	Pin 18 to X–PC4	X	Digital 48
E17-1 to E17-2	Pin 19 to GND	X	Dual PI/T
E17-2 to E17-3	Pin 19 to X–PC1	X	Digital 48
E18-1 to E18-2	Pin 17 to GND	X	Dual PI/T
E18-2 to E18-3	Pin 17 to X–PC0	X	Digital 48
E19-1 to E19-2	Pin 23 to GND	X	Dual PI/T
E19-2 to E19-3	Pin 23 to E3	X	Digital 48
E20-1 to E20-2	Pin 21 to GND	X	Dual PI/T
E20-2 to E20-3	Pin 21 to E4	X	Digital 48

Figure 13 Wire Jumper Usage for X 68230

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GND	GND	1		26	
CLK	+5V		2		27
Reset*	R/W*	3	28		
D0 IDSel*	4		29		
D1 n/c	5	30			
D2 MEMSel*	6		31		
D3 n/c	7	32			
D4 INTSel*	8		33		
D5 n/c	9	34			
D6 IOSel*	10		35		
D7 n/c	11	36			
D8 A1	12		37		
D9 n/c	13	38			
D10	A2	14		39	
D11	n/c	15	40		
D12	A3	16		41	
D13	IntReq0*	17	42		
D14	A4	18		43	
D15	n/c	19	44		
BS0*	A5	20		45	
n/c	n/c	21	46		
BS1*	A6	22		47	
n/c	Ack*	23	48		
+5V	n/c		24		49
GND	GND	25	50		

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 14 Logic Interface Pin Assignment

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application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron. Shunts may be replaced with wire-wrap® wires if desired.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of these screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

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Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from GreenSpring Computers contact your reseller. Products returned to GreenSpring Computers for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
GreenSpring Computers
1204 O'Brien Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax

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Shunt and Jumper Locations

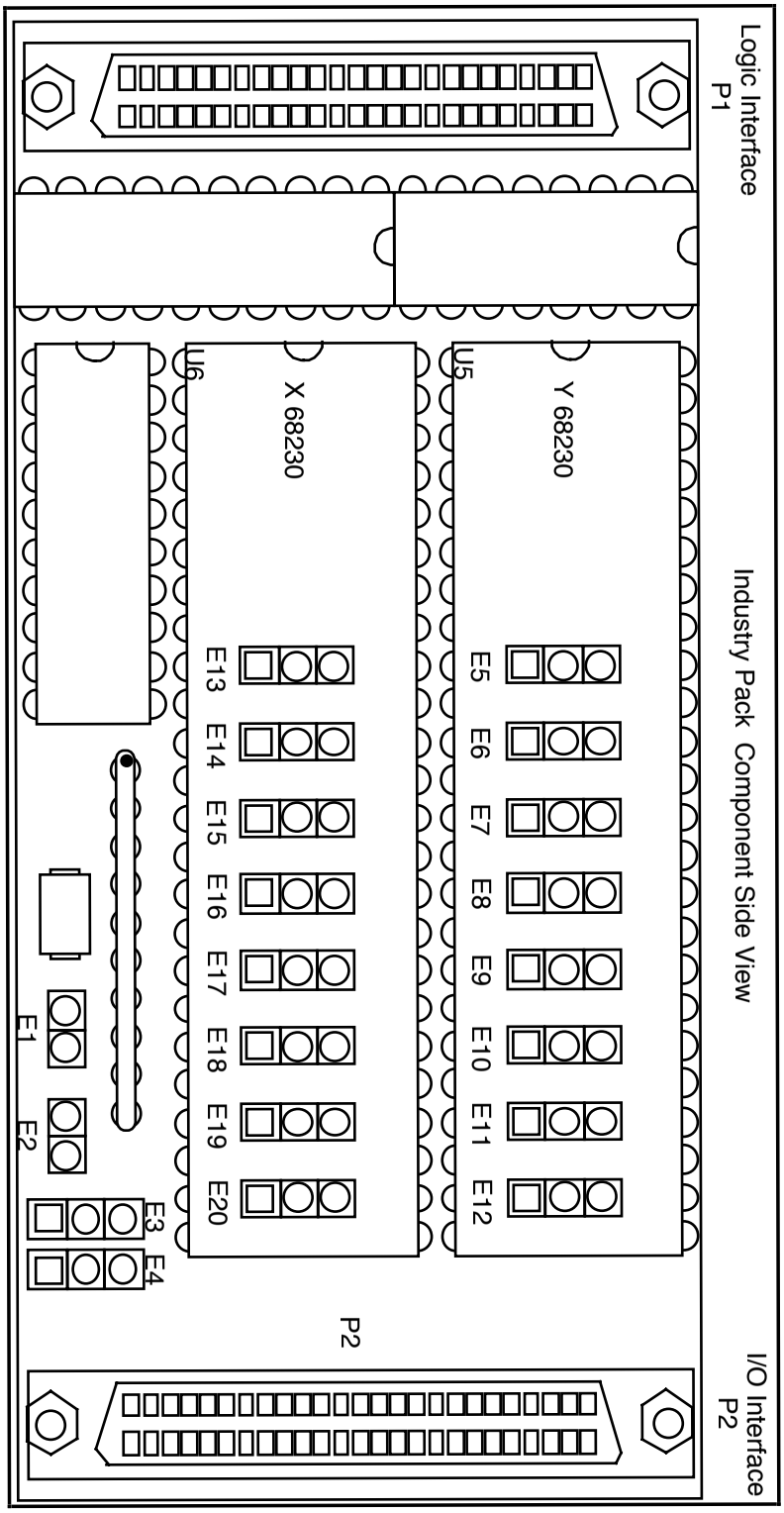


Figure 15 Location of Shunts and Jumpers

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	(32 lines if all features configured)
Data Transfer Modes	8-bit, 16-bit, double-buffered input, double-buffered output, non-latched input, single-buffered output, bi-directional, bit I/O
Timers	Two, 24-bit synchronous down counters Multi-mode, gated, with 5-bit prescaler
Timer Modes	Periodic interrupt, interrupt after timeout, watchdog timer, square wave output, elapsed time meter, external event counter
Interrupts	Eight unique vectored interrupts
Wait States	Zero on ID reads, One on I/O reads and writes, Three on interrupt cycles
Programmable Registers	48, 8-bit registers
I/O Interconnect	50-pin cable includes 48 lines and two grounds
Input Current	±20 μA typical
Drive Current	Sink: 2.4 mA min @ 0.5 V Source: 150 μA min @ 2.4 V
Dimensions	1.8 x 3.9 x 0.340 inches max
Power Requirements	+ 5 V @ 220 mA typ, no load
Environmental	0° C to 70° C operating 5 to 95% relative humidity (non condensing) -10 to + 85° C storage

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IP Dual PI/T–ENG KIT	IP with Technical Documentation, 6 foot cable, terminal block
IP Digital 48–ENG KIT	IP with Technical Documentation, 6 foot cable, terminal block

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Current manufacturing information, including schematics, programmed device listings, bills-of-material, and assembly diagrams are available from GreenSpring Computers as part of the Engineering Kit option or from your international distributor.

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