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User Manual

IP-Unidig-I-E

24 Line Input/Output with
Interrupts and
LineSafe™ ESD Protection
IndustryPack®

IP-Unidig-I-E

24 Line Input/Output with Interrupts and LineSafe™ ESD Protection IndustryPack®

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Product Description

The IP-Unidig-I-E is part of the IndustryPackTM family of modular I/O components. It provides 24 lines of digital I/O, with any line capable of generating an interrupt. All the I/O lines feature GreenSpring's unique LineSafe electrostatic discharge (ESD) protection circuit, making the IP ideally suited for rugged industrial applications. Each line may be dynamically and individually configured for either input or output. Both internal read back and direct read registers are provided for ease of software development. 16-bit word and 8-bit byte operations are supported. The IP-Unidig-I-E is pin and software compatible with the IP-Unidig-E IndustryPack™.

The IP-Unidig-I-E conforms to the Industry Pack Interface Specification. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module with final system implementation on a different one.

The industry standard 50-pin interface cable may be terminated in a screw terminal block, an OPTO-22™ Direct I/O Interface Module, or user-determined hardware. Alternate grounds on this cable assure reliable signals.

The interrupt latch circuits are edge sensitive with programmable polarity and are controlled through the following five 24-bit registers: interrupt pending, interrupt request, interrupt polarity, interrupt enable, and interrupt clear. Each line corresponds to one bit in each of the registers, making programming uniform and simple. This architecture also prevents the loss of an event during the execution of the interrupt service routine.

Writing a one to any line turns off the output driver, allowing a passive pull up resistor to set the line to a logic high. Writing a zero to any line turns on the driver, driving the line to a logic low. For input use, a one is written to the corresponding line - this is the power up default. For output use, the binary value desired is written to the corresponding line.

Two separate locations in I/O space are provided for each signal line. The first location is used to set the output state and also to read back the written value at the internal latch. This read back function is valuable to support bit operations (which are implemented by processors as read-modify-write cycles). It is also useful in debugging, making it possible to observe directly the last written value to the port. The second location is the direct read port, which is always used for reading input values. This register may also be used to verify the correct logic signal is actually on the interface cable.

Figure 1 shows a block diagram of the IP-Unidig-I-E.

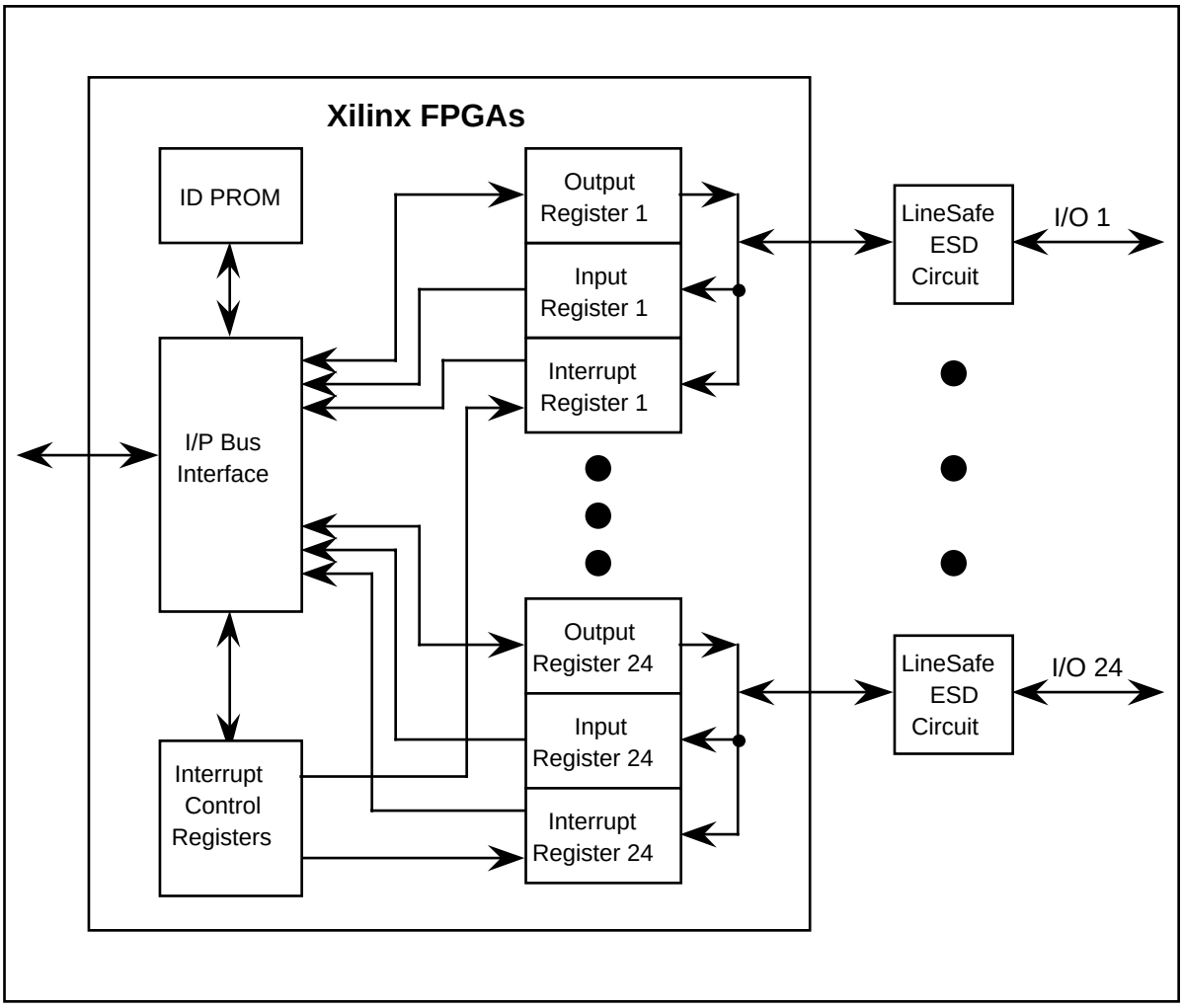


Figure 1 Simplified Block Diagram

VMEbus Addressing

IP-Unidig-I-E normally is accessed one word at a time in the host's I/O space. Alternatively, byte or long word accesses may be used. If long words are used, the host (or support module) must map 32-bit long words into two 16-bit cycles. This is common for 68020 and 68030 implementation of the I/O space.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1—16
base + $2	word	write	Output lines 17—24
base + $0	word	read	Read back lines 1—16
base + $2	word	read	Read back lines 17—24
base + $4	word	read	Direct read lines 1—16
base + $6	word	read	Direct read lines 17—24
base + $10	word	read/write	Interrupt Vector Register
base + $12	word	read/write	Interrupt Enable Register lines 1—16
base + $14	word	read/write	Interrupt Enable Register lines 17—24
base + $16	word	read/write	Interrupt Polarity Register lines 1—16
base + $18	word	read/write	Interrupt Polarity Register lines 17—24
base + $1A	word	write	Interrupt Clear Register lines 1—16
base + $1C	word	write	Interrupt Clear Register lines 17—24
base + $1A	word	read	Interrupt Pending Register lines 1—16
base + $1C	word	read	Interrupt Pending Register lines 17—24

Figure 2 VME Bus Addressing, Word Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for word accesses.

Bit map of words at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $2, base + $6, base + $14, base + $18 and base + $1C

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of the Interrupt Vector Register at base + $10

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vec. Bit:	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Alternate Byte Access, I/O Space

base + $0	byte	write	Output lines 9—16
base + $1	byte	write	Output lines 1—8
base + $3	byte	write	Output lines 17—24
base + $0	byte	read	Read back lines 9—16
base + $1	byte	read	Read back lines 1—8
base + $3	byte	read	Read back lines 17—24
base + $4	byte	read	Direct read lines 9—16
base + $5	byte	read	Direct read lines 1—8
base + $7	byte	read	Direct read lines 17—24
base + $11	byte	read/write	Interrupt Vector Register
base + $12	byte	read/write	Interrupt Enable Register lines 9—16
base + $13	byte	read/write	Interrupt Enable Register lines 1—8
base + $15	byte	read/write	Interrupt Enable Register lines 17—24
base + $16	byte	read/write	Interrupt Polarity Register lines 9—16
base + $17	byte	read/write	Interrupt Polarity Register lines 1—8
base + $19	byte	read/write	Interrupt Polarity Register lines 17—24
base + $1A	byte	write	Interrupt Clear Register lines 9—16
base + $1B	byte	write	Interrupt Clear Register lines 1—8
base + $1D	byte	write	Interrupt Clear Register lines 17—24
base + $1A	byte	read	Interrupt Pending Register lines 9—16
base + $1B	byte	read	Interrupt Pending Register lines 1—8
base + $1D	byte	read	Interrupt Pending Register lines 17—24

Figure 3 VME Bus Addressing, Byte Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for byte accesses.

Bit map of bytes at base + $1, base + $5, base + $13, base + $17 and base + $1B

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $3, base + $7, base + $15, base + $19 and base + $1D

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of the Interrupt Vector Register at base + $11

Data Bit #	7	6	5	4	3	2	1	0
Vec. Bit:	7	6	5	4	3	2	1	0

Alternate Long Word Access, I/O Space

base + $0	long	write	Output lines 1—24
base + $0	long	read	Read back lines 1—24
base + $4	long	read	Direct read lines 1—24
base + $10	long	read/write	Interrupt Vector Register
base + $12	long	read/write	Interrupt Enable Register lines 1—24
base + $16	long	read/write	Interrupt Polarity Register lines 1—24
base + $1A	long	write	Interrupt Clear Register lines 1—24
base + $1A	long	read	Interrupt Pending Register lines 1—24

Figure 4 VME Bus Addressing, Long Word Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for long word accesses.

Bit map of long words at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of long word at base + $10

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Vec. Bit:	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vec. Bit:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is still transferred on data lines D7..D0.

Word addresses on the NuBus are the same as for VME. Word data is transferred on data lines D15..D0.

ISA (IBM PC-AT) Addressing

Both word and byte address modes are supported by the IP-Unidig-I-E. The actual application will depend on the carrier card. See the carrier card manual for details.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1—16
base + $2	word	write	Output lines 17—24
base + $0	word	read	Read back lines 1—16
base + $2	word	read	Read back lines 17—24
base + $4	word	read	Direct read lines 1—16
base + $6	word	read	Direct read lines 17—24
base + $10	word	read/write	Interrupt Vector Register
base + $12	word	read/write	Interrupt Enable Register lines 1—16
base + $14	word	read/write	Interrupt Enable Register lines 17—24
base + $16	word	read/write	Interrupt Polarity Register lines 1—16
base + $18	word	read/write	Interrupt Polarity Register lines 17—24
base + $1A	word	write	Interrupt Clear Register lines 1—16
base + $1C	word	write	Interrupt Clear Register lines 17—24
base + $1A	word	read	Interrupt Pending Register lines 1—16
base + $1C	word	read	Interrupt Pending Register lines 17—24

Figure 5 ISA Bus Addressing, Word Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for word accesses.

Bit map of words at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $2, base + $6, base + $14, base + $18 and base + $1C

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of the Interrupt Vector Register at base + $10

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vec. Bit:	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Alternate Byte Access, I/O Space

base + $0	byte	write	Output Lines 1—8
base + $1	byte	write	Output Lines 9—16
base + $2	byte	write	Output Lines 17—24
base + $0	byte	read	Read-back Lines 1—8
base + $1	byte	read	Read-back Lines 9—16
base + $2	byte	read	Read-back Lines 17—24
base + $4	byte	read	Direct Read Lines 1—8
base + $5	byte	read	Direct Read Lines 9—16
base + $6	byte	read	Direct Read Lines 17—24
base + $10	byte	read/write	Interrupt Vector Register
base + $12	byte	read/write	Interrupt Enable Register lines 1—8
base + $13	byte	read/write	Interrupt Enable Register lines 9—16
base + $14	byte	read/write	Interrupt Enable Register lines 17—24
base + $16	byte	read/write	Interrupt Polarity Register lines 1—8
base + $17	byte	read/write	Interrupt Polarity Register lines 9—16
base + $18	byte	read/write	Interrupt Polarity Register lines 17—24
base + $1A	byte	write	Interrupt Clear Register lines 1—8
base + $1B	byte	write	Interrupt Clear Register lines 9—16
base + $1C	byte	write	Interrupt Clear Register lines 17—24
base + $1A	byte	read	Interrupt Pending Register lines 1—8
base + $1B	byte	read	Interrupt Pending Register lines 9—16
base + $1C	byte	read	Interrupt Pending Register lines 17—24

Figure 6 ISA Bus Addressing, Byte Access

Bit map of bytes at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $1, base + $5, base + $13, base + $17 and base + $1B

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $2, base + $6, base + $14, base + $18 and base + $1C

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of the Interrupt Vector Register at base + $10

Data Bit #	7	6	5	4	3	2	1	0
Vec. Bit:	7	6	5	4	3	2	1	0

I/O Pin Wiring

This section gives the pin assignments and wiring recommendations for IP-Unidig-I-E.

The pin numbers given in Figure 2 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O 1	1	GND	2
I/O 2	3	GND	4
I/O 3	5	GND	6
I/O 4	7	GND	8
I/O 5	9	GND	10
I/O 6	11	GND	12
I/O 7	13	GND	14
I/O 8	15	GND	16
I/O 9	17	GND	18
I/O 10	19	GND	20
I/O 11	21	GND	22
I/O 12	23	GND	24
I/O 13	25	GND	26
I/O 14	27	GND	28
I/O 15	29	GND	30
I/O 16	31	GND	32
I/O 17	33	GND	34
I/O 18	35	GND	36
I/O 19	37	GND	38
I/O 20	39	GND	40
I/O 21	41	GND	42
I/O 22	43	GND	44
I/O 23	45	GND	46
I/O 24	47	GND	48
n/c	49	GND	50

Figure 7 I/O Pin Assignment

Caution

Note that when the IP-Unidig-I-E is used to directly connect with OPTO 22, Allen Bradley, Grayhill or similar compatible parallel opto-isolation panels that these panels number their channels starting with pin 47. Thus the IP-Unidig-I-E line number ordering and the OPTO Panel line number ordering are *reversed*.

IndustryPack Logic Interface Pin Assignment

Figure 30 below gives the pin assignments for the IndustryPack Logic Interface on the IP-Unbuffered Digital Interrupt I/O. Pins marked n/c below are defined by the specification, but are not used on IP-Unbuffered Digital Interrupt I/O. Also see the User Manual for your IP Carrier board for more information.

GND	GND	1		26	
CLK	+5V		2		27
Reset*	R/W*	3		28	
D0 IDSel*	4		29		
D1 n/c	5	30			
D2 n/c	6		31		
D3 n/c	7	32			
D4 INTSel*	8		33		
D5 n/c	9	34			
D6 IOSel*	10		35		
D7 n/c	11	36			
D8 A1	12		37		
D9 n/c	13	38			
D10	A2	14		39	
D11	n/c 15		40		
D12	A3	16		41	
D13	IntReq0*	17		42	
D14	A4	18		43	
D15	n/c 19		44		
BS0*	A5	20		45	
BS1*	n/c 21		46		
–12V	A6	22		47	
+12V	Ack*	23		48	
+5V	n/c	24		49	
GND	GND	25		50	

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 8 Logic Pin Assignment

Programming

Programming the IP requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Support Module. This document refers to this address as "base".

Initialization

The IP-Unidig-I-E does not require any special initialization sequence. However, upon reset, the IP requires a minimum delay of 300 milliseconds before any accesses are made by the host system. This is the time it takes the Xilinx FPGAs to configure themselves. All the registers are cleared on reset, and all I/O lines are set to be inputs. Additionally, external voltage should not be applied to any I/O line when the IP is unpowered. This will damage the Xilinx FPGAs. Turning power on and off to all components in the system with a single switch will eliminate this potential problem.

Data I/O

Each of the 24 bits may be individually set as input or output. To set a bit to be input, write a "1" to the I/O bit location. This is the default on reset.

To write a zero on the I/O signal line, write a "0" to the I/O bit location. To write a one on the I/O signal line, write a "1" to the I/O bit location. Writing a one and setting the signal line to input mode is the same. Passive pull-up resistors are used with tri-state drivers to implement the interface.

Data may be read from two sets of address locations. The first set of locations, base + 0 and base + 2 for word operations, function as the Internal Read Back Register. The data latched in the Output Latch is read from these addresses. They support processor bit operations implemented as read-modify-write cycles, and are also useful for debugging purposes.

The second set of locations, base + 4 and base + 6 for word operations, is the Direct Read Register. Data is latched into the Input Register on the rising edge of the 8 MHz IP Clock. Figure 10 in the Theory of Operations section shows a block diagram.

Using word access, up to 16 bits may be programmed at once. The IP implements a read back register at the same address used for writing to the signal line I/O bits. This permits "set bit" and "clear bit" instructions to be used in programming, which are implemented by the host hardware as read-modify-write cycles. Thus, single bits at well as bit fields may be accessed.

The IP may also be accessed using byte or long word accesses. If long word accesses are used from a 68020, 68030, or 68040 host, the I/O space must be mapped into "D16". 68000 and 68010 hosts internally map all long word accesses into 16 bits, so no special precaution is necessary.

Interrupts

The IP-Unidig-I-E uses five 24-bit registers to control interrupt generation. Each bit in each register corresponds to one I/O line, simplifying software development. Inputs are not debounced. Users may need to provide this feature either in software or with external hardware if noisy inputs, such as mechanical switches, are used to generate interrupts. Interrupts from all enabled I/O lines are OR'd together and are asserted on IntReq0*. IntReq1* is not used. The IP responds to an interrupt cycle by putting out its 8-bit vector from the Interrupt Vector Register onto the data bus.

Interrupt Enable Register

The Interrupt Enable Register is used to enable and disable interrupts from individual I/O channels. Programming any bit to a "1" enables an interrupt from the corresponding I/O channel. Programming any bit to a "0" disables an interrupt from the corresponding I/O channel.

For the IP to actually request an interrupt, an edge or level must be seen on the corresponding I/O channel. Since the IP monitors interrupts regardless of the state of the enable bit, it is possible to get an interrupt immediately upon enabling any bit in this register.

The Interrupt Enable Register is cleared on reset. Thus, all channels are disabled from generating interrupts on reset.

Interrupt Polarity Register

The Interrupt Polarity Register is used to set the polarity of the transition which is to generate an interrupt for each I/O channel. Programming any bit to a "1" will generate an interrupt when the input data changes from a logic zero to a logic one on the corresponding I/O channel. Programming any bit to a "0" will generate an interrupt when the input data changes from a logic one to a logic zero. For the IP to actually request an interrupt, the corresponding bit in the Interrupt Enable Register must be "1".

The Interrupt Polarity Register is cleared on reset. This makes the default to interrupt on a falling edge for all I/O channels.

The IP's logic monitors writing to this register. If a bit in this register is changed, and the static input on the corresponding channel matches the programmed bit, the interrupt flip-flop for that channel is set. This feature is critical to prevent the loss of an interrupt due to a channel transition which might occur during an interrupt service routine.

Example: The software reads an input, determines it is zero, then enables that channel to generate an interrupt on a rising edge. Between the read and the write, however, the input changed to one. With this special logic, an interrupt is immediately generated, or generated at the end of the current routine if interrupts are masked. Without the logic, the input transition would have been lost.

If the software does not care what the current state of the input channels is and does not wish to receive any immediate interrupts, then the procedure is (1) disable interrupts in the processor, (2) program the IP's Polarity Register, (3) write a one to all channels of the Clear Interrupt Register, (4) enable interrupts in the processor.

Example: Interrupts are desired only on falling edges of lines 1—5. With interrupts disabled, write zero to the low word of the Interrupt Polarity Register, address base + 0x16. Write 0x1F to the low word of the Interrupt Clear Register, address base + 0x1A, to clear any potential interrupts on lines 1—5. Write the interrupt vector to Interrupt Vector Register. Enable interrupts by writing 0x1F to the low word of the Interrupt Enable Register, address base + 0x12.

Inverting a bit in this register each time the corresponding bit generates an interrupt will result in an interrupt for both rising and falling edges.

Clear Interrupt Register and Pending Interrupt Register

These two registers are used to detect and clear pending interrupts from any combination of channels. Both registers access the same interrupt flip-flops. They are arranged as one read-only register, the Pending Interrupt Register, and one write-only register, the Clear Interrupt Register.

The flip-flops that make up these two registers are set only by a transition on an input channel of the programmed polarity. They are cleared by the software writing to the Clear Interrupt Register or by IP Reset.

Reading a one in the Pending Interrupt Register means the corresponding channel either has generated an interrupt if that channel is enabled, or has an interrupt pending if that channel is disabled. A pending interrupt will drive the interrupt request line as soon as the corresponding bit in the Interrupt Enable Register is set to "1".

Both interrupts and pending interrupts are cleared for any channel by writing a one to the corresponding bit position in the Clear Interrupt Register. In general, only channels which have been detected as pending by a read of the Pending Interrupt Register should be cleared. This will prevent the loss of an interrupt which arrives between the read and write. If the write to the Clear Interrupt Register were to be all "1"s, an interrupt arriving on a new channel between the read and write would be lost. Writing a "0" to any bit in the Clear Interrupt Register has no affect on the corresponding channel.

Note that for simplicity, the host software need only read the Pending Interrupt Register, then immediately write the same value to the Clear Interrupt Register. The software may then check the bits in that byte, taking whatever actions are required by the one or more channels recognized to need service.

To clear all pending and latent interrupts, the software writes all "1"s to the Clear Interrupt Register. The Pending Interrupt register is cleared on reset, which clears all interrupts and pending interrupts.

Interrupt Vector Register

The IP has an eight bit read/write register to hold the interrupt vector required to service IP interrupts.

All interrupts from one IP-Unidig-I-E use the same vector. The Pending Interrupt Register is used to determine what combination of channels need service. This allows the software to handle any number of equally weighted channels in a single interrupt service routine.

This register is cleared on reset.

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-Unidig-I-E is shown in Figure 9 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers, Inc.. The ID PROM on the IP-Unidig-I-E is implemented in the Xilinx FPGA device.

The location of the ID PROM in the host's address space is dependent on the carrier board used. For most VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)	
17	CRC for bytes used	(87)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(00)
0F	reserved	(00)
0D	Revision	(A1)
0B	Model No IP-Unidig-I-E	(67)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 9 ID PROM Data (hex)

Theory of Operation

IndustryPack Standards

The IP-Unidig-I-E is part of the IndustryPack™ family of modular I/O products. It meets the IndustryPack Logic Specification. (Contact GreenSpring Computers, Inc. for a copy of this Specification.) It is assumed the reader is at least casually familiar with both this document and 68000 processor architecture.

Control Logic

All control logic is contained within a two Xilinx FPGAs. They are clocked by the 8 MHz IP Logic clock from the Support Module. The IP responds to I/O and ID selects. It does not respond to memory selects, however the MEMSel* line is routed to the FPGA, enabling easy modification for special needs.

The IP does not require wait states for either read or write cycles. Thus, the FPGA generates Ack* on the clock cycle following either I/O or ID Select. Hold cycles (from the Support Module) are supported for both read and write cycles by extending Ack* as required. If no hold cycles are requested by the Support Module, the IP is capable of supporting the full 8 MByte per second data transfer rate of the IP Logic Interface Specification.

I/O Data Lines

All input and output latches and buffers are contained within the Xilinx FPGA. Each I/O line has GreenSpring's unique LineSafe ESD protection circuit for added ruggedness. This circuit puts a 33Ω resistor in series and the equivalent of a 1100 pF capacitor to ground on each I/O line. Standard ESD handling precautions should still be used as the IP Logic Interface lines are unprotected. Additionally, external voltage should not be applied when the IP is unpowered. This will damage the Xilinx FPGAs. Turning on and off all power supplies at the same time will eliminate this problem.

Outputs use active low tri-state buffers which are controlled by the individual output lines. In this manner, they implement an open drain connection, being enabled when the output is low and disabled when the output is high. Three 10 KΩ resistor networks pull up the I/O lines to +5V when the outputs are disabled. RN1 pulls up I/O Lines 9—16, RN2 pulls up I/O Lines 17—24, and RN3 pulls up I/O Lines 1—8. These resistors may be replaced with other values, as long as the total sink current necessary to drive the pullup and load on each line low is less than the four milliamps specified for each pin of the Xilinx chip.

Interrupts

The interrupt generation circuitry consists of an edge detector and a level sensor which feed the input of a latch. The edge detector uses two latches in series clocked by the 8 MHz IP Clock to compare the current state of the I/O line with the previous state. If the two states are different and the difference matches the polarity set in the Polarity Register, the Interrupt Latch is set. If the Interrupt Enable bit is set for that I/O line, an interrupt is generated on IntReq0*. This series of latches means there will be a minimum 125 ns. delay (one 8 MHz clock pulse) from the time the I/O line transitions until the interrupt is generated. Individual interrupts are cleared by writing a "1" to the corresponding bit in the Interrupt Clear Register.

The level sensor is only active when writing to the Interrupt Polarity Register. If a "1" is written to a bit in the Interrupt Polarity Register, corresponding to a rising edge interrupt, and the level on the I/O line is already a "1", the level sensor will generate a pending interrupt. If the Interrupt Enable bit is set for that I/O line, an interrupt is generated on IntReq0*. This can be used to ensure an edge will not

be missed when generating interrupts on both the rising and falling edge. In this case, the interrupt service routine (ISR) should change the Interrupt Polarity Register. If the I/O line has transitioned already, an interrupt will be generated immediately. When the ISR completes, the interrupt will be waiting.

If a bit is used as an output, it will still generate an interrupt when it is written to if the corresponding bit in the Interrupt Enable Register is set. If this is undesired, care must be taken to enable interrupts only for those bits used as input.

Figure 10 shows a block diagram of the structure for each I/O line.

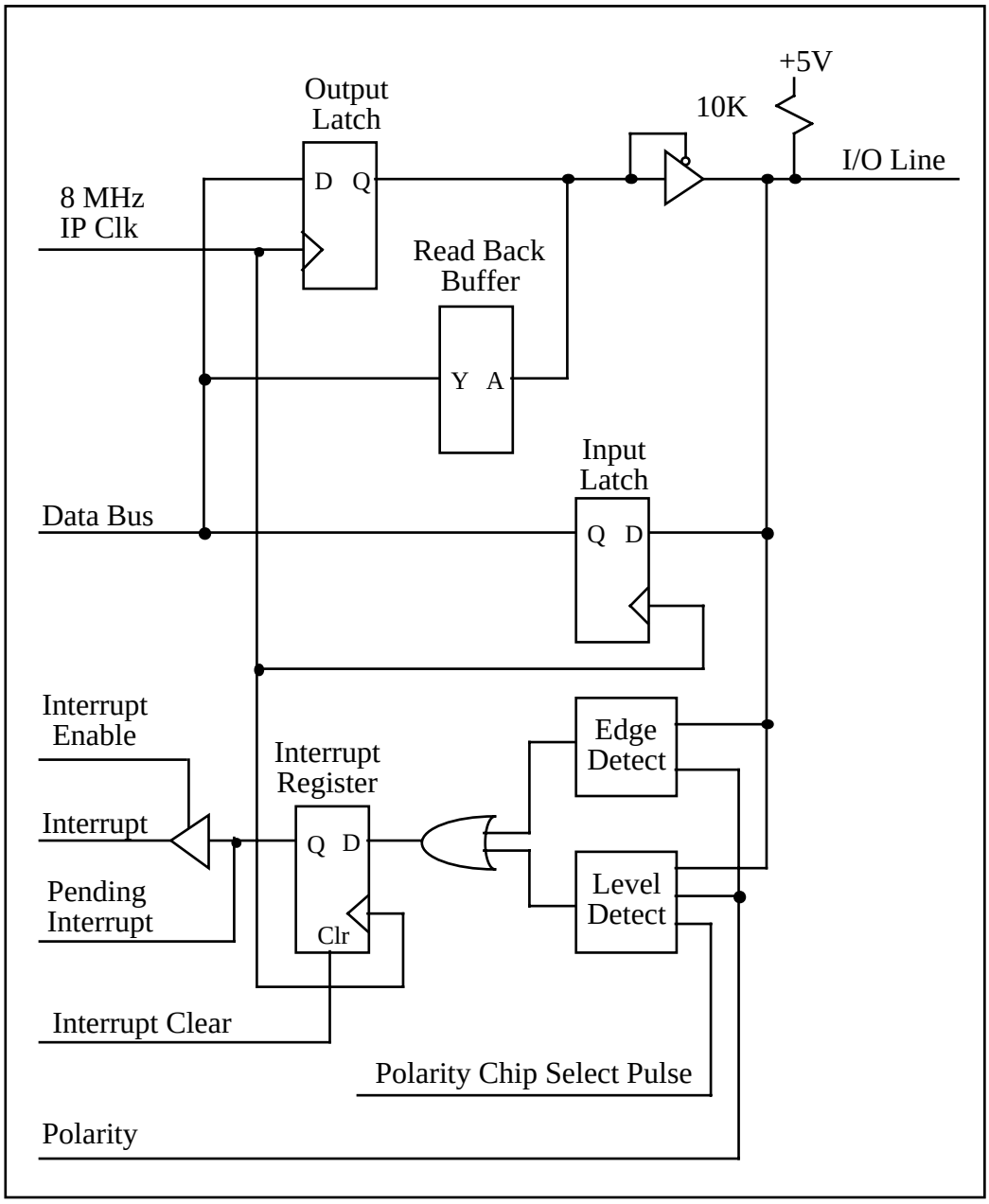


Figure 10 I/O Line Block Diagram

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-UniDig-I-E is constructed out of 0.062 inch thick FR4 V0 material. The four copper layers consist of two signal layers on the top and bottom, and two internal power and ground plane layers.

Through hole and surface mounting of components are used. IC sockets use gold plated screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and have gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four M2 metric stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, then the temperature difference between the component and the solder side is one degree Celsius.

Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to GreenSpring Computers. All replaced products become the sole property of GreenSpring Computers.

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Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
GreenSpring Computers
1204 O'Brien Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax

Specifications

Logic Interface	Industry Pack™ Logic Interface
Digital Interface	24 digital signal lines with latched inputs and outputs. Each line is either an input or an output Alternate grounds on the interface cable
Interface Level	TTL Tri-state with 10 KΩ pull up resistor standard 4 mA current sink
Software Interface	Seven 24-bit registers: output read back input interrupt enable interrupt pending interrupt polarity interrupt clear One 8-bit register: interrupt vector
Initialization	300 millisecond delay from reset Forces all lines to be inputs Clears all registers Clears and disables all interrupts
Interrupts	All lines can be programmed to generate an interrupt Programmable polarity - rising or falling edge Interrupts are cleared by writing a 1 to the appropriate interrupt clear bit Programmable vector
Access Mode	Byte or word in I/O Space Byte or word in ID Space
Wait States	Zero
Transfer Rate	8 Mbytes/second maximum, continuous
Onboard Options	All options are software programmable
Dimensions	Standard Single High Industry Pack width and length 1.8 x 3.9 inches
Construction:	Conformal Coated FR4 4 layer Printed Circuit Surface mounted components
Temperature Coefficient:	0.89 W/°C for uniform heat across IP
Power Requirements	+5.0 VDC, 40 mA typical

Order Information

IP-Unidig-I-E	IndustryPack with 24 I/O lines and interrupt capability
IP-Unidig-I-E-ENG KIT	which includes: six foot 50-pin cable 50-screw terminal block Technical documentation

Schematics

Schematics are provided here for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification. All information following is Copyright GreenSpring Computers, Inc.

Current manufacturing information, including schematics, programmed device listings, bill-of-material, and assembly diagrams are available from GreenSpring Computers as part of the Engineering Kit option or from your international distributor.

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