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User's Manual

SPI-200

Quad IndustryPack®
Carrier for DSP-Link3 Processor Boards

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SPI-200
Quad IndustryPack Carrier for
DSP-Link3 Processor Boards

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Product Description

The SPI-200 is a four slot IndustryPack® carrier that uses a DSP-Link3 connection for communication with the host processor. It is a full size ISA card but all communication with the processor is done through the DSP-Link3 connector. It does not have any connections to the ISA bus except power and ground. The DSP-Link3 connection is made through a high density 64 pin ribbon cable. The SPI-200 adds a broad range of I/O and memory capabilities to DSP-Link3 processor systems and is appropriate for rugged industrial and commercial configurations.

The SPI-200 provides full support for the ANSI/VITA 4-1995 IP Module Specification and the DSP-LINK3 Product Requirement Specification Document Rev. 0.94. Each IndustryPack slot may be individually configured for either 8 MHz or 32 MHz operation. The carrier supports four single-wide IPs, two double-wide or a combination. All accesses to the IndustryPacks use the upper 16 bits of the 32 bit DSP-Link3 data bus and use Ready-Controlled cycles. Each IndustryPack slot has a page register to allow the full 8 MB of memory space defined by the IndustryPack Module Specification. The page registers may be accessed by either Standard or Standard Fast ASTRB/ cycles.

The SPI-200 provides protected, filtered +5V, +12V, and –12V supplies to all the IndustryPack by means of passive "T" filters, capacitors and fuses. The three terminal filters provide excellent RF rejection of power supply conducted noise.

With up to 200 I/O lines per slot and up to four IndustryPack modules per SPI-200, users can achieve a very high level of I/O density. IndustryPacks are available with a wide range of functions including serial and parallel I/O, analog to digital conversion and digital to analog conversion, motion control, memory and data communication. Carrier boards are available for other industry standard buses, including VMEbus, PCI bus, cPCI bus, Futurebus+, G64/G96, ISA bus , and VXIbus.

Key Features

- DSP-Link3 interface through 64 pin ribbon connector
- Supports four IndustryPacks®
- Ready Controlled cycles for all IP accesses
- Four 11 bit page registers allow full 8 Mbyte memory decoding for each IP
- Two 16 bit control registers
- Each IPs' interrupts may be programmed to any of the four DSP-Link interrupt lines
- Programmable 8 or 32 MHz. operation in each slot
- Shunt selection to one of four base addresses.
- Up to 200 I/O lines supported
- Built-in timer to detect IP bus errors
- RF filters on all power lines
- Four 50 pin IDC connectors

A block diagram of the board is shown in Figure 1.

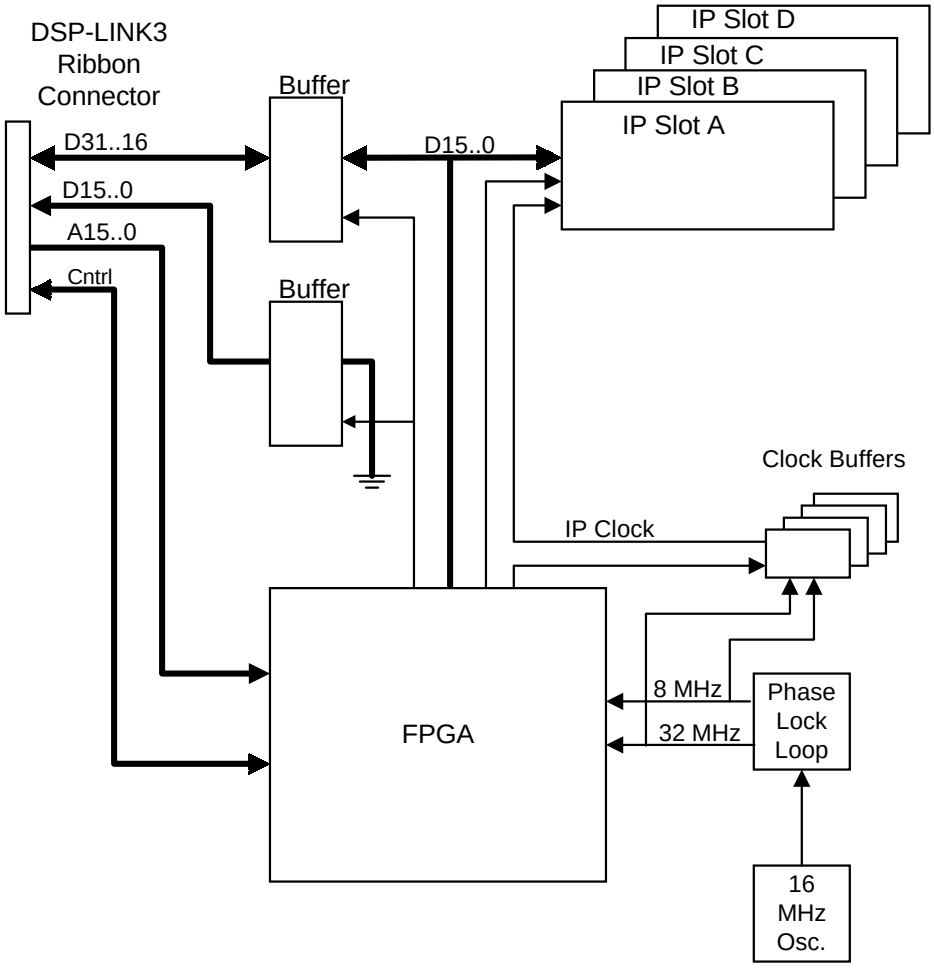


Figure 1 Block Diagram

SPI-200 Addressing

Addressing Overview

The DSP-Link3 interface has 16 address lines A15..A0. They are broken down to decode one of four boards, one of four IPs and one of four spaces on the IP. In general, IPs support both byte and word access cycles, however the DSP-Link3 interface does not. **All accesses to IPs are done with long words, with the data in the upper word, D31..D16, mapped to D15..D0 on the IP bus. This corresponds to word accesses on the IPs. Byte accesses to IPs are not supported on the SPI-200.** A0 on the DSP-Link3 interface maps to A1 on the IP bus, so incrementing a DSP-Link3 address by one will access consecutive words on the IP. The lower 16 bits of the DSP-Link3 bus will be read as all '0's and should be written as all '0's as well. All IPs are accessed with Ready Controlled cycles. The two control registers are accessed with Standard cycles while the page registers may be accessed with either Standard or Standard Fast ASTRB/ cycles.

Each of the different DSP-Link3 cycle types will generally have a different base address on the processor board. Check the manual for the specific addresses for the board used. The following tables can then be used as offsets to each of the spaces. The address for each IP register will be the result of the following calculation:

Processor Board DSP-Link3 Cycle Type + Board ID + IP Slot + IP Space + IP Register Offset.

The following sections will explain how to calculate the Board ID, IP Slot and IP Space addresses. Consult the IP User's Manual for the IP Register Offset.

Board Selection

The upper two bits, A15 and A14, are used to select one of four boards. The possible base addresses are 0x0000, 0x4000, 0x8000 and 0xC000. Two three pin shunts on the SPI-200, E2 and E3 correspond to the two address bits. Figure two lists a table of the possible combinations. Please see the Shunt section for a more detailed description.

Shunt E2	Shunt E3	Corresponding Address A15, A14	Board Base Address
Pos. 1	Pos. 1	00	0x0000
Pos. 1	Pos. 2	01	0x4000
Pos. 2	Pos. 1	10	0x8000
Pos. 2	Pos. 2	11	0xC000

Figure 2 Board Selection Table

IP Addressing

Two bits, A13 and A12, are used to select one of four IndustryPacks. Figure three lists the corresponding address map for the four IndustryPack slots.

A13	A12	IP Slot
0	0	A
0	1	B
1	0	C
1	1	D

Figure 3 IP Slot Addresses

There are four spaces for each IndustryPack: IO, ID, Int and Memory. Each of these is accessed at a fixed offset from the board and slot base address. Additionally, there are two control registers on the SPI-200 which are at a fixed offset from the board base address. Figure four lists the base address offsets for each of the spaces.

Address A11:A0	Name	Cycle Type
400 - 401	Board 0, Internal General Control and Status Register	Standard Access
440 - 441	Board 0, Internal Interrupt Control and Status Register	Standard Access
040 - 07F	IO Space	Ready Controlled
080 - 0BF	ID Space	Ready Controlled
0C0 - 0FF	Int Space	Ready Controlled
800 - FFF	Memory Space	Ready Controlled
800 - FFF	Page Register	Standard or Standard FAST Access, /ASTRB Cycle, Read only

Figure 4 Memory Map

Example 1: To access the ID space for Slot C on Board 1, the address offset added to the DSP-Link3 Ready Controlled base address would be 0x6080.

I/O Space

The I/O space on each IP is fixed at 64, 16-bit words (128 bytes). The four IP I/O spaces are accessible at fixed offsets from the SPI-200's Board and Slot address, as shown in Figure 4. IPs typically do not fully decode their entire 64 word space. All accesses to the IO space are translated to word accesses on the IP. See each IP's User Manual for details of its registers.

***Note**: Each IP may or may not fully decode its I/O space. Incomplete decoding will often cause IP registers to appear in multiple places within the 64 word I/O space. IPs may have different read and write maps. If an IP does not respond*

to an invalid access, the SPI-200 bus timer will respond and set the corresponding bus error bit in the General Control and Status register alert the software.

ID Space

Each IP must have an ID PROM. The ID space on each IP is fixed at 64, 16-bit words. *The ID space above 32 bytes is reserved for future use.* This ID PROM is required by the ANSI/VITA 4 IP Module Specification 1.0. This ID PROM data is at least 12 bytes and is found in the lowest byte of the first 12 words. Newer Industry Packs may support the ID PROM Data Format II which uses 16-bit words instead of 8-bit bytes. The ID PROM provides information about the IP, which is defined in the IP Module Specification and the IP's User Manual. This information includes the IP's manufacturer, model code, and manufacturing revision level. It may also include a driver identification code and calibration information.

Figure 5 below shows the required information in each ID PROM. See the IP Module Specification and the Users Manual for each IP for additional information.

$FF 2*nn 2*nn $33	user space pack specific space	
0x0B	CRC	
0x0A	No of bytes used	[= nn]
0x09	Driver ID, high byte	
0x08	Driver ID, low byte	
0x07	reserved	(0x00)
0x06	Revision	
0x05	Model No	
0x04	Manufacturer ID	
0x03	ASCII "C" or “H”	(0x43 or 0x48)
0x02	ASCII "A"	(0x41)
0x01	ASCII "P"	(0x50)
0x00	ASCII "I"	(0x49)

Figure 5 Required IP ID PROM Information

The “C” at 0x03 is for 8 MHz IPs, while the “H” is for IPs which can run at 32 MHz.

Example 2: The data read in Example 1 would be 0xXX490000, where the XX is undefined, but usually either 0x00 or 0xFF, depending on the IP.

Memory Space Accesses

The memory space of an IP is optional, and varies in size up to eight megabytes per IP. Implementation among IPs varies widely. It may be used for RAM, EPROM, Flash, video frame

buffers, communication data buffers, SRAM, local processor space, expanded registers space, special functions, or some combination of these. The memory is generally but not always 16-bits wide.

The SPI-200 supports the full 8 MBytes of memory space through the use of a separate 11 bit Page Register for each IP. The contents of the page register are combined with the low 11 address bits during a Ready Controlled cycle to an IP Memory space, producing the 22 address bits for a IP memory cycle. Each page allows direct access to 2K words. The value written into the page register is the low 11 bits of the address during a Standard /ASTRB or Standard FAST ASTRB/ cycle. The data during this write is not used, but should be set to '0's. The page registers are write only.

Interrupt Space

IndustryPacks® have an IntSel* cycle which is used to read an interrupt vector during an interrupt acknowledge cycle. The DSP-Link3 interface does not directly support this type of cycle. The SPI-200 has a separate memory space, the INT space, to generate IntSel* cycles. A read of address 0 will read the interrupt vector associated with IP IntReq0*, while a read of address 1 will read the vector for IP IntReq1*.

The interrupt space of each IP slot is directly accessible at any time. Typically, the Interrupt Service Routine (ISR) will access the INT space to determine the local cause of the interrupt. A read to the INT space will generate an IP Interrupt Cycle. During this cycle, the IP places its interrupt vector on the data lines. Some IPs may require this access to clear the interrupt. Check the IP's User Manual for specific details on clearing interrupts. Reading the INT space is not necessary for IPs which don't require it.

Please refer to the General Control and Status register bit map section below for more information.

IP Bus Time-Out

The SPI-200 has an IP bus error timer. When enabled, the SPI-200 will time out if the IP being accessed does not respond within 32 usecs. This allows the IP slots to be interrogated during start up to determine if an IP is installed or not. Without this feature, accessing an IP slot which does not respond will lock up the processor. Accesses to addresses other than a valid IP slot will not start the timer, resulting in a hung processor.

When the Bus Error feature is enabled, the hardware will create a "bus reply" for an IP that does not respond. A bit in the General Control and Status register will be set indicating a bus error was detected.

Please refer to the Control and Status register bit map section below for more information.

General Control and Status Register

The General Control and Status Register (GCSR) on the SPI-200 is used to select the clock speed for each IP Slot, enable interrupts, indicate when a bus error has occurred and indicate the status of the power for each IP.

Bit #	Definition	Access
0	IP Slot A Clock Select	Read/Write
1	IP Slot B Clock Select	Read/Write
2	IP Slot C Clock Select	Read/Write
3	IP Slot D Clock Select	Read/Write
4	Interrupt 0 Enable	Read/Write
5	Interrupt 1 Enable	Read/Write
6	Interrupt 2 Enable	Read/Write
7	Interrupt 3 Enable	Read/Write
8	Bus Error	Read/Write
9	Test	Read/Write
10	IP Reset Status	Read
11	Reserved	Read
12	Reserved	Read
13	Reserved	Read
14	Reserved	Read
15	Reserved	Read

Figure 6 General Control and Status Register

General Control and Status Register Bit Definitions:

Bit [0] LSB IP Slot A Clock Select
This bit determines the frequency of the IP Clock for Slot A. Writing a “1” sets the clock to 32 MHz. Writing a “0” sets the clock to 8 MHz. “0” is the power up and reset default.

Bit [1] IP Slot B Clock Select
This bit determines the frequency of the IP Clock for Slot B. Writing a “1” sets the clock to 32 MHz. Writing a “0” sets the clock to 8 MHz. “0” is the power up and reset default.

Bit [2] IP Slot C Clock Select
This bit determines the frequency of the IP Clock for Slot C. Writing a “1” sets the clock to 32 MHz. Writing a “0” sets the clock to 8 MHz. “0” is the power up and reset default.

Bit [3] IP Slot D Clock Select
This bit determines the frequency of the IP Clock for Slot D. Writing a “1” sets the clock to 32 MHz. Writing a “0” sets the clock to 8 MHz. “0” is the power up and reset default.

Bit [4] /INT0 Enable
Writing a “1” to this bit enables the DSP-LINK3 /INT0 line. Writing a “0” to this bit disables the /INT0 interrupt. The mapping of the IP Interrupts to the DSP-LINK3 lines is controlled by bits [15..8] in the Interrupt Control Register. “0” is the power up and reset default.

Bit [5] /INT1 Enable

Writing a “1” to this bit enables the DSP-LINK3 /INT1 line. Writing a “0” to this bit disables the /INT1 interrupt. The mapping of the IP Interrupts to the DSP-LINK3 lines is controlled by bits [15..8] in the Interrupt Control Register. “0” is the power up and reset default.

Bit [6] /INT2 Enable
Writing a “1” to this bit enables the DSP-LINK3 /INT2 line. Writing a “0” to this bit disables the /INT2 interrupt. The mapping of the IP Interrupts to the DSP-LINK3 lines is controlled by bits [15..8] in the Interrupt Control Register. “0” is the power up and reset default.

Bit [7] /INT3 Enable
Writing a “1” to this bit enables the DSP-LINK3 /INT3 line. Writing a “0” to this bit disables the /INT3 interrupt. The mapping of the IP Interrupts to the DSP-LINK3 lines is controlled by bits [15..8] in the Interrupt Control Register. “0” is the power up and reset default.

Bit [8] Bus Error
When read as a “1”, this bit indicates a previous cycle has tried to access a non-functioning or non-existent IP. The SPI-200 generates a /Ready signal for all address spaces within its decode range. If an IP has not responded within 32 usec., the control logic will generate the /Ready signal to keep the DSP-LIN3 Master from hanging. This bit will be set high when the /Ready signal is internally generated. It must be cleared by writing a “0”, which is the power up and reset default.

Bit [9] Test
This bit is a latched test point connected to TP5 on the board. It may be used as a scope or logic analyzer trigger. When written as a “1”, the TP5 test point will be at 5V. This bit has no affect on the functionality of the SPI-200 or any of the IPs loaded on it. This bit may be used for other purposes in future revisions. It is reset on power up and reset.

Bit [10] IP Reset Status
This bit reflects the status of the IP Reset* line. When the board is first powered up, or after a DSP-Link3 /Reset, this bit will be read as a “1” while the IP Reset* signal is asserted. This allows software to determine when the IPs are out of reset. Any accesses to an IP while the IP Reset* signal is asserted will result in an IP Bus Error. This bit will be read as a “0” once the IP Reset* signal has been de-asserted.

Bit [11..15] Reserved
This bit is reserved for future use and will be read as “0”s. It is recommended it be written a “0” when writing to the General Control and Status Register.

Interrupt Control and Status Register

The Interrupt Control and Status Register (ICSR) on the SPI-200 is used to determine the source of an interrupt and to control the mapping of each IP Slot's Interrupts to a DSP-Link3 /INTx line.

Bit #	Definition	Access
0	IP A IntReq 0	Read
1	IP A IntReq 1	Read
2	IP B IntReq 0	Read
3	IP B IntReq 1	Read
4	IP C IntReq 0	Read
5	IP C IntReq 1	Read
6	IP D IntReq 0	Read
7	IP D IntReq 1	Read
8..9	Slot A Interrupt Map	Read/Write
10..11	Slot B Interrupt Map	Read/Write
12..13	Slot C Interrupt Map	Read/Write
14..15	Slot D Interrupt Map	Read/Write

Figure 7 Interrupt Control and Status Register

Interrupt Control and Status Register Bit Definitions:

Bit [0] LSB IP A IntReq0
This bit indicates the /IntReq0 line from IP A is asserted. Since both the interrupts from IP A are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot A is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. "0" is the power up and reset default for IPs.

Bit [1] IP A IntReq1
This bit indicates the /IntReq1 line from IP A is asserted. Since both the interrupts from IP A are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot A is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. "0" is the power up and reset default for IPs.

Bit [2] IP B IntReq0
This bit indicates the /IntReq0 line from IP B is asserted. Since both the interrupts from IP B are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot B is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. "0" is the power up and reset default for IPs.

Bit [3] IP B IntReq1
This bit indicates the /IntReq1 line from IP B is asserted. Since both the interrupts from IP B are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot B is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. "0" is the power up and reset default for IPs.

Bit [4] IP C IntReq0
This bit indicates the /IntReq0 line from IP C is asserted. Since both the interrupts from IP C are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot C

is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. “0” is the power up and reset default for IPs

Bit [5] IP C IntReq1
This bit indicates the /IntReq1 line from IP C is asserted. Since both the interrupts from IP C are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot C is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. “0” is the power up and reset default for IPs.

Bit [6] IP D IntReq0
This bit indicates the /IntReq0 line from IP D is asserted. Since both the interrupts from IP D are mapped to the same DSP-LINK3 signal, the DSP-LINK3 Master must read this bit if the IP in slot D is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. “0” is the power up and reset default for IPs.

Bit [7] IP D IntReq1
This bit indicates the /IntReq1 line from IP D is asserted. Since both the interrupts from IP D are mapped to the same DSP-LIN3 signal, the DSP-LINK3 Master must read this bit if the IP in slot D is capable of generating both /IntReq0 and /IntReq1 signals. This bit is read only and the actual interrupt must be cleared by the IP. “0” is the power up and reset default for IPs.

Bits [9..8] Slot A Interrupt Map
These two bits control the mapping of the IP Slot A interrupts. Both IntReq0* and IntReq1* lines are logically OR’d together and run to one of the DSP-LINK3 /INT[0..3] lines. The specific /INTx line is encoded by these two bits. The power up and reset default for these bits is “00”. The following table lists the mapping:

Bits [9..8]	DSP-Link3 /INT line
00	/INT0
01	/INT1
10	/INT2
11	/INT3

Bits [11..10] Slot B Interrupt Map
These two bits control the mapping of the IP Slot B interrupts. Both IntReq0* and IntReq1* lines are logically OR’d together and run to one of the DSP-LINK3 /INT[0..3] lines. The specific /INTx line is encoded by these two bits. The power up and reset default for these bits is “00”. The following table lists the mapping:

Bits [11..10]	DSP-Link3 /INT line
00	/INT0
01	/INT1
10	/INT2
11	/INT3

Bits [12..13] Slot C Interrupt Map
These two bits control the mapping of the IP Slot C interrupts. Both IntReq0* and IntReq1* lines are logically OR’d together and run to one of the DSP-LINK3 /INT[0..3] lines. The specific /INTx line is encoded by these two bits. The power up and reset default for these bits is “00”. The following table lists the mapping:

Bits [13..12]	DSP-Link3 /INT line
00	/INT0
01	/INT1
10	/INT2
11	/INT3

Bits [15..14] Slot D Interrupt Map

These two bits control the mapping of the IP Slot D interrupts. Both IntReq0* and IntReq1* lines are logically OR'd together and run to one of the DSP-LINK3 /INT[0..3] lines. The specific /INTx line is encoded by these two bits. The power up and reset default for these bits is "00". The following table lists the mapping:

Bits [15..14]	DSP-Link3 /INT line
00	/INT0
01	/INT1
10	/INT2
11	/INT3

Programming

This section outlines key aspects of preparing to program IPs installed on the SPI-200.

Functional Description

The SPI-200 uses an Altera 10K10 part to convert the DSP-LINK3 cycles into IP Cycles. It has two 16 bit internal Control and Status Registers for managing the various features of the board which are accessed by Standard data cycles. The clock speed for each IP Slot is independently controlled and may be set at either 8 MHz or 32 MHz. Each IP has an 11 bit memory page register located in the Altera part. The contents of the page register is combined with the lower 11 address bits to form the 22 bit IP Memory Cycle address. The page registers are write only and are accessed by either Standard /ASTRB or Standard FAST ASTRB/ cycles.

The DSP-Link3 interface has 16 address lines A15..A0. They are broken down to decode one of four boards, one of four IPs and one of four spaces on the IP. **All accesses to IPs are done with long words, with the data in the upper word, D31..D16, mapped to D15..D0 on the IP bus. This corresponds to word accesses on the IPs. Byte accesses to IPs are not supported on the SPI-200.** A0 on the DSP-Link3 interface maps to A1 on the IP bus, so incrementing a DSP-Link3 address by one will access consecutive words on the IP. The lower 16 bits of the DSP-Link3 bus will be read as all '0's and should be written as all '0's as well. All IPs are accessed with Ready Controlled cycles. The two control registers are accessed with Standard cycles while the page registers may be accessed with either Standard or Standard Fast ASTRB/ cycles.

Initialization

The SPI-200 has an on board power monitor chip which generates a 350 msec. reset signal when the board is powered up. Any time +5V power drops below 4.5 V, the power monitor asserts the reset to the Altera chip and the IP Reset* signal. It remains asserted for a minimum of 350 msec. after power is restored. After this reset has been removed the Altera chip takes up to an additional 60 msec. to load from its PROM.

Software can determine the state of the SPI-200 by polling the CSR. During the time the Altera chip is loading, the CSR will read 0xFFFF, as the data bus transceiver will have its outputs disabled. Once the Altera chip has loaded, the CSR will read 0x0100 until the IP Reset* signal is removed, at which time the CSR will read 0x0000. Some IPs take additional time to load FPGAs or perform other initialization functions after IP Reset* is removed.

The assertion of the DSP-LINK3 /RESET signal does not re-initialize the Altera FPGA. It does reset the GCSR and ICSR, the IP State Machine and the Memory Page Registers. It also generates a 260 msec. IP Reset* signal.

IP Accesses

All IPs are accessed with Ready Controlled cycles. The SPI-200 does not insert any hold states and is capable of zero wait state IP accesses for all IP cycle types. Each of the different DSP-Link3 cycle types will generally have a different base address on the processor board. Check the manual for the specific addresses for the board used. The following tables can then be used as offsets to each of the spaces. The address for each IP register will be the result of the following calculation:

Processor Board DSP-Link3 Cycle Type + Board ID + IP Slot + IP Space + IP Register Offset.

See the Addressing section for the Board ID, IP Slot and IP Space values. The IP Register Offset will depend on the specific IP being accessed. See the IP Manual for this value.

Example 3: Read the first byte of the ID PROM in IP A on Board zero. The host Ready Controlled cycle base address is 0x600000.

1. Read 0x00490000 at 0x600080

Because the DSP-Link3 bus has only 16 address lines and the IP Bus has 22 address lines for memory cycles, each IP slot has an 11 bit page register. The page register bits make up the upper 11 address lines while the lower 11 address lines come directly from the DSP-Link3 address lines during an IP Memory cycle access. This gives a 2K word page size. The page register does not need to be re-written for accesses within the current page. The page register is written by either Standard /ASTRB or Standard FAST /ASTRB cycles. The value of the address lines are latched into the page register during the /ASTRB cycle, not the contents of the data lines. The data should be '0'. The page registers are write only.

Example 4: Write 0x9876 to the memory location 0x123456 in IP D on Board two. The host processor Standard FAST ASTRB/ cycle base address is 0x500000 and the Ready Controlled cycle base address is 0x600000.

1. Write 0 to 0x50B246 - sets the page register value to 0x246
2. Write 0x9876 to 0x60B456 - writes to the IP

Interrupts

The SPI-200 maps the two interrupts from each IP Slot to one of the four DSP-LINK3 /INTx signals. The specific /INTx signal is determined for each IP Slot by two bits in the ICSR. The interrupts from an IP slot may be mapped to any /INTx signal independent of the other slots. Each /INTx signal has a separate interrupt enable in the GCSR.

Example 5: Map IP A interrupts to /INT0, IP B interrupts to /INT3, IP C interrupts to /INT0 and keep IP D interrupts disabled by mapping them to /INT2.
1. Write 0x8C00 to ICSR - maps IP interrupts
2. Write 0x0XBX to the GCSR - enables /INT0 and /INT3 (X values will depend on the desired features utilized)

The lower eight bits of the ICSR reflect the state of the eight possible interrupt request lines. Interrupts are cleared by the accessing the IP. See the IP manual for a description of how to clear the interrupt.

The DSP-Link3 bus shares the four /INTx lines between all boards. If more than one board is using the same interrupt, it is the job of the Interrupt Service Routine (ISR) to determine the source and act accordingly. The ISR should read the low eight bits of the ICSR to establish if the SPI-200 caused the interrupt and which IP is generating the it if more than one IP is sharing the level. It can then call the appropriate routine to clear the interrupt.

All IPs capable of generating interrupts must also supply an Interrupt Vector during an interrupt acknowledge (IACK) cycle. Since the DSP-Link3 bus does not have an inherent IACK cycle, the SPI-200 has a separate address space for each IP which, when read from, will create an IACK cycle. Reading from offset address 0x0 will read the IntReq0* Interrupt Vector and address 0x1 will read the IntReq1* Interrupt Vector. The vector will normally be read inside the ISR. The vectors do not have to be read if the IP does nothing more with an IACK cycle than output the vector. This is the case with most IPs, but check the individual IP's documentation.

IP Bus Time-Out

The SPI-200 has an IP bus error timer. It will time out if the IP being accessed does not respond within 32 usecs. and generate an internal Acknowledge ending the DSP-Link3 cycle. Bit 8 in the GCSR will also be set indicating a bus error occurred. This allows the IP slots to be interrogated during start up to determine if an IP is installed or not. Without this feature, accessing an IP slot which does not respond will lock up the processor. Accesses to addresses other than a valid IP slot will not start the timer, resulting in a hung processor. The Bus Error bit in the GCSR must be cleared by writing a '0' to it. Please refer to the Control and Status register bit map section below for more information.

DSP-LINK3 Interface

The SPI-200 uses a 64 pin ribbon cable connector for the DSP-Link3 connection. All power and ground connections are made through the ISA card edge connector. The D0..D15 lines are driven low during read cycles and ignored during write cycles.

64 Pin Ribbon Connector Pin Assignment

Pin #	Signal		Pin #	Signal
1	V_{CC} [1]		2	A15
3	A14		4	A13
5	A12		6	A11
7	A10		8	A9
9	A8		10	A7
11	A6		12	A5
13	A4		14	A3
15	A2		16	A1
17	A0		18	R/W_
19	/RESET		20	GND
21	/DSTRB		22	GND
23	/ASTRB		24	GND
25	/RDY		26	GND
27	/INT0		28	GND
29	/INT1		30	GND
31	/INT2		32	GND
33	/INT3		34	GND
35	D31		36	D30
37	D29		38	D28
39	D27		40	D26
41	D25		42	D24
43	D23		44	D22
45	D21		46	D20
47	D19		48	D18
49	D17		50	D16
51	D15		52	D14
53	D13		54	D12
55	D11		56	D10
57	D9		58	D8
59	D7		60	D6
61	D5		62	D4
63	D3		64	D2
65	D1		66	D0
67	GND		68	RSVD

Figure 8 DSP-Link3 64 Pin Ribbon Connector Pin Assignment

1) V_{cc} from the ribbon connector is not used by the SPI-200. Power is taken from the ISA bus card edge connector.

IndustryPack Interface

Each IndustryPack is mounted to the SPI-200 on two 50 pin connectors. One connector, designated the Logic Connector, provides the interface to all the IP Bus signals. The other connector, designated the IO Connector, provides the 50 IO connections for each IP. Each IO Connector is routed to a right angle 50 pin latching IDC connector on the front panel. The IO Connector and front panel connector are wired pin for pin, making the IO pin out assignments for an IP the same as the front panel pin out.

Logic Connector Pin Assignments

The table below gives the pin assignments for the IndustryPack® Logic for each of the IP Slots on the SPI-200. The functions of the pins are defined by the ANSI/VITA 4-1995 IP Module Specification. The Error*, DMAck0*, DMAck1* signals have 4.7K Ohm pull up resistors and the DMAEnd* signal has a 1.2K Ohm pull up resistor. The functions of these pins are unsupported. The Strobe* lines from each IP slot are run to a separate pin on a four position shunt block.

Pin #	Signal		Pin #	Signal
1	GND		2	CLK
3	Reset*		4	D0
5	D1		6	D2
7	D3		8	D4
9	D5		10	D6
11	D7		12	D8
13	D9		14	D10
15	D11		16	D12
17	D13		18	D14
19	D15		20	BS0*
21	BS1*		22	-12V
23	+12V		24	+5V
25	GND		26	GND
27	+5V		28	R/W*
29	IDSel*		30	DMAReq0*
31	MemSel*		32	DMAReq1*
33	IntSel*		34	DMAck*
35	IOSel*		36	Reserved
37	A1		38	DMAEnd*
39	A2		40	Error*
41	A3		42	IntReq0*
43	A4		44	IntReq1*
45	A5		46	Strobe*
47	A6		48	Ack*
49	Reserved		50	GND

Figure 10 IP Logic Connector Pin Assignment

I/O Connector Pin Assignment

Pin #	Signal		Pin #	Signal
1	I/O 1		2	I/O 2
3	I/O 3		4	I/O 4
5	I/O 5		6	I/O 6
7	I/O 7		8	I/O 8
9	I/O 9		10	I/O 10
11	I/O 11		12	I/O 12
13	I/O 13		14	I/O 14
15	I/O 15		16	I/O 16
17	I/O 17		18	I/O 18
19	I/O 19		20	I/O 20
21	I/O 21		22	I/O 22
23	I/O 23		24	I/O 24
25	I/O 25		26	I/O 26
27	I/O 27		28	I/O 28
29	I/O 29		30	I/O 30
31	I/O 31		32	I/O 32
33	I/O 33		34	I/O 34
35	I/O 35		36	I/O 36
37	I/O 37		38	I/O 38
39	I/O 39		40	I/O 40
41	I/O 41		42	I/O 42
43	I/O 43		44	I/O 44
45	I/O 45		46	I/O 46
47	I/O 47		48	I/O 48
49	I/O 49		50	I/O 50

Figure 11 IP IO Connector Pin Assignment

Pin 1 on IP connectors is marked with a square pad, observable from the solder side of the respective board. Pin 1 is also shown on the silk-screen for each connector.

The pin assignment of the IP I/O connector is fixed by the connector manufacturer and repeated in the IP Module Specification. This assignment is shown in Figure 12 below.

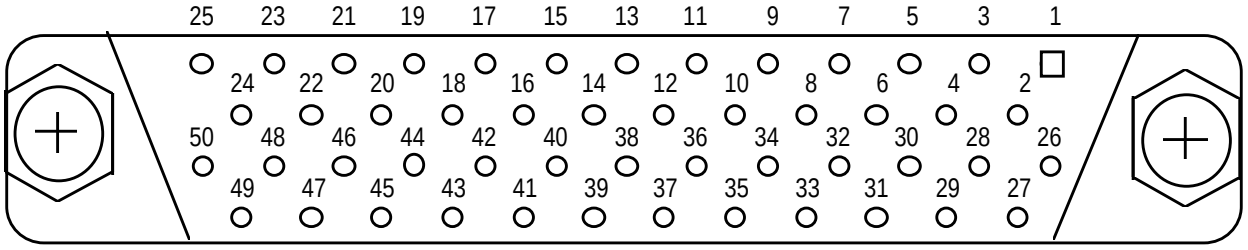


Figure 12 IndustryPack Connector Pin Numbering

(*Viewed from solder side of SPI-200)*

Each of the 50 pins on each I/O connector for the IndustryPack® slots A, B, C and D connects to an identically numbered pin on the four corresponding 50 pin IDC connectors.

Interfacing to the outside world—the I/O cabling—remains the responsibility of the system integrator or end-user/engineer. SBS Technologies offers cables and terminal blocks which may aid in debugging or be used for systems integration.

Installation of IndustryPacks

IndustryPacks are installed on the SPI-200 carrier board by simply snapping them in. Press the IP and the carrier board together with your fingers until the two pairs of mating connectors are flush. The connectors are keyed, so the IP can only be installed correctly. Proper anti-static handling procedures should be followed.

There are four locations for IPs. These are identified as Industry Pack A, Industry Pack B, Industry Pack C and Industry Pack D. The silk screen lettering on the SPI-200 shows the location of each.

After an IP has been installed, four stainless steel screws may be used to secure the IP to the carrier board. This is normally necessary only in high vibration or shock environments. Insert the screw through the IP and the two connectors. Attach the nut on the solder side of the SPI-200. Tighten using small tools, taking care not to damage either the IP or the support board. The screws used are standard (metric) M2 x 18 stainless slotted flat head. The screws and nuts are supplied with each IP.

User Options

Shunts & Test Points

The SPI-200 has two shunt for determining the board address and an IP Strobe* shunt block. It also has several test points available for configuration and debugging. The Test Points are labeled on the silk-screen.

E1 Strobe

Each IndustryPack® has one pin on the logic interface labeled "Strobe." This pin may be used for a digital strobe or clock signal related to the IPs functionality. On the SPI-200, this pin from each of the four IP slots is connected to one of the pins on the E1 shunt. Wires may be added to connect combinations of the IP Strobe lines together. The factory default is to leave all these pins unconnected. Figure 13 lists the connections.

Pin	IP Slot
1	Slot D
2	Slot C
3	Slot B
4	Slot A

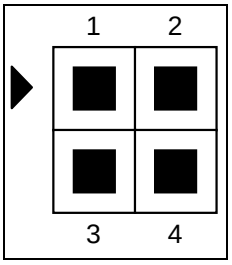
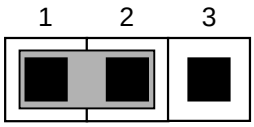


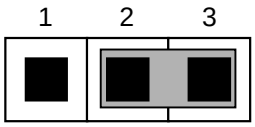
Figure 13 E1 Strobe Shunt Block

E2, E3 Board Select

The two three pin shunts, E2 and E3, are used to select one of four boards on the DSP-Link3 bus. The upper two address lines, A15 and A14 are used to decode the board select. Installing a shunt in position one (shunt on pin 1 and 2) pulls the line to logic low, installing it in position two (shunt on pin 2 and pin 3) pulls the line to a logic high. Figure 14 shows a table of the possible combinations. Removing a shunt is the same as putting it in position 2.



Position 1



Position 2

Shunt E2	Shunt E3	Corresponding Address A15, A14	Board Base Address
Position 1	Position 1	00	0x0000
Position 1	Position 2	01	0x4000
Position 2	Position 1	10	0x8000
Position 2	Position 2	11	0xC000

Figure 14 E2, E3 Board Select Shunts

Test points are provided to aid in diagnosing and debugging IndustryPack® logic interface problems. The test points labeled TPx may be used to attach scope probes. H1 is a header for downloading the Altera program when the U10 PROM is not installed. H2 is a header style connector with standard .025”sq. posts for logic analyzer connection. Neither of these headers is factory installed. SBS Technologies also has an IndustryPack® extender card, IP-BusProbe, with test points on all of the signals on the logic connector. This can aid in troubleshooting problems interfacing to IPs.

Test Points

Name	Function
TP1, TP2, TP3	Ground reference for test equipment
TP4	PLL Lock signal
TP5	GCSR Test bit
H2-1	GCSR Test bit
H2-2	R_Data_OE# - enables DSP-Link3 data read from IP
H2-3	Decode_En - Address line decode enable
H2-4	R_Data_Clk_En# - clock enable for buffer latching IP data on reads
H2-5	Mem_Addr_En - IP Memory cycle address enable
H2-6	W_Data_OE# - enables DSP-Link3 data written to IP
H2-7	Cyc_Sel_En - IP cycle select enable
H2-8	W_Data_Clk_En# - clock enable for buffer latching write data to IP
H2-9	TST7 - Internal Altera test point
H2-10	TST13 - Internal Altera test point

Electrical Interface

The SPI-200 uses an IDT162952 bi-directional register on the data lines D31..D16. This chip has balanced output drive and integral 25 Ohm internal series resistors as specified in the DSP-LINK3 Rev 0.94 Specification. The D15..D0 data lines have an IDT162244 with the input side tied to GND. This is enabled for reads only. All other lines are run directly into the Altera chip. The /INT0..3 output lines use 74F38 open collector NAND gates.

The /RESET, /DSTRB, /ASTRB, R/W, /RDY, /INT0..3 have passive 220 Ohm pull-up/330 Ohm pull-down termination resistors in sockets. These should be installed only on the last board on the ribbon cable the chain of DSP-Link3 boards.

Fuses

Caution: *SPI-200 has self resetting fuses added on the power inputs to all IP positions. This is consistent with safety related requirements of some organizations. Current limitation imposed by these fuses are shown in below:*

Supply	Applies To	Current	Fuse
+5V	IPs A,B,C,D combined	8.00 A @ 20°C, 4.88 A @ 70°C	F3
+12V	IPs A,B,C,D combined	5.00 A @ 20°C, 3.05 A @ 70°C	F1
–12V	IPs A,B,C,D combined	5.00 A @ 20°C, 3.05 A @ 70°C	F2

Figure 15 Fuse Chart

The fuses on the SPI-200 are Raychem PolySwitch® Resettable Fuses. These are positive temperature coefficient resistors that rapidly increase resistance in response to excessive currents. If the current rises above the rated current, the devices resistance abruptly rises, effectively turning off the power to the IP. Once the fault condition is removed, the switch cools and returns to its normal resistance, typically 0.05 Ohms. Figure 15 shows the current capacities for the IP's supplies at both 20°C and 70°C. All IP slots share the current from each of the fuses. The IP Specification limits each IP Module to 2 A for the +5V supply and 1 A for the ±12V supplies.

Construction and Reliability

IndustryPacks and their carriers were conceived and engineered for rugged industrial environments. The SPI-200 is constructed out of 0.062 inch thick FR4 material. The six copper layers consist of a power plane, ground plane, and four signal planes. The power planes significantly reduce conducted and emitted RF noise. They also assist in heat dissipation. Solder mask covers exposed traces on both sides.

Components are a mix of surface-mount and through-hole. Programmable ICs are socketed in low profile gold-plated screw-machine pin sockets. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed component into the socket. The factory can build socket-free boards, as well as extended temperature range boards, on special order.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is optionally secured to the carrier board with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

IndustryPacks provide a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of standard IPs. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Most of the components on the SPI-200 are CMOS. Many IPs are also primarily CMOS. Nonetheless adequate cooling of the host system is strongly recommended.

The SPI-200 features independent three-terminal pi filters on all power lines to the IndustryPacks. This aggressive filtering of high frequency noise allows precision analog and high speed digital IndustryPacks to be mixed in the same slot. The power line filters both block digital noise from elsewhere in the host system from entering an IP, and also block noise generated from an IP from entering the host system.

Warranty and Repair

SBS Technologies warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, SBS Technologies' sole responsibility shall be to repair, or at SBS's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to SBS. All replaced products become the sole property of SBS.

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Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS will not be responsible for damages due to improper packaging of returned items. For service on SBS products not purchased directly from SBS, contact your reseller. Products returned to SBS for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Technical Support
SBS Technologies, Inc.
1284 Corporate Center Drive
St. Paul, MN 55121-1245
Tel: (651) 905-4700
FAX: (651) 905-4701
Email: support.commercial@sbs.com

Specifications

This section gives the technical specification for the SPI-200.

Form Factor	Full size 16 bit ISA with DSP-LINK3 connector, no ISA Bus interface.
Number of IndustryPacks	Four single-wide, two double-wide or a combination.
DSP-Link3 cycles	Ready Controlled for IP access, Standard Access for all internal register accesses.
IP Clock - Rate	8 MHz or 32 MHz. Individually configurable on a per-IP basis.
IP Features Support	I/O, ID, Memory, Interrupts.
IP Memory Size Supported	8 MB per IP using separate page registers for each IP.
Memory Map	Linear, fixed.
Base Address	Four possible addresses set by two jumpers.
Interrupts	Each IPís interrupts are fully programmable to any DSP-LINK3 /INT line.
I/O Interconnect	Four 50-pin IDC connectors.
Electrical Interface	One filter and fuse for each of the +5V, +/- 12V power supplies running to all the IPs. Fuses are resettable +5V @ 250 mA typical without IPs +12V @ 0 mA typical without IPs -12V @ 0 mA typical without IPs
Environmental	0°C to 70°C operating 5 to 95% relative humidity (non-condensing) -10 to +85°C storage

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