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XM-302-1

Three Channel
RS-232D/RS-422/RS-485
Transition Module for
IP-CM302

User Manual

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XM-302-1

3 Channel RS-232D/RS-422/RS-485 Transition Module for IP-CM302

SBS Technologies, Inc.
1284 Corporate Center Drive
St. Paul, MN 55121
Tel (651) 905-4700
FAX (651) 905-4701
Email: support.commercial@sbs.com
http://www.sbs.com

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Product Description

The IP-CM302 Transition Module-1 (XM1) implements the physical layer interface for RS-232D, RS422, and RS-485 for the IP-CM302 (IP). Transition module for ISDN (2B + D) is planned in the future. The transition module connects to the IP via a standard 50-pin ribbon cable to the IP carrier board. This cable may be a maximum of six feet in length. This permits mounting the transition module wherever convenient for the OEM or the systems integrator. It does not have to reside in a VME slot, although a VME front panel is provided with the XM1 for convenience.

Three channels are provided by the XM1. Each channel is available via a three row female right angle DB-15 connector.

Selection of interface is made possible through shunt and socketed resistor pack installment. See User Option sections.

Power must be provided to the XM1 in +5, +12 and -12 volts. Power lines are fused on-board for safety reasons.

The XM1 is shipped with its three channels configured as RS-232D.

Figure 1 represents a block diagram of the XM1:

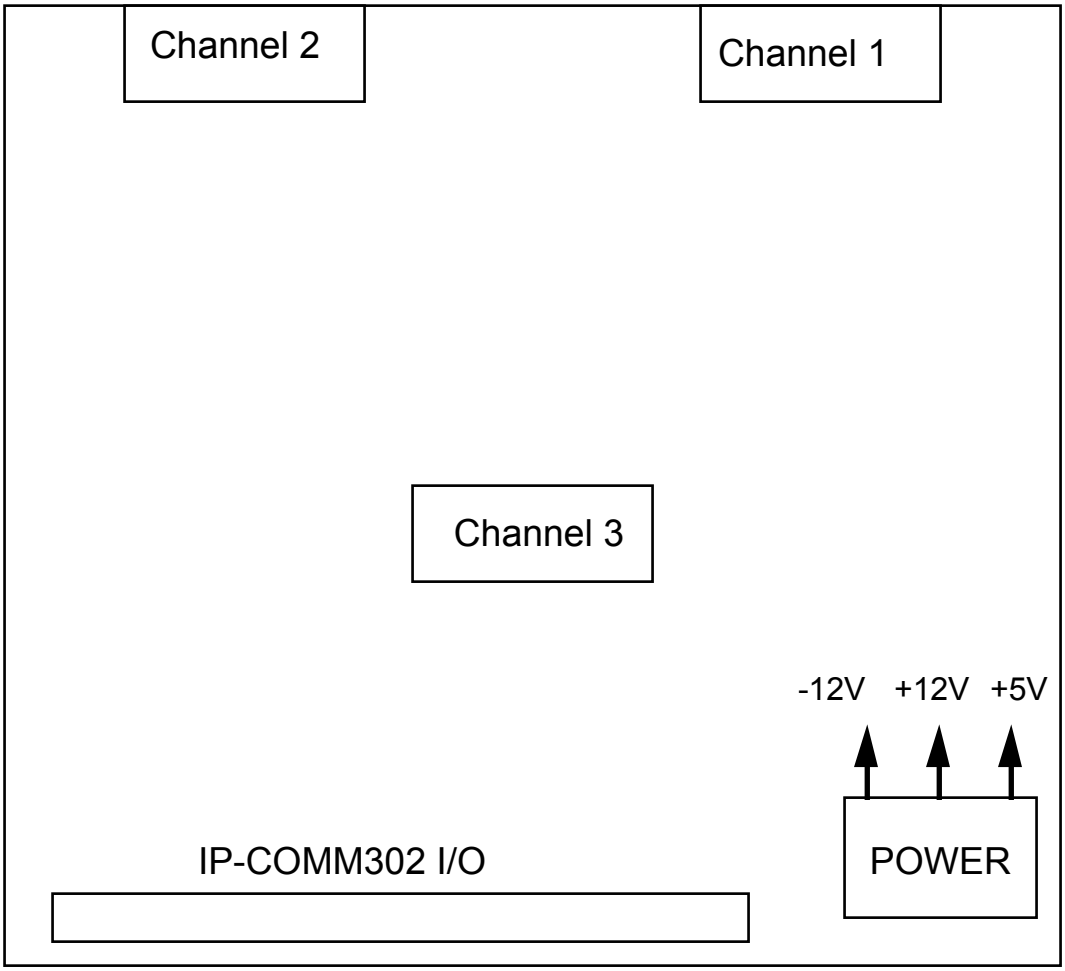


Figure 1 IP-CM302 Transition Module Block Diagram

Channel One User Options

RS-232D

Channel one is configured for RS-232D by shunt installment as outlined in figure 2.

E2.1 .. E2.15 - E1.1 .. E1.15	IN
E3.1 .. E3.15 - E1.1 .. E1.15	OUT
E18.1 - E18.2 E18.3 - E18.4 E18.5 - E18.6 E18.7 - E18.8	IN IN IN IN
E19.1 - E19.2 E19.3 - E19.4 E19.5 - E19.6	OUT OUT OUT
E14	OUT
E15	OUT
E16	OUT
E17.1 - E17.2	OUT

Figure 2 Channel One RS-232D Shunt Configuration

Transmit clock is configurable bidirectional. Receive clock is receive only. Figure 3 outlines how to configure clocks via shunt installment:

E11 in E12 out	TCLK1 is configured as transmit (default)
E11 out E12 in	TCLK1 is configured as receive
E13 in	RCLK1 is configured as receive (default)

Figure 3 Channel One RS-232D Transmit and receive Clock Configuration

Shunt E40 is DB-15 connector (J2) shell ground. If installed, the shell ground is connected to the signal ground.

None of the on-board resistor packs are relevant to RS-232 configuration and may be left out of their sockets.

General purpose I/O lines PB8 and PB9 are used as DTR1 and DSR1 signals respectively.

The RS-232 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-232-D. The drivers and receivers are MC1488 and MC1489 respectively.

The figure 4 below outlines the RS-232 signal mapping into J2 (DB-15) connector:

DB-15 Pin	RS-232 Signal	I/O
Shell	GND (Shield)	–
1	DCD (Recv. Line Sig. Det.)	I
2	RxD (Received Data)	I
3	TxD (Transmitted Data)	O
4	DTR (Data Terminal Ready)	O
5	GND (Signal Ground)	–
6	DSR (Data Set Ready)	I
7	RTS (Request To Send)	O
8	CTS (Clear To Send)	I
9	(Ring Indicator) Not Connected	
10	Not Connected	
11	Not Connected	
12	Not Connected	
13	TCLK (Transmit Clock)	I/O
14	Not Used	
15	RCLK (Receive Clock)	I

Figure 4 Channel One RS-232D Connector Pin Assignment

The default shunt installment is per figure 2 and 3.

RS-422

Channel one is configured for RS-422 by shunt installment as outlined in figure 5 below.

E2.1 .. E2.15 - E1.1 .. E1.15	OUT
E3.1 .. E3.15 - E1.1 .. E1.15	IN
E18.1 - E18.2 E18.3 - E18.4 E18.5 - E18.6 E18.7 - E18.8	OUT OUT OUT OUT
E19.1 - E19.2 E19.3 - E19.4 E19.5 - E19.6	IN IN IN
E14	OUT
E15	IN: TCLK1 in receive mode OUT: TCLK1 in transmit mode
E16	IN: RCLK1 in receive mode OUT: RCLK1 in transmit mode
E13	OUT
E12	OUT
E11	OUT

Figure 5 Channel One RS-422 Shunt Configuration

Transmit clock is configurable bidirectional by general purpose I/O line PB9. The PB9 driven to logic one transmits TCLK1 and driven to logic zero receives TCLK1. Upon power-up or reset the PB9 is set to logic zero therefore receiving TCLK1. Receive clock direction is determined by shunt E17 installment. E17 installed, configures RCLK1 in receive mode and removed, in transmit mode.

General purpose I/O line PB8 controls the output enable of TXD1. PB8 is used for RS-485 option and the user should set this bit to logic one for RS-422. The power-up or reset state of PB8 is logic zero.

DTR1 and DSR1 signals are omitted.

The RS-422 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-422A. The drivers and receivers are SN75176 and SN75173 respectively.

Resistor packs are provided to differentially terminate receiving RS-422 signals. Common termination value is 120Ω. Resistor packs are socketed allowing the user to install any value required. Figure 6 below outlines the resistor pack options.

RP10	do not install (used for RS-485 only)
RP11	do not install (used for RS-485 only)
RP12	do not install (used for RS-485 only)
RP13	install if TCLK1 is configured as receive do not install if TCLK1 is configured as transmit
RP14	IN
RP15	install if RCLK1 is configured as receive do not install if RCLK1 is configured as transmit

Figure 6 Channel One RS-422 Resistor Pack Configuration

The figure 7 below outlines the RS-422 signal mapping into J2 (DB-15) connector:

DB-15 Pin	RS-422 Signal	I/O
Shell	GND (Shield)	–
1	TxD+ (Transmitted Data)	O
2	DCD+ (Recv. Line Sig. Det.)	I
3	RTS+ (Request To Send)	O
4	RCLK+ (Receive Clock)	I/O
5	GND (Signal Ground)	–
6	DCD– (Recv. Line Sig. Det.)	I
7	RxD+ (Received Data)	I
8	RCLK– (Receive Clock)	I/O
9	CTS+ (Clear To Send)	I
10	TCLK+ (Transmit Clock)	I/O
11	TxD– (Transmitted Data)	O
12	RxD– (Received Data)	I
13	RTS– (Request To Send)	O
14	CTS– (Clear To Send)	I
15	TCLK– (Transmit Clock)	I/O

Figure 7 Channel One RS-422 Connector Pin Assignment

RS-485

Channel one is configured for RS-485 by shunt installment as outlined in figure 8.

E2.1 .. E2.15 - E1.1 .. E1.15	OUT
E3.1 .. E3.15 - E1.1 .. E1.15	IN
E18.1 - E18.2 E18.3 - E18.4 E18.5 - E18.6 E18.7 - E18.8	OUT OUT OUT OUT
E19.1 - E19.2 E19.3 - E19.4 E19.5 - E19.6	IN IN IN
E14	IN
E15	IN: TCLK1 in receive mode OUT: TCLK1 in transmit mode
E16	IN: RCLK1 in receive mode OUT: RCLK1 in transmit mode
E13	OUT
E12	OUT
E11	OUT

Figure 8 Channel One RS-485 Shunt Configuration

Transmit and receive signals TXD-/RXD- and TXD+/RXD+ are bidirectional. The general purpose I/O line PB8 controls the direction. TXD-/RXD- and TXD+/RXD+ are driven when PB8 is set and received if cleared. The default power-up or reset state of PB8 is logic zero therefore configuring TXD-/RXD- and TXD+/RXD+ in receive mode. Receive signal RXD is always in listen mode.

Transmit clock is configurable bidirectional by general purpose I/O line PB9. The PB9 driven to logic one transmits TCLK1 and driven to logic zero receives TCLK1. Upon power-up or reset the PB9 is set to logic zero therefore receiving TCLK1. Receive clock

direction is determined by shunt E17 installment. E17 installed configures RCLK1 in receive mode and removed in transmit mode.

DTR1 and DSR1 signals are omitted.

The RS-485 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-485A. The drivers and receivers are SN75176 and SN75173 respectively.

Resistor packs are provided to differentially terminate receiving RS-485 signals. Common termination value is 120Ω. Resistor packs are socketed allowing the user to install any value required. Figure 9 below outlines the resistor pack options.

RP10	install
RP11	do not install
RP12	install
RP13	install if TCLK1 is configured as receive do not install if TCLK1 is configured as transmit
RP14	IN
RP15	install if RCLK1 is configured as receive do not install if RCLK1 is configured as transmit

Figure 9 Channel One RS-485 Resistor Pack Configuration

RP10 and RP12 are used to bias the RS-485 drivers when tri-stated (PB8 and PB9 are set to logic zero). The common value is 1k. These RPs are socketed allowing the user to install other bias values.

Figure 10 below outlines the RS-485 signal mapping into J2 (DB-15) connector:

DB-15 Pin	RS-485 Signal	I/O
Shell	GND (Shield)	–
1	TxD+/RxD+ (Transmitted & Received Data)	I/O
2	DCD+ (Recv. Line Sig. Det.)	I
3	Not Connected	
4	RCLK+ (Receive Clock)	I/O
5	GND (Signal Ground)	–
6	DCD– (Recv. Line Sig. Det.)	I
7	Not Connected	
8	RCLK– (Receive Clock)	I/O
9	CTS+ (Clear To Send)	I
10	TCLK+ (Transmit Clock)	I/O
11	TxD–/RxD- (Transmitted and Received Data)	I/O
12	Not Connected	
13	Not Connected	
14	CTS– (Clear To Send)	I
15	TCLK– (Transmit Clock)	I/O

Figure 10 Channel One RS-485 Connector Pin Assignment

Channel Two User Options

RS-232D

Channel two is configured for RS-232D by shunt installment as outlined in figure 11.

E5.5 .. E5.15 - E4.1 .. E4.15	IN
E6.1 .. E6.15 - E4.1 .. E4.15	OUT
E28.1 - E28.2 E28.3 - E28.4 E28.5 - E28.6 E28.7 - E28.8	IN IN IN IN
E29.1 - E29.2 E29.3 - E29.4 E29.5 - E29.6	OUT OUT OUT
E24	OUT
E25	OUT
E26	OUT
E27.1 - E27.2	OUT

Figure 11 Channel Two RS-232D Shunt Configuration

Transmit clock is configurable bidirectional. Receive clock is receive only. Figure 12 outlines how to configure clocks via shunt installment.

E21 in E22 out	TCLK2 is configured as transmit (default)
E21 out E22 in	TCLK2 is configured as receive
E23 in	RCLK2 is configured as receive (default)

Figure 12 Channel Two RS-232D Transmit and receive Clock Configuration

Shunt E41 is DB-15 connector (J3) shell ground. If installed, the shell ground is connected to the signal ground.

None of the on-board resistor packs are relevant to RS-232 configuration and may be left out of their sockets.

General purpose I/O lines PB10 and BRG2 are used as DTR1 and DSR1 signals respectively.

The RS-232 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-232-D. The drivers and receivers are MC1488 and MC1489 respectively.

The figure 13 below outlines the RS-232 signal mapping into J3 (DB-15) connector:

DB-15 Pin	RS-232 Signal	I/O
Shell	GND (Shield)	–
1	DCD (Recv. Line Sig. Det.)	I
2	RxD (Received Data)	I
3	TxD (Transmitted Data)	O
4	DTR (Data Terminal Ready)	O
5	GND (Signal Ground)	–
6	DSR (Data Set Ready)	I
7	RTS (Request To Send)	O
8	CTS (Clear To Send)	I
9	(Ring Indicator) Not Connected	
10	Not Connected	
11	Not Connected	
12	Not Connected	
13	TCLK (Transmit Clock)	I/O
14	Not Used	
15	RCLK (Receive Clock)	I

Figure 13 Channel Two RS-232D Connector Pin Assignment

The default shunt installment is per figure 11 and 12.

RS-422

Channel two is configured for RS-422 by shunt installment as outlined in figure 14 below.

E5.1 .. E5.15 - E4.1 .. E4.15	OUT
E6.1 .. E6.15 - E4.1 .. E4.15	IN
E28.1 - E28.2 E28.3 - E28.4 E28.5 - E28.6 E28.7 - E28.8	OUT OUT OUT OUT
E29.1 - E29.2 E29.3 - E29.4 E29.5 - E29.6	IN IN IN
E24	OUT
E25	IN: TCLK2 in receive mode OUT: TCLK2 in transmit mode
E26	IN: RCLK2 in receive mode OUT: RCLK2 in transmit mode
E23	OUT
E22	OUT
E21	OUT

Figure 14 Channel Two RS-422 Shunt Configuration

Transmit clock is configurable bidirectional by general purpose I/O line BRG2. The BRG2 driven to logic one transmits TCLK2 and driven to logic zero receives TCLK2. Upon power-up or reset the BRG2 is set to logic zero therefore receiving TCLK2. Receive clock direction is determined by shunt E27 installment. E27 installed, configures RCLK2 in receive mode and removed, in transmit mode.

General purpose I/O line PB10 controls the output enable of TXD. PB10 is used for RS-485 option and the user should set this bit to logic one for RS-422. The power-up or reset state of PB10 is logic zero.

DTR2 and DSR2 signals are omitted.

The RS-422 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-422A. The drivers and receivers are SN75176 and SN75173 respectively.

Resistor packs are provided to differentially terminate receiving RS-422 signals. Common termination value is 120Ω. Resistor packs are socketed allowing the user to install any value required. Figure 15 below outlines the resistor pack options.

RP20	do not install (used for RS-485 only)
RP21	do not install (used for RS-485 only)
RP22	do not install (used for RS-485 only)
RP23	install if TCLK2 is configured as receive do not install if TCLK2 is configured as transmit
RP24	IN
RP25	install if RCLK2 is configured as receive do not install if RCLK2 is configured as transmit

Figure 15 Channel Two RS-422 Resistor Pack Configuration

The figure 16 below outlines the RS-422 signal mapping into J3 (DB-15) connector:

DB-15 Pin	RS-422 Signal	I/O
Shell	GND (Shield)	–
1	TxD+ (Transmitted Data)	O
2	DCD+ (Recv. Line Sig. Det.)	I
3	RTS+ (Request To Send)	O
4	RCLK+ (Receive Clock)	I/O
5	GND (Signal Ground)	–
6	DCD– (Recv. Line Sig. Det.)	I
7	RxD+ (Received Data)	I
8	RCLK– (Receive Clock)	I/O
9	CTS+ (Clear To Send)	I
10	TCLK+ (Transmit Clock)	I/O
11	TxD– (Transmitted Data)	O
12	RxD– (Received Data)	I
13	RTS– (Request To Send)	O
14	CTS– (Clear To Send)	I
15	TCLK– (Transmit Clock)	I/O

Figure 16 Channel Two RS-422 Connector Pin Assignment

RS-485

Channel two is configured for RS-485 by shunt installment as outlined in figure 17.

E5.1 .. E5.15 - E4.1 .. E4.15	OUT
E6.1 .. E6.15 - E4.1 .. E4.15	IN
E28.1 - E28.2 E28.3 - E28.4 E28.5 - E28.6 E28.7 - E28.8	OUT OUT OUT OUT
E29.1 - E29.2 E29.3 - E29.4 E29.5 - E29.6	IN IN IN
E24	IN
E25	IN: TCLK2 in receive mode OUT: TCLK2 in transmit mode
E26	IN: RCLK2 in receive mode OUT: RCLK2 in transmit mode
E23	OUT
E22	OUT
E21	OUT

Figure 17 Channel Two RS-485 Shunt Configuration

Transmit and receive signals TXD-/RXD- and TXD+/RXD+ are bidirectional. The general purpose I/O line PB10 controls the direction. TXD-/RXD- and TXD+/RXD+ are driven when PB10 is set and received if cleared. The default power-up or reset state of PB10 is logic zero therefore configuring TXD-/RXD- and TXD+/RXD+ in receive mode. Receive signal RXD is always in listen mode.

Transmit clock is configurable bidirectional by general purpose I/O line BRG2. The BRG2 driven to logic one transmits TCLK2 and driven to logic zero receives TCLK2. Upon power-up or reset the BRG2 is set to logic zero therefore receiving TCLK2. Receive clock direction is determined by shunt E27 installment. E27 installed configures RCLK2 in receive mode and removed in transmit mode.

DTR2 and DSR2 signals are omitted.

The RS-485 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-485A. The drivers and receivers are SN75176 and SN75173 respectively.

Resistor packs are provided to differentially terminate receiving RS-485 signals. Common termination value is 120Ω. Resistor packs are socketed allowing the user to install any value required. Figure 18 below outlines the resistor pack options.

RP20	install
RP21	do not install
RP22	install
RP23	install if TCLK2 is configured as receive do not install if TCLK2 is configured as transmit
RP24	IN
RP25	install if RCLK2 is configured as receive do not install if RCLK2 is configured as transmit

Figure 18 Channel Two RS-485 Resistor Pack Configuration

RP20 and RP22 are used to bias the RS-485 drivers when tri-stated (PB10 and BRG2 are set to logic zero). The common value is 1k. These RPs are socketed allowing the user to install other bias values.

Figure 19 below outlines the RS-485 signal mapping into J3 (DB-15) connector:

DB-15 Pin	RS-485 Signal	I/O
Shell	GND (Shield)	–
1	TxD+/RxD+ (Transmitted & Received Data)	I/O
2	DCD+ (Recv. Line Sig. Det.)	I
3	Not Connected	
4	RCLK+ (Receive Clock)	I/O
5	GND (Signal Ground)	–
6	DCD– (Recv. Line Sig. Det.)	I
7	Not Connected	
8	RCLK– (Receive Clock)	I/O
9	CTS+ (Clear To Send)	I
10	TCLK+ (Transmit Clock)	I/O
11	TxD–/RxD- (Transmitted and Received Data)	I/O
12	Not Connected	
13	Not Connected	
14	CTS– (Clear To Send)	I
15	TCLK– (Transmit Clock)	I/O

Figure 19 Channel Two RS-485 Connector Pin Assignment

Channel Three User Options

RS-232D

Channel Three is configured for RS-232D by shunt installment as outlined in figure 20.

E8.1 .. E8.15 - E7.1 .. E7.15	IN
E9.1 .. E9.15 - E7.1 .. E7.15	OUT
E38.1 - E38.2 E38.3 - E38.4 E38.5 - E38.6 E38.7 - E38.8	IN IN IN IN
E39.1 - E39.2 E39.3 - E39.4 E39.5 - E39.6	OUT OUT OUT
E34	OUT
E35	OUT
E36	OUT
E37.1 - E37.2	OUT

Figure 20 Channel Three RS-232D Shunt Configuration

Transmit clock is configurable bidirectional. Receive clock is receive only. Figure 21 outlines how to configure clocks via shunt installment:

E31 in E32 out	TCLK3 is configured as transmit (default)
E31 out E32 in	TCLK3 is configured as receive
E33 in	RCLK3 is configured as receive (default)

Figure 21 Channel Three RS-232D Transmit and receive Clock Configuration

Shunt E42 is DB-15 connector (J4) shell ground. If installed, the shell ground is connected to the signal ground.

None of the on-board resistor packs are relevant to RS-232 configuration and may be left out of their sockets.

General purpose I/O lines PB11 and BRG3 are used as DTR3 and DSR3 signals respectively.

The RS-232 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-232-D. The drivers and receivers are MC1488 and MC1489 respectively.

Figure 22 below outlines the RS-232 signal mapping into J4 (DB-15) connector:

DB-15 Pin	RS-232 Signal	I/O
Shell	GND (Shield)	–
1	DCD (Recv. Line Sig. Det.)	I
2	RxD (Received Data)	I
3	TxD (Transmitted Data)	O
4	DTR (Data Terminal Ready)	O
5	GND (Signal Ground)	–
6	DSR (Data Set Ready)	I
7	RTS (Request To Send)	O
8	CTS (Clear To Send)	I
9	(Ring Indicator) Not Connected	
10	Not Connected	
11	Not Connected	
12	Not Connected	
13	TCLK (Transmit Clock)	I/O
14	Not Used	
15	RCLK (Receive Clock)	I

Figure 22 Channel Three RS-232D Connector Pin Assignment

The default shunt installment is per figure 20 and 21.

RS-422

Channel Three is configured for RS-422 by shunt installment as outlined in figure 23 below.

E8.1 .. E8.15 - E7.1 .. E7.15	OUT
E9.1 .. E9.15 - E7.1 .. E7.15	IN
E38.1 - E38.2 E38.3 - E38.4 E38.5 - E38.6 E38.7 - E38.8	OUT OUT OUT OUT
E39.1 - E39.2 E39.3 - E39.4 E39.5 - E39.6	IN IN IN
E34	OUT
E35	IN: TCLK3 in receive mode OUT: TCLK3 in transmit mode
E36	IN: RCLK3 in receive mode OUT: RCLK3 in transmit mode
E33	OUT
E32	OUT
E31	OUT

Figure 23 Channel Three RS-422 Shunt Configuration

Transmit clock is configurable bidirectional by general purpose I/O line BRG3. The BRG3 driven to logic one transmits TCLK3 and driven to logic zero receives TCLK3. Upon power-up or reset the BRG3 is set to logic zero therefore receiving TCLK3. Receive clock direction is determined by shunt E37 installment. E37 installed, configures RCLK3 in receive mode and removed, in transmit mode.

General purpose I/O line PB11 controls the output enable of TXD1. PB11 is used for RS-485 option and the user should set this bit to logic one for RS-422. The power-up or reset state of PB11 is logic zero.

DTR3 and DSR3 signals are omitted.

The RS-422 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-422A. The drivers and receivers are SN75176 and SN75173 respectively.

Resistor packs are provided to differentially terminate receiving RS-422 signals. Common termination value is 120Ω. Resistor packs are socketed allowing the user to install any value required. Figure 24 below outlines the resistor pack options.

RP30	do not install (used for RS-485 only)
RP31	do not install (used for RS-485 only)
RP32	do not install (used for RS-485 only)
RP33	install if TCLK3 is configured as receive do not install if TCLK3 is configured as transmit
RP34	IN
RP35	install if RCLK3 is configured as receive do not install if RCLK3 is configured as transmit

Figure 24 Channel Three RS-422 Resistor Pack Configuration

The figure 25 below outlines the RS-422 signal mapping into J4 (DB-15) connector:

DB-15 Pin	RS-422 Signal	I/O
Shell	GND (Shield)	–
1	TxD+ (Transmitted Data)	O
2	DCD+ (Recv. Line Sig. Det.)	I
3	RTS+ (Request To Send)	O
4	RCLK+ (Receive Clock)	I/O
5	GND (Signal Ground)	–
6	DCD– (Recv. Line Sig. Det.)	I
7	RxD+ (Received Data)	I
8	RCLK– (Receive Clock)	I/O
9	CTS+ (Clear To Send)	I
10	TCLK+ (Transmit Clock)	I/O
11	TxD– (Transmitted Data)	O
12	RxD– (Received Data)	I
13	RTS– (Request To Send)	O
14	CTS– (Clear To Send)	I
15	TCLK– (Transmit Clock)	I/O

Figure 25 Channel Three RS-422 Connector Pin Assignment

RS-485

Channel Three is configured for RS-485 by shunt installment as outlined in figure 26.

E8.1 .. E8.15 - E7.1 .. E7.15	OUT
E9.1 .. E9.15 - E7.1 .. E7.15	IN
E38.1 - E38.2 E38.3 - E38.4 E38.5 - E38.6 E38.7 - E38.8	OUT OUT OUT OUT
E39.1 - E39.2 E39.3 - E39.4 E39.5 - E39.6	IN IN IN
E34	IN
E35	IN: TCLK3 in receive mode OUT: TCLK3 in transmit mode
E36	IN: RCLK3 in receive mode OUT: RCLK3 in transmit mode
E33	OUT
E32	OUT
E31	OUT

Figure 26 Channel Three RS-485 Shunt Configuration

Transmit and receive signals TXD-/RXD- and TXD+/RXD+ are bidirectional. The general purpose I/O line PB11 controls the direction. TXD-/RXD- and TXD+/RXD+ are driven when PB11 is set and received if cleared. The default power-up or reset state of PB11 is logic zero therefore configuring TXD-/RXD- and TXD+/RXD+ in receive mode. Receive signal RXD is always in listen mode.

Transmit clock is configurable bidirectional by general purpose I/O line BRG3. The BRG3 driven to logic one transmits TCLK3 and driven to logic zero receives TCLK3. Upon power-up or reset the BRG3 is set to logic zero therefore receiving TCLK3. Receive clock direction is determined by shunt E37 installment. E37 installed configures RCLK3 in receive mode and removed in transmit mode.

DTR3 and DSR3 signals are omitted.

The RS-485 drivers and receivers are in full conformance with the specification of EIA Standard No. EIA-485A. The drivers and receivers are SN75176 and SN75173 respectively.

Resistor packs are provided to differentially terminate receiving RS-485 signals. Common termination value is 120Ω. Resistor packs are socketed allowing the user to install any value required. Figure 27 below outlines the resistor pack options.

RP30	install
RP31	do not install
RP32	install
RP33	install if TCLK3 is configured as receive do not install if TCLK3 is configured as transmit
RP34	IN
RP35	install if RCLK3 is configured as receive do not install if RCLK3 is configured as transmit

Figure 27 Channel Three RS-485 Resistor Pack Configuration

RP30 and RP32 are used to bias the RS-485 drivers when tri-stated (PB11 and BRG3 are set to logic zero). The common value is 1k. These RPs are socketed allowing the user to install other bias values.

Figure 28 below outlines the RS-485 signal mapping into J4 (DB-15) connector:

DB-15 Pin	RS-485 Signal	I/O
Shell	GND (Shield)	–
1	TxD+/RxD+ (Transmitted & Received Data)	I/O
2	DCD+ (Recv. Line Sig. Det.)	I
3	Not Connected	
4	RCLK+ (Receive Clock)	I/O
5	GND (Signal Ground)	–
6	DCD– (Recv. Line Sig. Det.)	I
7	Not Connected	
8	RCLK– (Receive Clock)	I/O
9	CTS+ (Clear To Send)	I
10	TCLK+ (Transmit Clock)	I/O
11	TxD–/RxD- (Transmitted and Received Data)	I/O
12	Not Connected	
13	Not Connected	
14	CTS– (Clear To Send)	I
15	TCLK– (Transmit Clock)	I/O

Figure 28 Channel Three RS-485 Connector Pin Assignment

I/O Pin Wiring

This section gives the pin assignment for the XM1 I/O connector (J1) and power connector (P1).

Power connector (P1) pin assignment is provided in figure 29

Pin Number	Power
1	+5V
2	+12V
3	-12V
4	GND

Figure 29 Power Connector (P1) Pin Assignment

Pin one of P1 is indicated by square pad.

The recommended P1 manufacturer is Molex 26-48-1046. The mating cable connector is Molex 26-03-4041.

The channel I/O receptacles installed in J2, J3, and J4 are female 3-row DB-15 connectors.

The pin numbers given in Figures 31 correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the J1 numbers on the XM1. The third column gives the IP 68302-PQFP132 pin numbers as connected to the 50-pin IP I/O connector.

The pin numbering assignment of the J1 connector is shown below in Figure 30. Note pin 1 is square.

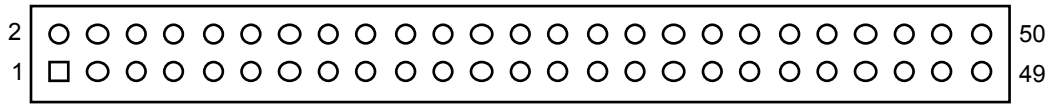


Figure 30 Flat Cable Connector Pin Numbering, Viewed from solder side of XM1

The user must adhere to figure 30 physical pin numbering when they mate their cable into the J1 connector. The user is cautioned that if J1 connector is a right angle its pin 1 is aligned with pin 49 of the cable, but, however if the J1 is straight, pin 1 aligns with pin 1 of the cable. Because of right angle J1 pin alignment conflict, the XM1 is shipped with straight J1.

The half-can sized crystal (Y1) allows the user to provide an optional baud rate generator clock to the IP. This part is socketed to allow the user to install a crystal at a required frequency. Pin 43 of J1 is the output of Y1.

J1 Pin Number	Signal	MC68302 Pin Number
1	RXD1/L1RXD	52
2	GND	
3	TXD1/L1TXD	80
4	GND	
5	RCLK1/L1CLK	82
6	GND	
7	TCLK1/L1SY0/SDS1	81
8	GND	
9	CD1/L1SY1	50
10	GND	
11	CTS1/L1GR	51
12	GND	
13	RTS1/L1RQ/GCIDCL	79
14	GND	
15	BRG1	76
16	GND	
17	RXD2/PA0	53
18	GND	
19	TXD2/PA1	54
20	GND	
21	RCLK2/PA2	55
22	GND	
23	TCLK2/PA3	56
24	GND	
25	CTS2/PA4	58
26	RTS2/PA5	59
27	CD2/PA6	60
28	BRG2/SDS2/PA7	61
29	GND	
30	RXD3/PA8	63
31	GND	
32	TXD3/PA9	64
33	GND	
34	RCLK3/PA10	65
35	GND	
36	TCLK3/PA11	66
37	GND	
38	CTS3/SPRXD	49
39	RTS3/SPTXD	78
40	CD3/SPCLK	77
41	BRG3/PA12	68
42	GND	
43	TIN1/PB3	111
44	GND	
45	IRQ1	97
46	GND	
47	PB8	118
48	PB9	119
49	PB10	120
50	PB11	121

Figure 31 XM1 I/O Connector (J1) Pin Assignment

Construction and Reliability

Transition modules were conceived and engineered for rugged industrial environments. The XM1 is constructed out of 0.062 inch thick FR4 V0 material. The four copper layers consist of two signal layers on the top and bottom, and two internal layers. Two internal layers are dedicated to power and ground planes.

The XM1 provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Repair

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS will not be responsible for damages due to improper packaging of returned items. For service on SBS Products not purchased directly from SBS contact your reseller. Products returned to SBS for repair by other than the original customer will be treated as out-of-warranty.

Specifications

This section gives the technical specification for the XM1

Number of Channels:	Three serial channels
I/O Interface:	Serial synchronous and asynchronous. RS232, RS-422, RS485
Performance:	See the MC68302 User Manual
Interface Connectors:	50 pin flat cable 4 pin power cable Three miniature 3-row female DB-15
Dimensions:	3.931 x 5.750 inches (Width X Length)
Construction:	4 Layer Printed Circuit, Through Hole and Surface Mount Components.
Temperature Coefficient:	.89 W/°C for uniform heat across IP
Test conditions	20°C, typical
Power Requirements	+5 VDC, 80 mA typ, fused at 0.5A +12 VDC, 40 mA typ, fused at 0.5A –12 VDC, 40 mA typ,fused at 0.5A
Environmental	Operating temperature: 0° to +70°C Humidity: 5% - 95% non-condensing Storage temperature: –10° to +85°C

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