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High Speed Serial HSS-PMC-CC User's Manual









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Applies to models:
HSS-PMC-CC04, HSS-PMC-CC08

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High Speed Serial HSS-PMC-CC User's Manual

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1: Introduction

This chapter introduces the *HSS-PMC-CC User's Manual*. It describes the contents of this manual, and the terminology and conventions used in this manual. The sections are as follows:

- Manual Overview
- HSS-PMC-CC Description
- Terminology
- Conventions



Cross Reference: Appendix A gives a brief summary of technical revisions made to this manual.

1.1 Manual Overview

This manual applies to the following model numbers (the last digit in the model number indicates the number of ports/channels):

- HSS-PMC-CC04
- HSS-PMC-CC08

Use this manual to familiarize yourself with the High Speed Serial HSS-PMC-CC card.

This manual contains the following chapters:

- Introduction (this chapter)
- Installing the Hardware
- Building the Driver
- Addressing
- Programming

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1.2 HSS-PMC-CC Description

The High Speed Serial HSS-PMC-CC module provides four or eight ports of high-speed serial data communications on a single-wide PMC module. You can use the HSS-PMC-CC module in many data communications, LAN/WAN networking and telecommunications applications. It supports a maximum data rate of 10 Mbit/sec for synchronous protocols using an external clock. The HSS-PMC-CC module supports up to 2 Mbit/sec for asynchronous protocols and popular baud rates of up to 921.6 Kbaud available using the standard 14.7456 MHz oscillator in RS-422 interface mode. Each of the ports are fully programmable to support many high performance serial communications protocols, such as asynchronous, HDLC, and SDLC. Figure 1.2.1 shows a simplified block diagram of the HSS-PMC-CC module.

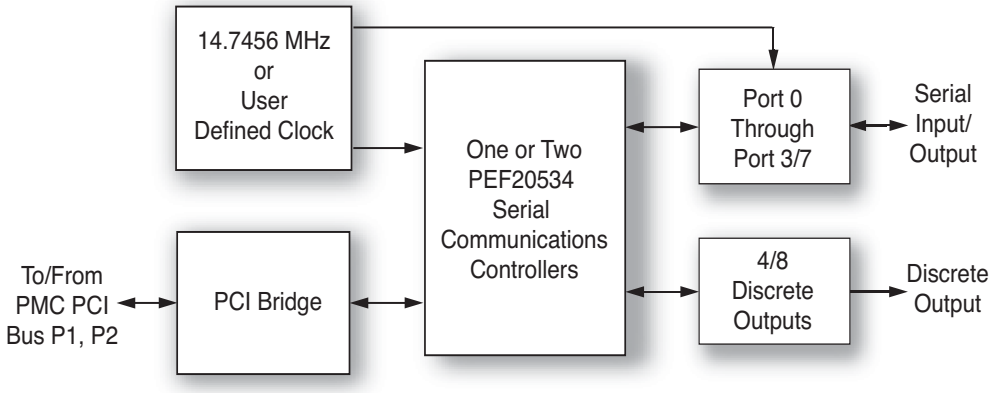


Figure 1.2.1: Simplified Block Diagram of HSS-PMC-CC Module

The HSS-PMC-CC module supports a wide selection of physical interfaces, configurable by software. You can individually select ports as RS-232 or RS-422/RS-485. This requires no hardware reconfiguration. Handshaking signal pairs for each port are also available.

In addition to the standard 14.7456 MHz oscillator, a user-defined oscillator is available for custom baud rate generation. Each port fully supports interrupts. Interrupts sources include transmission error, reception error, completions of transmit packets and completions of receive packets.

In the block diagram shown in Figure 1.2.1, a PCI bridge interfaces the PMC PCI bus to the HSS-PMC-CC module. The eight port version uses two high performance Siemens/Infineon PEF20534 Serial Communications Controllers that are responsible for eight ports of serial I/O. The four port version uses one PEF20534 that is responsible for four ports of serial I/O. Each port can support multiple protocols and uses Maxim's Multi-protocol Transceivers (MAX3160) and analog switches for various termination options.

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You must plug the HSS-PMC-CC into a CPU slot that has bus mastering capability.

A VxWorks Driver is available for the HSS-PMC-CC for asynchronous operation.

The HSS-PMC-CC provides the following key features:

- Four or eight ports of high-speed serial I/O
- Maximum data rate of 10 Mbit/sec (synchronous) and 2 Mbit/sec (asynchronous)
- Asynchronous, HDLC, and SDLC communication protocols supported
- RS-232, RS-422, or RS-485 physical interfaces supported
- Four user discrete outputs on the four port version or eight user discrete outputs on the eight port version
- PCI bus master capability for DMA transfers

1.3 Terminology

Table 1.3.1 defines some of the basic terms used throughout this manual.

Table 1.3.1: Basic Terminology

Term	Meaning
Bus	A single RS-232, RS-422, or RS-485 bus connection
DSCC4	DMA Supported Serial Communications Controller
HSS	High Speed Serial

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1.4 Conventions

The following conventions appear in this document. These conventions may differ from those used in other SBS publications. The subsections listed below describe each convention in more detail:

- Typographic Conventions
- Words Having Special Meaning
- Compound Keystrokes and Menu Selections
- Symbols

1.4.1 Typographic Conventions

Table 1.4.1 shows the typographic conventions used in this document.

Table 1.4.1: Typographic Conventions

Element	Use in Body Text	Use in Procedures
Italic	➢ Document, chapter, section, and topic titles and cross references ➢ Emphasis	➢ Filenames and directory paths
Bold	➢ (Not used in body text)	➢ Controls, dialogs, menus, and text or numeric fields that appear on the screen ➢ Keys on your keyboard
`Courier Roman`	➢ Code examples	➢ Simulating the appearance of screens
`Courier Bold`	➢ Library function calls and syntax. ➢ Emphasizing lines of code	➢ Commands and other information that you type as given
Angle brackets, e.g.,< >	➢ Enclosing variable information that you type (without the brackets) in place of a dummy variable	➢ Enclosing variable information that you type (without the brackets) in place of a dummy variable

The point size of the text varies depending on whether it is used in body text, code examples, notes, screens, or procedures.

1.4.2 Words Having Special Meaning

In procedures, the words "Enter" (or "enter") and "Type" (or "type") have special meanings that are indicated in Table 1.4.2.

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Table 1.4.2: Words with Special Meaning

Word	Meaning
Enter	Key in the specified text or variable information and press the **Return** key.
Type	Key in the specified text. Do not press **Return**.

1.4.3 Compound Keystrokes and Menu Selections

Compound Keystrokes

Whenever a procedure instructs you to press multiple keys, a double angle bracket "»" separates the names of the keys. Table 1.4.3 shows an example.

Menu Selections

Whenever a procedure instructs you to select an item from a pull-down menu, a double angle bracket "»"separates the menu items. Table 1.4.3 shows an example.

Table 1.4.3: Compound Keystrokes and Menu Selection Examples

Instruction	Meaning
Press **Ctrl** » **Alt** » **Delete**.	Press the **Ctrl**, **Alt**, and **Delete** keys simultaneously.
Select **File** » **Open**.	Select **Open** from the **File** menu.

1.4.4 Symbols

The following symbols appear throughout this manual:



Warning: Paragraphs next to this symbol contain information critical to module operation or to your safety.



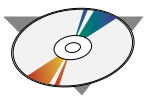
Note: Paragraphs next to this symbol contain information important to module operation.



Tip: Paragraphs next to this symbol contain useful tips.



Cross Reference: Paragraphs next to this symbol contain cross references to a related page in this manual.



Software Cross Reference: Paragraphs next to this symbol contain cross references to software media included with this product.

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2: Before You Begin

The sections in this chapter describe what to do after receiving and prior to installing your card. The sections are as follows:

- What You Should Have Received
- Unpacking the Card
- What You Will Need

2.1 What You Should Have Received

- HSS-PMC-CC Card - A 4-port or an 8-port HSS-PMC-CC interface card
- SBS Resource CD containing the following:
  - Device drivers necessary to support the interface between the HSS-PMC-CC card and your PC system
  - Product documentation

2.2 Unpacking the Card



Warning: This is an electronic product that is sensitive to electrostatic discharge. Take normal precautions in handling the card to prevent damage.

- Carefully unpack the card and inspect it for physical damage that might have occurred during shipping.
- If you have a damaged card, contact the SBS technical support group that handles maintenance, repairs, and warranties in Albuquerque. When you call us, give us the serial number of your card, and have the card available in case we have questions about its condition.

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2.3 What You Will Need

The HSS-cPCI3U-CC product package includes all items required to operate the card on your chassis.

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3: Installing the Hardware

This chapter provides instructions on how to configure and install the HSS-PMC-CC hardware.

3.1 Installing the Card

To install the HSS- PMC-CC, you mount it on a host card. The first subsection describes the layout and pinout descriptions of the connectors. The remaining subsection describes how to install the card.

- Layout and Connector Pinouts
- Installing the Conductive-Cooled HSS-PMC-CC



Warning: This is an electronic product that is sensitive to electrostatic discharge. Take normal precautions in handling the board to prevent damage.

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3.1.1 Layout and Connector Pinouts

Figure 3.1.1 through Figure 3.1.5 show the layout, connector locations, and connector pinout description for the HSS-PMC-CC card.

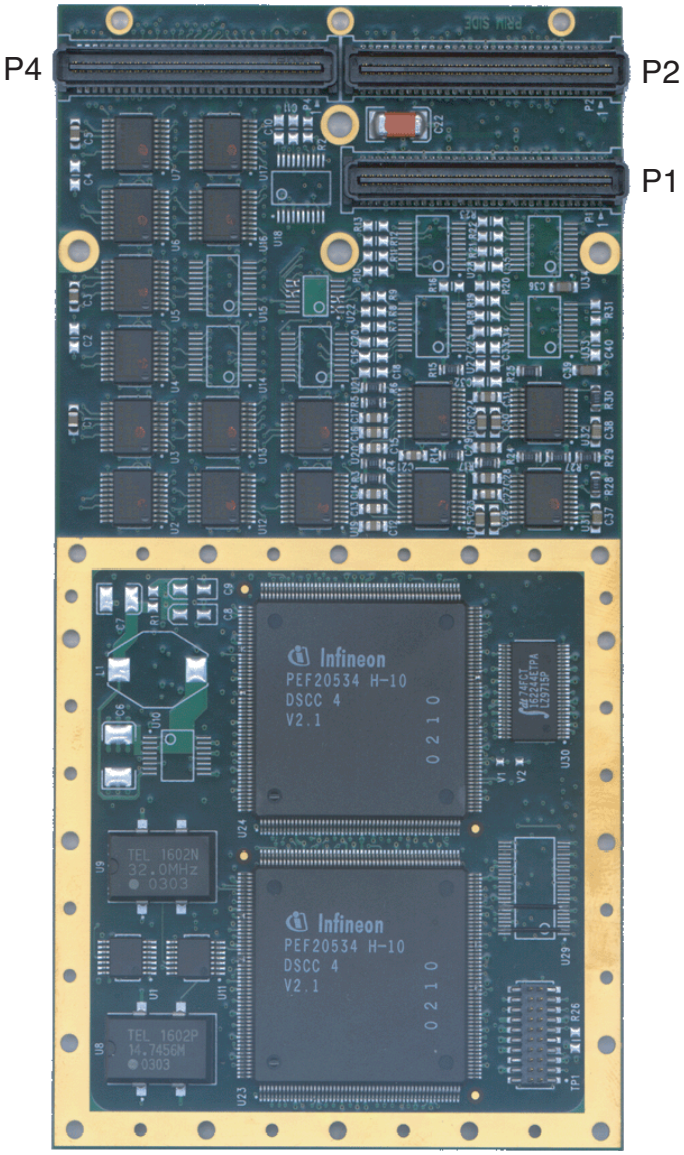


Figure 3.1.1: HSS-PMC-CC-8 Conductive Cooled Layout and Connector Locations

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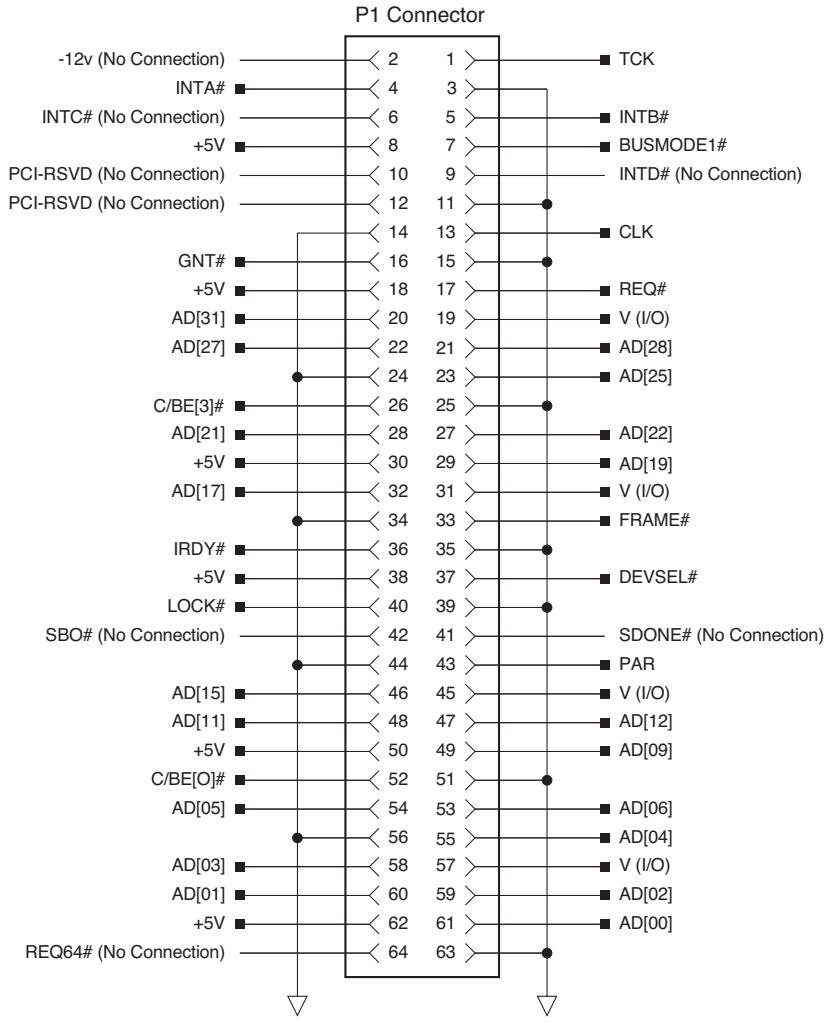


Figure 3.1.2: PMC P1 Connector PCI Pin Assignments

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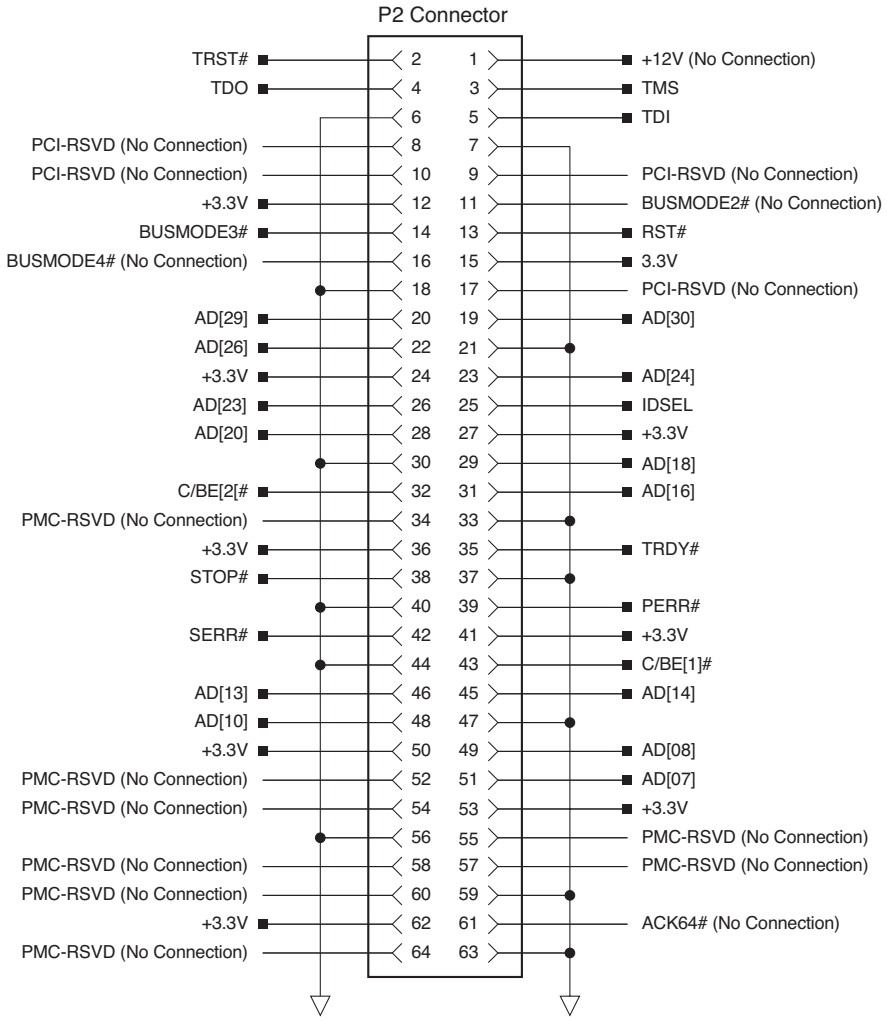


Figure 3.1.3: PMC P2 Connector PCI Pin Assignments

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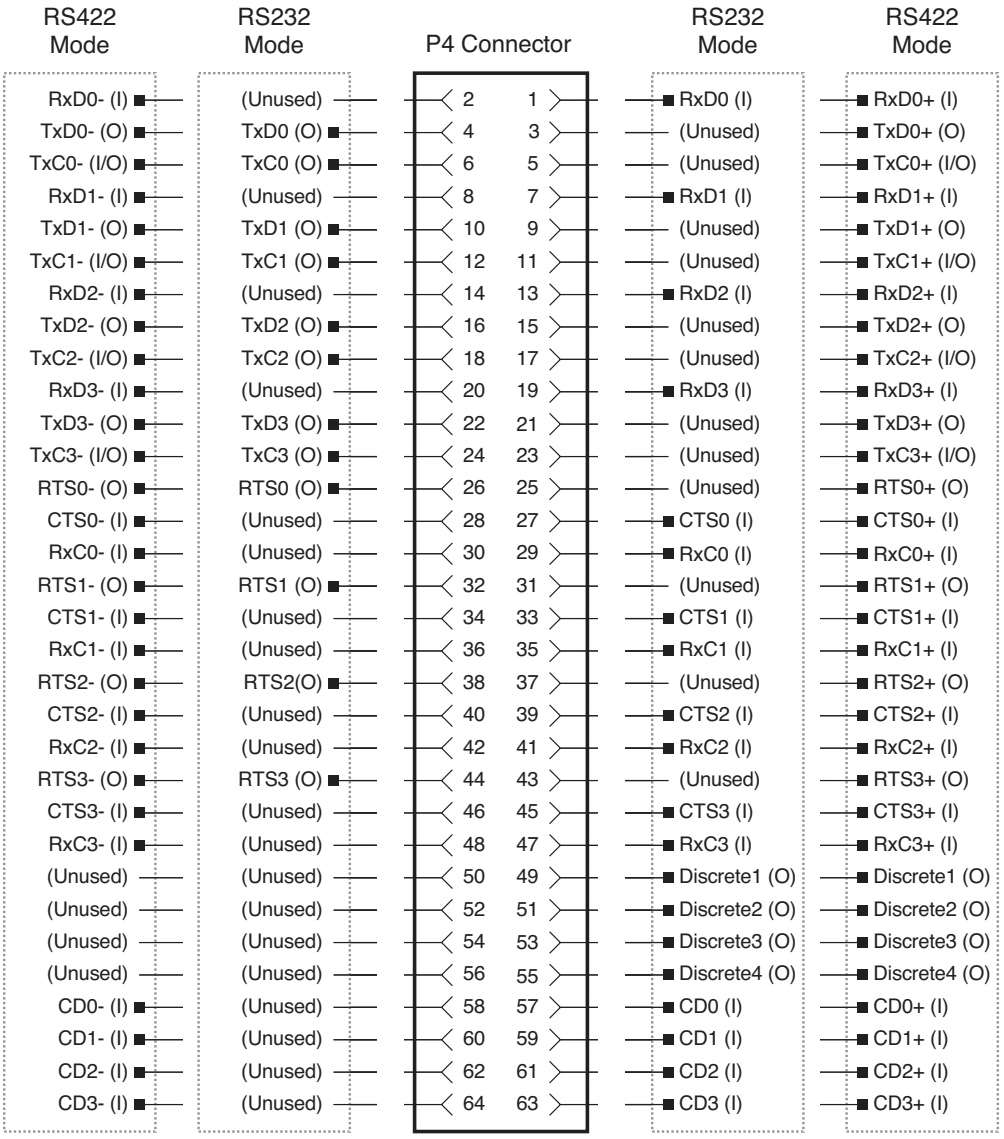


Figure 3.1.4: PMC P4 Connector Pinouts – Four Port Version

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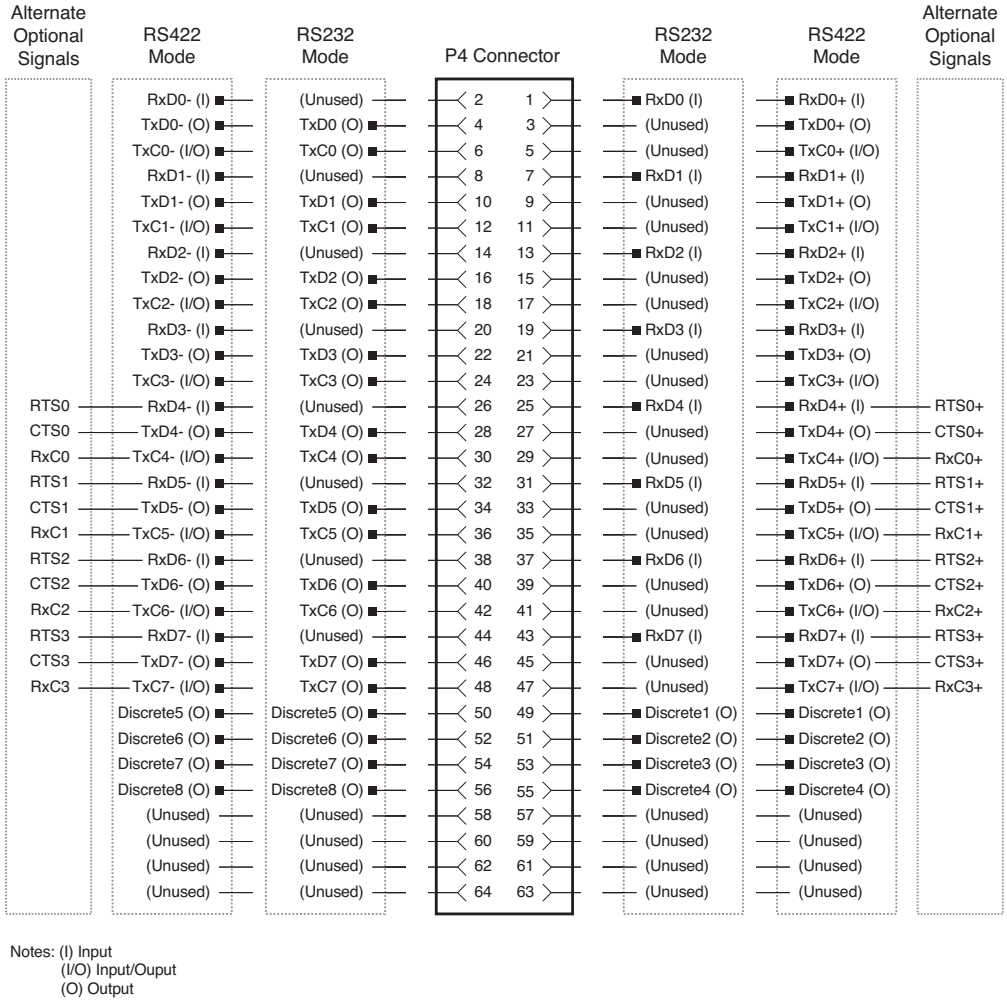


Figure 3.1.5: PMC P4 Connector Pinouts – Eight Port Version

3.1.2 Installing the Conductive-Cooled HSS-PMC-CC

Figure 3.1.6 depicts the conductive-cooled HSS-PMC-CC assembly mounting on a host card. Table 3.1.1 describes the recommended and alternative methods for mounting the card. After mounting the HSS-PMC-CC on the host card, install the host card in your system.

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Table 3.1.1: Mounting Methods for Conductive-Cooled HSS-PMC-CC

Screw Size	Recommended Mounting– Free running helical insert	Alternate Mounting 1– Free running tapped aluminum	Alternate Mounting 2– Locking helical insert
2mm	Apply Loctite 222MS, and torque to 30 in-oz.	Apply Loctite 222MS, and torque to 24 in-oz.	Torque additional 5 in-oz. after head is flush
2.5mm	Apply Loctite 222MS, and torque to 60 in-oz.	Apply Loctite 222MS, and torque to 45 in-oz.	Torque additional 8 in-oz. after head is flush

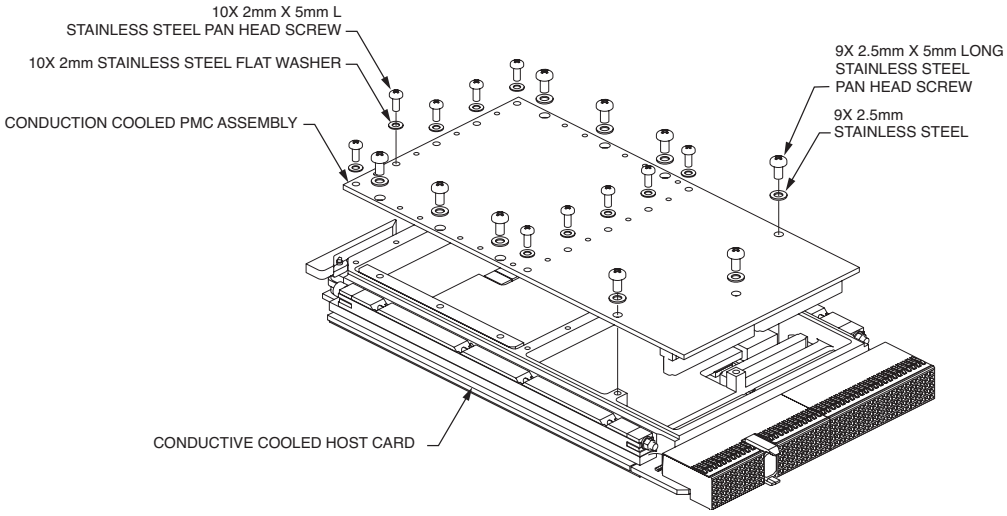


Figure 3.1.6: Conductive-Cooled HSS-PMC-CC Mounting to Host Card

Tip: Refer to Figure 3.1.1 for connector locations and to Figure 3.1.2 through Figure 3.1.4 for connector pinouts.

Table 3.1.2 lists the fastener quantity, vendor part number, description, and vendor for the mounting of the conductive-cooled HSS-PMC-CC to a host card.

Table 3.1.2: Fasteners Needed for Mounting HSS-PMC-CC

Item	Qty	Mfg Part Number	Description	Vendor
1	9	1940-M250-M5-2A21	2.5 mm pan head screw x 5 mm long, stainless steel	Barnhill Bolt
2	10	1940-M2-M5-2A21	2 mm pan head screw x 5 mm long, stainless steel	Barnhill Bolt
3	9	1926-M250-A-2	M2.5 stainless steel flat washer	Barnhill Bolt
4	10	1926-M2-A-2	M2 stainless steel flat washer	Barnhill Bolt

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3.2 Specifications

Table 3.2.1 lists the specifications for the HSS-PMC-CC board.

Table 3.2.1: Specifications

Specification	Description
Form Factor	PMC
PCI Interface	33 MHz, 32-bit, master/slave Bus mastering required
PMC Conformance	PCI Protocol and Electrical Rev 2.0 Specification
PCI Interface/Serial Controller	Siemens PEF 20534
Number of Serial Ports	Four or eight
Maximum Data Rate	Asynchronous: 2 Mbits/sec Synchronous: 10 Mbits/sec
Physical Levels Supported	RS-232, RS-422, RS-485
Protocols Supported	Asynchronous UART, HDLC, SDLC
RS-422 and RS-485 Signals Supported	See Figure 3.1.4 and Figure 3.1.5.
RS-232 Signals Supported	See Figure 3.1.4 and Figure 3.1.5.
Discrete Outputs	24 mA balanced line driver outputs utilizing 74FTC162244: Four for the four port version Eight for the eight port version
FIFOs per DSCC4	Local Receive 17 x 32-bit, each port Local Transmit 8 x 32-bit, each port Central Receive 128 x 32-bit Central Transmit 128 x 32-bit
On-Board Oscillators	Selectable 14.7456 MHz or User-Defined to support standard/custom asynchronous baud rates (Custom version only)
DMA Controllers per DSCC4	Four Ports per DSCC4
Rear panel I/O	Via PMC P4
Front panel I/O	Not supported
Dimensions	74.0 mm x 149.0 mm
Weight	Will not exceed 0.159 kg (0.35 lb)
Power Requirements	+5.0 VDC (typical): 860 mA operating EIA 485 mode 640 mA operating EIA 422 mode 430 mA operating EIA-232 mode
Environmental	Operating temperature: -40 to +85°C Humidity: 5 to 95% non-condensing Storage: -65 to +150°C

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4: Building the Driver

The following section describes how to build the VxWorks Driver for your target system.

4.1 Building the VxWorks Driver for Your Target System

Use the one of the following instructions to build the driver for the target system in which you are installing the HSS-PMC-CC card.

- Downloadable Application Instructions
- Bootable Image Instructions

4.1.1 Downloadable Application Instructions

Use the following instructions to build the downloadable application.

1. Build a downloadable project for the target system. Include the HSS driver files.
2. Rebuild.
3. Load the *.out* files.

   The driver is ready to use on the target system.

4.1.2 Bootable Image Instructions

Use the following instructions to build the bootable image.

1. Build a custom VxWorks image. Include the HSS driver files into the project.
2. Rebuild.
3. Reboot with the new image.

   The driver is ready to use on the target system.

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5: Addressing

5.1 PMC/PCI Interface

The Host system accesses the HSS-PMC-CC via a 33MHz 32-bit PMC interface that is PCI specification 2.1 compliant. The HSS-PMC-CC hardware configures the DMA Supported Serial Communications Controller (DSCC4) Bus Interface into the PCI mode (DEMUX connects to V_{SS}). Figure 5.1.1 shows the PCI configuration registers of the HSS-PMC-CC.

31	16	15	0
Device ID (=2102H)		Vendor ID(=110AH)	
Status		Command	
Class Code			Revision ID (=00H)
BIST	Header Type	Latency Timer	Cache Line Size
Base Address Register: contains base address of DSCC4 on-chip registers			
Base Address Register: (Not used on HSS-PMC-CC)			
Base Address Register (Not used)			
Base Address Register (Not used)			
Base Address Register (Not used)			
Base Address Register (Not used)			
Reserved			
Reserved			
Expansion ROM Base Address (Not used)			
Reserved			
Reserved			
Max_Lat (=0AH)	Min_Gnt (=02H)	Interrupt Pin (=01H)	Interrupt Line (=00H)

Figure 5.1.1: PCI Configuration Space

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5.1.1 PCI Slave Interface Register Access

The HSS-PMC-CC PCI Slave interface provides access to the DSCC4 registers from the Host system through the use of PCI Memory Read and PCI Memory Write transactions. Registers addresses are an offset to the Base Address Configuration Register Value. The HSS-PMC-CC does not support PCI I/O Read or Write commands as a PCI slave.

5.1.2 PCI Master Interface DMA Access

Associated data and structures are kept in Host memory for each DSCC4 by PCI Master DMA PCI Memory Read and PCI Memory Write transactions. The HSS-PMC-CC PCI Master interface accesses the Host system memory through the use of PCI Memory Read and PCI Memory Write transactions. In order for the HSS-PMC-CC to operate, the Host memory maintains the data and structures.

5.1.3 Interrupts

All sources of Interrupts from each DSCC4 go to the PMC INTA signal. These sources include: SCC transmit, SCC reception, DMA controller and peripheral blocks. In addition, each DSCC4 maintains a linked list of interrupt status words in Host memory for each interrupt type.

5.1.4 DSCC4 Registers

Each of the two DSCC4 device registers divides into three groups: global registers that control each general DSCC4 operation, four identical sets of registers that control the four SCCs (Serial Communication Controllers), and General Purpose Port (GPP) registers that control the multiprotocol physical serial interface and the user programmable discrete output lines. Table 5.1.1 is an overview of a DSCC4 register set and associated address ranges. The complete register address calculation is the sum of the PCI Base Address Register and the register offset.

Table 5.1.1: DSCC4 Device Registers

Description	Offset Range
Global DSCC4 Registers	0000 00FFH
SCC0 Registers	0100 017FH
SCCl Registers	0180 01FFH
SCC2 Registers	0200 027FH
SCC3 Registers	0280 02FFH
Gen. Purpose Port Registers	0400 0408H

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5.2 Register Map

5.2.1 Global Registers

Table 5.2.1 lists the offset address to each of the global control registers used to configure and control the DSCC4 DMA controller, central FIFO's and general device functions. The Global Registers addresses are the listed offset from the PCI Base Address Register Value.

Table 5.2.1: DSCC4 Global Registers

Offset	Register	Description
0000H	GCMDR	Global Command Register
0004H	GSTAR	Global Status Register
0008H	GMODE	Global Mode Register
000CH	IQLENR0	IQ Length Register 0
0010H	IQLENR1	IQ Length Register 1
0014H	IQSCCORXBAR	IQ SCC0 RX Base Address Register
0018H	IQSCC1RXBAR	IQ SCC1 RX Base Address Register
001CH	IQSCC2RXBAR	IQ SCC2 RX Base Address Register
0020H	IQSCC3RXBAR	IQ SCC3 RX Base Address Register
0024H	IQSCC0TXBAR	IQ SCC0 TX Base Address Register
0028H	IQSCC1TXBAR	IQ SCC1 TX Base Address Register
002CH	IQSCC2TXBAR	IQ SCC2 TX Base Address Register
0030H	IQSCC3TXBAR	IQ SCC3 TX Base Address Register
0034H	FIFOCR4	FIFO Control Register 4
003CH	IQCFGBAR	IQ CFG Base Address Register
0040H	IQPBAR	IQ Peripheral Base Address Register
0044H	FIFOCR1	FIFO Control Register 1
0048H	FIFOCR2	FIFO Control Register 2
004CH	FIFOCR3	FIFO Control Register 3
0050H	CH0CFG	Channel 0 Configuration Register
0054H	CH0BRDA	Channel 0 Base Rx Descriptor Address
0058H	CH0BTDA	Channel 0 Base Tx Descriptor Address
005CH	CH1CFG	Channel 1 Configuration Register
0060H	CH1BRDA	Channel 1 Base Rx Descriptor Address
0064H	CH1BTDA	Channel 1 Base Tx Descriptor Address
0068H	CH2CFG	Channel 2 Configuration Register

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Offset	Register	Description
006CH	CH2BRDA	Channel 2 Base Rx Descriptor Address
0070H	CH2BTDA	Channel 2 Base Tx Descriptor Address
0074H	CH3CFG	Channel 3 Configuration Register
0078H	CH3BRDA	Channel 3 Base Rx Descriptor Address
007CH	CH3BTDA	Channel 3 Base Tx Descriptor Address
0098H	CH0FRDA	Channel 0 First Rx Descriptor Address
009CH	CH1FRDA	Channel1 First Rx Descriptor Address
00A0H	CH2FRDA	Channel 2 First Rx Descriptor Address
00A4H	CH3FRDA	Channel 3 First Rx Descriptor Address
00B0H	CH0FTDA	Channel 0 First Tx Descriptor Address
00B4H	CH1FTDA	Channel 1 First Tx Descriptor Address
00B8H	CH2FTDA	Channel 2 First Tx Descriptor Address
00BCH	CH3FTDA	Channel 3 First Tx Descriptor Address
00C8H	CH0LRDA	Channel 0 Last Rx Descriptor Address
00CCH	CH1LRDA	Channel 1 Last Rx Descriptor Address
00D0H	CH2LRDA	Channel 2 Last Rx Descriptor Address
00D4H	CH3LRDA	Channel 3 Last Rx Descriptor Address
00E0H	CH0LTDA	Channel 0 Last Tx Descriptor Address
00E4H	CH1LTDA	Channel 1 Last Tx Descriptor Address
00E8H	CH2LTDA	Channel 2 Last Tx Descriptor Address
00ECH	CH3LTDA	Channel 3 Last Tx Descriptor Address

5.2.2 SCC Port Address Offset

Table 5.2.2 lists the offset starting address for each of the four sets of registers used to configure and control the individual SCC (Serial Communications Controllers). Each of the four SCCs implements the complete SCC register set. A specific SCC starting address offset distinguishes the individual ports. The SCC registers addresses are the sum of the PCI Base Address Register value, the SCC starting offset address and the register offset.

Table 5.2.2: SCC Starting Address Offsets

SCC (Port)	Starting Offset (hex)
SCC0 (Port 1)	0x100
SCC1 (Port 2)	0x180
SCC2 (Port 3)	0x200
SCC3 (Port 4)	0x280

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5.2.3 SCC Registers

Table 5.2.3 lists the offset for each individual register in the SCC register set. Address the SCC registers by adding the PCI Base Address Register value, the SCC starting offset address and the desired register offset.

Table 5.2.3: SCC Registers

Offset	Type	Register	Description
0000H	W	CMDR	Command Register
0004H	R	STAR	Status Register
0008H	R/W	CCR0	Channel Configuration Register
000CH	R/W	CCR1	Channel Configuration Register
0010H	R/W	CCR2	Channel Configuration Register
0014H	R/W	ACCM	Async Control Character Map Register
0018H	R/W	UDAC	User Defined Async Character
001CH	R/W	TSAX	Time-Slot Assignment Register Tx
0020H	R/W	TSAR	Time-Slot Assignment Register Rx
0024H	R/W	PCMMTX	PCM Mask Register Tx
0028H	R/W	PCMMRX	PCM Mask Register Rx
002CH	R/W	BRR	Baud Rate Register
0030H	R/W	TIMR	Timer Register
0034H	R/W	XADR	Transmit Address Register
0038H	R/W	RADR	Receive Address Register
003CH	R/W	RAMR	Receive Address Mask Register
0040H	R/W	RLCR	Receive Length Check Register
0044H	R/W	XNXFR	XON/XOFF Register
0048H	R/W	TCR	Termination Character Register
004CH	R/W	TICR	Tx Immediate Character Register
0050H	R/W	SYNCR	Synchronization Character Register
0054H	R/W	IMR	Interrupt Mask Register
0058H	R/W	ISR	Interrupt Status Register

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5.2.4 Internal Loop Test Mode

To provide fast and efficient testing, you can operate the SCC in a test mode by setting the TLP bit in register CCR1 (offset Ch). This connects the on-chip serial data input and output signals (TxD, RxD) generating a local loop back. See Figure 5.2.1. This allows you to perform a self-test of the SCC.

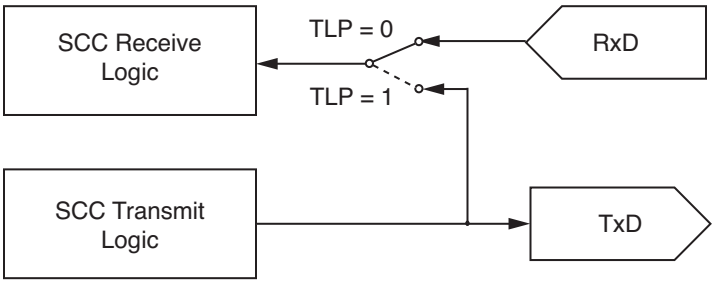


Figure 5.2.1: SCC Test Loop

The transmit data remains connected to pin TxD during test loop operation (pin TxD always receives transmit data). The GPP must disable the TX Enable in order not to transmit externally.

It is necessary to use a sufficient clock mode for test loop operation so that receiver and transmitter operate with the same frequencies depending on the clock supply.

Note: Test loop operation is not supported in high speed port operation.

5.2.5 GPP Registers

Table 5.2.4 lists the GPP registers. You use the GPP registers to select the physical serial interface for each of the eight ports. To address the GPP ports, add the register offset to the PCI Base Address Register value.

Table 5.2.4: General Purpose Port Registers

Offset	Register	Description
0400H	GPDIR	General Purpose Port Direction Register
0404H	GPDATA	General Purpose Port Data Register
0408H	GPIM	General Purpose Port Interrupt Mask Register

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6: Programming

6.1 Physical Interface

6.1.1 GPP Initialization

Each of the DSCC4's 16-bit General Purpose Bus registers selects the four Serial Port (Physical) Interfaces for a total of eight. Host initialization code programs the DSCC4 Global Mode Register to configure the peripheral block to 16-bit General Purpose Bus mode by writing a `0x4` to bits 18 through 16 (GMODE.PERCFG[2:0]). In addition, the GPP (General Purpose Port) GPDIR register is written with `0x0000FFFF` configuring all General Purpose pins as outputs. Data written to the GPDATA register controls the physical interface selection (see subsection 6.1.2). Before initialization, pull-up resistors pull the general purpose bus high to avoid any spurious outputs.

6.1.2 GPP Port Mapping

Once the GPP is initialized, the Physical Serial Interface selection for each port is made via the GPDATA register. Four bits of the 16-bit data port control each port. A Maxim Multiprotocol MAX3160 transceiver provides the Multiprotocol Interface (MPI) for set for each port. Three mode pins provide control. The first bit BICLK in each four bit group, controls the direction of the bi-directional clock (0 = input, 1 = output). The second bit RS485 selects the protocol (0 = RS-232, 1 = RS-422/485). The third bit, ENBL, enables the port (0 = disable, 1 = enable). Finally, the fourth bit, D[4:1], (reserved) selects user programmable discrete outputs (see note below). Figure 6.1.1 shows the interconnection of the General Purpose Bus to the Multiprotocol Interface pins.

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MSB								
15	14	13	12	11	10	9	8	Bit
Port 3/Port 7				Port 2/Port 6				Port #
D4/SRC	ENBL	RS485	BICLK	D3	ENBL	R485	BICLK	MPI pin

							LSB	
7	6	5	4	3	2	1	0	Bit
Port 1/Port 5				Port 0/Port 4				Port #
D2	ENBL	RS485	BICLK	D1	ENBL	RS485	BICLK	MPI pin

Figure 6.1.1: GPDATA Register to Multiprotocol Interface Mapping



Note: Bit 15 D4/SRC on the second SCC (reserved) selects one of two oscillators present on the HSS. Setting bit 15 selects the Standard Oscillator (14.7456 Mhz). Clearing bit 15 selects the User-Defined Oscillator.

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6.2 Physical Interface Selection

Table 6.2.1 lists the Physical Interface selections for each port. The selection is chosen by writing the four bits in the GPP register that correspond to each of the four or eight ports. (See "GPP Port Mapping" on page 25.) After power on or PMC reset, all four/eight ports are in the high impedance mode (0xF) until programmed otherwise.

Table 6.2.1: Physical Interface Selection Guide

Physical Interface Mode	TxC Signal Mode	MPI Control Bits D	ENBL	RS485	BICLK	Notes
RS-232	Receiver / Driver	X	1	0	0 / 1	None
RS-422	Receiver / Driver	X	1	1	0 / 1	None
RS-485	Receiver / Driver	X	1	1	0 / 1	None
High Impedance	Receiver / Driver	X	0	X	X	Reset Mode

6.2.1 RS-232 Mode

In RS-232 mode, all circuits are unbalanced-bipolar V.28 specification compliant. Cable termination is unnecessary as the receiver supplies the necessary 5 k resistor to ground. Table 6.2.2 details the serial signal configuration for RS-232 mode.

Table 6.2.2: RS-232 Mode Signal Definition

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	V.28	None	Single Ended
RxD	V.28	5K (Receiver)	Single Ended
TxC as a Receiver	V.28	5K (Receiver)	Single Ended
TxC as a Driver	V.28	None	Single Ended
RxC	V.28	5K (Receiver)	Single Ended
RTS	V.28	None	Single Ended
CTS	V.28	5K (Receiver)	Single Ended
CD (4 Channel Only)	V.28	5K (Receiver)	Single Ended

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6.2.2 RS-422/RS-485 Mode

In RS-422/RS-485 mode, all circuits are balanced V.11 standard compliant. Table 6.2.3 details the serial signal configuration for RS-422/RS-485 mode.

Table 6.2.3: RS-422/RS-485 Mode Signal Definition

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	V.11	None	Differential
RxD	V.11	120 Ohm + 1800 pF	Differential
TxC as a Receiver	V.11	None	Differential
TxC as a Driver	V.11	120 Ohm + 1800 pF	Differential
RxC	V.11	None	Differential
RTS	V.11	None	Differential
CTS	V.11	None	Differential
CD (4 Channel Only)	V.11	None	Differential

6.2.3 High Impedance Mode

Table 6.2.4 details the serial signal configuration for the High Impedance Mode.

Table 6.2.4: High Impedance Mode Signal Definition

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	High Impedance	V.11	N/A
RxD	High Impedance	V.11	N/A
TxC as a Receiver	High Impedance	V.11	N/A
TxC as a Driver	High Impedance	V.11	N/A
RxC	High Impedance	V.11	N/A
RTS	High Impedance	None	N/A
CTS	High Impedance	None	N/A
CD (4 Channel Only)	High Impedance	None	N/A

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6.3 Baud Rate Selection

The HSS-PMC-CC provides a flexible set of serial clocking and data recovery solutions. Complex user-specific choices, such as the communication protocol, the clock source, the clock mode and the physical interface mode determine baud rate limitations for the HSS-PMC-CC.



Note: Maximum baud rates given in this section do not reflect external user-controlled issues, such as cable quality, cable length, cable impedance, and far-end termination.

6.3.1 Maximum Baud Rates

Table 6.3.1, Table 6.3.2, and Table 6.3.3 show the maximum baud rates allowed on the HSS-PMC-CC.

Table 6.3.1: Baud Rates Using an External Clock

Communication Protocol	Physical Interface	Maximum Baud Rate
Synchronous	RS-422	10.0 Mbaud
	RS-232	115.2 kbaud
Isochronous	RS-422	1.8432 Mbaud
	RS-232	115.2 kbaud
Asynchronous	RS-422	921.6 kbaud
	RS-232	115.2 kbaud

Table 6.3.2: Baud Rates Using the Standard 14.7456MHz Oscillator

Communication Protocol	Physical Interface	Maximum Baud Rate
Synchronous	RS-422	1.8432 Mbaud
	RS-232	115.2 kbaud
Isochronous	RS-422	1.8432 Mbaud
	RS-232	115.2 kbaud
Asynchronous	RS-422	921.6 kbaud
	RS-232	115.2 kbaud

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Table 6.3.3: Baud Rates Using a User Oscillator

Communication Protocol	Physical Interface	Maximum Baud Rate
Synchronous	RS-422	2.0 Mbaud
	RS-232	115.2 kbaud
Isochronous	RS-422	2.0 Mbaud
	RS-232	115.2 kbaud
Asynchronous	RS-422	2.0 Mbaud
	RS-232	115.2 kbaud

6.3.2 Example of Asynchronous Baud Rates

The DSCC4 provides an independently programmable baud rate generator for each port. You can use this in conjunction with the on-board 14.7456 MHz oscillator to provide commonly used asynchronous baud rates. You set the baud rate for each port by programming the Bit Clock Rate bit in the SCC Channel Configuration Register (CCRO.BCR) and the BRM and BRN fields of the SCC Baud Rate Register (BRR.BRM(3..0) and BRR.BRN(5..0)). For asynchronous communication, you set the CCR.BCR to one, providing a 16-times clock. The Baud Rate Register (BRR) controls the baud rate using the following formula:

$$Fbr = \frac{Fin}{(N+1)(D)2^{M}}$$

Where:

- M = 0-15 in BRM(3..0)
- N = 0-63 in BRN(5..0)
- D = 16 (BCR=1)
- Fbr = frequency of the desired baud rate.
- Fin = frequency in = 14.7456 MHz



Note: There is an errata on BRM which states that it must not exceed a value of M=14 (although the specified value is 15).

Table 6.3.4 lists the BRM and BRN values for popular baud rates in Asynchronous 16X Mode.

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Table 6.3.4: Common Asynchronous (16X) Baud Rates

Baud Rate	BRM(3..0) Value	BRN(5..0) Value
50	0x09	0x23
200	0x07	0x23
300	0x06	0x2F
600	0x05	0x2F
1,200	0x04	0x2F
2,400	0x03	0x2F
4,800	0x02	0x2F
9,600	0x01	0x2F
19,200	0x00	0x2F
38,400	0x00	0x17
57,600	0x00	0x0F
76,800	0x00	0x0B
115,200	0x00	0x07
230,400	0x00	0x03
460,800	0x00	0x01
921,600	0x00	0x00

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6.4 User Options

6.4.1 User Oscillator

When using the HSS-PMC-CC in systems where an external clock is not supplied and the standard oscillator is not an even multiple of the desired baud rate, you can choose to have a customer-defined oscillator installed at the time of manufacture. This provides the user selection of either the standard or custom oscillator for I/O ports 0-3/0-7.

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A: Revisions

The table in this appendix gives a brief summary of any technical revisions made to this manual. When reading this manual online, you can jump to the first citation of a revision by clicking the links in blue.



Note: Only technical revisions appear in the table. Most even numbered pages contain a date stamp in the footer. If the footer date is more recent then the latest revision date given in the table, then the newest revision of this manual contains only *non-technical* revisions.

Revision Number	Revision Date	Description
2	20 May 2004	Added information about the HSS-PMC-CC04 card. The HSS-PMC-CC04 card is first cited in the Manual Overview section of Chapter 1. This revision also incorporates all previous revisions to this manual.
2.01	3 Aug 2005	Corrected the number of ports for each DSCC4 to four ports per DSCC4 beginning at Table 3.2.1.
2.02	13 Sep 2005	Added Alternate Optional Signals to Figure 3.1.5.

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