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PMC-3101-BP-CC

Conduction Cooled Dual
Fast Ethernet PMC

User Manual

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PMC-3101-BP-CC
Dual Fast Ethernet PMC

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Product Description

The PMC-3101-BP-CC provides two independent high-performance Fast Ethernet interface controller ports on a single-wide PCI Mezzanine Card (PMC). The Ethernet network interface complies with the IEEE 802.3 specification for 10BaseT and 100BaseTx. Both full duplex and half-duplex modes are supported.

The PMC-3101-BP-CC includes 3 Kbytes of transmit and 3 Kbytes of receive FIFO, allowing back-to-back transmission with minimum interface latency. It also features a 10BaseT and 100BaseTx auto-detection CSMA/CD interface controller.

The physical interface is supported via the built-in Physical Layer Interface Unit in the Ethernet controller. It supports a number of sophisticated features, including auto negotiation, collision detection, link detection, Manchester encoding/decoding (10BaseTx), 4B/5B encoding/decoding (100BaseTx), and scrambling/descrambling (100BaseTx). The PMC-3101-BP-CC's two ports are accessed via the rear panel P4 connector.

The PMC-3101-BP-CC is supported for popular operating systems including VxWorks. The card is compliant with standard single-wide PMC specifications IEEE P1386.1.

Key Features

- Two 10BaseT/100BaseTx Ethernet ports
- Rear-panel I/O via P4
- Single-wide PMC form factor
- Indicators for speed, link, and activity
- Auto-negotiating protocol
- Two 3 Kbyte FIFOs
- Drivers for VxWorks
- Conduction-cooled

Block Diagram

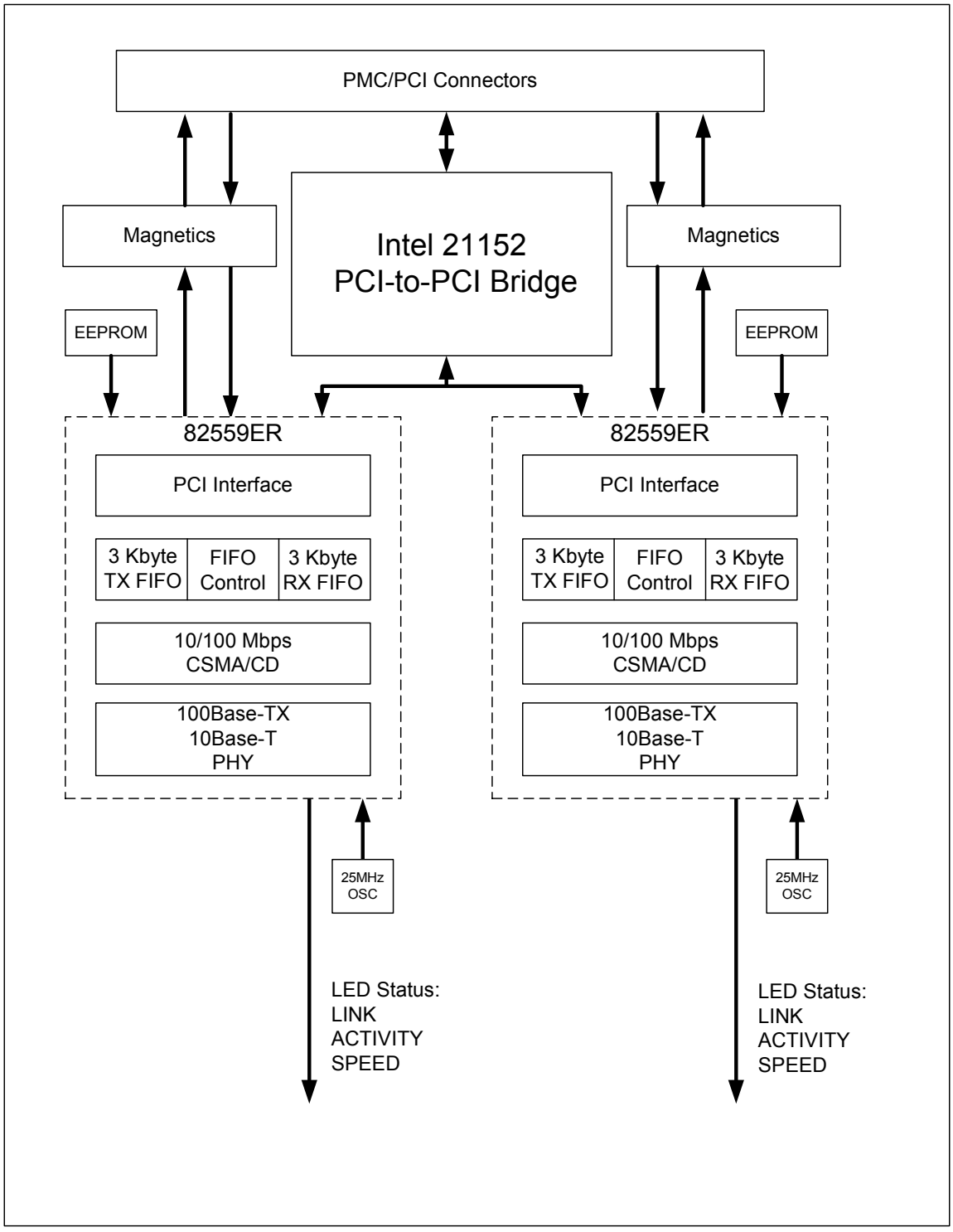


Figure 1 Block Diagram

Software Drivers

A VxWorks driver, VSRD-FEIEND, is available from SBS Technologies, Inc. for both Power PC and x86 platforms.

Programming

PMC/PCI Interface

The PMC-3101-BP-CC is accessed by the host system via a 33 MHz 32-bit PMC interface that is PCI Specification 2.1 compliant. The host accesses a PCI-PCI bridge that drives a secondary PCI bus connected to both 82559ER Ethernet chips.

The PCI configuration registers for the two 82559ER Ethernet chips on the PMC-3101-BP-CC are listed in the figure below.

31 16	15 0	Addr
Device ID = 1209h	Vendor ID = 8086h	00h
Status	Command	04h
Class Code	Revision ID = 08h	08h
BIST / Header Type	Latency Timer / Cache Line Size	0Ch
CSR Memory Mapped Base Address Register		10h
CSR I/O Mapped Base Address Register		14h
Flash Memory Mapped Base Address Register		18h
Reserved Base Address Register		1Ch
Reserved Base Address Register		20h
Reserved Base Address Register		24h
Reserved		28h
Subsystem ID = 0009h	Subsystem Vendor ID = 8086h	2Ch
Expansion ROM Base Address Register		30h
Reserved	Cap_Ptr	34h
Reserved		38h
Max_Lat / Min_Gnt	Interrupt Pin / Interrupt Line	3Ch
Power Management Capabilities	Next Item Pointer / Capability ID	DCh
Reserved / Data	Power Management CSR	E0h

Figure 2 PCI Configuration Registers for 82559ER

The following table lists the PCI configuration information for the bridge chip.

31 16	15 0	Addr
Device ID = 0024h	Vendor ID = 1011h	00h
Status	Command	04h
Class Code	Revision ID = 05h	08h
Reserved / Header Type	Primary Latency Timer / Cache Line Size	0Ch
Reserved		10h
Reserved		14h
Secondary Latency Timer / Subordinate Bus Number	Secondary Bus Number / Primary Bus Number	18h
Secondary Status	I/O Limit Address / I/O Base Address	1Ch
Memory Limit Address	Memory Base Address	20h
Prefetchable Memory Limit Address	Prefetchable Memory Base Address	24h
Prefetchable Memory Base Address Upper 32 Bits		28h
Prefetchable Memory Limit Upper 32 Bits		2Ch
I/O Limit Address Upper 16 Bits	I/O Base Address Upper 16 Bits	30h
Reserved	ECP Pointer	34h
Reserved		38h
Bridge Control	Interrupt Pin / Reserved	3Ch
Arbiter Control	Diagnostic Control / Chip Control	40h
Reserved		44h – 60h
Reserved / Reserved	Reserved /	64h
Reserved		68h
Reserved		6Ch – DBh
Power Management Capabilities	Next Item Ptr / Capability ID	70h
Data / PMCSR Bridge Support Extensions	Power Management CSR	74h
Reserved		E4h – FFh

Figure 3 PCI Configuration Registers for 21152AB PCI-PCI Bridge

Please note that revision 21152AB of the PCI bridge chip used on this card is now obsolete. Future versions of the card will use version 21152BB of the PCI bridge chip. The 21152BB is backwards compatible with the 21152AB and has been validated by SBS. It, however, has different vendor, device and revision IDs. If you card is fitted with the 21152BB, please use the following vendor, device, and revision IDs for configuration.

31 16		15 0		Addr
Device ID = B152h		Vendor ID = 8086h		00h
Status		Command		04h
Class Code			Revision ID = 00h	08h
Reserved	Header Type	Primary Latency Timer	Cache Line Size	0Ch
Reserved				10h
Reserved				14h
Secondary Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status		I/O Limit Address	I/O Base Address	1Ch
Memory Limit Address		Memory Base Address		20h
Prefetchable Memory Limit Address		Prefetchable Memory Base Address		24h
Prefetchable Memory Base Address Upper 32 Bits				28h
Prefetchable Memory Limit Upper 32 Bits				2Ch
I/O Limit Address Upper 16 Bits		I/O Base Address Upper 16 Bits		30h
Reserved			ECP Pointer	34h
Reserved				38h
Bridge Control		Interrupt Pin	Reserved	3Ch
Arbiter Control		Diagnostic Control	Chip Control	40h
Reserved				44h – 60h
Reserved	Reserved	Reserved		64h
Reserved				68h
Reserved				6Ch – DBh
Power Management Capabilities		Next Item Ptr	Capability ID	70h
Data	PMCSR Bridge Support Extensions	Power Management CSR		74h
Reserved				E4h – FFh

Figure 3a PCI Configuration Registers for 21152BB PCI-PCI Bridge

Secondary PCI Bus

The following table lists Ethernet chip configuration on the secondary PCI bridge.

Ethernet Port	Device Number on Secondary PCI Bus	Interrupt Pin on Primary PCI Bus
1	0	INTA#
2	1	INTB#

Figure 4 Device and Interrupt Assignment for Ethernet Ports

MAC Addresses

Unique Ethernet addresses are assigned to the two Ethernet ports at the factory. For convenience, the two addresses are shown on human- and machine-readable labels affixed to the backside of the board.

Connectors and Indicators

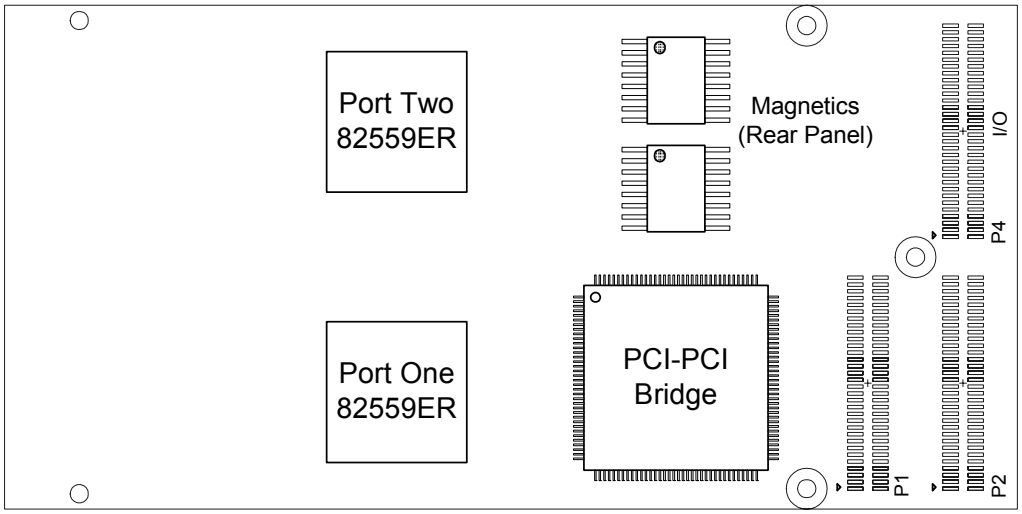


Figure 5 PMC-3101-BP-CC Placement Diagram

LED Indicators

Each Ethernet port provides three LED status indicators. The LED functions are listed in the table below.

Name	Signal	Description
ACT	Activity	Indicates either transmit or receive activity. When there is activity, the LED is on. When there is no activity, the LED is off.
LINK	Link Integrity	Indicates link integrity. If link is good in either 10 or 100 Mbps mode, the LED is on. If link is bad, the LED is off.
100	Speed	This LED is on if the data rate is 100 Mbps and off if it is at 10Mbps. The LED retains its last known state when the link is down.

Figure 6 LED Status Definitions

Rear Panel Ethernet Pin Assignment

PMC-3101-BP-CC-BP has only rear panel Ethernet access. Rear panel connections to the Ethernet interface on the PMC-3101-BP-CC are made via the 64-pin PMC P4 connector. Pin assignments are listed in the table below.

P4 Pin Number	Signal Name	P4 Pin Number	Signal Name
1	N/C	2	N/C
3	N/C	4	N/C
5	N/C	6	N/C
7	N/C	8	N/C
9	N/C	10	N/C
11	N/C	12	N/C
13	N/C	14	N/C
15	N/C	16	N/C
17	N/C	18	N/C
19	N/C	20	N/C
21	N/C	22	N/C
23	Port 1 common	24	Port 1 common
25	Port 1 TX+	26	Port 1 RX+
27	Port 1 common	28	Port 1 common
29	Port 1 TX-	30	Port 1 RX-
31	N/C	32	N/C
33	Port 2 common	34	Port 2 common
35	Port 2 TX+	36	Port 2 RX+
37	Port 2 common	38	Port 2 common
39	Port 2 TX-	40	Port 2 RX-
41	N/C	42	N/C
43	N/C	44	N/C
45	N/C	46	N/C
47	N/C	48	N/C
49	N/C	50	N/C
51	N/C	52	N/C
53	N/C	54	N/C
55	N/C	56	N/C
57	N/C	58	N/C
59	N/C	60	N/C
61	N/C	62	N/C
63	N/C	64	N/C

Figure 7 Rear Panel I/O Pin Assignment

N/C = Not Connected

PMC P1 Connector Pin Assignment

Pin Number	Signal Name	Signal Name	Pin Number
1 (N/C)	TCK	-12V	2 (BP)
3	Ground	INTA#	4
5	INTB#	INTC#	6 (N/C)
7	BUSMODEl#	+5V	8
9 (N/C)	INTD#	PCI-RSVD	10 (N/C)
11	Ground	PCI-RSVD	12 (N/C)
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19 (BP)	V (I/O)	AD[31]	20
21	AD[28]	AD [27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31 (BP)	V (I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40
41 (N/C)	SDONE#	SBO#	42 (N/C)
43	PAR	Ground	44
45 (BP)	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[O]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57 (BP)	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64 (N/C)

Figure 8 PMC P1 Connector PCI Pin Assignment

N/C = Not Connected, BP = Bypass only

PMC P2 Connector Pin Assignment

Pin Number	Signal Name	Signal Name	Pin Number
1 (BP)	+12V	TRST#	2 (N/C)
3 (N/C)	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD	8 (N/C)
9 (N/C)	PCI-RSVD	PCI-RSVD	10 (N/C)
11 (N/C)	BUSMODE2#	+3.3V	12 (BP)
13	RST#	BUSMODE3#	14
15 (BP)	3.3V	BUSMODE4#	16
17 (N/C)	PCI-RSVD	Ground	18
19	AD[30],	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24 (BP)
25	IDSEL	AD[23]	26
27 (BP)	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34 (N/C)
35	TRDY#	+3.3V	36 (BP)
37	Ground	STOP#	38
39	PERR#	Ground	40
41 (BP)	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50 (BP)
51	AD[07]	PMC-RSVD	52 (N/C)
53 (BP)	+3.3V	PMC-RSVD	54 (N/C)
55 (N/C)	PMC-RSVD	Ground	56
57 (N/C)	PMC-RSVD	PMC-RSVD	58 (N/C)
59	Ground	PMC-RSVD	60 (N/C)
61 (N/C)	ACK64#	+3.3V	62 (BP)
63	Ground	PMC-RSVD	64 (N/C)

Figure 9 PMC P2 Connector PCI Pin Assignment

N/C = Not Connected, BP = Bypass only

Specifications

Form Factor	Single PMC
PMC Conformance	32-bit PMC Specification IEEE P1386.1
PCI Interface	32-bit, 33 MHz master and slave, 3.3/5V signaling PCI Specification, Revision 2.2
PCI Controller	Intel 21152
Number of Ports	Two, independent
Ethernet Controllers	Intel 82559ER
Protocols	Ethernet 10BaseT, 100BaseTx
Receive/Transmit FIFOs	3 Kbytes each
Rear Panel Panel I/O Access	PMC P4
Indicators	Speed, activity, link
Dimensions	74.0 mm x 143.75 mm
Weight	0.06 kg (0.15 lb)
Power Requirements	+5 VDC, 50 mA typ. +3.3 VDC, 270 mA typ
Environmental	Operating temperature: 0° to +70°C Humidity: 5% to 95% non-condensing Storage: –40° to +85°C

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