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Hardware Reference Manual

PMC-HS-Serial*

Publication No. 89002090 Rev. D.0

abaco SYSTEMS

Document History

Revision	Date	Description
D.0	February 2017	Rebranded to Abaco Systems

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About This Manual

Conventions

Notices

This manual may use the following types of notice:



WARNING

Warnings alert you to the risk of severe personal injury.



CAUTION

Cautions alert you to system danger or loss of data.



NOTE

Notes call attention to important features or instructions.



TIP

Tips give guidance on procedures that may be tackled in a number of ways.



LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.

LINK
https://www.abaco.com/products/pmc-hs-serial-11050-201-serial-communications-pmc

Third-party Documents

NOTE
Technical literature describing components used on the PMC-HS Serial is available from the manufacturers' websites.

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1 • Introduction

This manual describes the PMC-HS-Serial* card (hereafter referred to as the PMC-HS-Serial), quad channel, high-speed serial PCI Mezzanine Card (PMC).

The Abaco Systems PMC-HS-Serial provides four channels of high-speed serial data communications on a single-wide PMC. The PMC-HS-Serial can be used in many data communications Local and Wide Area Networks (LAN/WAN) networking and telecommunications applications. A maximum data rate of 10 Megabits per second (Mbit/s) is supported for synchronous protocols utilizing an external clock. Up to 2 Mbit is supported for asynchronous protocols, with popular baud rates of up to 921.6 Kbaud available using the standard 14.7456 Megahertz (MHz) oscillator in RS422 interface mode. Each of the four channels is fully programmable to support many high-performance serial communications protocols, such as asynchronous, MonoSYNC, BISYNC, HDLC, SDLC, LAPB, LAPD, ISDN, and PPP.

The PMC-HS-Serial supports a wide selection of physical interfaces, configurable by software alone. Channels can be individually selected as RS232, RS422, EIA-449, EIA-530, or V.35. No hardware reconfiguration is required. Seven signal pairs for each channel are available at the rear-panel P4 connector and the front panel I/O connector. An optional transition cable is available to interface the 68-pin front panel I/O connector to four DB25s.

A 14.7456 MHz oscillator provides standard asynchronous baud rates. In addition, a user-supplied oscillator location is available for custom baud rate generation. Interrupts are fully supported for each channel. Interrupts sources include transmission error, reception error, completions of transmit packets, and completions of receive packets.

The module has a central receive FIFO and a central transmit FIFO, each 128 deep by 32 bits wide. Additionally, each channel has a local receive FIFO 17 deep by 32 bits wide, and a local transmit FIFO of 8 deep by 32 bits wide. Eight DMA controllers are available to enable the central FIFO to burst into shared memory. The PMC-HS-Serial must be inserted into a CPU slot with bus-mastering capability.

The PMC-HS-Serial uses a high performance Siemens® PEB20534 Serial Communication Controller (DSCC4®) with integral PCI bus interface.

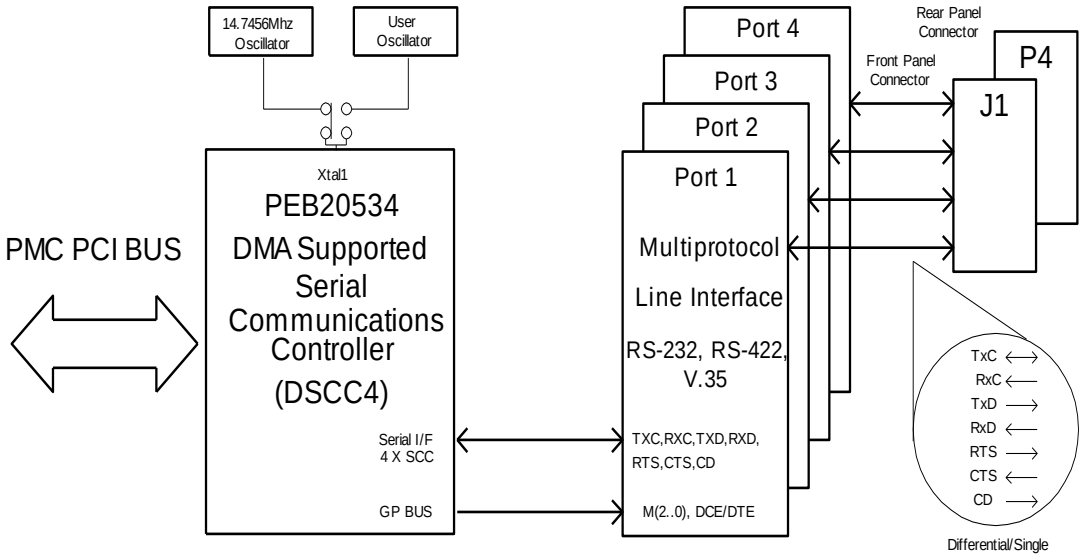
Linux and VxWorks® drivers are available for download from the Abaco website: https://www.abaco.com.

1.1 Features

The PMC-HS-Serial features the following components as shown in a simple block diagram in Figure 1-1:

- Four channels of high speed serial
- Maximum data rate of 10 Mbit/s (synchronous) and 2 Mbit/s (asynchronous)
- Asynchronous, monosync, bisync, HDLC, SDLC, LAPB, LAPD, ISDN, and PPP communication protocols supported
- RS232, RS422, EIA-449, EIA-530, or V.35 physical interfaces supported
- 306 x 32-bit total FIFO
- PMC module with front and rear panel I/O
- PCI bus master

Figure 1-1 Block Diagram



1.2 Addressing

This section provides addressing information.

1.2.1 PMC/PCI Interface

The PMC-HS-Serial is accessed by the Host system via a 33 MHz 32-bit PMC interface that is PCI specifications 2.1 compliant. The DSCC4 Bus Interface is configured into PCI mode by PMC-HS-Serial hardware (DEMUX is connected to VSS). Table 1-1 lists the **PCI Configuration Registers** of the PMC-HS-Serial.

Table 1-1 PCI Configuration Space

31 16		15 0	
Device ID (=2102H)		Vendor ID(=110AH)	
Status		Command	
Class Code		Revision ID(=00H)	
BIST	Header Type	Latency Timer	Cache Line Size
Base Address Register: contains base address of DSCC4 on-chip registers			
Base Address Register: (not used on PMC-HS-SERIAL)			
Base Address Register (not used)			
Base Address Register (not used)			
Base Address Register (not used)			
Base Address Register (not used)			
Reserved			
Reserved			
Expansion ROM Base Address(not use)			
Reserved			
Reserved			
Max_Lat (=0AH)	Min_Gnt (=02H)	Interrupt Pin (=01H)	Interrupt Line (=00H)

1.2.2 PCI Slave Interface Register Access

The PMC-HS-Serial PCI Slave Interface provides access to the DSCC4 registers from the Host system through the use of PCI Memory read and write transactions. Registers are addressed as an offset to the **Base Address Configuration Register** value. The PMC-HS-Serial does not support PCI I/O read or write commands as a PCI slave.

1.3 PCI Master Interface DMA Access

Data and structures are kept by the DSCC4 in Host memory by PCI Master DMA PCI Memory Read and PCI Memory Write transactions. The ability to become a Bus Master is a system requirement of the PMC-HS-Serial.

The PMC-HS-Serial PCI Master interface accesses the Host system memory through the use of PCI Memory Read and PCI Memory Write transactions. In order for the PMC-HS-Serial to operate, data and structures must be maintained in Host memory. The ability to become a Bus Master is a system requirement of the PMC-HS-Serial.

1.4 Interrupts

All sources of interrupts from the DSCC4 are routed to the PMC INTA signal. These sources include: SCC transmit, SCC reception, DMA controller and peripheral blocks. In addition, the DSCC4 maintains a linked list of interrupt status words in Host memory for each interrupt type.

1.5 DSCC4 Registers

The DSCC4 registers on the PMC-HS-Serial are organized into the following three groups:

- Global registers that control the general DSCC4 operation
- Four identical sets of registers that control the four Serial Communication Controllers (SCCs)
- General Purpose Port (GPP) registers that control the multi-protocol physical serial interface.

Table 1-2 presents an overview of the DSCC4 register set and associated address ranges. The complete register address is calculated as the sum of the **PCI Base Address Register** and the register offset.

Table 1-2 DSCC4 Registers

Description	Offset Range
Global	0000 00FFH
SCC0	0100 017FH
SCCl	0180 01FFH
SCC2	0200 027FH
SCC3	0280 02FFH
General Purpose Port	0400 0408H

1.6 Register Map

This section lists the DSCCR Registers.

1.6.1 Global Registers

Table 1-3 lists the offset address to each Global control register used to configure and control the DSCC4 DMA controller, central FIFOs, and general device functions. Global Registers are addressed as the listed offset from the **PCI Base Address Register** value.

Table 1-3 DSCC4 Global Registers

Offset	Register	Description
0000H	GCMDR	Global Command Register
0004H	GSTAR	Global Status Register
0008H	GMODE	Global Mode Register
000CH	IQLENR0	IQ Length Register 0
0010H	IQLENR1	IQ Length Register 1
0014H	IQSCCORXBAR	IQ SCC0 RX Base Address Register
0018H	IQSCC1RXBAR	IQ SCC1 RX Base Address Register
001CH	IQSCC2RXBAR	IQ SCC2 RX Base Address Register
0020H	IQSCC3RXBAR	IQ SCC3 RX Base Address Register
0024H	IQSCC0TXBAR	IQ SCC0 TX Base Address Register
0028H	IQSCC1TXBAR	IQ SCC1 TX Base Address Register
002CH	IQSCC2TXBAR	IQ SCC2 TX Base Address Register
0030H	IQSCC3TXBAR	IQ SCC3 TX Base Address Register
0034H	FIFOCR4	FIFO Control Register 4
003CH	IQCFGBAR	IQ CFG Base Address Register
0040H	IQPBAR	IQ Peripheral Base Address Register
0044H	FIFOCR1	FIFO Control Register 1
0048H	FIFOCR2	FIFO Control Register 2
004CH	FIFOCR3	FIFO Control Register 3
0050H	CH0CFG	Channel 0 Configuration Register
0054H	CH0BRDA	Channel 0 Base Rx Descriptor Address
0058H	CH0BTDA	Channel 1 Base Tx Descriptor Address
005CH	CH1CFG	Channel 1 Configuration Register
0060H	CHIBRDA	Channel 1 Base Rx Descriptor Address
0064H	CH1BTDA	Channel 1 Base Tx Descriptor Address
0068H	CH2CFG	Channel 2 Configuration Register
006CH	CH2BRDA	Channel 2 Base Rx Descriptor Address
0070H	CH2BTDA	Channel 2 Base Tx Descriptor Address
0074H	CH3CFG	Channel 3 Configuration Register
0078H	CH3BRDA	Channel 3 Base Rx Descriptor Address
007CH	CH3BTDA	Channel 3 Base Tx Descriptor Address
0098H	CH0FRDA	Channel 0 First Rx Descriptor Address
009CH	CH1FRDA	Channel I First Rx Descriptor Address

Offset	Register	Description
00A0H	CH2FRDA	Channel 2 First Rx Descriptor Address
00A4H	CH3FRDA	Channel 3 First Rx Descriptor Address
00B0H	CH0FTDA	Channel 0 First Tx Descriptor Address
00B4H	CHIFTDA	Channel I First Tx Descriptor Address
00B8H	CH2FTDA	Channel 2 First Tx Descriptor Address
00BCH	CH3FTDA	Channel 3 First Tx Descriptor Address
00C8H	CH0LRDA	Channel 0 Last Rx Descriptor Address
00CCH	CH1LRDA	Channel 1 Last Rx Descriptor Address
00D0H	CH2LRDA	Channel 2 Last Rx Descriptor Address
00D4H	CH3LRDA	Channel 3 Last Rx Descriptor Address
00E0H	CH0LTDA	Channel 0 Last Tx Descriptor Address
00E4H	CH1LTDA	Channel I Last Tx Descriptor Address
00E8H	CH2LTDA	Channel 2 Last Tx Descriptor Address
00ECH	CH3LTDA	Channel 3 Last Tx Descriptor Address

1.6.2 SCC Port Address Offset

Table 1-4 lists the offset starting address for each of the four sets of registers used to configure and control the SCCs. The complete SCC register set is implemented for each of the four SCCs. Individual ports are distinguished by a specific SCC starting address offset. The SCC registers are addressed by the sum of the **PCI Base Address Register** value, the SCC starting offset address, and the register offset.

Table 1-4 SC Starting Address Offsets

SCC (Port)	Starting Offset (hex)
SCC0 (Port 1)	0x100
SCC1 (Port 2)	0x180
SCC2 (Port 3)	0x200
SCC3 (Port 4)	0x280

1.6.3 SCC Registers

Table 1-5 lists the offset for each individual register in the SCC register set. The SCC registers are addressed by adding the **PCI Base Address Register** value, the SCC starting offset address, and the desired register offset.

Table 1-5 SCC Registers

Offset	Type	Register	Description
0000H	W	CMDR	Command Register
0004H	R	STAR	Status Register
0008H	R/W	CCR0	Channel Configuration Register
000CH	R/W	CCR1	Channel Configuration Register
0010H	R/W	CCR2	Channel Configuration Register
0014H	R/W	ACCM	Async Control Character Map Register
0018H	R/W	UDAC	User Defined Async Character
001CH	R/W	TSAX	Time-Slot Assignment Register Tx
0020H	R/W	TSAR	Time-Slot Assignment Register Rx
0024H	R/W	PCMMTX	PCM Mask Register Tx
0028H	R/W	PCMMRX	PCM Mask Register Rx
002CH	R/W	BRR	Baud Rate Register
0030H	R/W	TIMR	Timer Register
0034H	R/W	XADR	Transmit Address Register
0038H	R/W	RADR	Receive Address Register
003CH	R/W	RAMR	Receive Address Mask Register
0040H	R/W	RLCR	Receive Length Check Register
0044H	R/W	XNXFR	XON/XOFF Register
0048H	R/W	TCR	Termination Character Register
004CH	R/W	TICR	Tx Immediate Character Register
0050H	R/W	SYNCR	Synchronization Character Register
0054H	R/W	IMR	Interrupt Mask Register
0058H	R/W	ISR	Interrupt Status Register

1.6.4 GPP Registers

Table 1-6 lists the GPP registers used to select the physical serial interface for each of the four ports. The GPP ports are addressed by adding the register offset to the **PCI Base Address Register** value.

Table 1-6 General Purpose Port Registers

Offset	Register	Description
0400H	GPDIR	General Purpose Port Direction Register
0404H	GPDATA	General Purpose Port Data Register
0408H	GPIM	General Purpose Port Interrupt Mask Register

2 • Programming

This chapter describes selections for the physical interface and as well as clocking information.

2.1 GPP Initialization and Port Mapping

Selection of the four serial port physical interfaces is accomplished via the DSCC4 16-bit General Purpose Bus.

2.1.1 Initialization

Host initialization code must program the **DSCC4 Global Mode Register** to configure the peripheral block to 16-bit General Purpose Bus mode, by writing a 0x4 to bits 18 through 16 (GMODE.PERCFG[2:0]). In addition, the GPP **GPDIR Register** must be written with 0x0000FFFF configuring all General Purpose pins as outputs. Data written to the **GPDATA Register** controls the physical interface selection (*see GPP Port Mapping*). Before initialization, the general purpose bus is pulled high by PMC-HS-Serial hardware. Thus, reading the GPDATA with the GPDIR set to inputs (0x00000000 or default) yields a 0xXXXXFFFF. This value distinguishes the PMC-HS-Serial from other Abaco products that are based on the DSCC4.

2.1.2 Port Mapping

Once the GPP is initialized, the Physical Serial Interface is selected for each port via the **GPDATA Register**. Each port is controlled by four bits of the 16-bit data port. The Multi-Protocol Interface (MPI) is provided by a Linear Technology Multi-Protocol LTC1343/LTC1543/LTC1544 transceiver/terminator set for each port controlled by three-mode pins (M2,M1 and M0), and one DCE pin (D). Table 2-1 shows the interconnection of the General Purpose Bus to the Multi-Protocol Interface pins.

Table 2-1 GPDATA Register to Multi-Protocol Interface Mapping

MSB															LSB
Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Port 4				Port 3				Port 2				Port 1			
D	**M2**	**M1**	**M0**	**D**	**M2**	**M1**	**M0**	**D**	**M2**	**M1**	**M0**	**D**	**M2**	**M1**	**M0**

where: **M[2:0]** = Mode pin
D = DCE pin

2.2 Physical Interface Selection

Table 2-2 lists the Physical Interface selections for each port. The selection is chosen by writing the four bits in the **GPP Register** that correspond to each of the four ports (see GPP Port Mapping). After power-on or PMC reset, all four ports are in the high-impedance mode (0xF) until programmed otherwise.

Table 2-2 Physical Interface Selection Guide

Physical Interface Mode	TxC Signal Mode	MPI Control Bits				Notes
		D	M2	M1	M0	
RS232	Receiver	0	1	1	0	
	Driver	1				
RS422 / RS530	Receiver	0	0	1	0	
	Driver	1				
RS530A	Receiver	0	0	0	1	CD is configured as single ended RS423 in this mode. All other signals are RS422.
	Driver	1				
V.35	Receiver	0	1	0	0	
	Driver	1				
High Impedance	Receiver	X	1	1	1	Reset Mode.
	Driver					

RS232 Mode

In RS232 mode, all circuits are unbalanced bipolar V.28 specification compliant. Cable termination is not necessary as the receiver supplies the necessary 5K resistor to ground. Table 2-3 details the serial signal configuration for RS232 mode.

Table 2-3 RS232 Mode Signal Definitions

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	V.28	None	Single Ended
RxD	V.28	5K (Receiver)	Single Ended
TxC as a Receiver	V.28	5K (Receiver)	Single Ended
TxC as a Driver	V.28	None	Single Ended
RxC	V.28	5K (Receiver)	Single Ended
RTS	V.28	None	Single Ended
CTS	V.28	5K (Receiver)	Single Ended
CD	V.28	5K (Receiver)	Single Ended

RS422/RS530 Mode

In RS422/RS530 mode, all circuits are balanced V.11 standard compliant. Table 2-4 details the serial signal configuration for RS422/RS530 mode.

Table 2-4 RS422/RS530 Mode Signal Definitions

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	V.11	None	Differential
RxD	V.11	V.11	Differential
TxC as a Receiver	V.11	V.11	Differential
TxC as a Driver	V.11	None	Differential
RxC	V.11	V.11	Differential
RTS	V.11	None	Differential
CTS	V.11	None	Differential
CD	V.11	None	Differential

RS530A Mode

RS530A mode is identical to RS422/RS530 mode, except CD is a single-ended RS423 input. If this mode is selected and the source of CD is a differential RS422 signal, then unreliable operation of CD may occur.

Table 2-5 details the serial signal configuration for RS530A mode.

Table 2-5 RS530A Mode

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	V.11	None	Differential
RxD	V.11	V.11	Differential
TxC as a Receiver	V.11	V.11	Differential
TxC as a Driver	V.11	None	Differential
RxC	V.11	V.11	Differential
RTS	V.11	None	Differential
CTS	V.11	None	Differential
CD	V.10	None	Single Ended

V.35 Mode

In V.35 mode, the clock and data signals are balanced V.35 compliant, while the control signals are unbalanced V.28 compliant. Table 2-6 details the serial signal configuration for V.35 mode.

Table 2-6 V.35 Mode Signal Definition

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	V.35	V.35	Differential
RxD	V.35	V.35	Differential
TxC as a Receiver	V.35	V.35	Differential
TxC as a Driver	V.35	V.35	Differential
RxC	V.35	V.35	Differential
RTS	V.28	None	Single Ended
CTS	V.28	None	Single Ended
CD	V.28	None	Single Ended

High Impedance Mode

Table 2-7 details the serial signal configuration for High Impedance mode.

Table 2-7 High Impedance Mode Signal Definition

Signal	Driver/Receiver Mode	Termination Type	Signal Type
TxD	High Impedance	V.11	N/A
RxD	High Impedance	V.11	N/A
TxC as a Receiver	High Impedance	V.11	N/A
TxC as a Driver	High Impedance	V.11	N/A
RxC	High Impedance	V.11	N/A
RTS	High Impedance	None	N/A
CTS	High Impedance	None	N/A
CD	High Impedance	None	N/A

2.3 Baud Rate Selection

The PMC-HS-Serial provides a rich and flexible set of serial clocking and data recovery solutions. Baud rate limitations on the PMC-HS-Serial are determined by a combination of complex user-specific choices, such as the communication protocol, the clock source, the clock mode and the physical interface mode.



NOTE

The maximum baud rates given in this section do not reflect external user-controlled issues, such as cable quality, cable length, cable impedance, and far-end termination.

2.3.1 Maximum Baud Rates

The following three tables (Table 2-8, Table 2-9, and Table 2-10) show the maximum baud rates allowed on the PMC-HS-Serial card.

Table 2-8 Baud Rates Using an External Clock

Communication Protocol	Physical Interface	Maximum Baud Rate
Synchronous	RS422/V.35	10.0 Mbaud
	RS232	115.2 Kbaud
Isochronous	RS422/V.35	1.8432 Mbaud
	RS232	115.2 Kbaud
Asynchronous	RS422/V.35	921.6 Kbaud
	RS232	115.2 Kbaud

Table 2-9 Baud Rates Using the Standard 14.7456 MHz Oscillator

Communication Protocol	Physical Interface	Maximum Baud Rate
Synchronous	RS422/V.35	1.8432 Mbaud
	RS232	115.2 Kbaud
Isochronous	RS422/V.35	1.8432 Mbaud
	RS232	115.2 Kbaud
Asynchronous	RS422/V.35	921.6 Kbaud
	RS232	115.2 Kbaud

Table 2-10 Baud Rates Using a User Oscillator

Communication Protocol	Physical Interface	Maximum Baud Rate
Synchronous	RS422/V.35	2.0 Mbaud
	RS232	115.2 Kbaud
Isochronous	RS422/V.35	2.0 Mbaud
	RS232	115.2 Kbaud
Asynchronous	RS422/V.35	2.0 Mbaud
	RS232	115.2 Kbaud

Example Asynchronous Baud Rates

The DSCC4 provides an independently programmable Baud Rate Generator (BRG) for each port that may be used in conjunction with the onboard 14.7456 MHz oscillator to provide commonly used asynchronous baud rates. The baud rate for each port is set by programming the Bit Clock Rate bit in the **SCC Channel Configuration Register** (CCRO.BCR) and the BRM and BRN fields of the **SCC Baud Rate Register** [BRR.BRM(3...0) and BRR.BRN(5...0)]. For asynchronous communication, the CCR BCR is set to one, providing a 16 times clock. The baud rate is then controlled by the **Baud Rate Register** (BRR) using the formula:

```
fbrg = fin/((N+1) * 2^M * D)
```

where:

`M` = 0-15 in BRM(3...0)
`N` = 0-63 in BRN(5...0)
`D` = 16 (BCR=1)
`fbrg` = Frequency of the desired baud rate
`fin` = Frequency in = 14.7456 MHz

Table 2-11 lists the BRM and BRN values for popular baud rates in Asynchronous 16X Mode.

Table 2-11 Common Asynchronous (16) Baud Rates

Baud Rate	BRM(3...0) Value	BRN(5...0) Value
50	0x09	0x23
200	0x07	0x23
300	0x06	0x2F
600	0x05	0x2F
1,200	0x04	0x2F
2,400	0x03	0x2F
4,800	0x02	0x2F
9,600	0x01	0x2F
19,200	0x00	0x2F
38,400	0x00	0x17
57,600	0x00	0x0F
76,800	0x00	0x0B
115,200	0x00	0x07
230,400	0x00	0x03
460,800	0x00	0x01
921,600	0x00	0x00

3 • User-Supplied Oscillator

When the PMC-HS-Serial is used in systems where an external clock is not supplied and the standard 14.7456 MHz oscillator is not an even multiple of the desired baud rate, a user-supplied oscillator may be installed.

3.1 User-Supplied Oscillator Location

The user-supplied oscillator must be installed in the User Oscillator Location (OSC2).

WARNING

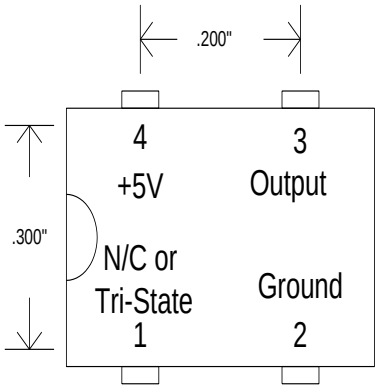
The user-supplied oscillator installation procedure requires the soldering and removal of surface mounted electronic components and should be done only by qualified personnel in a static-controlled environment.

3.2 User-Supplied Oscillator Specifications

The user-supplied oscillator must be a HCMOS/TTL 5.0V D.C. device in a 4-pin, J-lead, surface mount package and must be less than or equal to 33.33 MHz with a 10% (or better) duty cycle. The pin assignment and lead spacing is shown in Figure 3-1.

Common frequency tolerance is 100ppm, but tighter tolerances are available if the application demands it. The Ecliptek® Corporation EC1400-10.000M is an example of a 10.000 MHz oscillator that is suitable for user-supplied oscillator use.

Figure 3-1 User-Supplied Oscillator Pinout and Dimensions



3.3 User-Supplied Oscillator Precaution

As a precaution, please read the following warning:



WARNING

The User-Supplied Oscillator installation procedure requires the soldering and removal of sensitive surface mounted electronic components and should be done only by qualified personnel in a static-controlled environment.

3.4 User-Supplied Oscillator Installation

To install the User-Supplied Oscillator, perform the following steps:

1. Solder the user-supplied oscillator in position “OSC2”.
2. Remove and retain resistor “R5”.
3. Solder the resistor removed in step two in position “R6”.

4 • Connector Signal Assignment

This chapter provides pin assignment information for connectors.

4.1 Front Panel Serial I/O Pin Assignment

To make front panel connections to the serial I/O interface on the PMC-HS-Serial, use a 68-pin SCSI III style connector with pin assignments as described in Table 4-1.

Table 4-1 Front Panel Serial I/O Pin Assignment

Front Panel Connector J1 Pin #	Port #	Signal Mnemonics			Front Panel Connector J1 Pin #	Port #	Signal Mnemonics		
		RS232	RS530	V.35			RS232	RS530	V.35
1	1	CD	CDA/+	CD	35	2	CD	CDA/+	CD
2			CDB/-		36			CDB/-	
3		RXD	RXDA/+	RXDA/+	37		RXD	RXDA/+	RXDA/+
4		RTS	RTSA/+	RTS	38		RTS	RTSA/+	RTS
5		TXD	TXDA+	TXDA/+	39		TXD	TXDA/+	TXDA/+
6		CTS	CTSA+	CTS	40		CTS	CTSA/+	CTS
7			RTSB/-		41			RTSB/-	
8			CTSB/-		42			CTSB/-	
9		GND	GND	GND	43		GND	GND	GND
10			TXDB/-	TXDB/-	44			TXDB/-	TXDB/-
11			RXDB/-	RXDB/-	45			RXDB/-	RXDB/-
12		TXC	TXCA/+	TXCA/+	46		TXC	TXCA/+	TXCA/+
13			TXCB/-	TXCB/-	47			TXCB/-	TXCB/-
14			GND	GND	48			GND	GND
15		RXC	RXCA/+	RXCA/+	49		RXC	RXCA/+	RXCA/+
16			RXCB/-	RXCB/-	50			RXCB/-	RXCB/-
17	3	CD	CDA/+	CD	51	4	CD	CDA/+	CD
18			CDB/-		52			CDB/-	
19		RXD	RXDA/+	RXDA/+	53		RXD	RXDA/+	RXDA/+
20		RTS	RTSA/+	RTS	54		RTS	RTSA/+	RTS
21		TXD	TXDA/+	TXDA/+	55		TXD	TXDA/+	TXDA/+
22		CTS	CTSA/+	CTS	56		CTS	CTSA/+	CTS
23			RTSB/-		57			RTSB/-	
24			CTSB/-		58			CTSB/-	
25		GND	GND	GND	59		GND	GND	GND
26			TXDB/-	TXDB/-	60			TXDB/-	TXDB/-
27			RXDB/-	RXDB/-	61			RXDB/-	RXDB/-
28		TXC	TXCA/+	TXCA/+	62		TXC	TXCA/+	TXCA/+
29			TXCB/-	TXCB/-	63			TXCB/-	TXCB/-
30			GND	GND	64			GND	GND
31		RXC	RXCA/+	RXCA/+	65		RXC	RXCA/+	RXCA/+
32			RXCB/-	RXCB/-	66			RXCB/-	RXCB/-
33	4	Reserved (INB/-)			67		Reserved (OUTB/-)		
34		Reserved (INA/+)			68		Reserved (OUTA/+)		

4.2 Rear Panel Serial I/O Pin Assignment

Rear panel connections to the serial I/O interface are made on the PMC-HS-Serial using the 64-pin PMC P4 connector with pin assignments as described in Table 4-2.

Table 4-2 Rear Panel Serial I/O Pin Assignment

Rear Panel Connector P4 Pin #	Port #	Signal Mnemonics			Rear Panel Connector P4 Pin #	Port #	Signal Mnemonics		
		RS232	RS530	V.35			RS232	RS530	V.35
1	1	CD	CDA/+	CD	33	3	CD	CDA/+	CD
2			CDB/-		34			CDB/-	
3		RXD	RXDA/+	RXDA/+	35		RXD	RXDA/+	RXDA/+
4		RTS	RTSA/+	RTS	36		RTS	RTSA/+	RTS
5		TXD	TXDA/+	TXDA/+	37		TXD	TXDA/+	TXDA/+
6		CTS	CTSA/+	CTS	38		CTS	CTSA/+	CTS
7			RTSB/-		39			RTSB/-	
8			CTSB/-		40			CTSB/-	
9		GND	GND	GND	41		GND	GND	GND
10			TXDB/-	TXDB/-	42			TXDB/-	TXDB/-
11			RXDB/-	RXDB/-	43			RXDB/-	RXDB/-
12		TXC	TXCA/+	TXCA/+	44		TXC	TXCA/+	TXCA/+
13			TXCB/-	TXCB/-	45			TXCB/-	TXCB/-
14			GND	GND	46			GND	GND
15		RXC	RXCA/+	RXCA/+	47		RXC	RXCA/+	RXCA/+
16			RXCB/-	RXCB/-	48			RXCB/-	RXCB/-
17	2	CD	CDA/+	CD	49	4	CD	CDA/+	CD
18			CDB/-		50			CDB/-	
19		RXD	RXDA/+	RXDA/+	51		RXD	RXDA/+	RXDA/+
20		RTS	RTSA/+	RTS	52		RTS	RTSA/+	RTS
21		TXD	TXDA/+	TXDA/+	53		TXD	TXDA/+	TXDA/+
22		CTS	CTSA/+	CTS	54		CTS	CTSA/+	CTS
23			RTSB/-		55			RTSB/-	
24			CTSB/-		56			CTSB/-	
25		GND	GND	GND	57		GND	GND	GND
26			TXDB/-	TXDB/-	58			TXDB/-	TXDB/-
27			RXDB/-	RXDB/-	59			RXDB/-	RXDB/-
28		TXC	TXCA/+	TXCA/+	60		TXC	TXCA/+	TXCA/+
29			TXCB/-	TXCB/-	61			TXCB/-	TXCB/-
30			GND	GND	62			GND	GND
31		RXC	RXCA/+	RXCA/+	63		RXC	RXCA/+	RXCA/+
32			RXCB/-	RXCB/-	64			RXCB/-	RXCB/-

4.3 PMC P1 Connector Pin Assignments

Table 4-3 lists the PMC P1 Connector PCI pin assignments, where:

N/C = Not Connected

BP = Bypass Only

Table 4-3 PMC P1 Connector PCI Pin Assignment

Pin Number	Signal Name	Signal Name	Pin Number
1 (N/C)	TCK	-12V	2 (BP)
3	Ground	INTA#	4
5 (N/C)	INTB#	INTC#	6 (N/C)
7	BUSMODEI#	+5V	8
9 (N/C)	INTD#	PCI-RSVD	10 (N/C)
11	Ground	PCI-RSVD	12 (N/C)
13	CLK	Ground	14
15	Ground	GNT#	16
17	REQ#	+5V	18
19 (N/C)	V (I/O)	AD[31]	20
21	AD[28]	AD [27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31 (N/C)	V (I/O)	AD[17]	32
33	FRAME#	Ground	34
35	Ground	IRDY#	36
37	DEVSEL#	+5V	38
39	Ground	LOCK#	40 (N/C)
41 (N/C)	SDONE#	SBO#	42 (N/C)
43	PAR	Ground	44
45 (N/C)	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	Ground	C/BE[O]#	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57 (N/C)	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64#	64 (N/C)

4.4 PMC P2 Connector Pin Assignments

Table 4-4 lists the PMC P2 Connector PCI pin assignments, where:

N/C = Not Connected

BP = Bypass Only

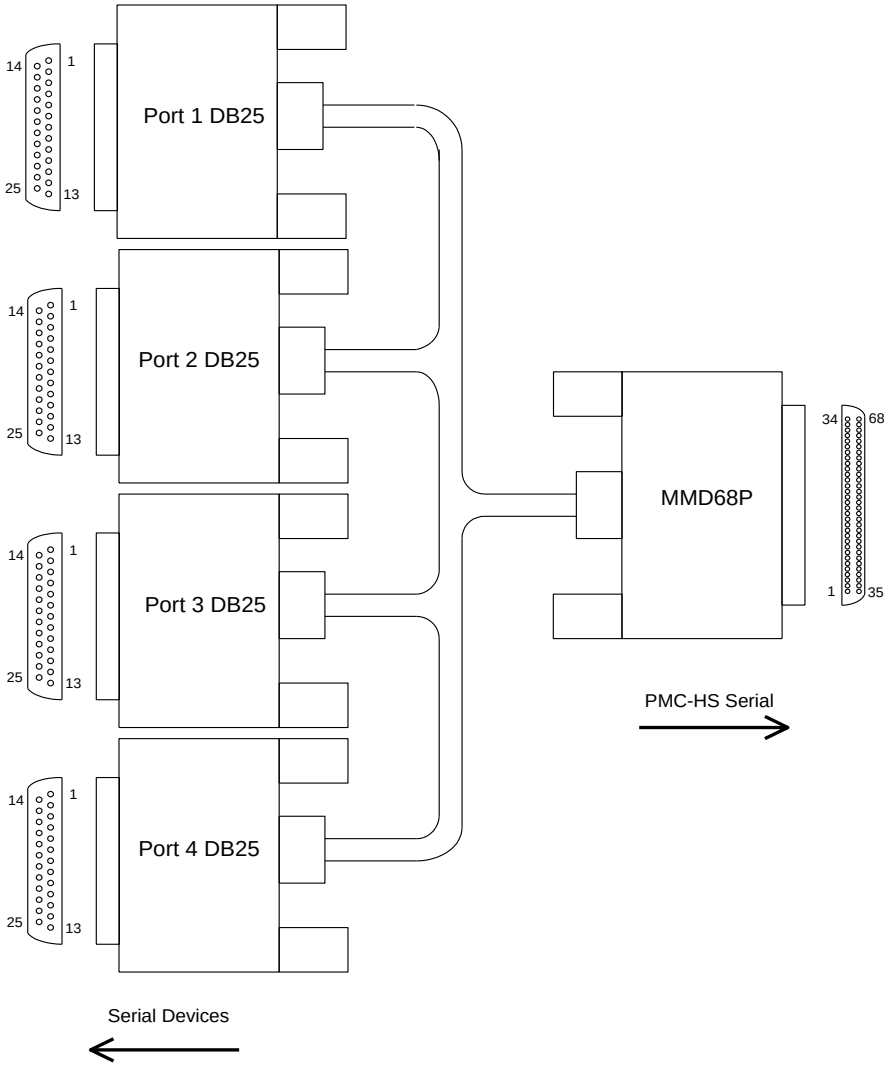
Table 4-4 PMC P2 Connector Pin Assignments

Pin Number	Signal Name	Signal Name	Pin Number
1 (BP)	+12V	TRST#	2 (N/C)
3 (N/C)	TMS	TDO	4 (N/C)
5 (N/C)	TDI	Ground	6
7	Ground	PCI-RSVD	8 (N/C)
9 (N/C)	PCI-RSVD	PCI-RSVD	10 (N/C)
11 (N/C)	BUSMODE2#	+3.3V	12 (BP)
13	RST#	BUSMODE3#	14
15 (BP)	3.3V	BUSMODE4#	16
17 (N/C)	PCI-RSVD	Ground	18
19	AD[30],	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24 (BP)
25	IDSEL	AD[23]	26
27 (BP)	+3.3V	AD[20]	28
29	AD[18]	Ground	30
31	AD[16]	C/BE[2]#	32
33	Ground	PMC-RSVD	34 (N/C)
35	TRDY#	+3.3V	36 (BP)
37	Ground	STOP#	38
39	PERR#	Ground	40
41 (BP)	+3.3V	SERR#	42
43	C/BE[1]#	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50 (BP)
51	AD[07]	PMC-RSVD	52 (N/C)
53 (BP)	+3.3V	PMC-RSVD	54 (N/C)
55 (N/C)	PMC-RSVD	Ground	56
57 (N/C)	PMC-RSVD	PMC-RSVD	58 (N/C)
59	Ground	PMC-RSVD	60 (N/C)
61 (N/C)	ACK64#	+3.3V	62 (BP)
63	Ground	PMC-RSVD	64 (N/C)

5 • Front Panel Cable

The Front Panel Cable is supplied with the PMC-HS-Serial engineering kit. The Front Panel Cable (shown in Figure 5-1) consists of a MMD 68-pin male connector that mates with the Front Panel connector and one DB2 (25-pin "D") male connector for each of the four serial ports. The pinout of the DB25 connectors is compatible with RS232 and RS530 applications.

Figure 5-1 Front Panel Cable



5.1 Front Panel Cable Signal Assignment

Table 5-1 lists the Front Panel Cable Signal Assignment.

Table 5-1 Front panel Cable Signal Assignment

DB25 Connector/ Port #	DB25 Pin #	MMD-68 Pin #	Signal Mnemonic	DB25 Connector/ Port #	DB25 Pin #	MMD-68 Pin #	Signal Mnemonic
1	2	5	TXDA/+	2	2	39	TXDA/+
	3	3	RXDA/+		3	37	RXDA/+
	4	4	RTSA/+		4	38	RTSA/+
	5	6	CTSA/+		5	40	CTSA/+
	7	9	GND		7	43	GND
	8	1	CDA/+		8	35	CDA/+
	9	16	RXCB/-		9	50	RXCB/-
	10	2	CDB/-		10	36	CDB/-
	12	13	TXCB/-		12	47	TXCB/-
	13	8	CTSB/-		13	42	CTSB/-
	14	10	TXDB/-		14	44	TXDB/-
	15	12	TXCA/+		15	46	TXCA/+
	16	11	RXDB/-		16	45	RXDB/-
	17	15	RXCA/+		17	49	RXCA/+
	19	7	RTSB/-		19	41	RTSB/-
3	2	21	TXDA/+	4	2	55	TXDA/+
	3	19	RXDA/+		3	53	RXDA/+
	4	20	RTSA/+		4	54	RTSA/+
	5	22	CTSA/+		5	56	CTSA/+
	7	25	GND		7	59	GND
	8	17	CDA/+		8	51	CDA/+
	9	32	RXCB/-		9	66	RXCB/-
	10	18	CDB/-		10	52	CDB/-
	12	29	TXCB/-		12	63	TXCB/-
	13	24	CTSB/-		13	58	CTSB/-
	14	26	TXDB/-		14	60	TXDB/-
	15	28	TXCA/+		15	62	TXCA/+
	16	27	RXDB/-		16	61	RXDB/-
	17	31	RXCA/+		17	65	RXCA/+
	19	23	RTSB/-		19	57	RTSB/-

5.2 Custom Front Panel Cable Information

A custom front panel cable can be made with a ribbon cable style 68-pin connector and one or more crimp and poke serial connectors. The Amp® Inc. part number for the SCSI III 68-pin male ribbon connector is 749621-7. An example of a DB25 crimp and poke male connector is the Amp Inc. 205208-1. For higher speed differential signaling, a twisted pair cable with 100 Ohm impedance is recommended.



NOTE

For additional information on cables such as ordering a new cable, contact your Abaco Technical Support or Sales representative.

6 • Installation

Before working with any Abaco component, take the necessary precautions to prevent electrostatic discharge (ESD), which can damage the system.

6.1 Installation Precautions

The following general safety precautions represent warnings of certain dangers of which Abaco Systems is aware. Failure to comply with these or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of the equipment. Abaco Systems assumes no liability for the user's failure to comply with these requirements.

Also follow all warning instructions contained in associated system equipment manuals.

WARNING

Use extreme caution when handling, testing, and adjusting this equipment. This device may operate in an environment containing potentially dangerous voltages.

Ensure that all power to the system is removed before installing any device.

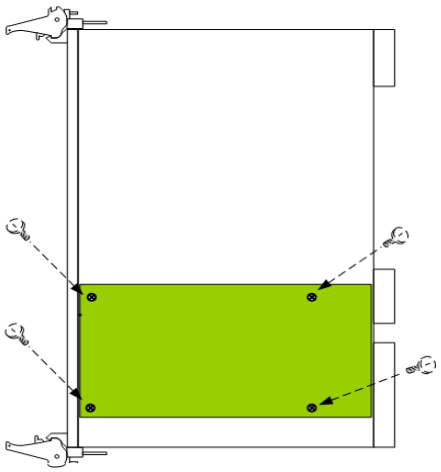
To minimize shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet IEC safety standards.

6.2 Installation Procedure

To install the PMC-HS Serial, perform the following steps.

1. Turn the system power OFF.
2. Remove the host board from the chassis, if currently installed.
3. Locate the PMC connector on the host board.
4. Remove the four screws from the bottom of the standoff of the PMC.
5. Align the connectors on the card with the connectors on the host board.
6. Carefully push the module into the mating connectors on the host board.
7. Use the four screws to connect the PMC stand-offs to the host board.
8. Re-insert the host board into the chassis.
9. The chassis may now be powered up.

Figure 6-1 Attaching the PMC-HS-Serial



7 • Specification

Table 7-1 PMC-HS-Serial Specification

Form Factor	PMC
PCI Interface	33 MHz, 32-bit, master/slave Bus mastering required
PMC Conformance	PCI Protocol and Electrical Rev 2.0 Specification.
PCI Interface/Serial Controller	Siemens PEB 20534
Number of Serial Channels	Four
Maximum Data Rate	Asynchronous: 2 Mbit/s Synchronous: 10 Mbit/s
Physical Levels Supported	RS232, RS422, EIA-449, EIA-530, V.35
Protocols Supported	Asynchronous UART, bisync, monosync, HDLC, SDLC, LAPB, LAPD, PPP, ISDN BRI
RS422, EIA-449, EIA-530 Signals Supported	RxD+, RxD-, RxC+, RxC-, CTS+, CTS-, CD+, CD-, TxD+, TxD-, TxC+, TxC-, RTS+, RTS-
RS232 Signals Supported	RxD, RxC, CTS, CD, TxD, TxC, RTS
V.35 Signals Supported	TxD+, TxD-, RxD+, RxD-, TxC+, TxC-, RxC+, RxC-, CTS, RTS, CD
FIFOs	Local Receive 17 x 32-bit, each channel Local Transmit 8 x 32-bit, each channel Central Receive 128 x 32-bit Central Transmit 128 x 32-bit
Onboard Oscillator	14.7456 MHz to support standard asynch baud rates. User-supplied oscillator location is available for custom baud rate generation.
DMA Controllers	Eight
Front Panel I/O	68-pin high density female connector
Rear Panel I/O	Via PMC P4
Dimensions	75.0 mm x 150.0 mm
Weight	0.085 kg (0.19 lb)
Power Requirements	+5.0 VDC (typical): 860 mA operating V.35 mode 640 mA operating EIA 422 mode 430 mA operating EIA-232 mode
Environmental	Operating temperature: 0 to 70°C Humidity: 5 to 95% non-condensing Storage: -40 to +85°C

Glossary

BISYNC	(**BI**nary **SYNC**hronous) A major category of synchronous communications protocols used in mainframe networks. BISYNC communications require the synchronization of both sending and receiving devices before transmission of data is started.
Downstream transaction	A data transfer in which the initiator is on a PCI bus closer to the host system than the target is. See also Upstream transaction.
EMI	ElectroMagnetic Interference.
Expansion enclosure	The expansion chassis with installed backplane and power supply.
Expansion Unit	Includes the host card, expansion enclosure and its components, and the interface cables. See expansion enclosure.
Expansion Unit Cable	Connects the host card and the backplane controller card installed in the expansion enclosure.
GByte	Gigabyte. Two to the thirtieth power (exactly 1,073,741,824) bytes.
Hz	Hertz.
Host card	The Abaco circuit card that installs in the host computer.
Host system	The computer system to which the expansion enclosure is attached.
Initiator	Same as Master.
ISR	Interrupt Service Routine.
KByte	Kilobyte. Two to the tenth power (exactly 1024) bytes.
LED	Light Emitting Diode. The indicator lights on the expansion enclosure are LEDs.
Master	One of the two devices involved in a data transfer. The master initiates the transfer to the target. See also Target.
MByte	Megabyte. Two to the twentieth power (exactly 1,048,576) bytes.
MByte/s	Megabytes per second. Exactly 1,000,000 bytes per second.
MHz	Megahertz.
msec	Millisecond. 1/1,000 of a second.
nsec or ns	Nanosecond. 1/1,000,000,000 of a second.
PCI	Peripheral Component Interconnect.
PCI to PCI Bridge	A device that interconnects two PCI buses so that the buses operate independently, yet can communicate with each other.
Round-Robin Arbitration	A system used by the Expansion Unit to force the add-in cards to take turns using the PCI bus.
Target	One of the two devices involved in a data transfer. The target responds to the master's request. See also Master.
Upstream transaction	A data transfer in which the initiator is on a PCI bus further away from the host system than the target is. See also Downstream transaction.

µsec Microsecond. 1/1,000,000 of a second.

Window A range of addresses that the Unit responds to for a specific function; a reserved area of memory.

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Publication No. 89002090 Rev. D.0

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