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PMC-3210
&
PMC-3211

PMC with 4 Full Duplex Serial Channels

User Manual

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PMC-3210 & PMC-3211
PMC with 4 Full Duplex Serial Channels

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Product Description

Introduction

The PMC-3210 and the PMC-3211 provides up to four full duplex serial ports, based on the Zilog Z85230 Serial Communications Controller (SCC). Two Z85230 ESCCs are used to implement four serial ports that are factory configured for RS-232-C for the PMC-3210. The PMC-3211 is factory configured for two RS-232-C ports and two RS-422; each serial port has two dedicated DMA channels. The PMC-3210 does not included DMA support.

Each serial channel has an independent baud rate generator. A 16MHz oscillator is used to provide standard asynchronous baud rates. Baud rate is software configurable from 50 bps to 125 kbps, via the on-board programmable baud rate generator. In addition, programmable bit length, parity and stop bits are provided to support all asynchronous protocols.

Both PMCs are compliant with standard PMC specifications IEEE P1386.1. Both are also direct replacements for SciTech SciCom PMCs.

Key Features

The following is a brief description of the features the PMC-3210 and PMC-3211 provide. For additional information refer to the specific section in this manual.

- PCI Slave — The PCI slave interface provides access to PCI configuration registers, Z85230 registers, and for the PMC-3211 the DMA registers.
- PCI Master — The PCI master interface allows the DMA controllers to transfer serial data directly to/from PCI memory. This feature is available only on the PMC-3211.
- PCI DMA — Each DMA channel provides an individual 32-bit transfer counter, 32-bit address register, 32-bit data holding register, and interrupt and control bits. These features are only available on the PMC-3211.
- Z85230 — Each Z85230 SCC provides two independent full duplex serial channels, capable of data rates as high as 4.0Mbit/s.
- RS-232/422 — PMC-3210 supports RS-232 only. PMC-3211 supports both RS-232 and RS-422.

Product highlights include:

- Direct replacement for SciTech SciCom PMC (with DMA use PMC-3211; without DMA use PMC-3210)
- Four full-duplex serial communication channels
- Asynchronous transfers from 50 bps – 125 Kbps
- PMC-3210 is factory configured for RS-232-C
- PMC-3211 is factory configured for RS-232 or RS-422
- Front panel I/O
- Direct PCI bus interface (32-bit, 33MHz), bus slave operation only

Block Diagram

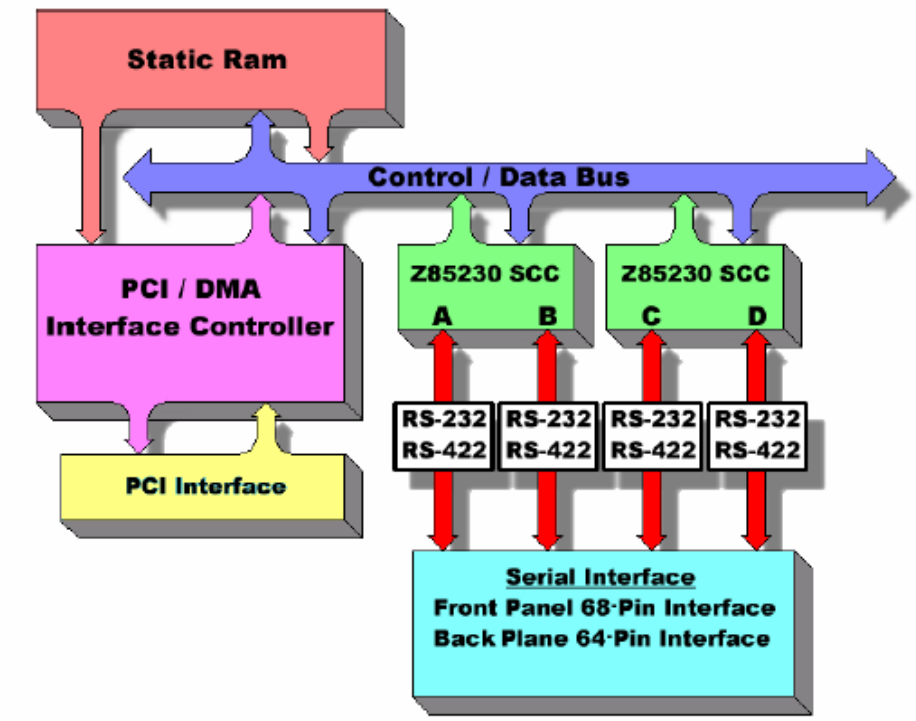


Figure 1. Block Diagram

Additional Technical Documents Available

- Z85230 Zilog DATACOM ICs, Zilog Inc., 1991.
- *PCI Local Bus Specification. Revision 2.0*, April 30, 1993; PCI Special Interest Group.
- Draft Standard Physical and Environmental Layers of PCI Mezzanine Cards: PMC P1386.1/Draft 1.7 February 27, 1995.
- Draft for a Common Mezzanine Card Family: CMC P1386/Draft 1.7 February 27, 1995.
- *EIA Standard RS-232-C*, August 1969. Interface Between Data Terminal Equipment and Data Communication Equipment Employing Serial Binary Data Interchange.
- *EIA Standard RS-422-A*, December 1978. Electrical Characteristics of Balanced Voltage Digital Interface Circuits.
- *EIA Standard 530,* March 1987. High Speed 25-Position Interface for Data Terminal Equipment and Data Circuit-Terminating Equipment.

The Printed Circuit Board

The figure below indicates the jumper configurations and options.

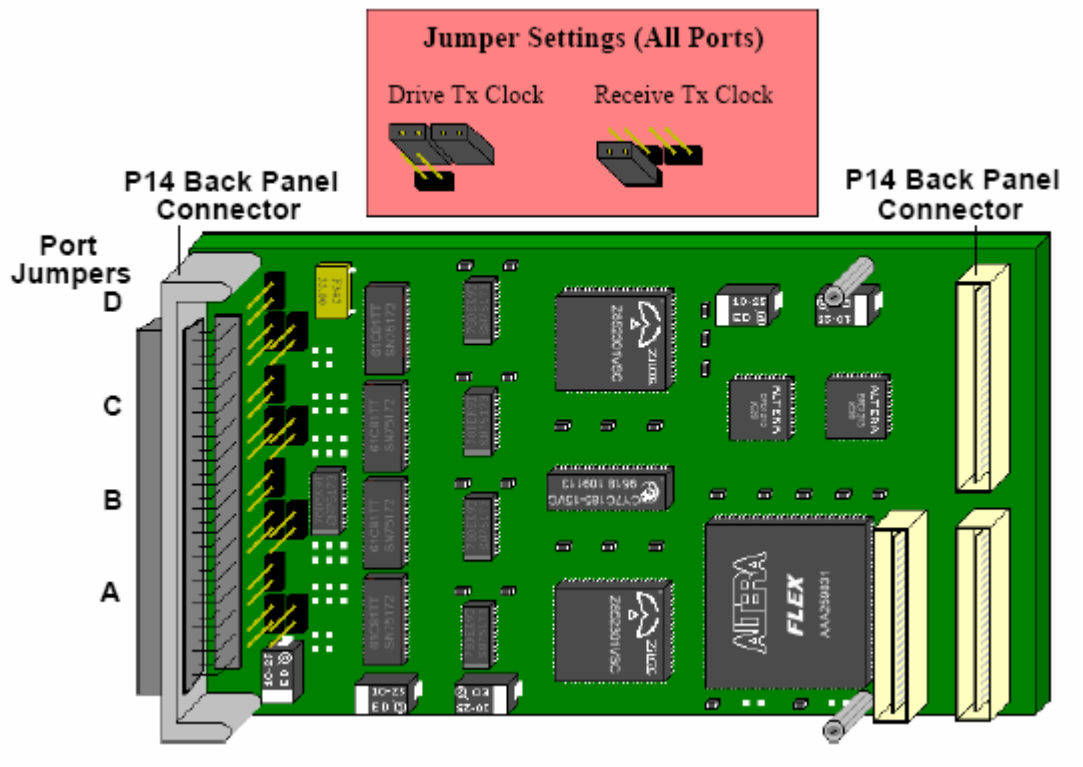


Figure 2. Jumper Diagram

Installation

The PMCs can be damaged by Electrostatic Discharge (ESD). Please follow proper grounding techniques when handling this and other electronic devices.

When installing the PMC, hold the card at an angle while sliding the faceplate into the opening on the baseboard. Align the P11 and P12 connectors and gently press the card into place. Be careful not to force the card onto the baseboard, or you may damage one or both devices.

Once installed, secure the card to the baseboard using the 4 mounting holes on the baseboard.

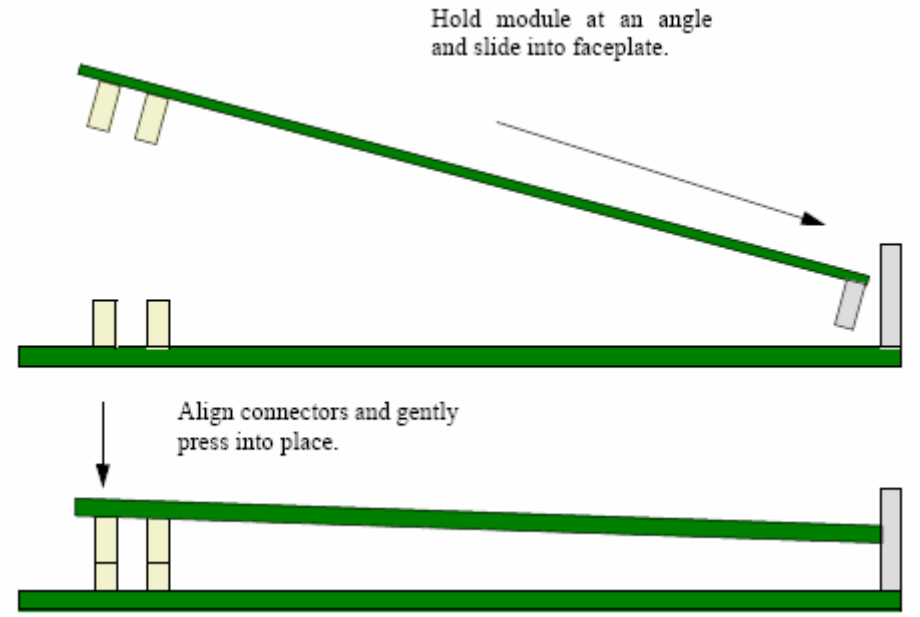


Figure 3. PMC Installation

The PMC/PCI Interface

Introduction

The PMCs conform to the PMC interface specification, which is based on the PCI bus interface standard. This chapter describes the implementation of these interface standards.

The PMC interface standard defines the physical and environmental aspects of the PCI mezzanine card interface. The PMC-3210 and PMC-3211 are single width cards that can provide I/O through a 68-pin front panel connector or through a back plane P2 (VMEbus) connector.

The PCI interface standard defines the electrical aspects of the interface. The PMCs provide a PCI compliant slave interface, allowing the host module to transfer data to/from the serial interface controllers. The PMC-3211 also provides a PCI master interface, which allows data transfers directly to/from the serial interface to be performed by DMA.

Configuration Space

The PCI interface defines a standard programming model for the configuration of PCI devices. This interface is defined as the configuration space. This section defines the PMC-3210 and PMC 3211 implementation of the PCI configuration space. The table below shows the configuration space, as defined by the PCI bus specification. Following the table is a description of each register, as implemented on the PMCs.

Index	**31 24**	**23 16**	**15 8**	**7 0**
0	Device ID		Vendor ID	
4	Status		Command	
8	Class Code			Revision ID
C	BIST	Header Type	Latency Timer	Cache Line Size
10	I/O Space Base Address Register (D31-D8)			
14-38	Reserved			
3C	Max Latency	Min Grant Time	Interrupt Pin	Interrupt Line
40-FF	Reserved			

Figure 4. PCI Configuration Registers

The location of the configuration registers is defined by the host board. The host board assigns a specific address line to the module interface by connecting it to the IDSEL pin on the PMC interface. To determine the configuration register locations, refer to the manual for the host board. Below is a definition of the PCI configuration registers, as implemented by these PMCs.

Register	Mode	Register Definition
Device ID		This read only register identifies the PCI device.
0XC0	R	Slave only (232 or 422)
0XC1	R	Master/Slave (232 or 422)
Vendor ID	R	This read only register identifies the PCI device vendor. The vendor ID is 0000H.
Status	R/W	The status register is a 16-bit register used to record status information for PCI bus related events. These PMCs implement the following bits: D31 R/W Detected Parity Error D26-25 R DEVSEL timing (returns 01) D24 R/W Data Parity Detected
Command	R/W	The command register controls the ability of the PMC to respond to cycles. The PMC implements the following bits: D6 R/W Parity Error Response D2 R/W PCI Master Enable D0 R/W I/O Space Enable
Class Codes	R	This register is not implemented and will always return 000000H.
Revision ID	R	This register returns the revision level of the PMC.
BIST	R	The PMC does not support Built-In-Self-Test.
Header Type	R	Always returns 00H, indicating standard header type.
Latency Timer	R	The latency timer always returns 00H.
Cache Line	R	This register is not implemented and will always return 00H.
I/O Base	R/W	The I/O base address register allows the system configuration software to build its address map. When enabled by bit D0 in the Command register, the upper 24 bits define a 256 byte range of memory. Reading this register indicates the base address of the I/O registers.
Max Latency	R	This register is not implemented and will always return 00H.
Min Gnt	R	This register is not implemented and will always return 00H.
Interrupt Pin	R	Returns 01H, indicating use of INTA# for device interrupts.
Interrupt Line	R	This register is not implemented and will always return 00H

Figure 5. PCI Configuration Registers

PCI Interrupts

The PMC supports interrupts on the INTA# pin only. This is reflected in the Interrupt Pin register of the configuration space. The PMC also implements the 8-bit interrupt line register used to communicate interrupt routing information to system configuration software.

PMC Connectors

The PMC provides the two required connectors (P11 and P12) that implement the 32- bit PCI interface.

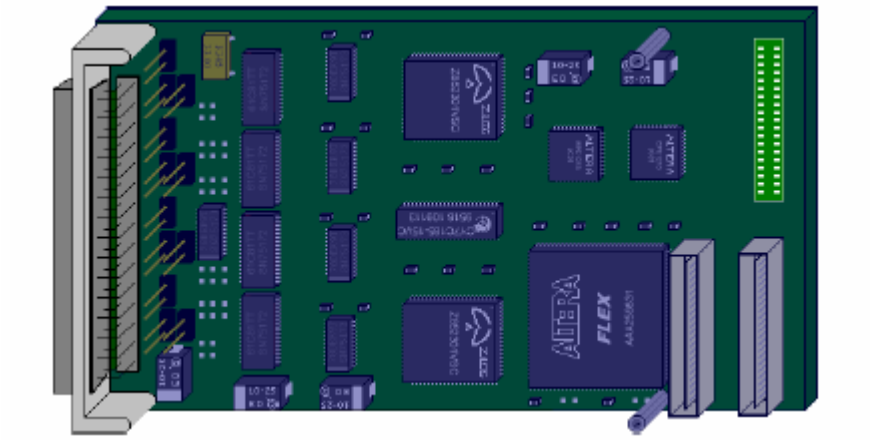


Figure 6. Front Panel I/O Configuration

PMC Pin Assignments

The PCM requires the support of the PCI signal connections (P11 and P12). The following table indicates the PMC connector pin assignments, assuming the back plane connection is to a VMEbus host board. For other host boards, refer to the host board manual to determine signal routing to the back plane.

Pin	P11	P12	P14	Pin	P11	P12	P14
1	-	+12V	C1	2	-12V	-	A1
3	GROUND	-	C2	4	INTA*	-	A2
5	INTB*	-	C3	6	INTC*	GROUND	A3
7	BMODE1*	GROUND	C4	8	+5V	-	A4
9	INTD*	-	C5	10	-	-	A5
11	GROUND	BMODE2*	C6	12	-	-	A6
13	CLK	RST*	C7	14	GROUND	BMODE3*	A7
15	GROUND	-	C8	16	GNT*	BMODE4*	A8
17	REQ*	-	C9	18	+5V	GROUND	A9
19	-	AD30	C10	20	AD31	AD29	A10
21	AD28	GROUND	C11	22	AD27	AD26	A11
23	AD25	AD24	C12	24	GROUND	-	A12
25	GROUND	IDSEL	C13	26	C/BE3*	AD23	A13
27	AD22	-	C14	28	AD21	AD20	A14
29	AD19	AD18	C15	30	+5V	GROUND	A15
31	-	AD16	C16	32	AD17	C/BE2*	A16
33	FRAME*	GROUND	C17	34	GROUND	-	A17
35	GROUND	TRDY*	C18	36	IRDY*	-	A18
37	DEVSEL*	GROUND	C19	38	+5V	STOP*	A19
39	GROUND	PERR*	C20	40	LOCK*	GROUND	A20
41	-	-	C21	42	-	SERR*	A21
43	PAR	C/BE1*	C22	44	GROUND	GROUND	A22
45	-	AD14	C23	46	AD15	AD13	A23
47	AD12	GROUND	C24	48	AD11	AD10	A24
49	AD09	AD08	C25	50	+5V	-	A25
51	GROUND	AD07	C26	52	C/BE0*	-	A26
53	AD06	-	C27	54	AD05	-	A27
55	AD04	-	C28	56	GROUND	GROUND	A28
57	-	-	C29	58	AD03	-	A29
59	AD02	GROUND	C30	60	AD01	-	A30
61	AD00	-	C31	62	+5V	-	A31
63	GROUND	GROUND	C32	64	-	-	A32

Figure 7. PMC Connector Pin Assignments

The Serial Interface

Introduction

The PMC-3210 and PMC-3211 use two Z85230 SCCs to implement four serial ports, configured for either RS-232 or RS-422. Each port has an independent baud rate generator and can operate in asynchronous or synchronous modes.

The PMC-3211 provides eight channels of DMA to efficiently move data between PCI memory and the Z85230 SCC. Each DMA channel supports either the transmit or the receive portion of one of the four serial ports. All references to DMA in this section apply only to the PMC-3211.

This manual section defines the interface to the Z85230, the operation of the DMA controllers and the interrupt support. Refer to *Zilog Datacom IC's Databook* for the programming details of the Z85230 SCC.

Register Interface

The serial registers provide the ability to access the Z85230 registers, access the DMA registers, and to access DMA and interrupt status and control. The serial registers are accessed using the PCI command types (encoded on C_BE[3:0]) for I/O read and I/O write.

The location of the serial registers is defined through the PCI configuration space. The system configuration software is required to initialize the I/O Base Address register. The Base Address register allows the serial registers to be mapped at any 1MB memory boundary in the I/O space. The system configuration software must enable the I/O space by setting bit D0 of the Control register, which is the I/O space enable.

The following table defines the serial register interface. The index indicates the offset into the I/O space defined by the I/O Base Address register. All areas marked “Reserved” are for future expansion and must not be accessed. The highlighted areas are only available on the PMC-3211.

Index	31 24	23 16	15 8	7 0
00-3F	PCI Configuration Registers			
40	DMA Status And Control Registers			
44-5F	Reserved			
60	Reserved			Port B Control
64	Reserved			Port A Control
68	Reserved			Port B Data
6C	Reserved			Port A Data
70	Reserved			Port D Control
74	Reserved			Port C Control
78	Reserved			Port D Data
7C	Reserved			Port C Data
80	Port A Transmit DMA Count			
84	Port A Receive DMA Count			
88	Port B Transmit DMA Count			
8C	Port B Receive DMA Count			
90	Port C Transmit DMA Count			
94	Port C Receive DMA Count			
98	Port D Transmit DMA Count			
9C	Port D Receive DMA Count			
A0	Port A Transmit DMA Address			
A4	Port A Receive DMA Address			
A8	Port B Transmit DMA Address			
AC	Port B Receive DMA Address			
B0	Port C Transmit DMA Address			
B4	Port C Receive DMA Address			
B8	Port D Transmit DMA Address			
BC	Port D Receive DMA Address			
C0	Port A Transmit DMA Holding			
C4	Port A Receive DMA Holding			
C8	Port B Transmit DMA Holding			
CC	Port B Receive DMA Holding			
D0	Port C Transmit DMA Holding			
D4	Port C Receive DMA Holding			
D8	Port D Transmit DMA Holding			
DC	Port D Receive DMA Holding			
E0-FF	Reserved			

Figure 8. Serial Registers

The first 64 bytes (40H) are a mirror of the configuration registers, which should only be modified through the configuration space.

When the DMA controller is in the process of modifying the DMA count or DMA address registers, access to the serial registers is restricted to avoid confusing the DMA controller. Any accesses during these register modifications will result in a slave retry termination. The requesting device must then release the bus, wait, and eventually retry the cycle.

Z85230 Registers

The PMC-3210 and PMC-3211 provide access to two Z85230 Serial Communications Controllers (SCC). Each SCC interface consists of two control and data ports. The Control port is used to address one of 16 internal registers and the Data port is used to pass data to or from control and interface registers. The registers can be accessed at the following offsets into the I/O Base Address, where xxx is the base address.

Register	Port A	Port B	Port C	Port D
Control	xxx0,0064	xxx0,0060	xxx0,0074	xxx0,0070
Data	xxx0,006C	xxx0,0068	xxx0,007C	xxx0,0078

Figure 9. Z85230 Registers

Control Reg	Data	
00		Reset the SCC internal address pointer
09 (WR9)	C0	Force a hardware reset
04 (WR4)	4C	Asynchronous Mode, x16 clock, 2 stop bits
05 (WR5)	EA	Setup Tx: Use RTS, Enable, 8-Bit Data, Auto Enables
01 (WR1)	00	Disable interrupts
0B (WR11)	56	Internal baud rate generator for Rx and Tx
0C (WR12)	32	Lower portion of 9600 baud rate time constant
0D (WR13)	00	Upper portion of 9600 baud rate time constant
0E (WR14)	03	Enable Baud Rate Generators

Figure 10. Z85230 Port Initialization

If initializing Port A with the I/O base address register at 1240,0000, the control register writes would be at 1240,0064 and the data writes would be at 1240,006C. In all cases, the control register value should be written first (to select the internal SCC register), followed by the data writes.

When using the internal baud rate generator, a 16-bit time constant must be loaded into the baud rate registers of the port. The time constant is calculated using the following equations, which assume the SCC is clocked at a 16MHz frequency:

Time Constant = (8,000,000 / baud rate) - 2 (for x1 mode)

Time Constant = (500,000 / baud rate) - 2 (for x16 mode)

As an example, the baud rate constant for 9600 baud would be 50 for a 16x clock, and 831 for a 1x clock.

DMA Registers

The DMA Register interface consists of an address, count, and data holding register for each channel, and a single status and control register for all eight DMA channels. The following table defines the DMA status and control register format. This register can be accessed as 8, 16, or 32 bits.

Bits	Mode	Definition
D31-25	R	These reserved bits always return 0 and must be 0 when written.
D24	R/W	The master interrupt enable bit allows the INTA# pin to be driven when any interrupt source is pending. This bit is 0 at reset, which disables interrupts. 0 Disables pending interrupts from driving INTA# 1 Allows pending interrupts to drive INTA#
D23-16	R/W	There are eight DMA interrupt pending bits; one for each channel. These bits are cleared at reset, indicating no DMA interrupts are pending. Each bit is set when the corresponding active DMA channel has reached its terminal count or encountered an error. The bits are defined as follows: D23 Port D Receive D22 Port D Transmit D21 Port C Receive D20 Port C Transmit D19 Port B Receive D18 Port B Transmit D17 Port A Receive D16 Port A Transmit Writes to the pending interrupt bits are ignored unless the corresponding mask bit (described below) is set on D7-D0 of this register. As an example, to set the Port A transmit DMA pending bit, you would write the value 00010001 to this register. A value of 00000001 would clear it. A write of 00FF0000 would be ignored, because no mask bits are set. A write of 000000FF would clear all pending interrupts.
D15-8	R/W	There are eight DMA enable bits; one for each channel. These bits are cleared at reset, indicating no DMA channels are enabled. The bits are defined as follows: D15 Port D Receive D14 Port D Transmit D13 Port C Receive D12 Port C Transmit D11 Port B Receive D10 Port B Transmit D9 Port A Receive D8 Port A Transmit Writes to the DMA enable bits are ignored unless the corresponding mask bit (described below) is set on D7-D0 of this register. As an example, to enable Port B transmit DMA, you would write the value 00000404 to this register. A value of 00000004 would clear it.
D7-0	W	There are eight DMA mask bits; one for each channel. These write-only bits are used to select an individual DMA channel when accessing the DMA enable or DMA interrupt pending bits. When set, the corresponding enable and pending bits will be modified; when cleared they are ignored. The bits are defined as follows: D7 Port D Receive D6 Port D Transmit D5 Port C Receive D4 Port C Transmit D3 Port B Receive D2 Port B Transmit D1 Port A Receive D0 Port A Transmit
D3-2	R	These two read only bits provide interrupt status. The interrupt handler should reference these and the DMA interrupt pending bits. They are defined as follows: D3 Z85230 Interrupt Pending (ports C and D) D2 Z85230 Interrupt Pending (ports A and B) Each Z85230 SCC shares an interrupt for two ports. To determine the specific source of an interrupt, the device needs to be interrogated further.

Figure 11. DMA Status and Control Register

To use DMA, the user must initialize the DMA address register and DMA count register before starting the DMA. Both registers are 32 bits wide and can only be read and written as 32 bits. The table below shows the format of these two registers.

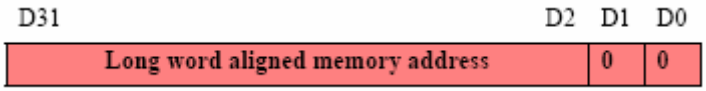


Figure 12. DMA Address Register

The lowest two data bits must always be set to 0. Because the DMA performs data packing and unpacking, it is only capable of transferring multiples of 4 bytes. Setting these bits to any value other than 0 will result in unpredictable behavior during the PCI transfers.

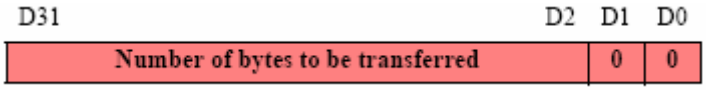


Figure 13. DMA Count Register

Again, the lowest two data bits must always be set to 0. Setting these bits to any value other than 0 will result in unpredictable behavior during the PCI transfers. Because the DMA performs data packing and unpacking, it is only capable of transferring multiples of 4 bytes.

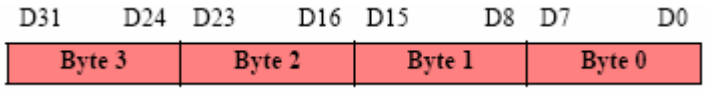


Figure 14. DMA Holding Register

The DMA holding register is the staging area for DMA byte packing and unpacking. Individual bytes are packed into 32-bit words, which are transferred to and from the PCI interface. This register will contain the last 4 bytes of data sent to the PCI bus and is only useful if the PCI transfer results in an error termination. However, the data may not be reliable.

DMA Termination

A DMA cycle will be terminated if the transfer count has reached zero or the PCI cycle resulted in an abnormal termination. In both cases the interrupt pending bit is set in the DMA status and control register, and the DMA channel is stopped. The user program can distinguish between the two causes of termination by reading the transfer count to determine if the count reached zero. If the count is not zero, the PCI transfer resulted in an error condition and the transfer has failed.

DMA Performance

The Z85230 is capable of transmitting data at 4.0 Mbit/s. Each DMA controller is capable of sustaining this rate of transfer. However, the combined aggregate rate of all eight channels at this maximum rate (32.0 Mbit/s) cannot be maintained by the DMA controller. The combined aggregate rate of all DMA channels is dependent on the application and the bus arbitration latency. In general, the total aggregate data rate for all eight channels should be kept below 17.5 Mbit/s. This would allow four channels to safely operate at the maximum data rate. When operating at data rates below 1.0Mbit/sec, there is sufficient bandwidth to operate all eight channels. Exceeding the data rate can cause data losses when receiving data and reduced performance when transmitting data.

Connectors

The front panel serial connector is the 68-position Amplimite .050 Series Right Angle receptacle (part number 750737-7). The mating connector is the Amplimite .050 Series Cable Plug (part number 749925-5). The figure below shows a front-view of the connector.

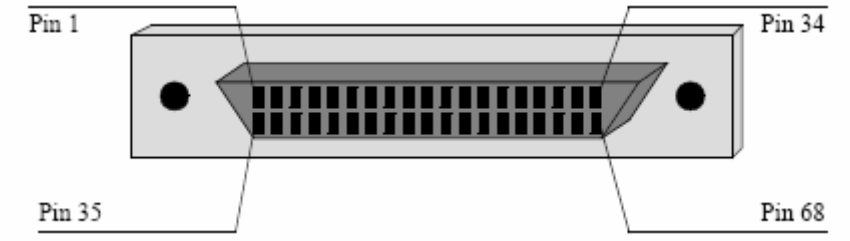


Figure 15. Serial Connector

The back plane connector is defined by the baseboard. The 64-pin PMC connector that routes the I/O signals to the back plane is described in the *PMC Connector* section of this manual.

The serial connector pinout is organized to allow inexpensive mass terminable ribbon connectors to be used, keeping connectivity costs lower (see *Serial Cables*). The following tables describe the serial port pins for the RS-232 and RS-422, organized by port.

Notice that port D is unique when I/O is routed out the back panel. In the back panel I/O case, the connector is 64 pins, instead of 68 pins, and the last four pins on port D are not available. This only affects 422 boards with I/O out the back panel.

RS-232		RS-422		Pin Number		
Dir	Name	Dir	Name	Front Panel	Back Panel	DB25
		In	RXD-	1	C1	14
In	RXD	In	RXD+	2	A1	2
In	RXC	In	RXC+	3	C2	15
Out	TXD	Out	TXD+	4	A2	3
		Out	TXD-	5	C3	16
In	DCD	In	DCD+	6	A3	4
I/O	TXC	I/O	TXC+	7	C4	17
Out	DTR	Out	DTR+	8	A4	5
		In	RXC-	9	C5	18
Out	RTS	Out	RTS+	10	A5	6
		In	DCD-	11	C6	19
	GND		GND	12	A6	7
In	CTS	In	CTS+	13	C7	20
		Out	DTR-	14	A7	8
		In	CTS-	15	C8	21
		I/O	TXC-	16	A8	9
		Out	RTS-	17	C9	22

Figure 16. Serial Port A Pin Assignments

RS-232		RS-422		Pin Number		
Dir	Name	Dir	Name	Front Panel	Back Panel	DB25
		In	RXD-	35	C18	14
In	RXD	In	RXD+	36	A18	2
In	RXC	In	RXC+	37	C19	15
Out	TXD	Out	TXD+	38	A19	3
		Out	TXD-	39	C20	16
In	DCD	In	DCD+	40	A20	4
I/O	TXC	I/O	TXC+	41	C21	17
Out	DTR	Out	DTR+	42	A21	5
		In	RXC-	43	C22	18
Out	RTS	Out	RTS+	44	A22	6
		In	DCD-	45	C23	19
	GND		GND	46	A23	7
In	CTS	In	CTS+	47	C24	20
		Out	DTR-	48	A24	8
		In	CTS-	49	C25	21
		I/O	TXC-	50	A25	9
		Out	RTS-	51	C26	22

Figure 17. Serial Port B Pin Assignments

RS-232		RS-422		Pin Number		
Dir	Name	Dir	Name	Front Panel	Back Panel	DB25
		In	RXD-	18	A9	14
In	RXD	In	RXD+	19	C10	2
In	RXC	In	RXC+	20	A10	15
Out	TXD	Out	TXD+	21	C11	3
		Out	TXD-	22	A11	16
In	DCD	In	DCD+	23	C12	4
I/O	TXC	I/O	TXC+	24	A12	17
Out	DTR	Out	DTR+	25	C13	5
		In	RXC-	26	A13	18
Out	RTS	Out	RTS+	27	C14	6
		In	DCD-	28	A14	19
	GND		GND	29	C15	7
In	CTS	In	CTS+	30	A15	20
		Out	DTR-	31	C16	8
		In	CTS-	32	A16	21
		I/O	TXC-	33	C17	9
		Out	RTS-	34	A17	22

Figure 18. Serial Port C Pin Assignments

RS-232		RS-422		Pin Number		
Dir	Name	Dir	Name	Front Panel	Back Panel	DB25
		In	RXD-	52	A9	14
In	RXD	In	RXD+	53	C10	2
In	RXC	In	RXC+	54	A10	15
Out	TXD	Out	TXD+	55	C11	3
		Out	TXD-	56	A11	16
In	DCD	In	DCD+	57	C12	4
I/O	TXC	I/O	TXC+	58	A12	17
Out	DTR	Out	DTR+	59	C13	5
		In	RXC-	60	A13	18
Out	RTS	Out	RTS+	61	C14	6
		In	DCD-	62	A14	19
	GND		GND	63	C15	7
In	CTS	In	CTS+	64	A15	20
		Out	DTR-	65	NC	8
		In	CTS-	66	NC	21
		I/O	TXC-	67	NC	9
		Out	RTS-	68	NC	22

Figure 19. Serial Port D Pin Assignments

The 68-pin connector is split into four 17-pin sections (one for each serial port), which have identical pinouts. Each port can be built to support either the RS-232 or RS-422 standard. The 64-pin connector is identical to the 68, but does not implement pins 65 through 68.

The module is designed to be a DTE device. Additional jumper selectable pull-ups have been added to allow the DCD and CTS handshaking signals to be biased true or false. This allows character transmission when connected to devices not supporting these handshaking signals.

Because of the limited number of available pins, the RS-422 interface is not entirely compliant. The non-compliant pins are DTR, CTS, and RxC. If full handshaking is required, a unique cable can be purchased to route the signals to the correct pins. Additional terminators have been added to all the inputs to be used if termination is required.

Serial Cables

The mass termination cable can easily be built using commonly used connectors and 68-pin ribbon cable. The figure below shows the layout of this cable.

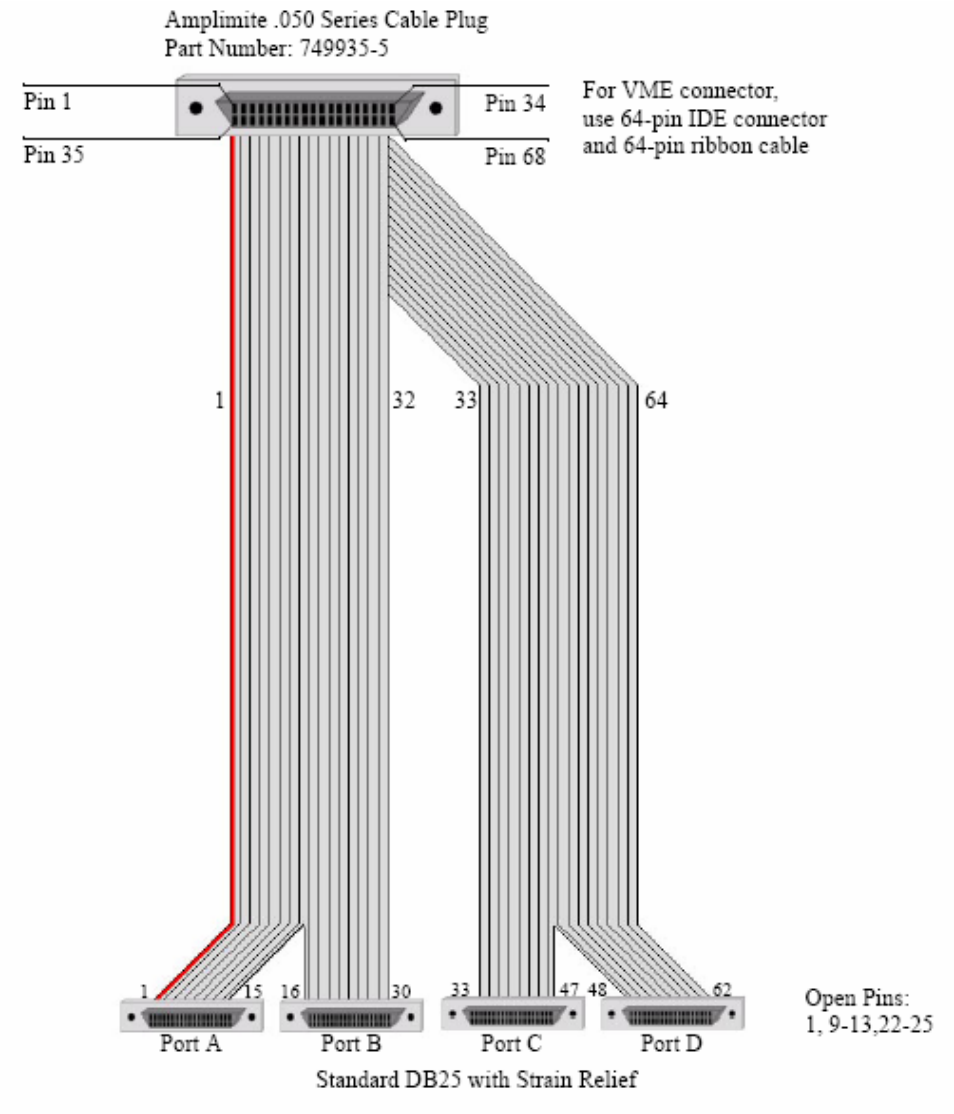


Figure 20. Mass Termination Cable

Specifications

Form Factor		Single-wide PMC
PCI Interface		33MHz, 32-bit, bus slave operation only PCI version 2.1
Number of Serial Channels		Four
Serial UART Controller		Zilog Z85230
Maximum Data Rate		125 kbps
Serial Port Interface:		
	PMC-3210	4 EIA-232
	PMC-3211	2 EIA-232 and 2 EIA-422
Protocol Support		Synchronous or asynchronous UART
Signals Supported		TxD, RxD, TxC, RxC, CTS, RTS, DCD, DTR
Front Panel I/O Access		68-pin high density female connector
Weight		0.09 kg (0.2 lbs.)
Dimensions		74.0 mm x 149.0 mm
Power Requirements: PMC-3210		+5 VDC: 215mA typical +12 VDC: 15mA typical, RS-232 -12 VDC: 15mA typical, RS-232
Power Requirements: PMC-3211		+5 VDC: 215mA typical +12 VDC: 15mA typical, RS-232 -12 VDC: 15mA typical, RS-232
Environmental		Operating temperature: 0° to +55° C, ambient, at board Humidity: 0% to +85% non-condensing Storage: -40° to +70° C

Repair

Service Policy

Before returning a product for repair, verify as soon as possible that the suspected unit is at fault; then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if it is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include the return address and telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service of SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

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