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TS-PMC FPGA Processor Technical Data Sheet

Release Version A

abaco SYSTEMS

How to Contact Abaco Systems

If you have any questions about this product, you can contact Abaco Systems through one of the following methods.

E-Mail:

support@abaco.com

Web:

http://www.abaco.com

Revision History

TS-PMC FPGA PROCESSOR TECHNICAL DATA SHEET REVISION HISTORY	
Revision	**Description**
2.0	Initial revision.
3.0.0	Product renamed to remove reference to Tsunami.
3.1	Product details re: transfer to Ottawa, ON facility; discontinuation of TS-PMC A40 option.
A	Rebranded to Abaco Systems

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Overview

The TS-PMC FPGA processor platform provides today's highest-throughput digital signal processing performance available on standard PMC systems.

The TS-Series architecture integrated with the Wave FPGA Tool Kit software and Altera®'s Quartus® and SOPC Builder development tools provide a platform for easy application development and fast time-to-market.

The TS-PMC platform offers one of Altera's industry-leading Stratix® FPGAs on a 64 bit/66 MHz PCI bus, with enough memory and high bandwidth I/O data paths to make full use of the outstanding processing power of the Stratix family. The TS-PMC offers a Micro-mezzanine connector that provides front or rear panel interface for I/O flexibility. User defined data can be routed through the P4 connection up to 1 Gigabytes/ sec

This document will provide the detailed technical specifications of the TS-PMC platform including data flow, I/O and memory resources available, and system processing details.



Figure 1. TS-PMC Board

Models Available

The TS-PMC board is available in six models. The following table highlights the differences between these models.

Table 1. TS-PMC Resources

TS-PMC Model	Altera Stratix FPGA Device	SRAM Memory	SDRAM Memory (standard configuration)
TS-PMC-3001C	EP1S30, speed grade 7	2 MB per bank, 4 MB total	128 MB per bank, 256 MB total
TS-PMC-3002N	EP1S30, Industrial speed grade 6	2 MB per bank, 4 MB total	128 MB per bank, 256 MB total (SDRAM Clock Rate limited to 80 MHz)
TS-PMC-3003i	EP1S30, Industrial, speed grade 6	2 MB per bank, 4 MB total	128 MB per bank, 256 MB total

Functional Block Diagram

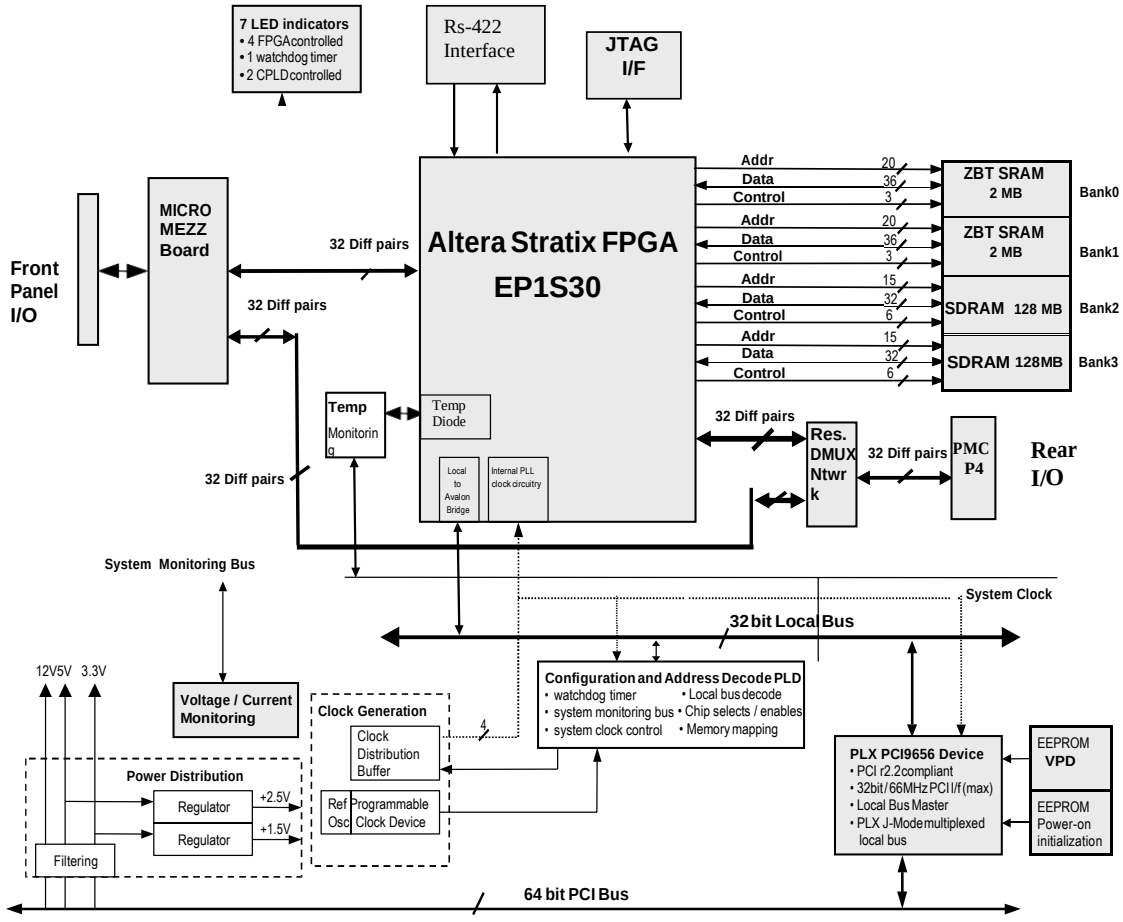


Figure 2. TS-PMC Board Block Diagram

FPGA Processor

The TS-PMC board contains one Stratix FPGA device from Altera Corporation. The DSP blocks, Softcore Nios processor, system-on-a-programmable-chip development tools, and Wave API software give developers maximum access to the Stratix and TS-PMC resources with minimum effort.

Stratix Device (Model Specific) Features	**EP1S30**
• Total Logic Elements	32,470
• TriMatrix memory	
• M512 RAM Blocks (32 X 18 bits) Simple Dual-Port	295
• M4K RAM Blocks (128 X36 bits) True Dual-Port	171
• M-RAM Blocks (4K X 144 bits) True Dual-Port	4
• PLLs (Fast / Enhanced)	8/2
• DSP Blocks (up to 36 bit X 36 bit Multiply and Add)	12
• Embedded multipliers (9 bit X 9 bit)	96

Other Stratix (Common) Device Features:

- Support for Nios Soft-core embedded processor
- Support for peripheral I/O and DSP building blocks
- Support for SignalTap II embedded logic analyzer

Complete information on the Altera Stratix devices can be found at:
http://www.altera.com

High Bandwidth High Capacity Memory

The TS-PMC platform comes equipped with high bandwidth SRAM and SDRAM memory devices. The TS-PMC provides two banks of ZBT SRAM memory and two banks of SDRAM memory.

TS-PMC Memory Capacity

For all members of the TS-PMC-3001 family the following memory banks (SRAM and SDRAM) are available:

- 2 MB SRAM per bank for a total of 4 MB ZBT SRAM
- 128 MB SDRAM per bank for a total of 256MB SDRAM
  (SDRAM Clock Rate limited to 80 MHz on conduction-cooled versions)

TS-PMC Memory Bandwidth

The peak throughput rates for each of the memory banks are listed below.

- 600 Mbytes/s data throughput per bank to SRAM
- 532 Mbytes/s data throughput per bank to SDRAM
  (non- conduction-cooled versions only)
- 320 Mbytes/s data throughput per bank to SDRAM
  (SDRAM Clock Rate limited to 80 MHz on conduction-cooled versions)

Combined, the non-conduction cooled variants of the TS-PMC has over 2 Gbytes/sec of aggregate memory throughput.

Similarly, for the conduction-cooled members of the TS-PMC family the aggregate memory throughput is over 1.8 Gbytes/sec.

PCI Bus Interface

The interface to the PCI bus is provided by a PLX PCI956 I/O accelerator. It functions as a master of the TS-PMC local bus to move data between the PCI bus and the TS-PMC resources. Two DMA channels are provided with channel arbitration. The Wave software API provides DMA functionality to host PC applications.

PCI Bus Interface Features:

- 64 bit / 66 MHz PCI bus interface
- 32 bit / 50 MHz TS-PMC local bus
- DMA data rates exceeding 140 Mbytes/s sustained, 533 Mbytes/s peak
- DMA block, scatter-gather and demand modes supported

High Bandwidth Data I/O Interface

Front Panel I/O Micro-Mezzanine Interface to FPGA

Electrical connection to the front panel I/O is provided through a Micro-Mezzanine (Micro-Mezz interface on the PMC board. Up to 32 LVDS pairs (or 64 single-ended) signals plus transmit and receive clocks can be used between the PMC and the Micro-Mezz. Depending on the Micro-Mezz board design, any mix of the 32 LVDS pairs may be used for transmit or receive.

FPGA to Rear I/O (via PMC P4 Connector)

Up to sixty-four signal lines can connect the PMC P4 connector to the FPGA. The sixty-four lines are routed on the PCB as 32 differential pairs but each pair can be run as two single-ended signals as well. These connections are dependent on the actual board assembly where a mix of P4 to FPGA and P4 to Micro-Mezz board connections are established. The standard default TS-PMC board assemblies are populated with half of the P4 connections (16 pairs) going to the FPGA and the remaining half (16 pairs) going to the Micro-Mezz connector. Contact the factory for alternate connections.

Auxiliary Digital I/O

The board provides a total of 4 RS-422 I/O ports via a 2x10 DIP connector socket. The differential impedance of each input and output RS-422 pair is 100Ω. A fused power pin is also provided for user applications.

Each of these ports will operate at up to a 25 MHz rate. These ports are not routed to any backplane or front panel connector.

Features:

- 2 RS-422 output pairs
- 2 RS-422 input pairs

JTAG Support

All devices that support the IEEE Std. 1149.1 (JTAG) boundary scan protocol are included in the JTAG chain on the TS-PMC board. This includes on-board SRAM devices, FPGA and PLDs, as well as the PLX PCI9656 I/O accelerator. There is one JTAG chain available on the TS-PMC board.

System Monitoring

TS-PMC provides system monitoring for temperature, voltage and current usage and generates an alert interrupt if any of the system criteria is violated. Additionally, there is a watchdog timer incorporated into the board design. After an FPGA is loaded with a program, the watchdog timer begins counting; if the countdown expires, the board is reset, an interrupt is generated, and the FPGAs are all unconfigured. Reset of the watchdog timer can be automatically managed by the Wave driver or it may be managed by application software. A Wave API function provides access to reset the watchdog timer.

Indicator LEDs

A bank of 7 LEDs is provided on the PMC module. One LED is dedicated to the status of the watchdog timer. The functionality of two of the LEDs is controlled by the PLD and can be controlled through the Wave device driver. The remaining four LEDs are general-purpose indicators that can be used by the user-specific FPGA application program.

System Clock Details

The TS-PMC system is designed to typically operate at a system reference frequency of 50MHz. Other reference frequencies can be used by adjusting the programmable clock source setting in the PLD through a Wave API call. Many data transfer, memory access and FPGA internal operations can operate at higher frequencies than the system reference.

The local reference clock is available to two of the four enhanced PLLs. The eight fast PLLs available on each Stratix FPGA are also available for TS-PMC FPGA development. All clock multiplication and division is handled within the Stratix devices.

Two enhanced PLLs are used for clock management between the Stratix device and the memory banks. Each external clock output can be delayed or advanced independently to enable high-speed synchronous memory access.

System Interrupts

Interrupt signals can be generated on the TS-PMC board by the application FPGA code. These interrupts can generate events on the host PC via the Wave device driver software, which can then be handled by the user host application software. Some interrupts are generated by the factory programmed PLD and indicate such occurrences as system monitoring alerts and watchdog timer events.

TS-PMC Performance

The table below lists the various primary data paths on a TS-PMC board and indicates the maximum performance that can be expected for each of them.

Table 2. TS-PMC Performance

Description	Clock Rate (MHz) Max	Data Width (Bits)	Throughput Mbytes/Sec Peak/Sustained
PCI:			
DMA access to FPGA Memory	50	64 PCI/ 32 Local	533 /170
FPGA to Memory:			
FPGA to/from SDRAM	133 (CL3) [1,2]	32	533 [2,3]
FPGA to/from ZBT SRAM	133	36	598
PMC(P4):			
P4 to/from FPGA	266	15+1clk (LVDS pairs)[4]	498/ total [5]
P4 to/from Micro-Mezz	166	15+1clk (LVDS pairs)[4]	311/ total [6]
Micro-MEZZ port:			
Micro-MEZZ to/From FPGA	166[7]	Any MIX of up to 30 LVDS pairs plus 1 xmit clk pair and 1 recv clk pair	Up to 622 Aggregate [7]

[1]CAS Latency 3 mode operation
[2]TS-PMC Commercial or Extended Temp versions; Conduction-cooled versions limited to 320 Mbytes/sec
[3]Largely dependent on memory controller and burst sizes
[4]LVDS pairs may be run as two single-ended lines as well (subject to the FPGA compiler pad placement constraints between single-ended and LVDS signals – see Stratix Data sheet).
[5]With 16 LVDS pairs from P4 to FPGA. (Standard board assembly)
[6]With 16 LVDS pairs from P4 to Micro Mezz (Standard board assembly).
[7]In LVDS mode and using dedicated LVDS clock lines

Detailed Hardware Specifications

Environmental Specifications

The TS-PMC is designed to operate in the following environmental specifications.

Commercial Assemblies

Operating temperature	Min. 0°C	Max. 60°C (at 100 LFM)
Storage temperature	Min. -45°C	Max. 85°C
Humidity (R.H. non-condensing)	Min. 10%	Max. 90%

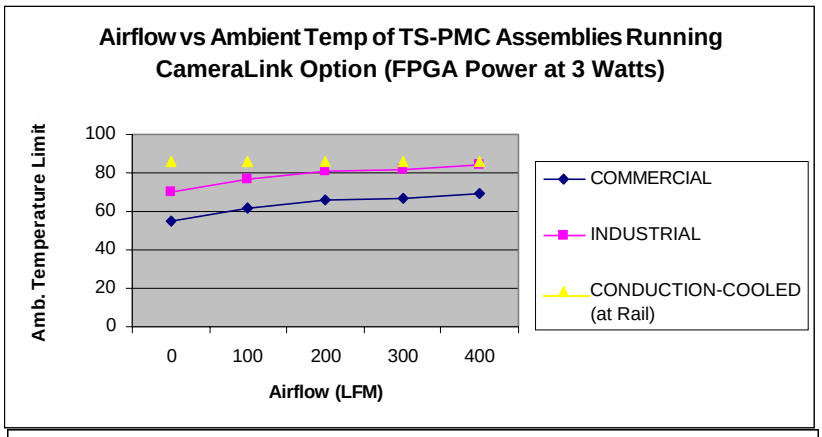
Extended Temperature Assemblies

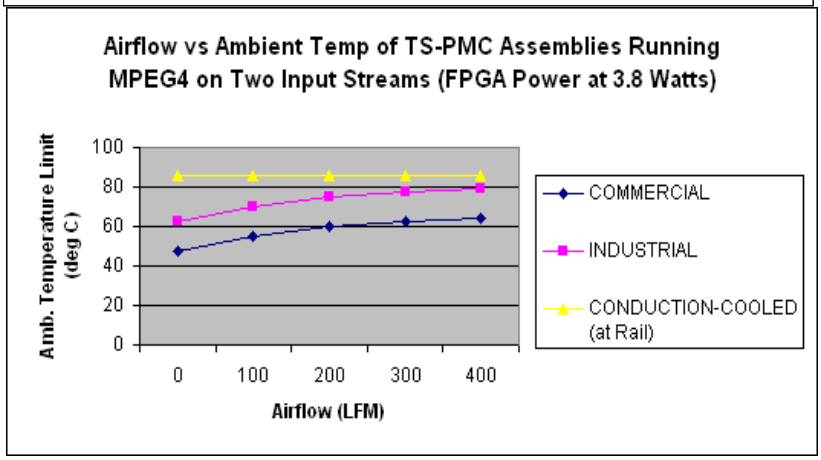
Operating temperature	Min. 0°C	Max. 75°C (at 100 LFM)
Storage temperature	Min. -45°C	Max. 85°C
Humidity (R.H. non-condensing)	Min. 10%	Max. 90%

Conduction-Cooled Assemblies

Operating temperature (at PMC board edge)	Min. 0°C	Max. 85°C
Storage temperature	Min. -45°C	Max. 100°C

Thermal Aspects for SomeTypical Applications:





Power Requirements

The actual power consumption is dependent on the FPGA gate utilization, clock rate and toggle rate in the specific application. The information below is based on a 'reasonable maximum' high power scenario and is calculated using Altera Statix Device Power Calculator Spreedsheet. Exceeding this power number will reduce the operating temperature range, or extra cooling measures must be taken.

Table 3. PMC with FPGA at 0.64 Watts Power Requirements (FPGA Unconfigured)

Rail	Current	Power Watts
+3.3 VDC	0.38	1.25
+5.0 VDC	0.15	.75
+12 VDC	0.005	0.06
-12 VDC	0	0.00
	Power Total = 2.06 W	

Table 4. PMC with FPGA at 3 Watts Power Requirements and Allocation

Rail	Current	Power Watts
+3.3 VDC	1.54	5.1
+5.0 VDC	0.5	2.5
+12 VDC	0.005	0.06
-12 VDC	0	0.00
	Power Total = 7.6 W (MAX)	

Table 5. PMC with FPGA at 5 Watts Power Requirements and Allocation

Rail	Current	Power Watts
+3.3 VDC	1.86	6.14
+5.0 VDC	.9	4.5
+12 VDC	0.005	0.06
-12 VDC	0	0.00
	Power Total = 10.64 W (MAX)	

Table 6. PMC with FPGA at 5 Watts Power & Video Micro Mezzanine Assembly Used

Rail	Current	Power Watts
+3.3 VDC	2.5	8.25
+5.0 VDC	.9	4.5
+12 VDC	0.005	0.06
-12 VDC	0	0.00
	Power Total = 12.81 W (MAX)	

Board Dimensions

The physical dimensions of the TS-PMC Module are compliant with VITA 32 Specification, as based on the IEEE 1386.1 PMC Module Specification.

Standards

Design

PICMG 2.0 R3.0	CompactPCI Specification
VITA 20-2001	Conduction Cooled PMC
VITA 30.1-2002	2mm Connector Equipment Practice on Conduction Cooled Euroboards
IEEE Std 1386-2001 Family	IEEE Standard for a Common Mezzanine Card (CMC)
IEEE Std 1386.1-2001	IEEE Standard Physical and Enviromental Layers for PCI Mezzanine Cards (PMC)
PICMG 2.3 R1.0	PMC on CompactPCI Specification

PCB Fab

The TS-PMC PCB conforms to IPC-A-600E Class 3

PCA Assembly

The TS-PMC Assembly conforms to IPC-A-610B Class 3

Optional Micro-Mezzanine ("Micro-Mezz") I/O Boards

Several mezzanine I/O boards are available for the TS-PMC board. The following sections detail the available mezzanine boards.

Front Panel LVDS I/O Micro-Mezz Module

An LVDS connection from the TS-PMC can be provided by the Front Panel LVDS I/O Micro-Mezzanine interface card. It is an I/O module designed to run on a TS-PMC board in accordance with the guidelines stated by the IEEE 1386-2001and VITA 32-2002 specifications. It provides 32 pairs of LVDS I/O on a SCSI-3 compatible 68-pin connector. Of the 32 LVDS pairs there are 30 pairs are "general use" and two "limited use" pairs as shown in Figure 4.

On-board EMI and ESD protection is provided for all I/O signals.

The Front Panel LVDS I/O Micro-Mezzanine Board will provide the following:

- 180-pin interface to a TS-PMC Card
- 68-pin I/O interface (SCSI-3 connector)
- Common-mode chokes on all I/O pairs for EMI suppression
- Schottky diode ESD protection on all I/O signals



Figure 3. Front Panel LVDS I/O Micro-Mezz

The simple block diagram in Figure 4 illustrates the board design.

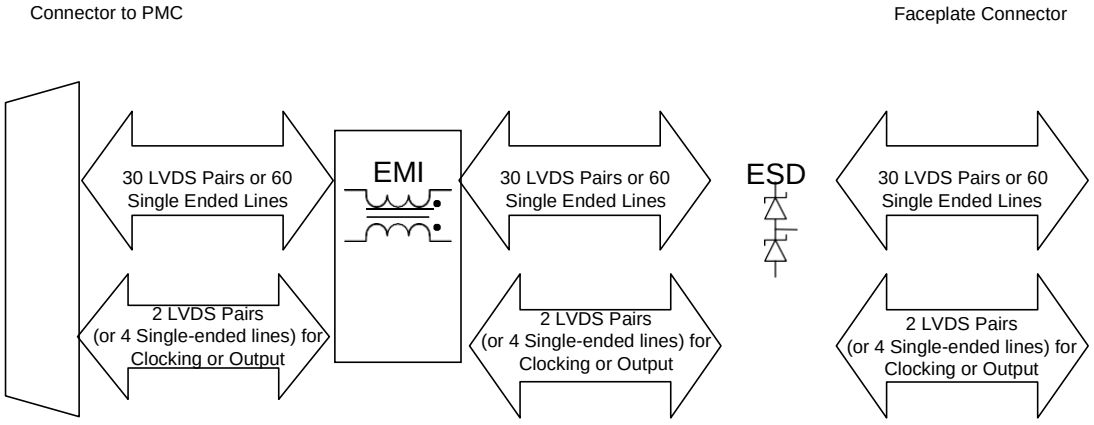


Figure 4. Front Panel LVDS I/O Board Block Diagram.

Performance

The table below lists the primary data paths for the TS-PMC Micro-Mezz and indicates the maximum performance that can be expected for each of the listed Micro-Mezz interface cards.

Table 7. Front Panel LVDS I/O Micro-Mezz Performance

Description	Clock Rate (MHz) Max	Data Width (Bits)	Throughput Mbytes/Sec Peak/Sustained
Micro-MEZZ to/From FPGA	166 [7]	15+1clk In / 15+1clk Out (LVDS Pairs) [4] (limited by SCSI-3 connector I/O)	332 IN and 332 OUT [7]

Front Panel RS-170 I/O Micro-Mezz Module



Figure 5. Front Panel (RS-170) I/O Micro-Mezz Module

The Front Panel Video Micro-mezzanine I/O adapter provides two video input channels and one video output channel. Each video channel can can select between two composite video inputs. Alternatively, each video channel can be configured to use its two video input connections to process a single S-Video stream (with Y and C inputs).

The output video channel can process composite or S-Video output formats and it does not need to match the input video type. When using S-Video sources or displays, you must connect the Y and C connectors to the video source or display accordingly.

An auxiliary eight bit ADC channel, via access from the PMC Rear P4 connector, is also provided on this Micro-Mezz module.

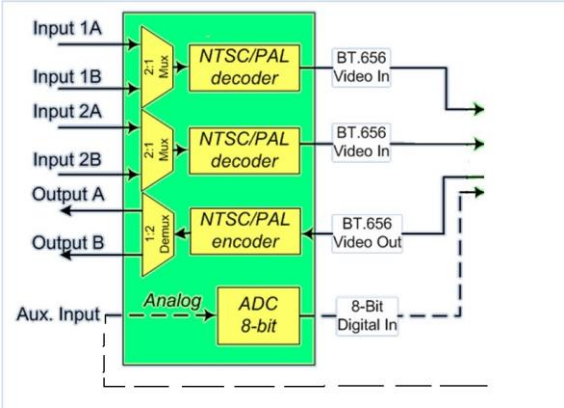


Figure 6. Front Panel (RS-170) Video Micro-Mezz Block Diagram

Both PAL and NTSC composite video format signals can be used with this Micro-Mezz adapter for video processing. The video format of the output channel does not need to match that of the selected input channel.

Performance

The following are the maximum operating frequencies and related throughputs for primary data paths on the board.

Table 8. TS-PMC Front Panrl (RS-170) Video MicroMezz Performance

Description	Clock Rate Max	Data Width (Bits)	Throughput Peak/Sustained
Digital Video Interfaces:			
Video Decoders	27 MHz	8	27 Mbytes/sec
Video Encoders	27 MHz	8	27 Mbytes/sec

Rear I/O (RS-170) Video Micro-Mezz Module

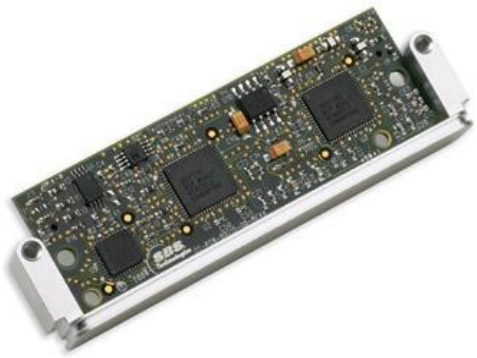


Figure 7. Rear I/O (RS-170) Video Micro-Mezz Module

The Rear I/O Video Micro-mezzanine I/O adapter provides two video input channels and one video output channel. Each video channel can process one video stream. Each video stream can be in any of the composite NTSC, PAL or SECAM formats

An auxiliary eight bit ADC channel, via access from the PMC Rear P4 connector, is also provided on this Micro-Mezz module.

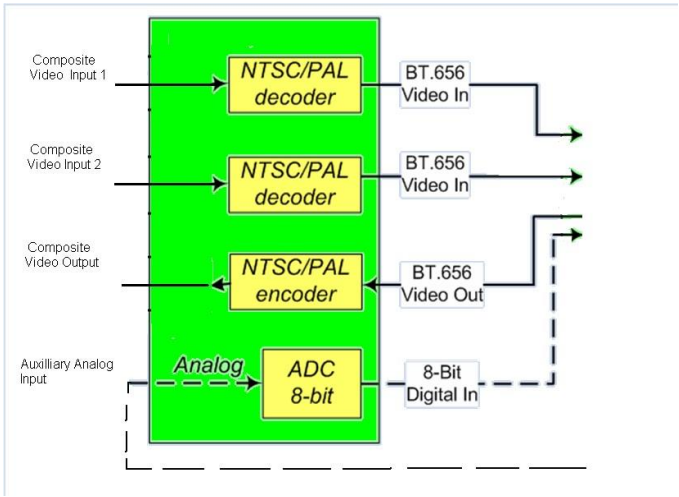


Figure 8. Rear RS-170 Video Capture Micromezz Block Diagram

Analog Video Connection To/From PMC

Pins 1-76 on the micromezz connector are routed directly between the micromezz card and the PMC P4 I/O connector. Within this signal group, pins 1-60 are referenced to a separate ground, allowing these pins to be used for analog signaling. All video inputs and optional output use these signals. Video I/O connects via a rear transition module, through the PMC carrier and the PMC to connect directly to the micromezz card.

Digital Video Connection to/from PMC FPGA

Each video encoder and decoder interfaces with the host PMC's FPGA via an ITU-R BT.656 digital interface, consisting of an 8-bit data path and a dedicated pixel clock. Four synchronization signals are also supported: Horizontal sync (HSYNC), Vertical Sync (VSYNC), Field ID (FID), and Subcarrier Frequency Lock (SFL).

Auxilliary Analog Input Channel

The micromezz supports one eight bit ADC channel for general use.This signal will be digitized by an on-board Analog to Digital converter, and passed on to the host PMC FPGA as a serial bit stream.

Performance

The following are the maximum operating frequencies and related throughputs for primary data paths on the board.

Table 9. TS- PMC Rear I/O (Rs-170) Video Micro-Mezz Performance

Description	Clock Rate Max	Data Width (Bits)	Throughput Peak/Sustained
Digital Video Interfaces:			
Video Decoders	27 MHz	8	27 Mbytes/sec
Video Encoders	27 MHz	8	27 Mbytes/sec

Custom Micro-Mezz Boards

Abaco Systems can develop additional mezzanine board configurations with software drivers and FPGA intellectual property for specific applications on a quick-turn around basis.

TS-PMC FPGA Development Kit Overview

The TS-PMC FPGA Development Kit provides all software and documentation required to quickly begin programming FPGA applications on the TS-PMC platform.

Development Kit Features

- Altera Nios Embedded Processor development kit software including the Altera Quartus II FPGA design software and Nios soft-core embedded processor
- Wave FPGA Developer's Manual and productivity utilities to accelerate Stratix FPGA development on the Tsunami platform
- Wave software API and device driver for Windows XP/2000 and Linux.
- Wave Library Reference
- Wave Programmer's Guide
- Wave driver source code to allow enhancements for user applications
- Wave FPGA Tutorials Manual to guide users through the development of their first FPGAs
- Altera ByteBlaster to integrate with the available FPGA test and debug tools (Signal Tap) from Altera
- Breakout cable and Nios cable are included for use with the Nios II soft-core processor. The Breakout cable also can be used as an Interface for the Digital I/O (RS422) connections.

Wave FPGA Developer's Guide

This guide provides all information required to write application specific FPGAs and target the TS-Series platform. Local bus functionality, memory interface connections, external and internal I/O, and clock connections are detailed. Additionally, productivity tools are provided to accelerate Stratix FPGA development on the TS-Series platform.

Wave FPGA Tool Kit

The Wave FPGA Tool Kit provides a device driver for TS-PMC support on the PCI bus. The functionality of the Wave software tools can be accessed by a host PC command-line utility, or the Wave API routines.

The Wave software supports the following functionality:

- Set TS-PMC board clock frequency
- Load the FPGA device with program binaries
- Support register read/write functions in single and block access modes.
- Provide fast DMA transfers

- Generate host PC events or semaphores based on a device driver or FPGA event. (e.g. TS-PMC interrupts)
- Monitors temperature, voltage, and current alerts from the TS-PMC system monitoring bus. (can be taken over by the host application software if desired)
- Handles the resetting of the watchdog timer. (can be taken over by the host application software if desired)

Support for Altera SOPC Builder

The Wave FPGA Tool Kit provides support for Altera's SOPC builder. A TS-PMC local bus to Avalon Bus Bridge is provided to enable development of FPGA designs that use Avalon compatible building blocks on the TS-Series platform. Also, external peripherals can be incorporated into the SOPC design using the digital I/O or sensor interface on the TS-Series platform.

The following SOPC components are provided with the Wave FPGA Tool Kit:

- PLX9656 Local to Avalon Bridge - a bridge between the TS-PMC local bus and in-FPGA Avalon bus to allow access to SOPC components from the host.
- Demand Mode DMA FIFO - supports demand mode DMA transfers to the host at up to the maximum throughput of the TS-PMC local bus
- Interrupt Controller - allows up to 32 simultaneous edge-triggered interrupts
- Encoder and Trigger I/O - supports up to 4 encoder inputs and up to 8 trigger inputs as well as support for up to 2 encoder outputs and 4 trigger outputs

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