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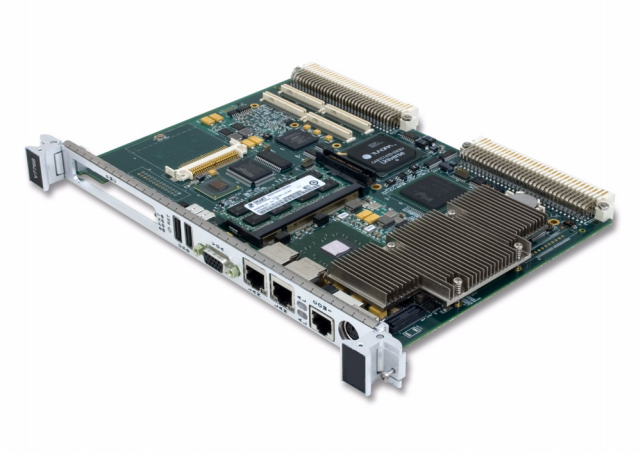
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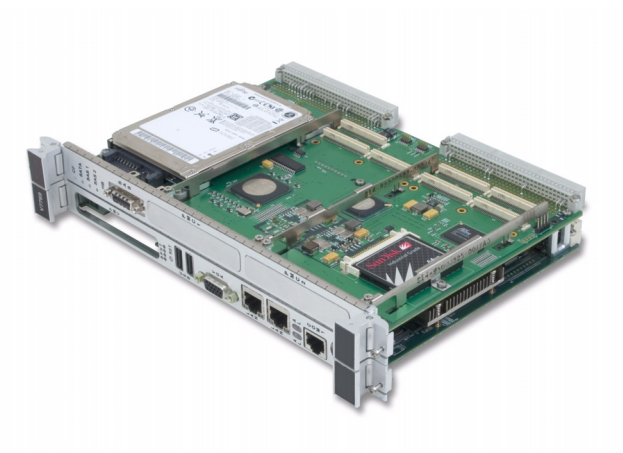
Hardware Reference

V7768/V7769*

Intel® Core™ Duo Processor VME Single Board Computer

THE V7768/V7769 IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2002/95/EC) CURRENT REVISION.





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Waste Electrical and Electronic Equipment (WEEE) Returns



GE is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

GE will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case by case basis. A WEEE management fee may apply.

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Overview

GE's V7768/V7769* are single board computers (SBCs) in a dual-slot, passively cooled, VME Eurocard form factor.

The V7768* is a full featured Intel® Core™ 2 Duo or Celeron® M-based SBC, and the V7769* is a full featured Intel Core 2 Duo-based SBC. The V7768/V7769 utilize the advanced technology of Intel's 945GM chipset and the ICH7-M I/O Controller Hub. The 945GM chipset runs on a 533 MHz front-side bus with the Celeron M processor and a 667 MHz front-side bus with the Core 2 Duo processor.

The V7768/V7769 are compliant with the VMEbus Specification VITA 1-1994 and feature a transparent PCI-to-VME bridge, allowing your board to function as a system controller or peripheral CPU in multi-CPU systems.

The V7768 is a single-slot board, and the V7769 is a dual-slot board. The V7769 has the same functionality as the V7768 and also connects to the ACC-0623* (which will be referred to as the mezzanine board throughout this manual), making it a dual-slot board. Because the functionality is so similar, this manual will refer to both boards (V7768/V7769) throughout unless the material is referring to the V7768 or V7769 only.

Desktop Features of the V7768/V7769

- Up to 2.0 GByte DDR2 SDRAM (One SODIMM)
- SVGA port (front I/O)
- Dual Gigabit Ethernet (GbE) (front I/O)
- One RS232/422 COM port (front I/O)
- One RS232/422 COM support (rear I/O)
- Two USB 2.0 ports (front I/O)
- Four USB 2.0 support (rear I/O)
- Supports two SATA connections (rear I/O)
- One 2.5-in. SATA hard drive (optional for V7769 only)
- Dual SAS connector (front I/O on V7769 only)
- Real-Time clock/calendar
- Front panel reset switch
- PS/2 Keyboard/Mouse connection (front I/O)
- Onboard parallel connector

The 945GM chipset allows the V7768/V7769 to be capable of executing many of today's desktop operating systems such as Microsoft®'s Windows® XP, Windows Vista®, Linux® 2.6.x, and VxWorks® 6.x. The standard desktop features of the V7768/V7769 are described in *Chapter 2: Standard Features* of this manual.

- Remote booting out the front panel only
- Up to 8 GByte of bootable CompactFlash (optional)
- PCI-X capable PMC site with VITA 35 P2 I/O (factory populated on V7768 and main board of V7769)
- VITA 1-1994 with byte swap
- 32 KByte NVRAM
- Software-selectable Watchdog Timer with reset
- PMC expansion site *Chapter 3: Embedded PC/RTOS Features*

The embedded features of the V7768/V7769 are described in Chapter 3 of this manual.

The V7768/V7769 are suitable for use in a variety of applications, such as: telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance processing power for VME in a single or dual slot is desired.

Intel 945GM Chipset

The V7768/V7769 incorporate the latest Intel chipset technology, the 945GM. The Intel 945GM chipset is an optimized integrated graphics solution with up to a 667 MHz system bus. The chipset has a low power design, advanced power management, supporting up to 2 GByte of DDR2 system memory. The 945GM is a Memory Controller Hub (MCH) component, providing the processor interface, system memory interface (DDR2 SDRAM) and SVGA port.

Key features for the 945GM:

- 533 MHz Processor system bus controller for the Celeron M
- 667 MHz Processor system bus controller for the Intel Core 2 Duo
- Up to 2 GByte DDR2 Memory via SODIMM
- High-speed DMI architecture interface for communication with the ICH7-M (I/O controller)

The 945GM supports the Intel ICH7-M I/O controller hub. The ICH7-M supports most of the high speed I/O interfaces of the V7768/V7769.

Key features for the ICH7-M:

- USB 2.0
- SATA
- IDE (Primary only)
- PCI
- PCI Express (PCIe)

Figure 1 V7768 Block Diagram

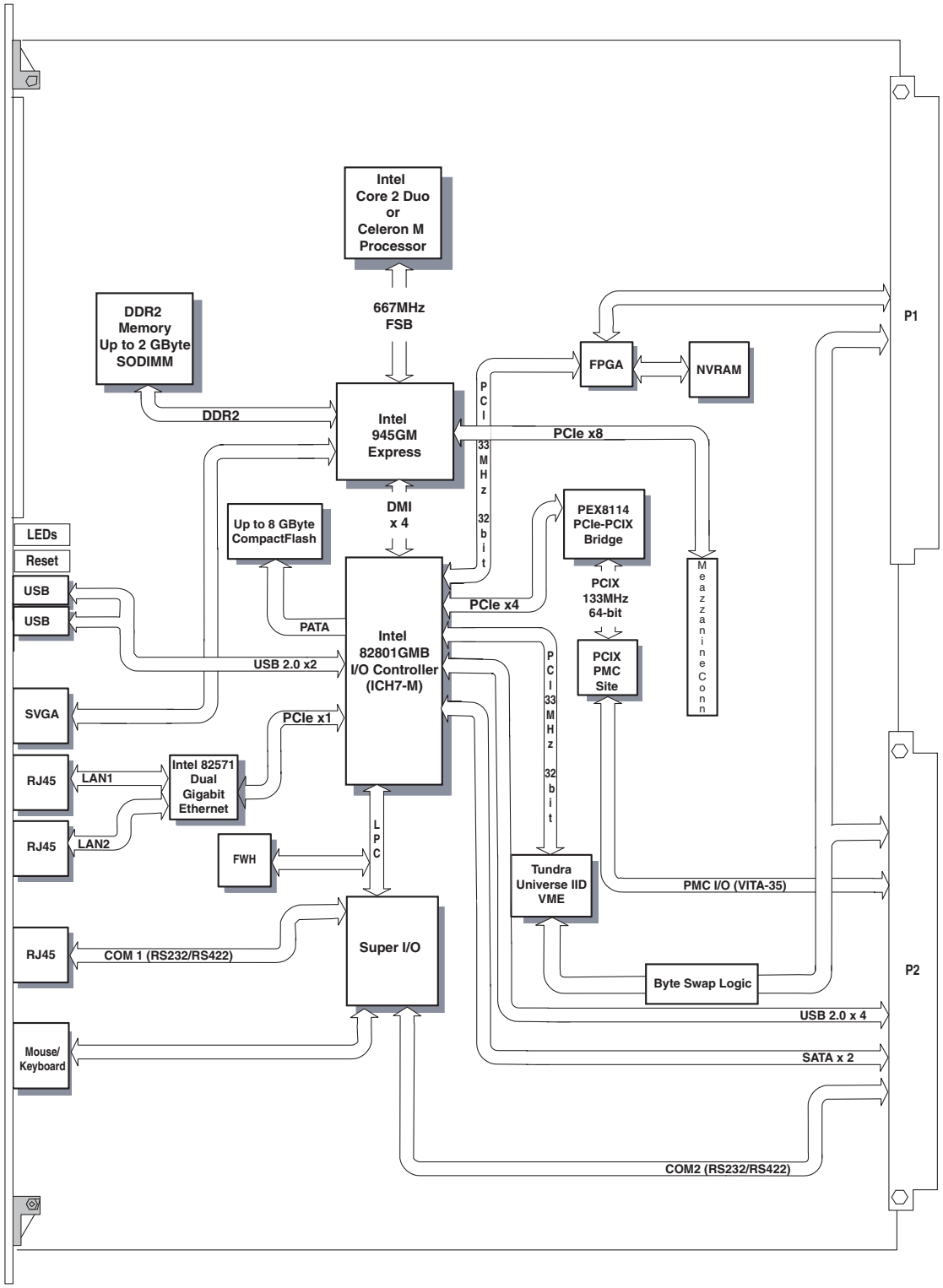


Figure 2 Illustration of V7768

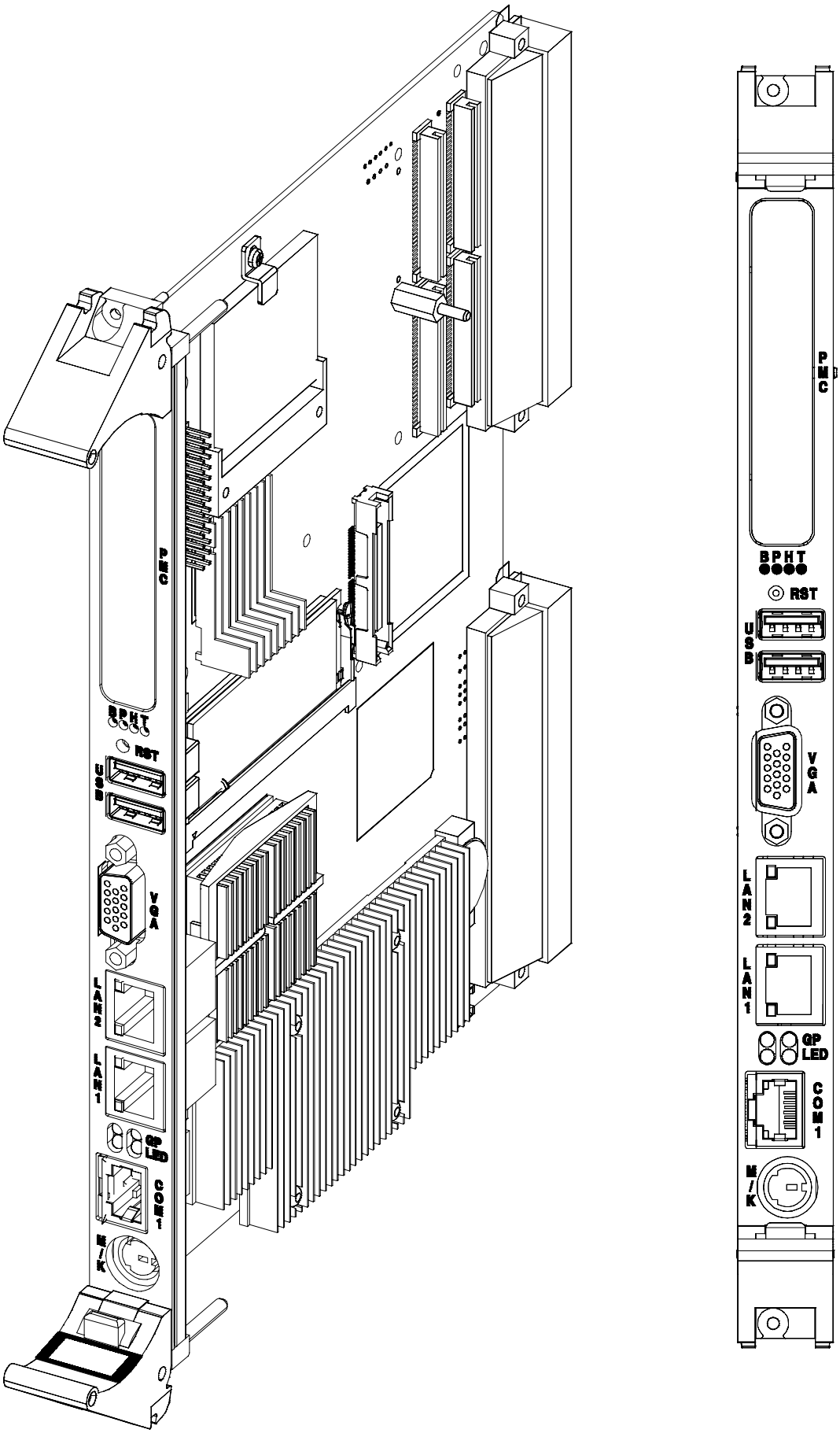


Figure 3 V7769 Block Diagram

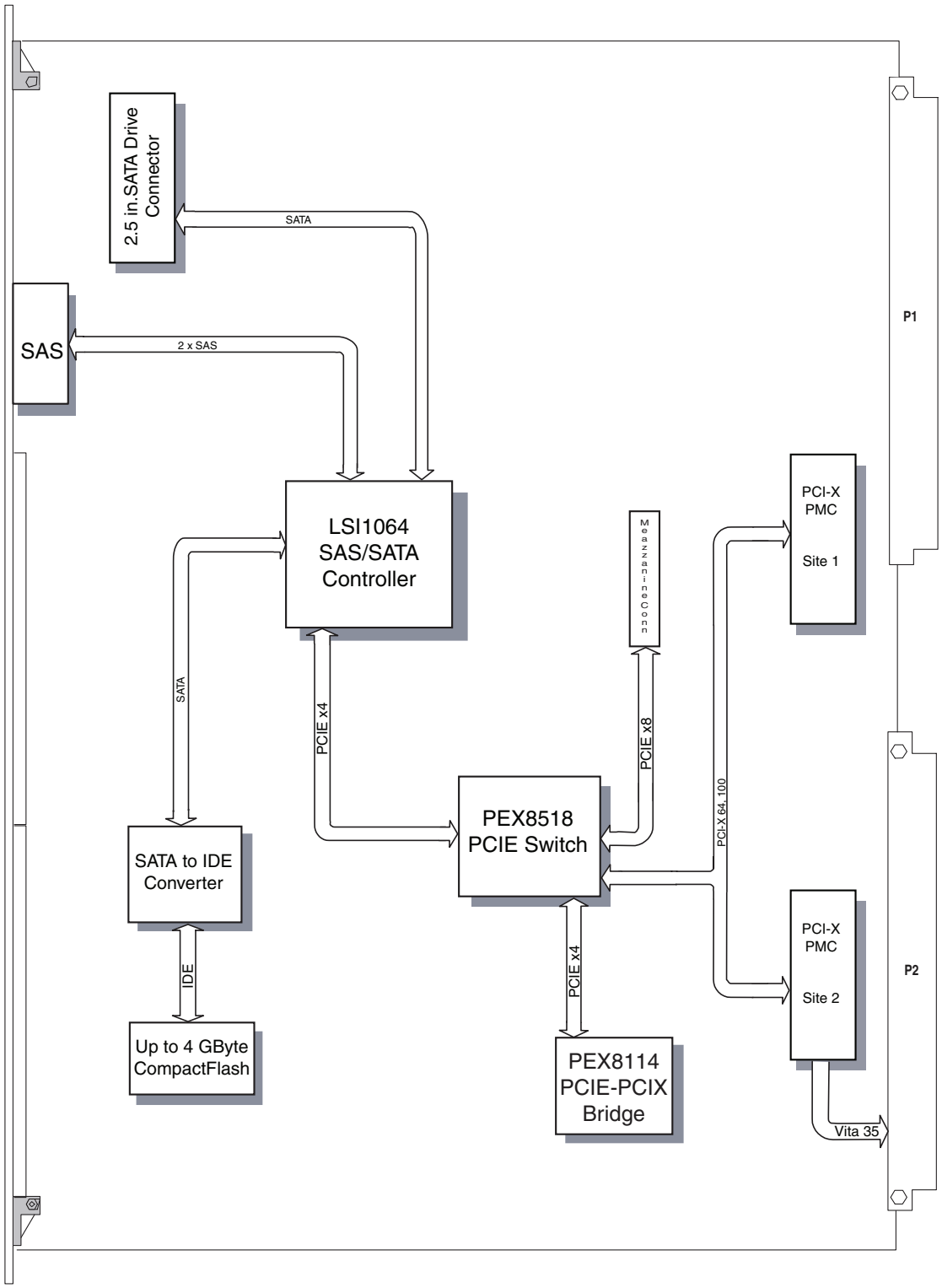
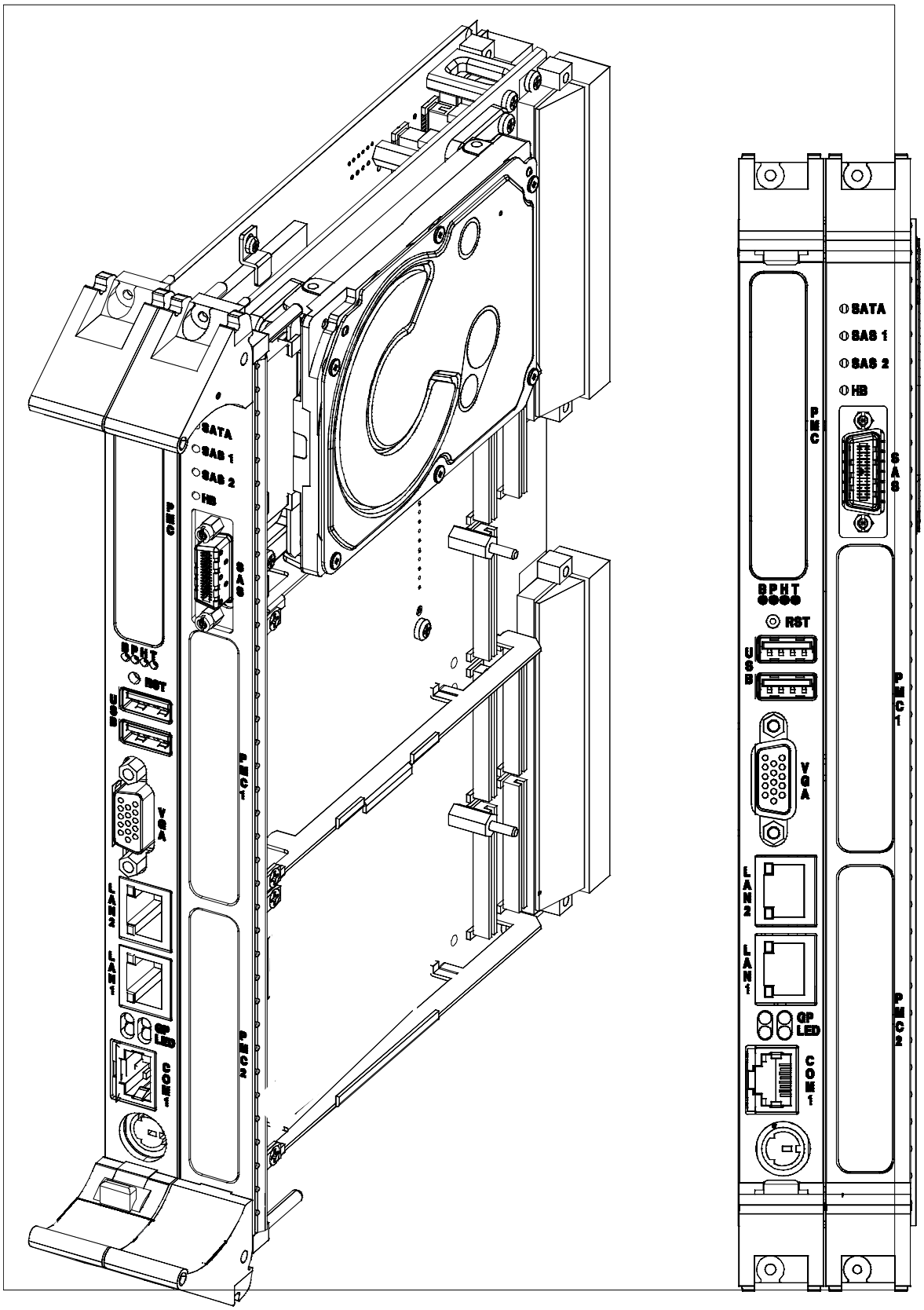


Figure 4 Illustration of V7769



Organization

This manual is composed of the following chapters and appendices:

Chapter 1 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup and operation of the V7768/V7769.

Chapter 2 - Standard Features describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 3 - Embedded PC/RTOS Features describes the unit features that are beyond standard functions.

Maintenance provides information relative to the care and maintenance of the unit.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - AMI BIOS Setup Utility describes the menus and options associated with the American Megatrends, Inc. (system) BIOS.

Appendix C - Remote Booting describes the menus and selections necessary to boot from the SBC remotely.

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January 2007, Order Number 312726-004

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September 2007, Revision 004, Order Number 314078-004

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November 2006, Order Number 309219-003

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January 2006, Order Number 307013-002

Intel 82571EB/82572EI Gigabit Ethernet Controller Product Datasheet
December 2006, Revision 2.0

PCI Local Bus Specification, Rev. 2.2
PCI Special Interest Group
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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

GE assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.



WARNING

Dangerous voltages, capable of causing death, are present in this system.
Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes



STOP

Informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.



WARNING

WARNING denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.



CAUTION

CAUTION denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.



NOTE

NOTE denotes important information. It calls attention to a procedure, practice, or condition which is essential to highlight.



TIP

Tip denotes a bit of expert information.



LINK

This is link text.

1 • Installation and Setup

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the V7768/V7769.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Customer Care along with a request for advice concerning the disposition of the damaged item(s).



CAUTION

Some of the components assembled on GE products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

1.2 Hardware Setup

The V7768/V7769 are factory populated with user-specified options as part of the V7768/V7769 ordering information. Contact Sales for ordering information at 1-800-322-3616. For option upgrades or for any type of repairs, contact customer care to receive a Return Material Authorization (RMA).

GE Customer Care is available at:
(1-800-433-2682), 1-780-401-7700.

Or, visit our website **www.ge-ip.com.**

The V7768/V7769 are tested for system operation and shipped with factory-installed header jumpers. The physical locations of the headers and connectors for the SBC with the PMC option are illustrated in **Figure 1-1 on page 21** and **Figure 1-1 on page 21**. The definitions of the connectors, headers and switches are included in Table 1-1 on page 22.



CAUTION

All jumpers marked *User Configured* in the following tables may be changed or modified by the user. All jumpers marked *Factory Configured* should not be modified by the user.

Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper not marked *User Configured* will void the Warranty and may damage the unit.

1.2.1 V7768 Board Layout Information

Figure 1-1 V7768 Connector Locations

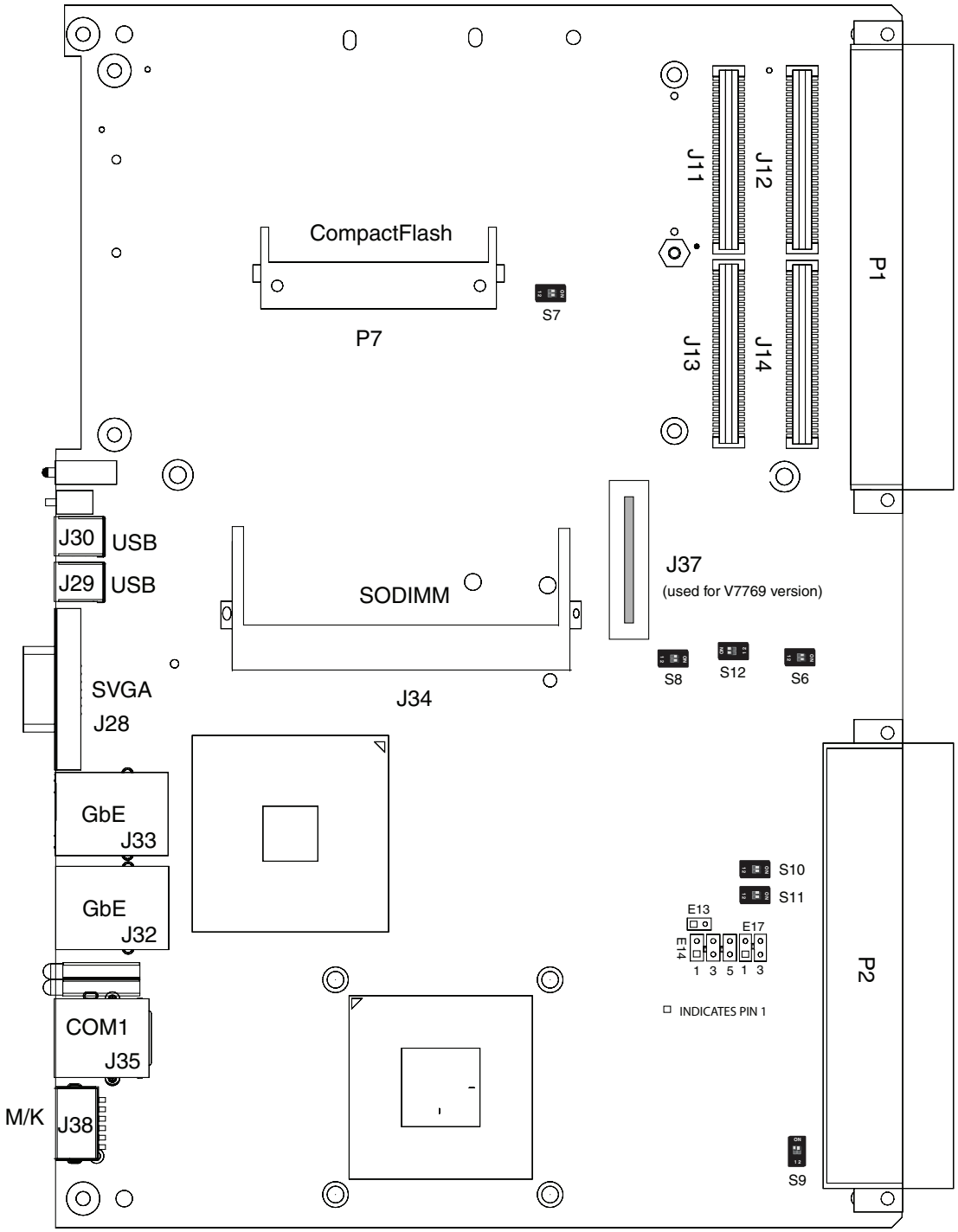


Table 1-1 V7768 Connectors and Switches

Connector	Function
P1	VME interface connector
P2	USB 2.0, Serial ATA, digital video, COM3 and COM4, Gigabit Ethernet
P7	CompactFlash socket
J34	SODIMM socket
J29 and J30	USB ports
J38	Mouse/Keyboard PS/2 Type connector
J15 and J18	Gigabit Ethernet connectors
J11, J12, J13 and J14	PMC Site connectors
J35	Serial port connector (COM1)
J28	SVGA connector
J37	Board to Board connector for V7769
Header	**Function**
E13	COM1 Configuration
E14	COM1 Configuration
E17	COM1 (RS422 Termination)
Switches	**Function**
S6	Mapping/Sysfail generation
S7	VME SYSRESET
S8	Factory Configurable
S9	Factory Configurable
S10	System Controller
S11	Battery enable
S12	RTC Reset and Boot Pause

Table 1-2 Universe IID Mapping/SYSFAIL Generation - Switch (S6)

Position	State	Function
1-4	**On**	**Enable SYSFAIL Generation**
1-4	Off	NO SYSFAIL after reset
2-3	**On**	**Map UNIV2 to Memory Space**
2-3	Off	Map UNIV2 to I/O Space

Table 1-3 VME Strapping - Switch (S7)

Position	State	Function
1-4	**On**	**Enable VME SYSRESET Driver**
2-3	**On**	**Enable SYSRESET Receiver**

Table 1-4 VME System Controller - Switch (S10)

Position	State	Function
1-4	On	Force VME controller based on 2-3 state
1-4	**Off**	**Enable auto system controller**
2-3	On	Force system controller (any slot)
2-3	**Off**	**Force non-system controller (any slot)**

Table 1-5 Battery Enable - Switch (S11)

Position	State	Function
1-4	**On**	**Enable Battery**
1-4	Off	Disable Battery
2-3	On	Factory Use Only
2-3	Off	Factory Use Only

CMOS Password

NOTE

The BIOS has the capability of password protecting casual access to the unit's CMOS setup screens. The CMOS Clear jumper allows the user to clear the password in the case of a forgotten password.

Table 1-6 Password Clear/BIOS Boot Mode - Switch (S12)

Position	State	Function
1-4	**Off**	**Normal**
1-4	On	Clear CMOS/Password
2-3	On	Boot with Post Errors
2-3	**Off**	**Boot Halt on Post Errors**

NOTE

The default settings in the tables are in **bold**.

To clear the CMOS password:

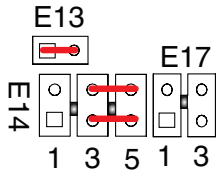
1. Turn off power to the unit.
2. Move switch S12 position 1 to On.
3. Wait approximately 5 seconds.
4. Move switch S12 position 1 to Off.
5. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared, and the CMOS will be set to its defaults.

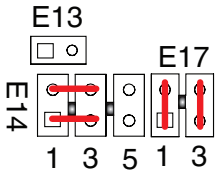
Table 1-7 COM1 Configuration (RS232/RS422 Select) - Header (E13, E14, E17)

Select	E13 Position	E14 Position	E17 Position
RS232	**In**	**3-5, 4-6**	**Both Out**
RS422 w/Termination	Out	1-3, 2-4	1-2, 3-4
RS422 w/o Termination	Out	1-3, 2-4	Both Out

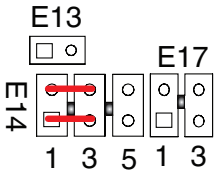
Figure 1-2 COM1 Termination Headers (E13, E14, E17)



RS232



RS422 w/Termination



RS422 w/o Termination

1.2.2 Mezzanine Board Layout Information (V7769)

Figure 1-3 Mezzanine Board Connector Locations

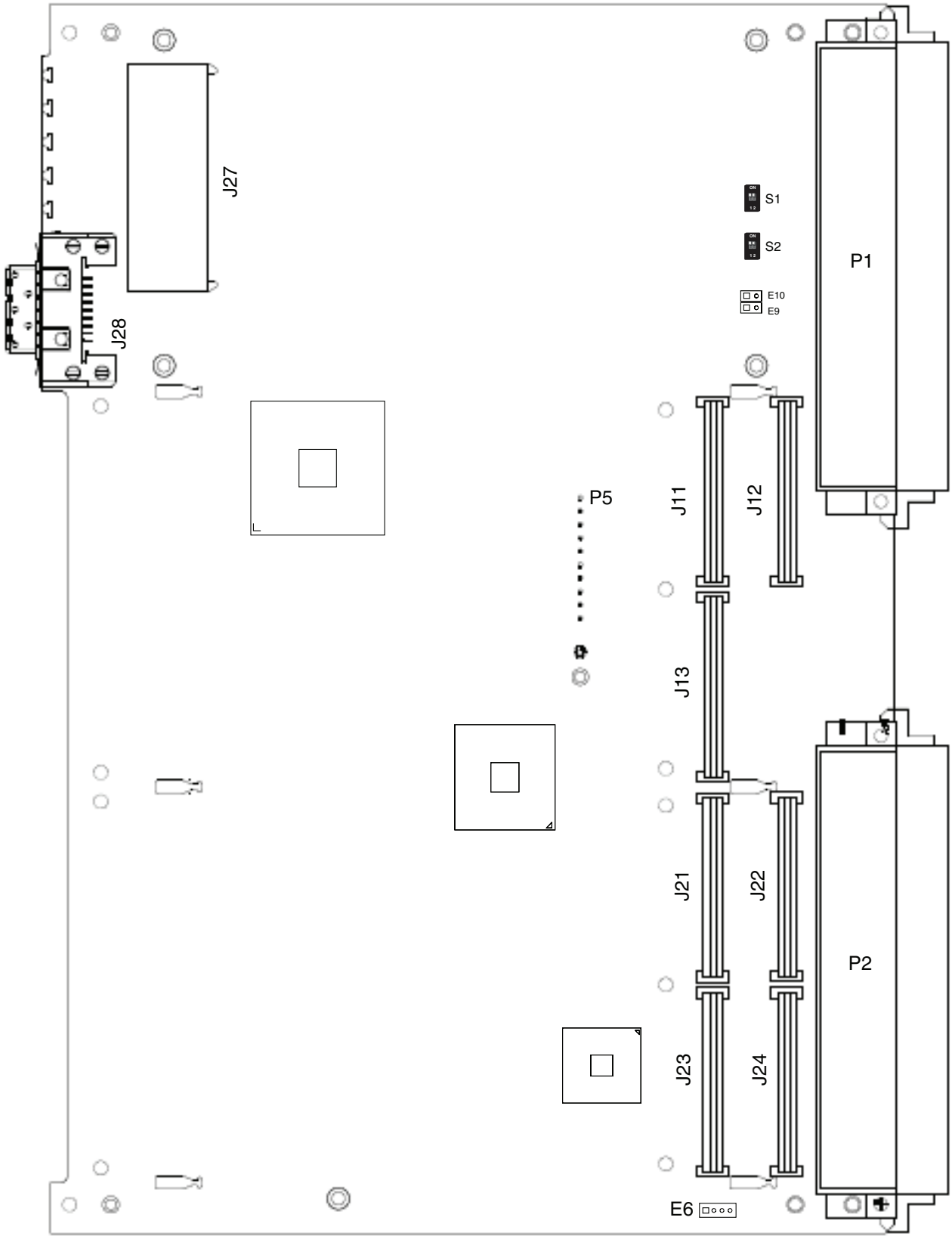


Table 1-8 Mezzanine Connectors and Switches

Connector	Function
P1	VME interface connector
P2	Vita 35 PCI-X PMC connector
P5	Board to Board connector
J11, J12, and J13	PCI-X PMC Site 1 connectors
J21, J22, J23 and J24	PCI-X PMC Site 2 connectors
J27	2.5 in. SATA drive connector
J28	SAS connector
Header	**Function**
E6	SMBus debug header
E9	Not Used
E10	Not Used
Switches	**Function**
S1	Reserved
S2	Enable/Disable JTAG

Table 1-9 Switch (S2) Settings

Position	State	Function
1-4	**Off**	**Disable JTAG**
1-4	On	Enable JTAG
2-3	Off	Not Used
2-3	On	Not Used

1.3 Installation

The V7768/V7769 conform to the VME physical specification for a 6U board. The V7768/V7769 can be used for the system controller or as a peripheral board. It can be plugged directly into any standard chassis accepting either type of board.

The following steps describe the GE-recommended method for installation and powerup of the V7768/V7769:

1. If a PMC module is to be used, connect it to the V7768/V7769 prior to board installation (as shown in **Figure 1-4 on page 28**). Refer to the Product Manual for the PMC module for configuration and setup.

   NOTE
   Air flow as measured at the output side of the heatsink is to be greater than 450 LFM.

2. Insert the V7768/V7769 into a VME chassis system controller or peripheral slot. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector. Use the ejector handles to firmly seat the board.
3. All needed peripherals can be accessed from the front panel or the rear I/O. Each connector is clearly labeled, and detailed pinouts are in ***Appendix A: Connector Pinouts***.
4. Connect a keyboard and mouse if the system has not been previously configured.
5. The V7768 features an optional CompactFlash Disk resident on the board. Refer to ***Chapter 3: Embedded PC/RTOS Features*** for setup details.
6. If an external drive module is installed, the BIOS Setup program must be used to configure the drive types. See ***Appendix B: AMI BIOS Setup Utility*** to properly configure the system.
7. If a drive module is present, install the operating system according to the manufacturer's instructions.

1.3.1 BIOS Setup

The V7768/V7769 has an onboard BIOS Setup program that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's CMOS Configuration. The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

Details of the V7768/V7769 BIOS setup program are included in ***Appendix B: AMI BIOS Setup Utility***.

Figure 1-4 Installing the PMC Card on the V7768/V7769

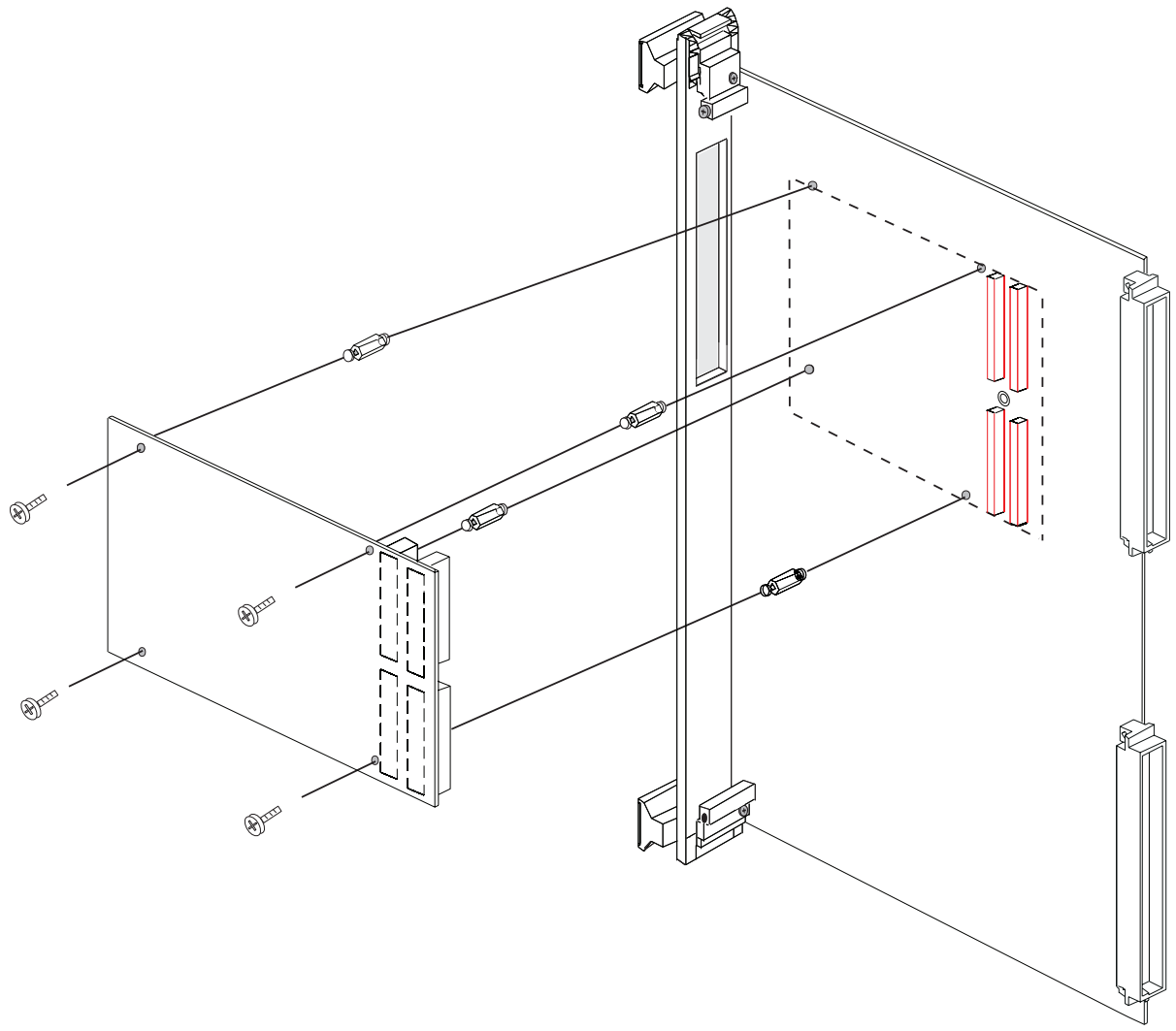


Figure 1-5 Backside Mounting for the PMC Card

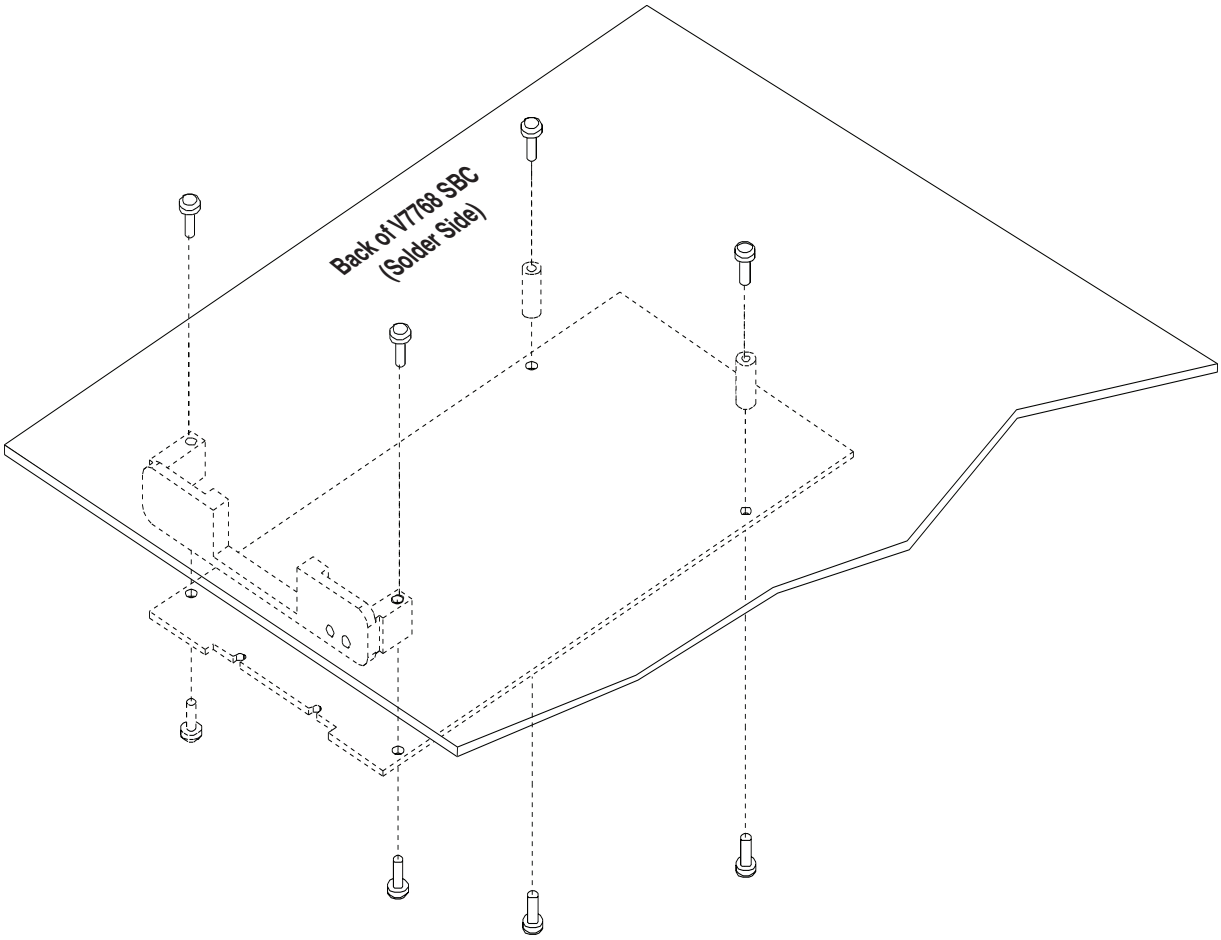
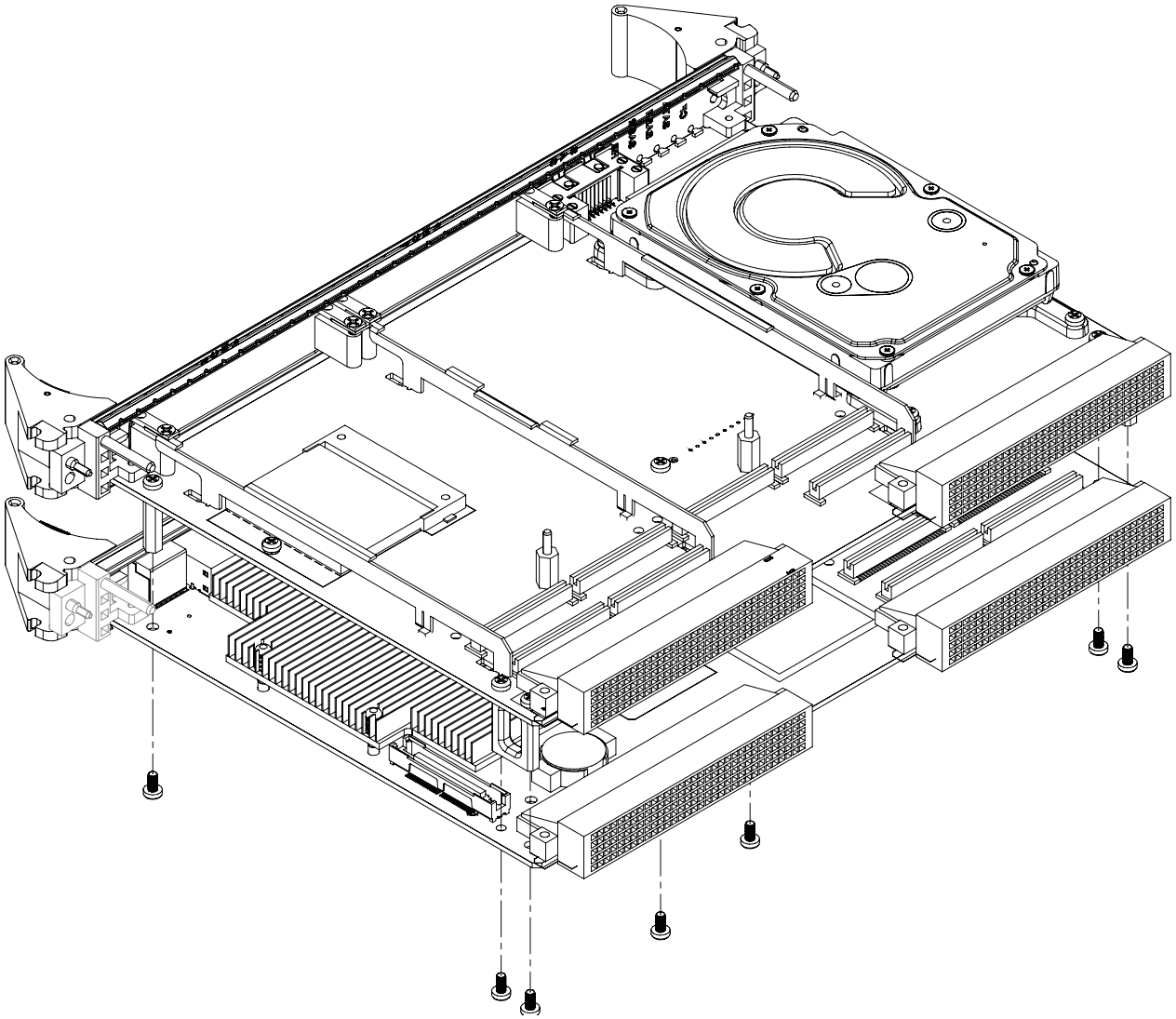


Figure 1-6 Installation of Mezzanine Board onto the Main Board



See **Figure 4 on page 15** for the image of the fully installed V7769.

1.4 Front/Rear Panel Connectors

The V7768/V7769 provide front panel access for the PMC expansion site, an optional Gigabit Ethernet port, one 10/100 RJ45 connector, one serial port, SVGA, keyboard/mouse, the manual reset switch and the status LEDs. A drawing of the V7768/V7769 front panels are shown in **Figure 1-7** and **Figure 1-8**. The front panel connectors and indicators are labeled as follows:

V7768

- USB — Dual USB 2.0 Ports
- LAN1 — 10/100/1000 Mbit Ethernet connector for port 1
- LAN2 — 10/100/1000 Mbit Ethernet connector for port 2
- M/K — Mouse/keyboard connector
- COM1 — Serial Port
- RST — Manual reset switch
- BPHT — Status LEDs
- VGA — Analog Video connector
- A L — Activity and Link Status LEDs for rear GbE

V7769

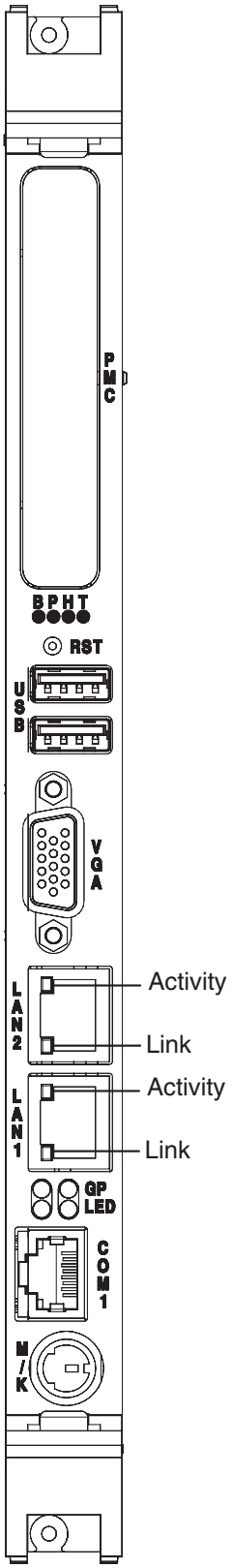
- SATA — Serial ATA Activity LED
- SAS1 — SAS Lane 1
- SAS2 — SAS Lane 2
- HB — Heartbeat LED for SAS/SATA controller

The V7768/V7769 provide rear I/O support for the following: digital video, two SATA ports, one Serial and four USB ports. The V7768/V7769 are compatible with GE's Rear Transition Modules ACC-0602RC and ACC-0603RC.

The front panel connectors, including connector pinouts and orientation, for the V7768/V7769 are defined in ***Appendix A: Connector Pinouts***.

1.5 Front Panel Layouts

Figure 1-7 V7768 Front Panel Layout



Status LEDs (from left to right)

Boot Done (B)	*Booting* - Indicates BIOS Boot is in progress. When LED is Off, CPU has finished POST and is ready (Red LED).
PWR (P)	*Power* - Indicates when power is applied to the board, (Green LED).
IDE (H)	*Activity Indicator* - Flashes when IDE activity is occurring, (Yellow LED).
Sysfail (T)	*VME failure* - Lights during VME SYSFAIL condition, (Red LED).

RST Switch

Reset	Allows the system to be reset from the front panel.

LAN1 and LAN2 LEDs

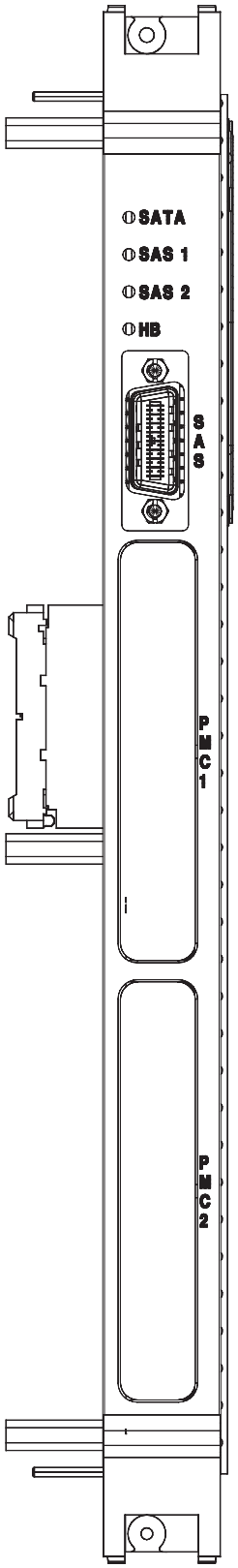
Activity	Indicates the Ethernet is active, (Yellow LED).
Link	10Base-T (LED Off) 100Base-TX (Yellow LED) or 1000Base-T (Green LED)

GP LED (User Configurable, general purpose LEDs)

Controlled by accessing I/O port 0xA4B bits 7-4. *The LEDs are turned off by setting the associated bit and turned on by clearing the associated bit.*

Upper/Right LED	- Bit 7
Upper/Left LED	- Bit 6
Lower/Right LED	- Bit 5
Lower/Left LED	- Bit 4

Figure 1-8 Mezzanine Front Panel Layout (for V7769)



Status LEDs (from top to bottom)

SATA	*SerialATA Activity* - LED will flash to indicate activity on the SATA drive, (Green LED).
SAS1	SCSI *Activity* - LED will flash to indicate activity on the first SAS Lane, (Green LED).
SAS2	*SCSI Activity* - LED will flash to indicate activity on the second SAS Lane, (Green LED).
HB	*Heartbeat Activity* - LED will flash to indicate activity on the secondary SCSI drive, (Green LED).

A *fault* is being indicated when any of the LEDs on the mezzanine board for the V7769 are red.

2 • Standard Features

The V7768/V7769 are single board computers loaded with either an Intel Core 2 Duo or Celeron M processor and compatible with modern industry standard desktop systems. The V7768/V7769 therefore retain industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB ports, CompactFlash drive, video controller and Ethernet controller) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the V7768/V7769.

2.1 BGA CPU

The V7768 is factory populated with either an Intel Core 2 Duo or Celeron M processor. The V7769 is factory populated with an Intel Core 2 Duo processor.

To change the memory size or CompactFlash size contact Customer Care to receive a Return Material Authorization (RMA).

GE Customer Care is available at:
(1-800-433-2682), 1-780-401-7700.

Or, visit our website **www.ge-ip.com.**

2.2 Physical Memory

The V7768/V7769 provide DDR2 Synchronous DRAM (SDRAM) as system memory. Memory can be accessed as bytes, words or longwords.

The SDRAM is accessible to the VME bus through the PCI-to-VME bridge and is addressable by the local processor.

The V7768/V7769 have a maximum memory configuration of 2 GByte of DDR2 SDRAM memory. This configuration calls for a single 2 GByte SODIMM (one 200-pin SODIMM DDR2 module). The SDRAM is dual-ported to the VME through the PCI-to-VME bridge and is addressable by the local processor, as well as the VME slave interface by another VME master. Caution must be used when sharing memory between the local processor and the VME to prevent a VME deadlock and to prevent a VME master from overwriting the local processor's operating system.



NOTE

When using the Configure utility of GE's IOWorks Access to configure RAM, do not request more than 25 percent of the physical RAM. Exceeding the 25 percent limit may result in known bugs that causes unpredictable behavior during the boot sequence, and requires the use of an emergency repair disk to restore the computer. It is recommended that an emergency repair disk be kept up-to-date and easily accessible.

The V7768/V7769 include 32 KByte of non-volatile SRAM which can be accessed by the CPU at any time, and is used to store system data that must not be lost during power-off conditions.

NOTE

Memory capacity may be extended as parts become available.

2.3 Memory Map

Table 2-1 Memory Map

Mode	Memory Address Range	Size	Description
Protected Mode	$FFFF 0000 - $FFFF FFFF	64 KByte	ROM BIOS Image
	$C000 0000 - $FFFE FFFF	0.9 GByte	Unused*
	$0010 0000 - $BFFF FFFF	3 GByte	Reserved for ** Onboard Extended Memory (not filled on all systems)
Real Mode	$E0000 - $FFFFF	128 KByte	
	$C0000 - $DFFFF	128 KByte	
	$A0000 - $BFFFF	128 KByte	
	$00000 - $9FFFF	640 KByte	

* This space can be used to set up protected mode PCI-to-VME windows (also referred to as PCI slave images). BIOS will also map onboard PCI based NVRAM, Timers and Watchdog Timers in this area.
** This space can be allocated as shared memory (for example, between the BGA CPU and VME Master). Note that if a PMC board is loaded, the expansion BIOS may be placed in this area.

2.4 I/O Port Map

Like a desktop system, the V7768/V7769 include special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64 KByte I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 2-2.

Table 2-2 V7768/V7769 I/O Address Map

I/O Address Range	Size in Bytes	HW Device	PC/AT Function
$000 - $00F	16		DMA Controller 1
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, System Configuration
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2
$0E0 - $16F	142		Reserved
$170 - $177	8	ICH7-M	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	ICH7-M	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip	Reserved
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super I/O Chip*	Secondary Floppy Disk Controller*
$378 - $37F	8	Super I/O Chip	Reserved
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Super I/O Chip*	Primary Floppy Disk Controller*
$3F8 - $3FE	7	Super I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF	256		Reserved
$500 - $CFF	2048		Reserved

*While these I/O ports are reserved for the listed functions, they are not implemented on the V7768/V7769. They are listed here to make the user aware of the standard PC usage of these ports.

2.5 Interrupts

2.5.1 Legacy PIC System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-3 along with their functions. Table 2-4 on page 38 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 2-4 on page 38.

The interrupt hardware implementation on the V7768/V7769 is standard for computers built around the PC architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the Programmable Interrupt Controller (PIC). The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 2-1 on page 42.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 2-3 Interrupt Line Assignments

IRQ	AT Function	Comments
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by V7768/V7769 PCI bus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2	
4	COM1	
5	Unused	
6	Floppy Controller	
7	Unused	
8	Real-Time Clock	
9	Old IRQ2	SVGA or Network I/O
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	
14	AT Hard Drive	
15	Flash Drive	

Table 2-4 Interrupt Vector Table

Interrupt No.		IRQ Line	Real Mode	Protected Mode
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VME Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Unassigned	Not Assigned
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	Not Assigned	Not Assigned
10	16		BIOS Video I/O	Coprocessor Error
11	17		System Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26		Time of Day	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode

Table 2-4 Interrupt Vector Table (Continued)

Interrupt No.		IRQ Line	Real Mode	Protected Mode
HEX	DEC			
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-6F	103-111		Reserved by DOS	Same as Real Mode
70	112	IRQ8	Real-Time Clock	
71	113	IRQ9	Redirect to IRQ2	
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	AT Hard Drive	
77	119	IRQ15	Flash Drive	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

2.5.2 PCI Interrupts

The PMC PCI-X sites of the V7769 connect Standard PCI Interrupt Lines to the PCI-E to PCI-X bridge as shown in Figure 2-1 on page 42. The PCI-E bridge (PLX PEX8114) converts the PCI INTx interrupts into virtual PCI Express interrupts that are signaled back to the chipset over the PCI Express Interface.

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are defined as "level sensitive," asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 2-1 on page 42 depicts the V7768/V7769 interrupt logic pertaining to FPGA timer operations and the PCI expansion site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The PIC accepts the PCI interrupts through lines that are defined by the BIOS.

PCI Device Interrupt Map

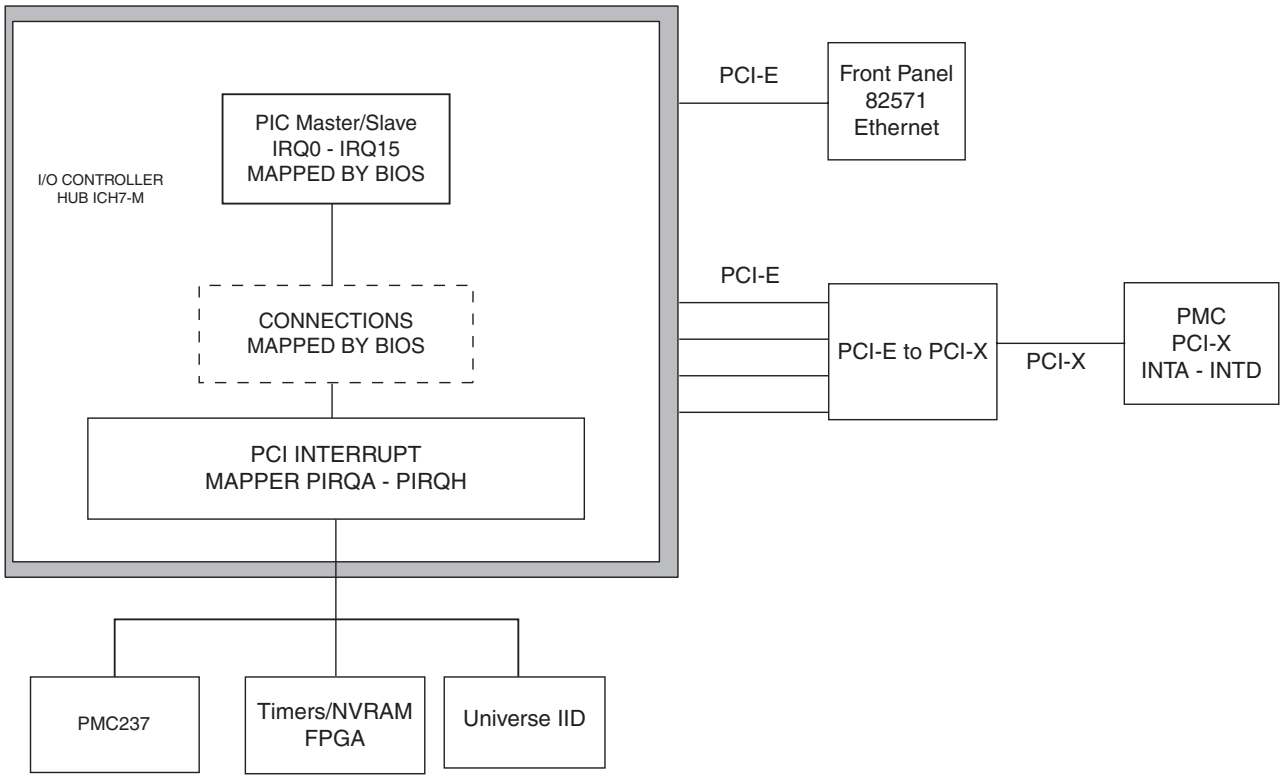
The PCI bus-based external devices include the PMC sites, Ethernet controller and the PCI-to-VME bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the ICH. This mapping is illustrated in Figure 2-1 on page 42 and is defined in Table 2-5.

Table 2-5 PCI Device Interrupt Mapping by the BIOS

Device	Component	Vendor ID	Device ID	ID Select	PCI IRQ	Arbitration Request Line
PCI-to-VME Bridge	Tundra Universe IID	0x10E3	0x0000	AD27	INTD	REQ1
Timer/SRAM FPGA	GE Proprietary	0x114A	0x0004	AD26	INTC	N/A
PMC	N/A	N/A	N/A	AD24	INTA, B, C, D	REQ0
Ethernet Controller	Intel 82571EB	0x8086	0x105E	N/A	N/A	N/A
PCI Host Bridge	GMCH	0x8086	0x27A0	N/A	N/A	N/A
VGA Controller	GMCH	0x8086	0x27A2	N/A	N/A	N/A
Integrated Graphics	GMCH	0x8086	0x27A6	N/A	N/A	N/A
PCI-LPC Bridge	ICH7-M	0x8086	0x27BD	N/A	N/A	N/A
USB UHCI Controller	ICH7-M	0x8086	0x27C8 0x27C9 0x27CA 0x27CB	N/A	N/A	N/A
USB EHCI	ICH7-M	0x8086	0x27CC	N/A	N/A	N/A
SMBus Controller	ICH7-M	0x8086	0x27DA	N/A	N/A	N/A
PCI-E Controller	ICH7-M	0x8086	0x27D0	N/A	N/A	N/A
PCI-E Controller	ICH7-M	0x8086	0x27E0	N/A	N/A	N/A
DMI-PCI Bridge	ICH7-M	0x8086	0x2448	N/A	N/A	N/A
PCI-E Switch*	PLX 8518	0x10B5	0x8518	N/A	N/A	N/A
PCI-E to PCI-X Bridge*	PLX 8114	0x10B5	0x8114	N/A	N/A	N/A
LSI SAS Controller*	LSI1064E	0x1000	0x0056	AD16	N/A	N/A
PCI-E Graphics Port	GMCH	0x8086	27A1	N/A	N/A	N/A
SATA Controller	ICH7-M	0x8086	27C4	N/A	N/A	N/A

* Only available on V7769.

Figure 2-1 Connections for the PC Interrupt Logic Controller



2.6 Integrated Peripherals

The V7768/V7769 incorporate an SMSC Super I/O (SIO) chip. The SIO provides the V7768/V7769 with two 16550 UART-compatible serial ports, keyboard and mouse ports, and general purpose I/O for system functions, available via the VME backplane connectors.

The SATA interface is provided by the Intel I/O Controller Hub chip (ICH7-M). It is routed out of the VME backplane P2 connector. The SATA interface supports two channels known as the primary and secondary channels.

Selection of drive type, along with detailed SATA selections, are available in the CMOS Advanced BIOS Setup Menu.

2.7 Ethernet Controller

The network capability is provided by the Intel 82571 Dual Ethernet Controller for Gigabit Ethernet. This Ethernet controller is PCI-E bus based and is software configurable. The V7768/V7769 support 10Base-T, 100Base-TX and 1000Base-T Ethernet.

10Base-T A network based on the 10Base-T standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ45 connector is used with the 10Base-T standard. 10Base-T has a maximum length of 100 meters.

100Base-TX The V7768/V7769 also support the 100Base-TX Ethernet. A network based on a 100Base-TX standard uses unshielded twisted-pair cables. 100Base-TX has a maximum length of 100 meters.

1000Base-T The V7768/V7769 support 1000Base-T Ethernet using the Intel 82571 dual Ethernet controller. The interface uses shielded cables with four pairs of conductors, along with an RJ45 connector on the front panel.



NOTE

Ethernet activity is noted on the front panel LEDs by a blinking yellow LED. The yellow LED will be on continuously when the Ethernet port is linked but with no activity.

2.8 Video Graphics Adapter

The SVGA port on the V7768/V7769 is controlled by the Intel 945GM Graphic and Memory Controller Hub (GMCH). The GMCH is hardware and BIOS compatible with the industry SVGA and digital video standards supporting both VESA high-resolution and extended video modes. Table 2-6 shows the graphics video modes supported by the GMCH video controller for analog monitors.

Table 2-6 Supported Graphics Video Resolutions for Windows XP (Analog)

Screen Resolution	Maximum Colors	Maximum Refresh Rates (Hz)
640 x 480	High and True are supported at all resolutions.	85
800 x 600		85
1024 x 768		85
1080 x 1280		75
1600 x 1200		60

Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 85 Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

3 • Embedded PC/RTOS Features

GE's V7768/V7769 feature additional capabilities beyond those of a typical desktop computer system. The units provide four software-controlled, general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The V7768 provides a bootable CompactFlash Disk system and 32 KByte of non-volatile RAM. Also, the V7768/V7769 support an embedded intelligent VME bridge to allow compatibility with the most demanding VME applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used.

3.1 VME Bridge

3.1.1 Features

- Complete six-line Address Modifier (AM-Code) programmability
- VME data interface with separate hardware byte/word swapping for master and slave accesses
- Support for VME64 multiplexed MBLT 64-bit VME block transfers
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VME arbiter (PRI, SGL and RRS modes are supported)
- VME BERR bus error timer (software programmable)
- Slave access from the VME to local RAM and mailbox registers
- Full-featured programmable VME requester (ROR, RWD and BCAP modes are supported)
- System Controller auto detection
- Complete VME master access through five separate Protected-mode memory windows

The V7768/V7769 support High Throughput DMA transfers of bytes, words and longwords in both Master and Slave configurations.

If Endian conversion is not needed, GE offers a special "Bypass" mode that can be used to further enhance throughput (not available for byte transfers).

The V7768/V7769 VME interface is provided by the PCI-to-VME bridge built around the Tundra Semiconductor Corporation Universe IID VME interface chip. The Universe IID provides a reliable high-performance 64-bit VME-to-PCI interface in one design. The functions and programming of the Universe-based VME interface are addressed in detail in a companion manual titled: *GE's Tundra Universe II Based VME Interface Product Manual (500-000211-000)*.

3.1.2 I²C/SMBus Temperature Sensor

The MAX6659MEE can be monitored and controlled on the SMBus at address 0x98 for the V7768/V7769. This will allow the user to monitor and set up the alarm ($\overline{\text{OVERT2}}$).

For more information on the Maxim MAX6659MEE contact them directly at:

1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

3.2 Embedded PCI Functions

The V7768/V7769 provide non-volatile RAM (NVRAM), timers and a Watchdog Timer via the PCI bus FPGA. These functions are required for embedded and real time applications. The PCI configuration space of these embedded functions is shown in Table 3-1.

Table 3-1 PCI Configuration Space Registers

31	16	15	0	Register Address
Device ID 0004		Vendor ID 114A		00h
Status		Command		04h
Class Code			Revision ID	08h
BIST	Header Type	Latency Timer	Cache Line Size	0Ch
PCI Base Address 0 for Memory-Mapped VME Control registers (BAR0)				10h
PCI Base Address 1 for Memory-Mapped 32 KByte NVRAM (BAR1)				14h
PCI Base Address 2 for Memory Mapped Watchdog and other timers (BAR2)				18h
Reserved				1Ch
Reserved				20h
Reserved				24h
Reserved				28h
Subsystem ID 7768		Subsystem Vendor ID 114A		2Ch
Reserved				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_gnt	Interrupt Pin	Interrupt Line	3Ch

The "Device ID" field indicates that the device is for VME products (00) and indicates the supported embedded feature set.

The "Vendor ID" and "Subsystem Vendor ID" fields indicate GE's PICMG® assigned Vendor ID (114A).

The "Subsystem ID" field indicates the model number of the product (7768).

3.3 Timers

The V7768/V7769 provide four user-programmable timers (two 16-bit and two 32-bit) which are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2 MHz, 1 MHz, 500 kHz and 250 kHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

3.3.1 Timer Control Status Register 1 (TCSR1)

The timers are controlled and monitored via the Timer Control Status Register 1 (TCSR1) located at offset 0x00 from the address in BAR2. The mapping of the bits in this register are shown in Table 3-2.

Table 3-2 TCSR1 Bit Mapping

Field	Bits	Read or Write
Timer 1 Caused IRQ	TCSR1[0]	R/W
Timer 1 Enable	TCSR1[1]	R/W
Timer 1 IRQ Enable	TCSR1[2]	R/W
Timer 1 Clock Select	TCSR1[4..3]	R/W
Timer 2 Caused IRQ	TCSR1[8]	R/W
Timer 2 Enable	TCSR1[9]	R/W
Timer 2 IRQ Enable	TCSR1[10]	R/W
Timer 2 Clock Select	TCSR1[12..11]	R/W
Timer 3 Caused IRQ	TCSR1[16]	R/W
Timer 3 Enable	TCSR1[17]	R/W
Timer 3 IRQ Enable	TCSR1[18]	R/W
Timer 3 Clock Select	TCSR1[20..19]	R/W
Timer 4 Caused IRQ	TCSR1[24]	R/W
Timer 4 Enable	TCSR1[25]	R/W
Timer 4 IRQ Enable	TCSR1[26]	R/W
Timer 4 Clock Select	TCSR1[28..27]	R/W
Reserved	All Other Bits	R/W
All of these bits default to "0" after system reset.		

Each timer has an independently selectable clock source which is selected by the bit pattern in the "Timer x Clock Select" field as shown in Table 3-3.

Table 3-3 Selectable Clock Source for Timers

Clock Ratio	MSb	LSb
2 MHz	0	0
1 MHz	0	1
500 kHz	1	0
250 kHz	1	1

Each timer can be independently enabled by writing a “1” to the appropriate “Timer x Enable” field. Similarly, the generation of interrupts by each timer can be independently enabled by writing a “1” to the appropriate “Timer x IRQ Enable” field.

If an interrupt is generated by a timer, the source of the interrupt may be determined by reading the “Timer x Caused IRQ” fields. If the field is set to “1”, then the respective timer caused the interrupt. Note that multiple timers can cause a single interrupt. Therefore, the status of all timers must be read to ensure that all interrupt sources are recognized.

A particular timer interrupt can be cleared by writing a “0” to the appropriate “Timer x Caused IRQ” field. Alternately, a write to the appropriate Timer x IRQ Clear (TxIC) register will also clear the interrupt. When clearing the interrupt using the “Timer x Caused IRQ” fields, note that it is very important to ensure that a proper bit mask is used so that other register settings are not affected. The preferred method for clearing interrupts is to use the “Timer x IRQ Clear” registers described on page 50.

3.3.2 Timer Control Status Register 2 (TCSR2)

The timers are also controlled by bits in the Timer Control Status Register 2 (TCSR2) located at offset 0x04 from the address in BAR2. The mapping of the bits in this register is shown in Table 3-4.

Table 3-4 TCSR2 Bit Mapping

Field	Bits	Read or Write
Read Latch Select	TCSR2[0]	R/W
Reserved	All Other Bits	R/W

All of these bits default to “0” after system reset.

The “Read Latch Select” bit is used to select the latching mode of the programmable timers. If this bit is set to “0”, then each timer output is latched upon a read of any one of its address. For example, a read to the TMRCCR12 register latches the count of timers 1 and 2. A read to the TMRCCR3 register latches the count of timer 3. This continues for every read to any one of these registers. As a result, it is not possible to capture the values of all four timers at a given instance in time. However, by setting this bit to “1”, all four timer outputs will be latched only on reads to the Timer 1 & 2 Current Count Register (TMRCCR12). Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR12 first (with a 32-bit read), followed by a read to TMRCCR3 and TMRCCR4. The first read (to the TMRCCR12 register) causes all four timer values to be latched at the same time. The subsequent reads to the TMRCCR3 and TMRCCR4 registers do not latch new count values, allowing the count of all timers at the same instance in time to be obtained.

3.3.3 Timer 1 & 2 Load Count Register (TMRLCR12)

Timers 1 & 2 are 16-bits wide and obtain their load count from the Timer 1 & 2 Load Count Register (TMRLCR12), located at offset 0x10 from the address in BAR2. The mapping of bits in this register is shown in Table 3-5.

Table 3-5 TMRLCR12 Bit Mapping

Field	Bits	Read or Write
Timer 2 Load Count	TMRLCR12[31..16]	R/W
Timer 1 Load Count	TMRLCR12[15..0]	R/W

When either of these fields are written (either by a single 32-bit write or separate 16-bit writes), the respective timer is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

3.3.4 Timer 3 Load Count Register (TMRLCR3)

Timer 3 is 32-bits wide and obtains its load count from the Timer 3 Load Count Register (TMRLCR3), located at offset 0x14 from the address in BAR2. The mapping of bits in this register is shown in Table 3-6.

Table 3-6 TMRLCR3 Bit Mapping

Field	Bits	Read or Write
Timer 3 Load Count	TMRLCR3[31..0]	R/W

When this field is written, Timer 3 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

3.3.5 Timer 4 Load Count Register (TMRLCR4)

Timer 4 is 32-bits wide and obtains its load count from the Timer 4 Load Count Register (TMRLCR4), located at offset 0x18 from the address in BAR2. The mapping of bits in this register is shown in Table 3-7.

Table 3-7 TMRLCR4 Bit Mapping

Field	Bits	Read or Write
Timer 4 Load Count	TMRLCR4[31..0]	R/W

When this field is written, Timer 4 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

3.3.6 Timer 1 & 2 Current Count Register (TMRCCR12)

The current count of timers 1 & 2 may be read via the Timer 1 & 2 Current Count Register (TMRCCR12), located at offset 0x20 from the address in BAR2. The mapping of bits in this register is shown in Table 3-8.

Table 3-8 TMRCCR12 Bit Mapping

Field	Bits	Read or Write
Timer 2 Count	TMRCCR12[31..16]	Read Only
Timer 1 Count	TMRCCR12[15..0]	Read Only

When either field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the Control Status Register (TCSR2). See the TCSR2 register description for more information on these two modes.

3.3.7 Timer 3 Current Count Register (TMRCCR3)

The current count of Timer 3 may be read via the Timer 3 Current Count Register (TMRCCR3), located at offset 0x24 from the address in BAR2. The mapping of bits in this register is shown in Table 3-9.

Table 3-9 TMRCCR3 Bit Mapping

Field	Bits	Read or Write
Timer 3 Count	TMRCCR3[31..0]	Read Only

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the Control Status Register (TCSR2). See the TCSR2 register description for more information on these two modes.

3.3.8 Timer 4 Current Count Register (TMRCCR4)

The current count of Timer 4 may be read via the Timer 4 Current Count Register (TMRCCR4), located at offset 0x28 from the address in BAR2. The mapping of bits in this register is shown in Table 3-10.

Table 3-10 TMRCCR4 Bit Mapping

Field	Bits	Read or Write
Timer 4 Count	TMRCCR4[31..0]	Read Only

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the Control Status Register (TCSR2). See the TCSR2 register description for more information on these two modes.

3.3.9 Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x30 from the address in BAR2, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (TCSR1). This register is write only and the data written is irrelevant.

3.3.10 Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x34 from the address in BAR2, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a

"0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (TCSR1). This register is write only and the data written is irrelevant.

3.3.11 Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x38 from the address in BAR2, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (TCSR1). This register is write only and the data written is irrelevant.

3.3.12 Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x3C from the address in BAR2, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (TCSR1). This register is write only and the data written is irrelevant.

3.4 Watchdog Timer

The V7768/V7769 provide a programmable Watchdog Timer (WDT) which can be used to reset the system if software integrity fails.

3.4.1 WDT Control Status Register (WCSR)

The WDT is controlled and monitored by the WDT Control Status Register (WCSR) which is located at offset 0x08 from the address in BAR2. The mapping of the bits in this register is shown in Table 3-11.

Table 3-11 WCSR Bit Mapping

Field	Bits	Read or Write
SERR/RST Select	WCSR[16]	R/W
WDT Timeout Select	WCSR[10..8]	R/W
WDT Enable	WCSR[0]	R/W

All of these bits default to "0" after system reset. All other bits are reserved.

The "WDT Timeout Select" field is used to select the timeout value of the WDT as shown in Table 3-12.

Table 3-12 Selecting Timeout Value of the WDT

Timeout	WCSR[10]	WCSR[9]	WCSR[8]
135 s	0	0	0
33.6 s	0	0	1
2.1 s	0	1	0
524 ms	0	1	1
262 ms	1	0	0
131 ms	1	0	1
32.768 ms	1	1	0
2.048 ms	1	1	1

The “SERR/RST Select” bit is used to select whether the WDT generates an SERR# on the local PCI bus or a system reset. If this bit is set to “0”, the WDT will generate a system reset. Otherwise, the WDT will make the local PCI bus SERR# signal active.

The “WDT Enable” bit is used to enable the Watchdog Timer function. This bit must be set to “1” in order for the Watchdog Timer to function. Note that since all registers default to zero after reset, the Watchdog Timer is always disabled after a reset. The Watchdog Timer must be re-enabled by the application software after reset in order for the Watchdog Timer to continue to operate. Once the Watchdog Timer is enabled, the application software must refresh the Watchdog Timer within the selected timeout period to prevent a reset or SERR# from being generated. The Watchdog Timer is refreshed by performing a write to the WDT Keepalive register (WKPA). The data written is irrelevant.

3.4.2 WDT Keepalive Register (WKPA)

When enabled, the Watchdog Timer is prevented from resetting the system by writing to the WDT Keepalive Register (WKPA) located at offset 0x0C from the address in BAR2 within the selected timeout period. The data written to this location is irrelevant.

3.5 NVRAM

The V7768/V7769 provide 32 KByte of non-volatile RAM. This memory is mapped in 32K of address space starting at the address in BAR1. This memory is available at any time and supports byte, short word and long word accesses from the PCI bus. The contents of this memory are retained when the power to the board is removed.

3.6 VME Control

Table 3-13 shows the register definitions for the V7768/V7769 (offset from BAR0).

Table 3-13 Register Definitions Offset from BAR0

Register and Offset	Bit Name	Bit	Definition
VMECOMM	MEC_SEL	0	Master Big-Endian Enable bit 1=Big Endian, 0=Little Endian
Offset 0x00	SEC_SEL	1	Slave Big-Endian Enable bit 1=Big Endian, 0=Little Endian
	ABLE	2	Auxiliary BERR Logic Enable bit 1=Aux. BERR Enabled, 0=Aux. BERR Disabled
	BTO	3	Bus Error Timer Enabled 1=Enable, 0=Disabled
	BTOV [1:0]	5:4	Timeout Value 00 - 16 µs 01 - 64 µs 10 - 256 µs 11 - 1.00 ms
	BERRI	6	BERR Interrupt Enable 1=Interrupt Enabled, 0=Interrupt Disabled
	BERRST	7	BERR Status Read/Clear bit R/WC 1=Clear BERR status, 0=Do nothing
	SFENA	8	Enables generation of VME SYSFAIL upon WDT timeout 1=Enable SYSFAIL generation, 0=Disable
	Unused	9	Not Used
	BPENA	10	Endian Conversion Bypass bit 1=bypass, 0=Not bypassed
	VBENA	11	VME Enable bit (VBENA) 1=Enabled, 0=Disabled
	Unused	21:12	Not Used
VBAM 0x04	VME_ADD	5:0	Latched VME Address Modifier
	Unused	31:6	Not Used
	SEC_SEL	0x001	
VBAR 0x08	VME_ADDR	All	Latched VME Address

Please refer to Table 3-1, “PCI Configuration Space Registers,” on page 46 for more information concerning BAR0.

3.7 CompactFlash Disk (V7768 Only)

The V7768 features an optional onboard CompactFlash mass storage system with a capacity of up to 8 GByte. This CompactFlash Disk appears to the user as an intelligent ATA (IDE) disk drive with the same functionality and capabilities as a “rotating media” IDE hard drive. The V7768 BIOS includes an option to allow the board to boot from the CompactFlash with user-provided operating system.

3.7.1 Configuration

The CompactFlash Disk resides on the V7768 as the secondary IDE bus master device (the secondary IDE bus slave device is not assignable).

3.8 Remote Ethernet Booting

The V7768/V7769 is capable of booting from a server using Gigabit Ethernet over a network utilizing the Boot ROM BIOS. The BIOS gives you the ability to remotely boot the V7768/V7769 using a PXE network protocol. The Ethernet must be connected through the GbE front panel (RJ45) connector to boot remotely. This feature allows users to create systems without the worry of disk drive reliability or the extra cost of adding CompactFlash drives.

3.8.1 Boot BIOS Features

- PXE boot support
- Detailed boot configuration screens
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

Maintenance

If a GE product malfunctions, please verify the following:

1. Software version resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return from Customer Care.**

GE Customer Care is available at: 1-800-433-2682 in North America, or +1-780-401-7700 for international calls. Or, visit our website at:

www.ge-ip.com

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

Compliance

This chapter provides the applicable information regarding regulatory compliance for the V7768/V7769.

GE's V7768/V7769 have been evaluated and has met the requirements for compliance to the following standards:

International Compliance

- EN55022:1998/CISPR 22:1997
- IEC61000-4-2
- IEC61000-4-3
- IEC61000-4-4
- IEC61000-4-5
- IEC61000-4-6

European Union (CE Mark)

- BS EN55024 (1998 w A1:01 & A2:03)
- BS EN55022 (Class A)

United States

- FCC Part 15, Subpart B, Section 109, Class A

Australia/New Zealand

- AS/NZS CISPR 22 (2002) Class A

Canada

- ICES-003 Class A

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class A



NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.



NOTE

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canadian Regulations

The V7768/V7769 Class A digital apparatus comply with Canadian ICES-003.



NOTE

Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfies ICES-003.

A • Appendix A: Connector Pinouts

The V7768/V7769 have several connectors for their I/O ports. Wherever possible, the V7768/V7769 use connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Figure A-1 shows the layout of the connectors on the V7768.

Figure A-1 V7768 Connector Layout

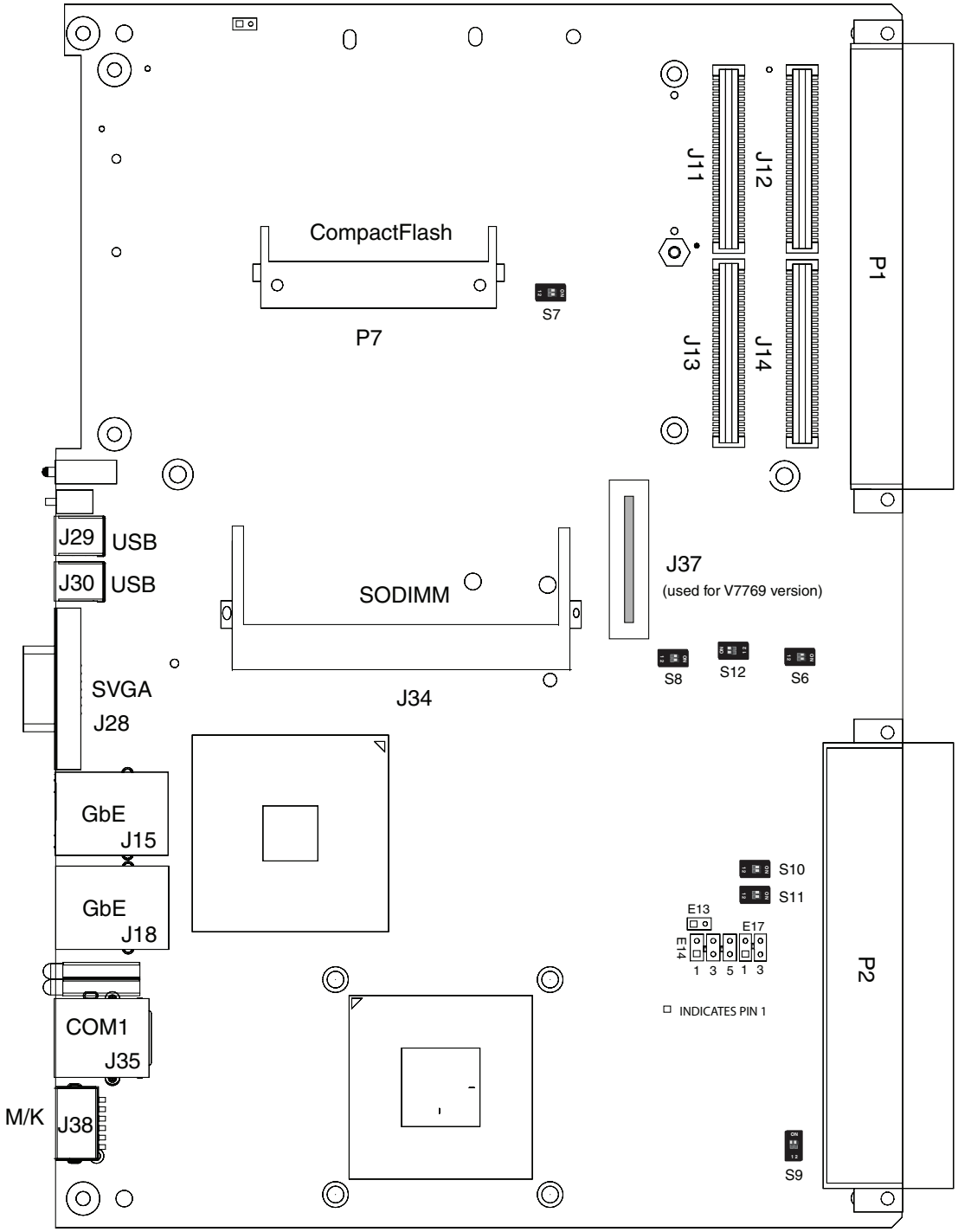
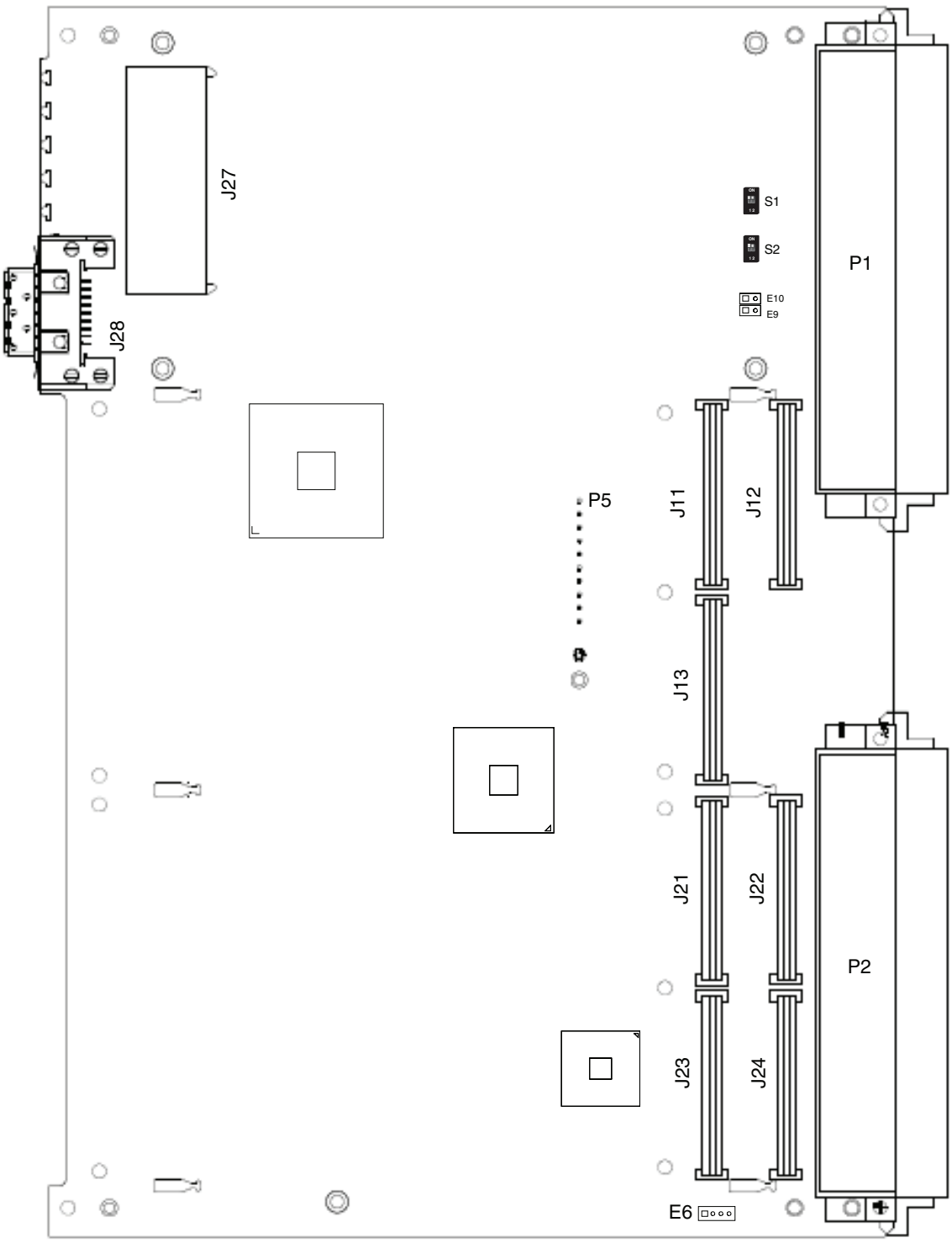


Figure A-2 V7769 Connector Pinout



A.1 V7768 VME Connectors and Pinouts (P1 and P2)

Figure A-3 shows the orientation of the P1 and P2 connectors on the V7768. Table A-1 shows the pinout for the VME P1 and P2 connectors.

Figure A-3 VME Connectors (P1/P2)

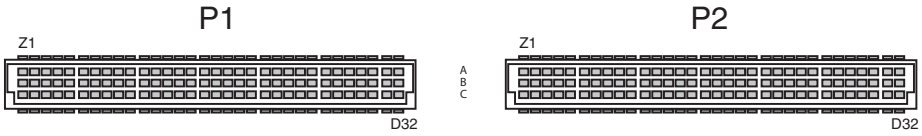


Table A-1 V7768 VME Connector Pinout (P1)

Pin No.	Row A	Row B	Row C	Row D	Row Z
1	D00	BBSY#	D08	+5 V	N/C
2	D01	BCLR#	D09	GND	GND
3	D02	ACFAIL#	D10	N/C	N/C
4	D03	BG0IN#	D11	N/C#	GND
5	D04	BG0OUT#	D12	N/C	N/C
6	D05	BG1IN#	D13	N/C	GND
7	D06	BG1OUT#	D14	N/C	N/C
8	D07	BG2IN#	D15	N/C	GND
9	GND	BG2OUT#	GND	VME_GA[5]#	N/C
10	SYSCLK	BG3IN#	SYSFAIL#	VME_GA[0]#	GND
11	GND	BG3OUT#	BERR#	VME_GA[1]#	N/C
12	DS1#	BR0#	SYSRESET#	N/C	GND
13	DS0#	BR1#	LWORD#	VME_GA[2]#	N/C
14	WRITE#	BR2#	AM5	N/C	GND
15	GND	BR3#	A23	VME_GA[3]#	N/C
16	DTACK#	AM0	A22	N/C	GND
17	GND	AM1	A21	VME_GA[4]#	N/C
18	AS#	AM2	A20	N/C	GND
19	GND	AM3	A19	N/C	N/C
20	IACK#	GND	A18	N/C	GND
21	IACKIN#	N/C	A17	N/C	N/C
22	IACKOUT#	N/C	A16	N/C	GND
23	AM4	GND	A15	N/C	N/C
24	A07	IRQ7#	A14	N/C	GND
25	A06	IRQ6#	A13	N/C	N/C
26	A05	IRQ5#	A12	N/C	GND
27	A04	IRQ4#	A11	N/C	N/C
28	A03	IRQ3#	A10	N/C	GND
29	A02	IRQ2#	A09	N/C	N/C
30	A01	IRQ1#	A08	N/C	GND
31	-12 V	N/C	+12 v	GND	N/C
32	+5 V	+5 V	+5 V	+5 V	GND

N/C indicates No Connection

Table A-2 V7768 VME Connector Pinout (P2)

Pin No.	Row A	Row B	Row C	Row D	Row Z
1	GND	+5V	SP1_TX	CONN[1]	CONN[2]
2	USB_P5N	GND	SP1_RTS#	CONN[3]	GND
3	USB_P5P	N/C	SP1_DTR#	CONN[4]	CONN[5]
4	USB_OC5#	A24	SP1_RX	CONN[6]	GND
5	GND	A25	SP1_DCD#	CONN[7]	CONN[8]
6	USB_P4N	A26	SP1_CTS#	CONN[9]	GND
7	USB_P4P	A27	SP1_DSR#	CONN[10]	CONN[11]
8	USB_OC4#	A28	SP1_RI#	CONN[12]	GND
9	GND	A29	RTM_SCONF_GP	CONN[13]	CONN[14]
10	USB_P3P	A30	VCC_5.0	CONN[15]	GND
11	USB_P3N	A31	-12 V	CONN[16]	CONN[17]
12	USB_OC3#	GND	GND	CONN[18]	GND
13	GND	+5 V	SATA1_RXN	CONN[19]	CONN[20]
14	USB_P2N	D16	SATA1_RXP	CONN[21]	GND
15	USB_P2P	D17	GND	CONN[22]	CONN[23]
16	USB_OC2#	D18	SATA1_TXN	CONN[24]	GND
17	GND	D19	SATA1_TXP	CONN[25]	CONN[26]
18	+5 V	D20	GND	CONN[27]	GND
19	+12 V	D21	GND	CONN[28]	CONN[29]
20	GND	D22	SATA2_RXN	CONN[30]	GND
21	N/C	D23	SATA2_RXP	CONN[31]	CONN[32]
22	N/C	GND	GND	CONN[33]	GND
23	GND	D24	SATA2_TXN	CONN[34]	CONN[35]
24	N/C	D25	SATA2_TXP	CONN[36]	GND
25	N/C	D26	GND	CONN[37]	CONN[38]
26	GND	D27	GND	CONN[39]	GND
27	N/C	D28	GND	CONN[40]	CONN[41]
28	N/C	D29	GND	CONN[42]	GND
29	GND	D30	N/C	CONN[43]	CONN[44]
30	N/C	D31	N/C	CONN[45]	GND
31	N/C	GND	N/C	GND	CONN[46]
32	GND	+5 V	N/C	+5 V	GND

N/C indicates No Connection

A.2 V7768 PCI-X PMC Connectors

A.2.1 V7768 PCI-X PMC Site Connector and Pinout (J11)

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-3 through A-5 show the pinouts for the PMC site connectors.

Figure A-4 V7768 PCI-X PMC Site Connector (J11)

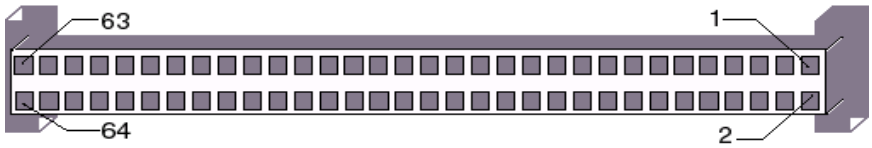


Table A-3 V7768 PCI-X PMC Site Connector Pinout (J11)

PMC Connector (J11)				PMC Connector (J11)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG_TCK_2	2	VCC_-12	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	RDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	VCC_5.0
7	BMODE1#	8	VCC_5.0	39	PCIXCAP	40	LOCK#
9	INTD#	10	N/C	41	SDONE#	42	PMC_SB0#
11	GND	12	N/C	43	PAR	44	GND
13	CLK	14	GND	45	VCC_3.3	46	AD[15]
15	GND	16	GNT0#	47	AD[12]	48	AD[11]
17	REQ0#	18	VCC_5.0	49	AD[9]	50	VCC_5.0
19	VCC_3.3	20	AD[31]	51	GND	52	CBE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	CBE[3]#	57	VCC_3.3	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	VCC_5.0	61	AD[0]	62	VCC_5.0
31	VCC_3.3	32	AD[17]	63	GND	64	REQ64#

N/C indicates No Connection

A.2.2 V7768 PCI-X PMC Site Connector and Pinout (J12)

Figure A-5 V7768 PCI-X PMC Site Connector (J12)

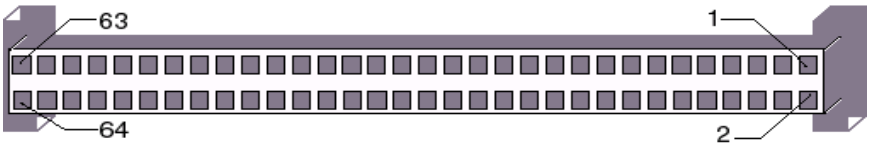


Table A-4 V7768 PCI-X PMC Site Connector Pinout (J12)

PMC Connector (J12)				PMC Connector (J12)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VCC_12.0	2	JTAG_TRST#	33	GND	34	N/C
3	JTAG_TMS_2	4	JTAG_TDO	35	TRDY#	36	VCC_3.3
5	JTAG_TDI	6	GND	37	GND	38	STOP#
7	GND	8	N/C	39	PERR#	40	GND
9	N/C	10	N/C	41	VCC_3.3	42	SERR#
11	BMODE2#	12	VCC_3.3	43	CBE[1]#	44	GND
13	PCIB_RESET#	14	BMODE3#	45	AD[14]	46	AD[13]
15	VCC_3.3	16	BMODE4#	47	M66EN	48	AD[10]
17	N/C	18	GND	49	AD[8]	50	VCC_3.3
19	AD[30]	20	AD[29]	51	AD[7]	52	N/C
21	GND	22	AD[26]	53	VCC_3.3	54	N/C
23	AD[24]	24	VCC_3.3	55	N/C	56	GND
25	PMC_IDSEL	26	AD[23]	57	N/C	58	N/C
27	VCC_3.3	28	AD[20]	59	GND	60	N/C
29	AD[18]	30	GND	61	ACK64#	62	VCC_3.3
31	AD16]	32	CBE[2]#	63	GND	64	N/C

N/C indicates No Connection

A.2.3 V7768 PCI-X PMC Site Connector and Pinout (J13)

Figure A-6 V7768 PCI-X PMC Site Connector (J13)

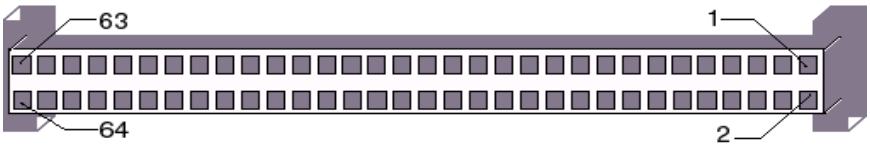


Table A-5 V7768 PCI-X PMC Site Connector Pinout (J13)

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]#	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	VCC_3.3	40	AD[44]
9	VCC_3.3	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	VCC_3.3	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	VCC_3.3	58	AD[32]
27	GND	28	AD[52]	59	N/C	60	N/C
29	AD[51]	30	AD[50]	61	N/C	62	GND
31	AD[49]	32	GND	63	GND	64	N/C

N/C indicates No Connection

A.2.4 Mezzanine PCI-X PMC Site Connector and Pinout (J14)

Figure A-7 Mezzanine PCI-X PMC Site Connector (J14)

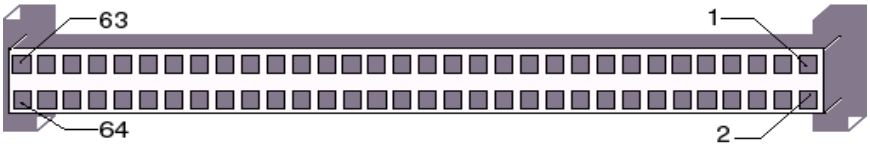


Table A-6 Mezzanine PCI-X PMC Site Connector Pinout (J14)

PMC Connector (J14)				PMC Connector (J14)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CONN(1)	2	CONN(2)	33	CONN(33)	34	CONN(34)
3	CONN(3)	4	CONN(4)	35	CONN(35)	36	CONN(36)
5	CONN(5)	6	CONN(6)	37	CONN(37)	38	CONN(38)
7	CONN(7)	8	CONN(8)	39	CONN(39)	40	CONN(40)
9	CONN(9)	10	CONN(10)	41	CONN(41)	42	CONN(42)
11	CONN(11)	12	CONN(12)	43	CONN(43)	44	CONN(44)
13	CONN(13)	14	CONN(14)	45	CONN(45)	46	CONN(46)
15	CONN(15)	16	CONN(16)	47	N/C	48	N/C
17	CONN(17)	18	CONN(18)	49	N/C	50	N/C
19	CONN(19)	20	CONN(20)	51	N/C	52	N/C
21	CONN(21)	22	CONN(22)	53	N/C	54	N/C
23	CONN(23)	24	CONN(24)	55	N/C	56	N/C
25	CONN(25)	26	CONN(26)	57	N/C	58	N/C
27	CONN(27)	28	CONN(28)	59	N/C	60	N/C
29	CONN(29)	30	CONN(30)	61	N/C	62	N/C
31	CONN(31)	32	CONN(32)	63	N/C	64	N/C

N/C indicates No Connection

A.3 V7769 Mezzanine Backplane Connectors (P1 and P2)

Figure A-8 V7769 Backplane Connectors (P1 and P2)

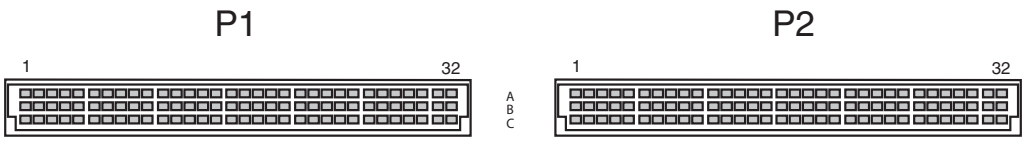


Table A-7 V7769 Backplane Connector Pinouts (P1 and P2)

Pin No.	P1 Row A Signal	P1 Row B Signal	P1 Row C Signal	P2 Row A Signal	P2 Row B Signal	P2 Row C Signal
1	N/C	N/C	N/C	N/C	+5 V	N/C
2	N/C	N/C	N/C	N/C	GND	N/C
3	N/C	N/C	N/C	N/C	N/C	N/C
4	N/C	BG0IN#	N/C	N/C	N/C	N/C
5	N/C	BG0OUT#	N/C	N/C	N/C	N/C
6	N/C	BG1IN#	N/C	N/C	N/C	N/C
7	N/C	BG1OUT#	N/C	N/C	N/C	N/C
8	N/C	BG2IN#	N/C	N/C	N/C	N/C
9	GND	BG2OUT#	GND	N/C	N/C	N/C
10	N/C	BG3IN#	N/C	N/C	N/C	N/C
11	GND	BG3OUT#	N/C	N/C	N/C	N/C
12	N/C	N/C	N/C	N/C	GND	N/C
13	N/C	N/C	N/C	N/C	+5 V	N/C
14	N/C	N/C	N/C	N/C	N/C	N/C
15	GND	N/C	N/C	N/C	N/C	N/C
16	N/C	N/C	N/C	N/C	N/C	N/C
17	GND	N/C	N/C	N/C	N/C	N/C
18	N/C	N/C	N/C	N/C	N/C	N/C
19	GND	N/C	N/C	N/C	N/C	N/C
20	N/C	GND	N/C	N/C	N/C	N/C
21	IACKIN#	N/C	N/C	N/C	N/C	N/C
22	IACKOUT#	N/C	N/C	N/C	GND	N/C
23	N/C	GND	N/C	N/C	N/C	N/C
24	N/C	N/C	N/C	N/C	N/C	N/C
25	N/C	N/C	N/C	N/C	N/C	N/C
26	N/C	N/C	N/C	N/C	N/C	N/C
27	N/C	N/C	N/C	N/C	N/C	N/C
28	N/C	N/C	N/C	N/C	N/C	N/C
29	N/C	N/C	N/C	N/C	N/C	N/C
30	N/C	N/C	N/C	N/C	N/C	N/C
31	-12 V	N/C	+12 V	N/C	GND	N/C
32	+5 V	+5 V	+5 V	N/C	+5 V	N/C

N/C indicates No Connection

A.4 V7769 Mezzanine PCI-X PMC Site 1 Connectors

A.4.1 Mezzanine PCI-X PMC Site 1 Connector and Pinout (J11)

The PMC carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-8 through A-10 show the pinouts for the PMC site connectors.

Figure A-9 Mezzanine PCI-X PMC Site Connector (J11)

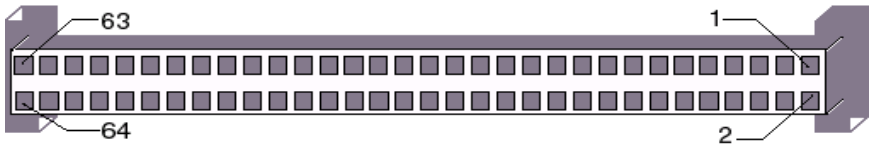


Table A-8 Mezzanine PMC Site Connector Pinout (J11)

PMC Connector (J11)				PMC Connector (J11)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG_TCK_2	2	VCC_-12	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	RDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	VCC_5.0
7	BMODE1#	8	VCC_5.0	39	PCIXCAP	40	LOCK#
9	INTD#	10	N/C	41	SDONE#	42	PMC_SB0#
11	GND	12	N/C	43	PAR	44	GND
13	CLK	14	GND	45	VCC_3.3	46	AD[15]
15	GND	16	GNT0#	47	AD[12]	48	AD[11]
17	REQ0#	18	VCC_5.0	49	AD[9]	50	VCC_5.0
19	VCC_3.3	20	AD[31]	51	GND	52	CBE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	CBE[3]#	57	VCC_3.3	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	VCC_5.0	61	AD[0]	62	VCC_5.0
31	VCC_3.3	32	AD[17]	63	GND	64	REQ64#

N/C indicates No Connection

A.4.2 Mezzanine PCI-X PMC Site 1 Connector and Pinout (J12)

Figure A-10 Mezzanine PCI-X PMC Site Connector (J12)

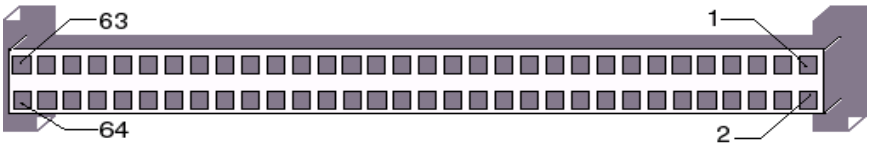


Table A-9 Mezzanine PCI-X PMC Site Connector Pinout (J12)

PMC Connector (J12)				PMC Connector (J12)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VCC_12.0	2	JTAG_TRST#	33	GND	34	N/C
3	JTAG_TMS_2	4	JTAG_TDO	35	TRDY#	36	VCC_3.3
5	JTAG_TDI	6	GND	37	GND	38	STOP#
7	GND	8	N/C	39	PERR#	40	GND
9	N/C	10	N/C	41	VCC_3.3	42	SERR#
11	BMODE2#	12	VCC_3.3	43	CBE[1]#	44	GND
13	PCIB_RESET#	14	BMODE3#	45	AD[14]	46	AD[13]
15	VCC_3.3	16	BMODE4#	47	M66EN	48	AD[10]
17	N/C	18	GND	49	AD[8]	50	VCC_3.3
19	AD[30]	20	AD[29]	51	AD[7]	52	N/C
21	GND	22	AD[26]	53	VCC_3.3	54	N/C
23	AD[24]	24	VCC_3.3	55	N/C	56	GND
25	PMC_IDSEL	26	AD[23]	57	N/C	58	N/C
27	VCC_3.3	28	AD[20]	59	GND	60	N/C
29	AD[18]	30	GND	61	ACK64#	62	VCC_3.3
31	AD16]	32	CBE[2]#	63	GND	64	N/C

N/C indicates No Connection

A.4.3 Mezzanine PCI-X PMC Site 1 Connector and Pinout (J13)

Figure A-11 Mezzanine PCI-X PMC Site Connector (J13)

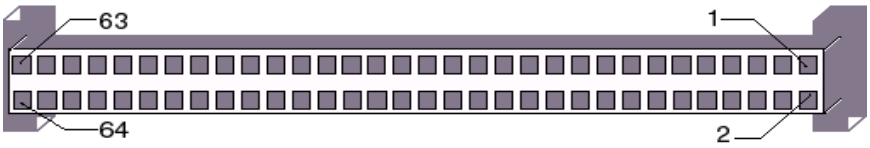


Table A-10 Mezzanine PCI-X PMC Site Connector Pinout (J13)

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]#	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	VCC_3.3	40	AD[44]
9	VCC_3.3	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	VCC_3.3	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	VCC_3.3	58	AD[32]
27	GND	28	AD[52]	59	N/C	60	N/C
29	AD[51]	30	AD[50]	61	N/C	62	GND
31	AD[49]	32	GND	63	GND	64	N/C

N/C indicates No Connection

A.5 V7769 Mezzanine PCI-X PMC Site 2 Connectors

A.5.1 Mezzanine PCI-X PMC Site 2 Connector and Pinout (J21)

The PMC carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-11 through A-14 show the pinouts for the PMC site connectors.

Figure A-12 Mezzanine PCI-X PMC Site Connector (J21)

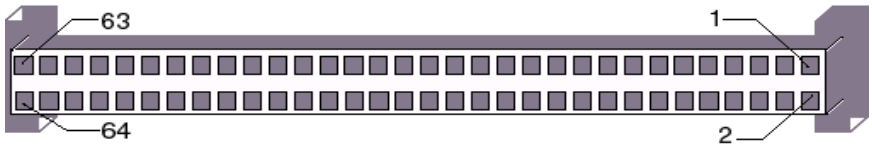


Table A-11 Mezzanine PMC Site Connector Pinout (J21)

PMC Connector (J21)				PMC Connector (J21)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	JTAG_TCK_2	2	VCC_-12	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	RDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	VCC_5.0
7	BMODE1#	8	VCC_5.0	39	PCIXCAP	40	LOCK#
9	INTD#	10	N/C	41	SDONE#	42	PMC_SB0#
11	GND	12	N/C	43	PAR	44	GND
13	CLK	14	GND	45	VCC_3.3	46	AD[15]
15	GND	16	GNT0#	47	AD[12]	48	AD[11]
17	REQ0#	18	VCC_5.0	49	AD[9]	50	VCC_5.0
19	VCC_3.3	20	AD[31]	51	GND	52	CBE[0]#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	CBE[3]#	57	VCC_3.3	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	VCC_5.0	61	AD[0]	62	VCC_5.0
31	VCC_3.3	32	AD[17]	63	GND	64	REQ64#

N/C indicates No Connection

A.5.2 Mezzanine PCI-X PMC Site 2 Connector and Pinout (J22)

Figure A-13 Mezzanine PCI-X PMC Site Connector (J22)

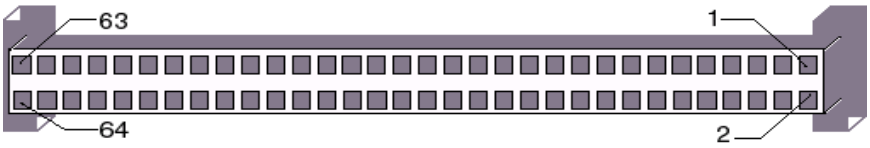


Table A-12 Mezzanine PCI-X PMC Site Connector Pinout (J22)

PMC Connector (J22)				PMC Connector (J22)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VCC_12.0	2	JTAG_TRST#	33	GND	34	N/C
3	JTAG_TMS_2	4	JTAG_TDO	35	TRDY#	36	VCC_3.3
5	JTAG_TDI	6	GND	37	GND	38	STOP#
7	GND	8	N/C	39	PERR#	40	GND
9	N/C	10	N/C	41	VCC_3.3	42	SERR#
11	BMODE2#	12	VCC_3.3	43	CBE[1]#	44	GND
13	PCIB_RESET#	14	BMODE3#	45	AD[14]	46	AD[13]
15	VCC_3.3	16	BMODE4#	47	M66EN	48	AD[10]
17	N/C	18	GND	49	AD[8]	50	VCC_3.3
19	AD[30]	20	AD[29]	51	AD[7]	52	N/C
21	GND	22	AD[26]	53	VCC_3.3	54	N/C
23	AD[24]	24	VCC_3.3	55	N/C	56	GND
25	PMC_IDSEL	26	AD[23]	57	N/C	58	N/C
27	VCC_3.3	28	AD[20]	59	GND	60	N/C
29	AD[18]	30	GND	61	ACK64#	62	VCC_3.3
31	AD16]	32	CBE[2]#	63	GND	64	N/C

N/C indicates No Connection

A.5.3 Mezzanine PCI-X PMC Site 2 Connector and Pinout (J23)

Figure A-14 Mezzanine PCI-X PMC Site Connector (J23)

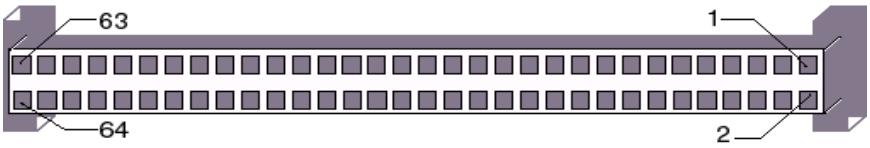


Table A-13 Mezzanine PCI-X PMC Site Connector Pinout (J23)

PMC Connector (J23)				PMC Connector (J23)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	AD[48]
3	GND	4	CBE[7]#	35	AD[47]	36	AD[46]
5	CBE[6]#	6	CBE[5]#	37	AD[45]	38	GND
7	CBE[4]#	8	GND	39	VCC_3.3	40	AD[44]
9	VCC_3.3	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	VCC_3.3	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	VCC_3.3	58	AD[32]
27	GND	28	AD[52]	59	N/C	60	N/C
29	AD[51]	30	AD[50]	61	N/C	62	GND
31	AD[49]	32	GND	63	GND	64	N/C

N/C indicates No Connection

A.5.4 Mezzanine PCI-X PMC Site 2 Connector and Pinout (J24)

Figure A-15 Mezzanine PCI-X PMC Site Connector (J24)

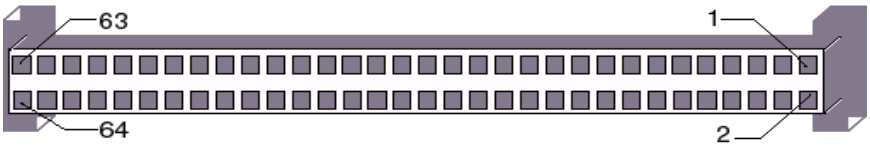


Table A-14 Mezzanine PCI-X PMC Site Connector Pinout (J24)

PMC Connector (J24)				PMC Connector (J24)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	CONN[1]	2	CONN[2]	33	CONN[33]	34	CONN[34]
3	CONN[3]	4	CONN[4]	35	CONN[35]	36	CONN[36]
5	CONN[5]	6	CONN[6]	37	CONN[37]	38	CONN[38]
7	CONN[7]	8	CONN[8]	39	CONN[39]	40	CONN[40]
9	CONN[9]	10	CONN[10]	41	CONN[41]	42	CONN[42]
11	CONN[11]	12	CONN[12]	43	CONN[43]	44	CONN[44]
13	CONN[13]	14	CONN[14]	45	CONN[45]	46	CONN[46]
15	CONN[15]	16	CONN[16]	47	N/C	48	N/C
17	CONN[17]	18	CONN[18]	49	N/C	50	N/C
19	CONN[19]	20	CONN[20]	51	N/C	52	N/C
21	CONN[21]	22	CONN[22]	53	N/C	54	N/C
23	CONN[23]	24	CONN[24]	55	N/C	56	N/C
25	CONN[25]	26	CONN[26]	57	N/C	58	N/C
27	CONN[27]	28	CONN[28]	59	N/C	60	N/C
29	CONN[29]	30	CONN[30]	61	N/C	62	N/C
31	CONN[31]	32	CONN[32]	63	N/C	64	N/C

N/C indicates No Connection

A.6 USB Connectors and Pinout (J29 and J30)

The two USB ports are industry standard 4-position shielded connectors. Figure A-16 shows a representation of the connectors, and Table A-15 shows the pinout (same for each).

Figure A-16 USB Connector (J29 and J30)

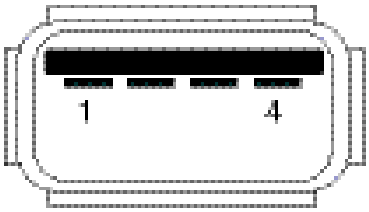


Table A-15 USB Connector Pinout (J29 and J30)

Pin	Signal	Function
1	USB_VCC	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

A.7 Gigabit Ethernet Connectors and Pinouts (J15 and J18)

The pinout diagram for the Gigabit Ethernet connector and pinout are shown in Figure A-17 and Table A-16.

Figure A-17 Gigabit Ethernet Connector (J18)

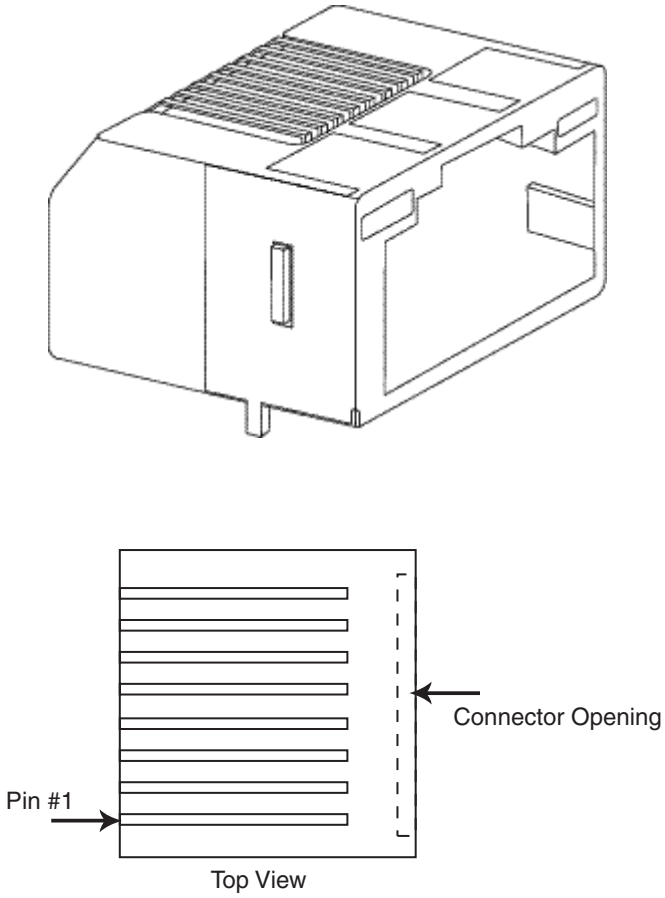


Table A-16 Gigabit Ethernet Connector Pinout (J18)

Pin	Signal	Function
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	TX_CT_OUT	Transmit Center Tap Out
5	TX_CT_OUT	Transmit Center Tap Out
6	RD-	Receive Data
7	RX_CT_OUT	Receive Center Tap Out
8	RX_CT_OUT	Receive Center Tap Out

A.8 Video Graphics Adapter and Pinout (J28)

The video port uses a standard high-density DB15 SVGA connector. Figure A-18 illustrates the pinout and Table A-17 gives a description.

Figure A-18 SVGA Connector (J28)

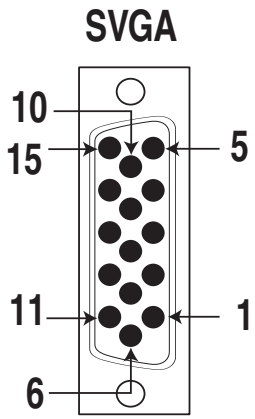


Table A-17 SVGA Connector Pinout (J28)

Pin	Signal
1	VGA_Video1_Red
2	VGA_Video1_Green
3	VGA_Video1_Blue
4	N/C
5	GND
6	GND
7	GND
8	GND
9	VCC_5.0
10	GND
11	N/C
12	VGA_DDC_Data
13	VGA_HSYNC
14	VGA_VSYNC
15	VGA_DDC_CLK

N/C indicates No Connection

A.9 Serial Connector and Pinout (J35)

COM 1 serial port connector is a standard RJ45 connector as shown in Figure A-19 and its pinout in Table A-18.

Figure A-19 Serial Connector (J35)

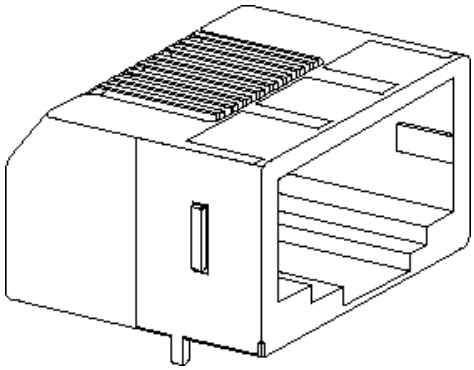


Table A-18 Serial Connector Pinout (J35)

Pin	RS232 Signal	RS422 Signal
1	DCD	RXD-
2	RTS	RTS+
3	GND	TXD-
4	TXD	TXD
5	RXD	RXD
6	GND	GND
7	CTS	CTS
8	DTR	DTR

A.10 Mouse/Keyboard Connector and Pinout (J38)

The mouse/keyboard connector is a standard 6-pin female mini-DIN PS/2 connector as shown in Figure A-20. The mouse/keyboard connector uses a “Y” splitter cable to separate the mouse and keyboard signals. The “Y” splitter cable is shown in Figure A-21, the pinout is shown in Table A-19.

Figure A-20 Mouse/Keyboard Connector (J38)

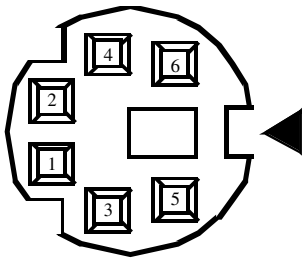


Table A-19 Mouse/Keyboard Connector Pinout (J38)

Pin	Direction	Function
1	In/Out	Mouse Data
	In/Out	Keyboard Data
3		Ground
4		+5 V
5	Out	Mouse Clock
6	Out	Keyboard Clock
Shield		Chassis Ground

An adapter cable is included with the V7768/V7769 to separate the keyboard and mouse connectors.

Figure A-21 Mouse/Keyboard Splitter Cable

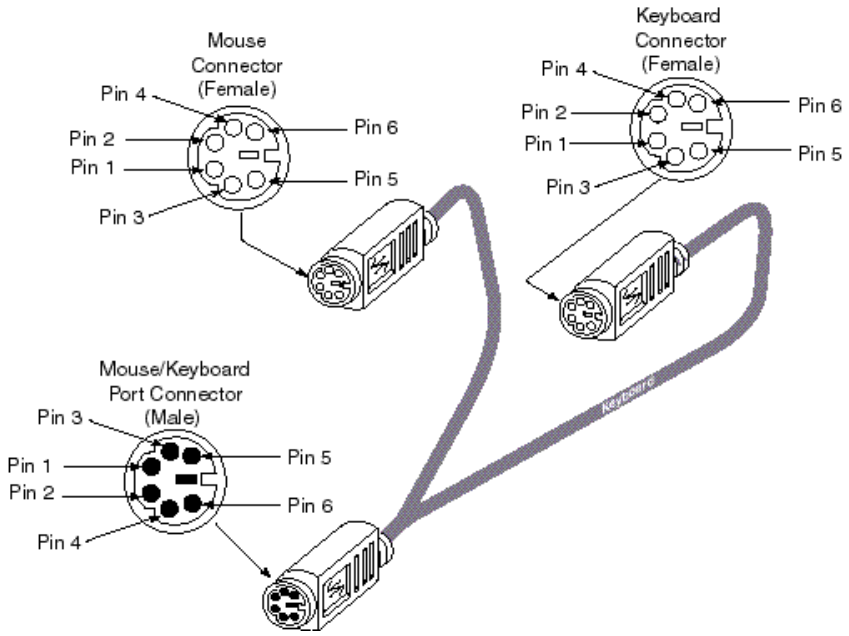


Table A-20 Mouse/Keyboard Splitter Cable Pinout

Keyboard			Mouse		
Pin	Direction	Function	Pin	Direction	Function
1	In/Out	Keyboard Data	1	In/Out	Mouse Data
2		Unused	2		Unused
3		Ground	3		Ground
4		+5 V	4		+5 V
5	Out	Keyboard Clock	5	Out	Mouse Clock
6		Unused	6		Unused
Shield		Chassis Ground	Shield		Chassis Ground

NOTE

The mouse/keyboard pinout shown in Table A-20 has pins 2 (Keyboard Data) and 6 (Keyboard Clock) signals on the Mouse cable. This may not work with some keyboard and mouse devices. We recommend that you contact Customer Service for more information.

A.11 V7769 Mezzanine SAS Connector and Pinout (J28)

Figure A-22 Mezzanine Connector (J28)

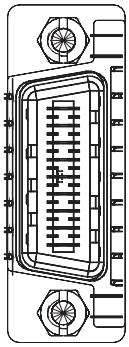


Table A-21 Mezzanine SAS Connector Pinout (J28)

Pin	Direction
S1	RX[0]+
S2	RX[0]-
S3	RX[1]+
S4	RX[1]-
S13	TX[1]-
S14	TX[1]+
S15	TX[0]-
S16	TX[0]+
G1-G9	GND

All pins not listed are not connected.

B • Appendix B: AMI BIOS Setup Utility

This appendix gives a brief description of the setup options in the system BIOS. Due to the custom nature of GE's SBCs, your BIOS options may vary from the options discussed in this appendix.

AMI refers to their BIOS setup screens as ezPORT. For a complete description of all the options available with the AMI BIOS, please visit www.ami.com and download their ezPORT PDF file. The options listed on AMI's web site may not be available on your system.

To Access the First Boot pop up screen press the F11 key at the beginning of boot.

To access the ezPORT setup screens, press the DEL key at the beginning of boot.

B.1 First Boot Menu

The V7768/V7769 have a First Boot pop up menu enabling the user to, *on a one time basis*, select a drive device to boot from. This feature is useful when installing from a bootable disk. For example, when installing an operating system from a CD, enter the First Boot menu and use the arrows keys to highlight ATAPI CD-ROM Drive. Press ENTER to continue with system boot.

This feature is accessed by pressing the F11 key at the very beginning of the boot cycle. The selection made from this screen applies to the current boot only, and will not be used during the next boot-up of the system. If you have trouble accessing this feature, disable the QuickBoot Mode in the Main BIOS setup screen. Exit, saving changes and retry accessing the First Boot menu.

Table B-1 AMI BIOS First Boot Menu

Boot Menu
1. + Removable Devices
2. + Hard Drive
3. ATAPI CD-ROM Drive
4. MBA UNDI (Bus 1 Slot 6) LAN 1

B.2 Main Menu

The Main BIOS setup menu screen has two main areas. The left frame displays all the options that can be configured. “Grayed-out” options cannot be configured. Options in blue can be configured. The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white and a text message in the right frame gives a brief description of the option.

The Main menu reports the BIOS revision, processor type and clock speed, and allows the user to set the system’s clock and calendar. Use the left and right arrow keys to select other screens.

Below is a sample of the Main screen. The information displayed on your screen will reflect your actual system.

Table B-2 AMI BIOS Main Menu

```
                              BIOS SETUP UTILITY
Main    Advanced    PCIPnP    Boot    Security    Chipset    Exit

System Overview                                  Use [Enter], [TAB]
                                                 Or [SHIFT-TAB] to
AMIBIOS                                          Select a field.
Version : 08.00.10
Build Date : 03/02/04                            Use [+] or [-] to
ID  : 07807_16                                   Configure system
                                                 Time.
Processor
Type  : Intel(R) Pentium (R) M processor 1600MH
Speed  : 1600MHz

System Memory
Size  : 1016MB

System Time     [11:39:40]                       ←→  Select Screen
System Date     [Tue 03/04/2004]                 ↑↓  Select Item
                                                 +-  Change Field
                                                 Tab Select Field
                                                 F1  General Help
                                                 F10 Save and Exit
                                                 ESC Exit
```

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B.3 Advanced BIOS Setup Menu

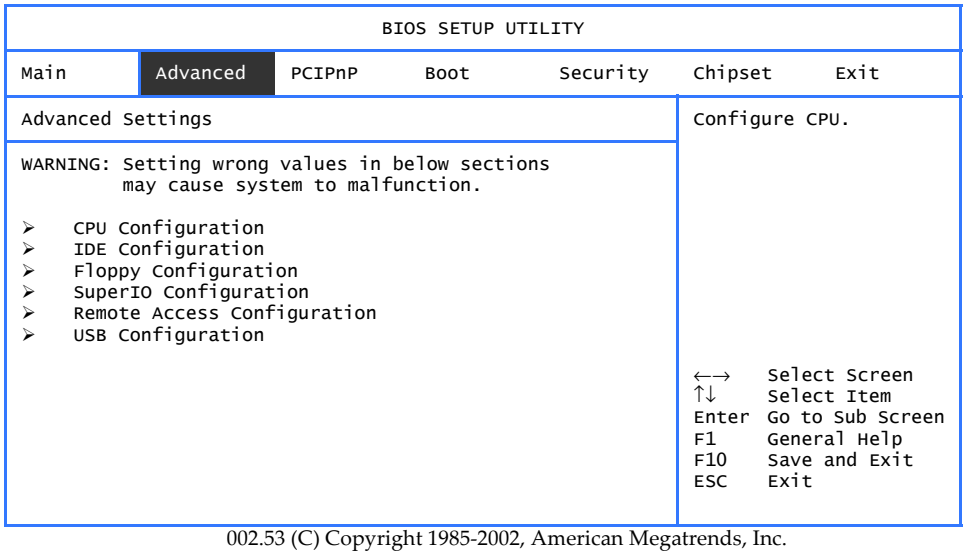
The Advanced BIOS Setup menu allows the user to configure some CPU settings, the IDE bus, other external devices and internal drives.

Select the *Advanced* tab from the ezPORT setup screen to enter the Advanced BIOS Setup screen. You can select the items in the left frame of the screen, such as Super I/O Configuration, to go to the sub menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. A sample of the Advanced BIOS Setup screen is shown below.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to *Chapter 1 "Installation and Setup"* for instructions on clearing the CMOS.

Table B-3 AMI BIOS Advanced Menu



Options shown may not be available on your system.

B.4 PCI/PnP Setup Menu

Included in this screen is the control of internal peripheral cards, as well as various interrupts. From this menu, the user can also determine if the system's plug-and-play is enabled or disabled.

NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to *Chapter 1 "Installation and Setup"* for instructions on clearing the CMOS.

Below is a sample screen of the PCI/PnP menu; options in your system may be different from those shown.

Table B-4 AMI BIOS PCI/PnP Menu

```
                                BIOS SETUP UTILITY
Main      Advanced    PCIPnP    Boot      Security    Chipset    Exit

Advanced PCI/PnP Settings                          NO: lets the BIOS
                                                   configure all the
WARNING: Setting wrong values in below sections    devices in the system.
         may cause system to malfunction.          YES: lets the
                                                   operating system
Plug & Play O/S                        [Yes]       configure Plug and
PCI Latency Timer                      [64]        Play (PnP) devices not
Allocate IRQ to PCI VGA                [Yes]       required for boot if
Palette Snooping                       [Disabled]  your system has a Plug
PCI IDE BusMaster                      [Disabled]  and Play operating
OffBoard PCI/ISA IDE Card              [Auto]      system.

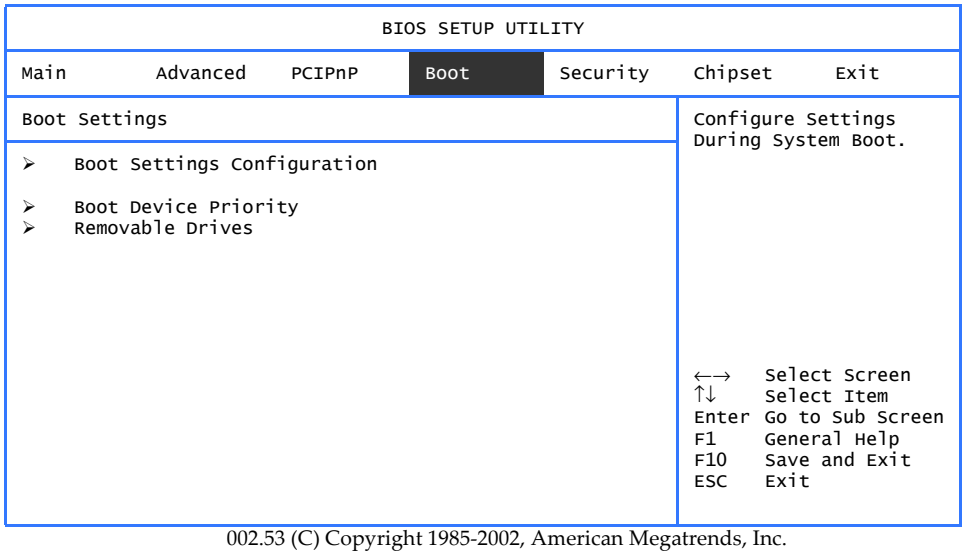

IRQ3                                   [Available]
IRQ4                                   [Available]
IRQ5                                   [Available]  ←→  Select Screen
IRQ7                                   [Available]  ↑↓  Select Item
IRQ9                                   [Available]  +-  Change Option
IRQ10                                  [Available]  F1  General Help
IRQ11                                  [Available]  F10 Save and Exit
IRQ14                                  [Available]  ESC Exit
```

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B.5 Boot Setup Menu

Use the Boot Setup menu to set the priority of the boot devices, including booting from a remote network. The devices shown in this menu are the bootable devices detected during POST. If a drive is installed that does not appear, verify the hardware installation. Also available in this screen are 'Boot Settings' which allow the user to set how the basic system will act, for example, support for PS/2 mouse and whether to use 'Quick Boot' or not.

Table B-5 AMI BIOS Boot Menu



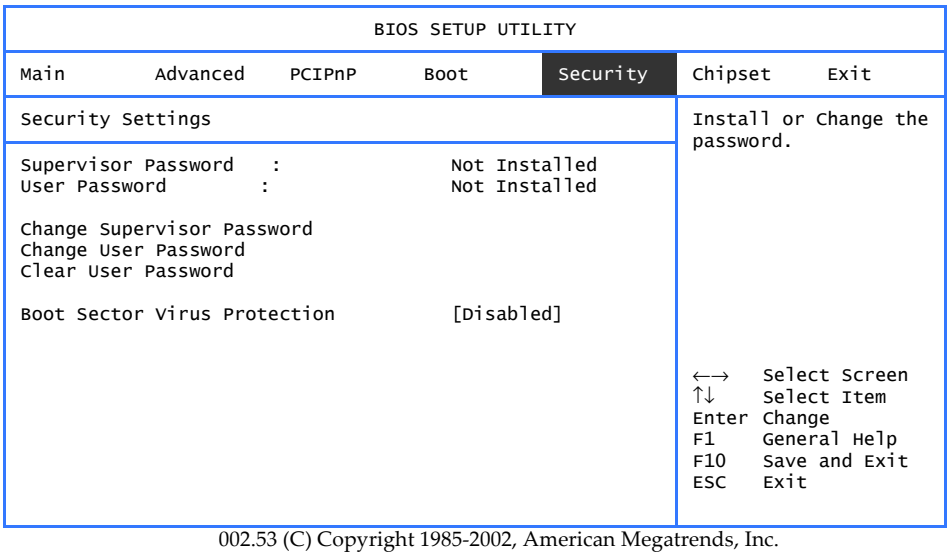
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B.6 Security Setup Menu

The ezPORT setup provides both a Supervisor and a User password. If you use both passwords, the Supervisor password must be set first.

The system can be configured so that all users must enter a password every time the system boots or when ezPORT setup is executed, using either the Supervisor password or User password.

Table B-6 AMI BIOS Security Menu



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To reset the security in the case of a forgotten password you must clear the NVRAM and reconfigure.

Refer to *Chapter 1 "Installation and Setup"* for how to clear the CMOS password.

B.7 Chipset Setup Menu

Select the various options for chipsets located in the system (for example, the CPU configuration and configurations for the North and South Bridge). The settings for the chipsets are processor dependent and care must be used when changing settings from the defaults set at the factory. Below is a sample of the Chipset Setup screen; the actual options on your system may vary.



NOTE

Changes in this screen can cause the system to malfunction. If problems are noted after changes have been made, reboot the system and access the BIOS. From the Exit menu select '`Load Failsafe Defaults`' and reboot the system. If the system failure prevents access to the BIOS screens, refer to *Chapter 1 "Installation and Setup"* for instructions on clearing the CMOS.

Table B-7 AMI BIOS Chipset Menu

```
                              BIOS SETUP UTILITY
Main      Advanced    PCIPnP    Boot      Security  Chipset   Exit

Advanced Chipset Settings                          Intel Montara GML
                                                   NorthBridge chipset
WARNING: Setting wrong values in below section     Configuration options.
         may cause system to malfunction.

➢  Intel Montara NorthBridge Configuration
➢  Hance Rapids SouthBridge Configuration
➢  CPCI (HINT HB6) Bridge Configuration
➢  Lan (8254EB) Port Routing Options

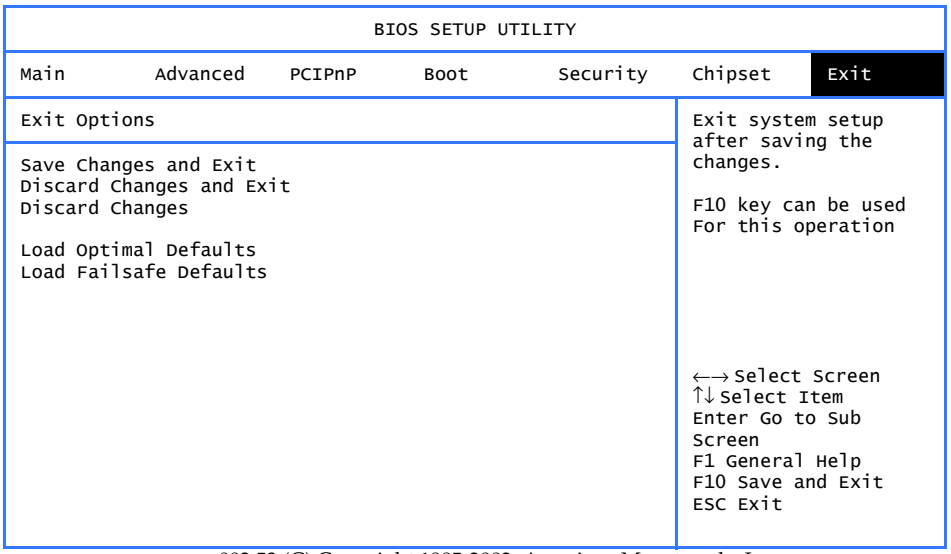
                                                   ←→   Select Screen
                                                   ↑↓   Select Item
                                                   Enter Go to Sub Screen
                                                   F1   General Help
                                                   F10  Save and Exit
                                                   ESC  Exit
```

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B.8 Exit Menu

Select the *Exit* tab from the ezPORT setup screen to enter the Exit BIOS Setup screen. You can display an Exit BIOS Setup option by highlighting it using the <Arrow> keys. The Exit BIOS Setup screen is shown below.

Table B-8 AMI BIOS Exit Menu



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If changes have previously been made in the BIOS and the system malfunctions, reboot the system and access this screen. Select 'Load Failsafe Defaults' and continue the reboot.

C • Appendix C: Remote Booting

The V7768/V7769 include a Boot-from-LAN BIOS option which allows the SBCs to be booted from a network. This appendix describes the procedures to enable this option and to select a LAN connection as the boot device.

NOTE

The options listed in this appendix may not be available on your system.

C.1 Enabling the Front Panel (FP) LAN

The LAN must be enabled in the Boot Setup Utility in order to perform a remote boot. The board will only remotely boot from the front panel LAN connection.

The *Chipset* menu of the BIOS Setup Utility allows the LAN to be enabled. Table C-1 shows the *Chipset* Menu. Use the arrow keys to highlight the *Onboard Devices Configuration*. Select *Onboard FP LAN* and enter <+> until the option is set to *Enabled*. Press F10 to Save and Exit the BIOS Setup Utility. This will allow the LAN to be a boot device.

Table C-1 Enable the Front Panel LAN for Remote Booting

BIOS SETUP UTILITY						
Main	Advanced	PCIPnP	Boot	Security		Exit
Advanced Chipset Settings					Intel Montara GML NorthBridge chipset Configuration options.	
WARNING: Setting wrong values in below section may cause system to malfunction. ➢ NorthBridge Configuration ➢ SouthBridge Configuration ➢ Onboard Devices Configuration					←→ Select Screen ↑↓ Select Item Enter Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit	

C.2 Boot Menus

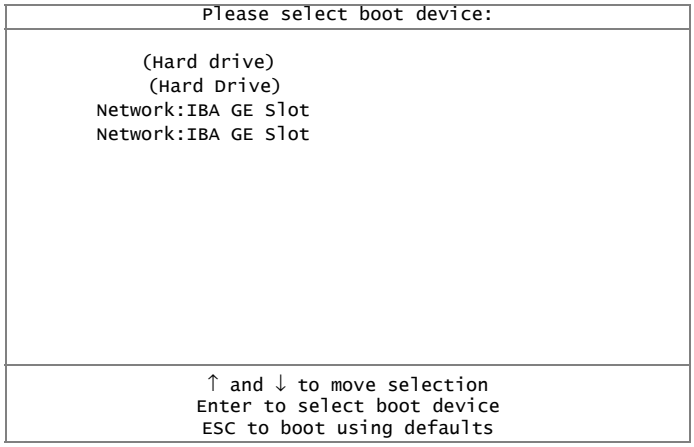
There are two methods of selecting the LAN as a boot device. The first method is the *First Boot* menu. The second is the *Boot* menu from the BIOS Setup Utility.

NOTE
The Front Panel (FP) LAN must be enabled in the BIOS Setup Utility before either method will work.

C.2.1 First Boot Menu

Press F11 at the very beginning of the boot cycle, which will access the *First Boot* menu. Selecting *Network:IBA GE Slot* to boot from the LAN in this screen applies to the current boot only. At the next reboot the V7768/V7769 will revert back to the setting in the Boot menu.

Table C-2 Boot-from-LAN BIOS First Boot Menu



Using the arrow keys, highlight *Network:IBA GE Slot*, and press ENTER key to continue with the system boot.

C.2.2 Boot Menu

The second method of selecting the Boot-from-LAN BIOS option is to press the DEL key during system boot. This will access the *BIOS Setup Utility*. Select the *Boot* menu, and then select the *Boot Device Priority* sub-menu. Use the arrow keys to highlight the *Network:IBA GE Slot* option. Repeat entering <+> until the desired network port is at the top of the list.

Advance to the *Exit* menu, select *Exit Saving Changes* and press ENTER. When the system prompts for confirmation, press *Yes*. The computer will then restart the system bootup. The system will boot from this connection until it is changed in the *BIOS Setup Utility*.

Table C-3 Boot-from-LAN BIOS Boot Menu

BIOS SETUP UTILITY		
	Boot	
Boot Device Priority		Specifies the boot sequence from the available devices.
1st Boot Device 2nd Boot Device 3rd Boot Device	[MBA UNDI (Bus2 Slot5)] [1st Floppy Drive] [Hard Drive]	←→ Select Screen ↑↓ Select Item +- Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

C.3 BIOS Features Setup

After the Intel Boot Agent has been enabled, the following information will appear at the top of the screen.

```
Initializing Intel (R) Boot Agent GE v1.2.40
PXE 2.1 Build 085 (WfM2.0)
Press Ctrl+S to enter Setup Menu...
```

Once you press CTRL-S, the Boot Agent setup menu will appear. PXE is the boot option available on the V7768/V7769. You can change the settings for the Setup Prompt and Setup Menu Wait Time. You can either enable or disable the prompt, and you can set the amount of wait time for the setup menu.

```
Network Boot Protocol    PXE (Preboot eXecution Environment)
Boot Order               Use BIOS Setup Boot Order
Show Setup Prompt        Enabled
Setup Menu Wait Timer    2 Seconds
```

Once the configuration is set, the SBC will begin to establish the new link.

```
Initializing Intel (R) Boot Agent GE v1.2.40
Copyright (C) 1997-2006, Intel Corporation
Initializing and establishing link...
```

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Additional Resources

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