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Hardware Reference Manual

VMICPCI-7055*/CPCI-7055RC*

PowerPC®-Based CompactPCI® Single Board Computer

THE CPCI-7055RC IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (RoHS) DIRECTIVE (2015/863) CURRENT REVISION.

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abaco SYSTEMS

Document History

Revision	Date	Description
F.0	July 2011	
G	January 2018	Rebrand to Abaco Systems format

Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case-by-case basis. A WEEE management fee may apply.

About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

Further Information

Abaco Website

You can find information regarding Abaco products on the following website:


LINK
https://www.abaco.com

Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.


LINK
https://www.abaco.com/download/cpci-7055cpci-7055rc-hardware-reference-manual

Third-party Documents

ANSI/VITA Standards


LINK
http://www.vita.com


NOTE
Technical literature describing components used on the CPCI-7055RC is available from the manufacturers' websites.

Technical Support Contact Information

You can find technical assistance contact details on the website Support page.


LINK
https://www.abaco.com/support

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:


LINK
support@abaco.com

Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Support page.


LINK
https://www.abaco.com/support

Do not return products without first contacting the Abaco Repairs facility.

Compliance Information

This chapter provides the applicable information regarding regulatory compliance for the VMICPCI-7055/CPCI-7055RC.

Abaco's VMICPCI-7055/CPCI-7055RC has been evaluated to and has met the requirements for compliance to the following standards:

International Compliance

- EN55022:1998/CISPR 22:1997
- IEC61000-4-2
- IEC61000-4-3
- IEC61000-4-4
- IEC61000-4-5
- IEC61000-4-6

European Union (CE Mark)

- BS EN55024 (1998 w A1:01 & A2: 03)
- BS EN55022 (Class A)

United States

- FCC Part 15, Subpart B, Section 109, Class A

Australia/New Zealand

- AS/NZS CISPR 22 (2002) Class A

Canada

- ICES-003 Class A

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class A



NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.



CAUTION

Changes or modifications not expressly approved by the party responsible for compliance could void

the user's authority to operate the equipment.

Canadian Regulations

The VMICPCI-7055/CPCI-7055RC Class A digital apparatus complies with Canadian ICES-003.



NOTE

Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfy ICES-003.

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Overview

Abaco Systems's VMICPCI-7055*/CPCI-7055RC* are full featured IBM® PowerPC® based, single board computers (SBCs) in a single-slot, passively cooled, Eurocard form factor that utilizes the advanced technology of the next generation Marvell® chipset. The VMICPCI-7055/CPCI-7055RC are compliant with the CompactPCI® Specification PICMG® 2.0, Rev. 3.0 and feature a universal PCI-to-PCI bridge, allowing the board to function as a system controller or peripheral SBC in multi-SBC systems.

The VMICPCI-7055/CPCI-7055RC provide features typically found on desktop systems such as:

- Up to 1 GByte DDR 400 SDRAM with ECC
- Support for three Gigabit Ethernets (one front access and two optional PICMG 2.16 compliant or standard Gigabit Ethernet (option dependent) via the CompactPCI J3)
- Ultra DMA IDE drive support (secondary IDE, requires VMIACC-7055/ ACC-7055RC)
- Three serial ports (one RS232 (COM0) via front panel, two RS232/422/485 (COM1 and COM2) via CompactPCI J3)
- Real-Time clock/calendar
- Front panel reset switch

The Marvell chipset allows the VMICPCI-7055/CPCI-7055RC to provide enhanced features such as Ultra DMA IDE support. The standard desktop features of the VMICPCI-7055/CPCI-7055RC are described in ***Chapter 2 Standard Features*** of this manual.

The VMICPCI-7055/CPCI-7055RC provide features useful to embedded applications such as:

- PICMG 2.16 support
- Universal CompactPCI support (system controller or peripheral)
- Remote Ethernet booting
- Up to 2 GByte of CompactFlash
- Software-selectable Watchdog Timer with reset

Additionally, the VMICPCI-7055/CPCI-7055RC offer two PMC expansion sites with front panel access and I/O routing to the J5 connector of the CompactPCI backplane. The VMICPCI-7055/CPCI-7055RC are capable of executing many of today's embedded operating systems such as VxWorks® or Linux®. The embedded features of the VMICPCI-7055/CPCI-7055RC are described in ***Chapter 3 Embedded PC/RTOS Features*** of this manual.

The VMICPCI-7055/CPCI-7055RC are suitable for use in applications ranging from telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data

acquisition systems and anywhere that the highest performance processing power in a single CompactPCI chassis slot is desired.

PowerPC RISC Microprocessor

The microprocessor used on the VMICPCI-7055/CPCI-7055RC is a 32-bit PowerPC 750GX architecture in a 0.13 micron CMOS technology with six levels of copper interconnect. The performance enhancements included in the microprocessor are:

- Onboard L2 cache with locking by way (1 MByte)
- L1 data cache availability
- Bus pipelining (consecutive data reads)
- Additional floating point unit (FPU) reservation station and improved reciprocal estimates

L1 Data Cache

The 750GX L1 data cache supports miss-under-miss access, meaning that with one miss outstanding, the cache can continue to be accessed until a second miss occurs. In previous PowerPC 750 microprocessor implementations the data bus width for bus interface unit (BIU) accesses of the L1 data cache array was 64 bits. To cast out or to reload a 256-bit cache line required four access cycles. On the 750GX, this bus has been expanded to 256 bits. As a result, cache line data bursts can be read from or written to the cache array in a single cycle, reducing cache contention between the BIU and the load-store unit.

L2 Cache

The 750GX processor is available with 1 MByte of L2 cache. The cache is two-way set associative; each way contains 4096 blocks and each block consists of two 32-byte sectors. Array read and write operations execute in one processor cycle. Writes to the array are 64 bits wide, while reads are 256 bits wide.

In addition, the L2 cache has an 8-bit ECC for every 64-bit word in memory that can be used to correct a majority of single bit errors and detect multiple bit errors. The L2 tags also support parity and locking by way.

Bus Pipelining

The 60x bus has decoupled address and data buses, allowing transactions to be pipelined on the bus. That is, the address operation for a second transaction can be initiated before the data operation for a previous transaction is complete. The 750GX BIU allows pipelined read transactions to a depth of two back-to-back reads.

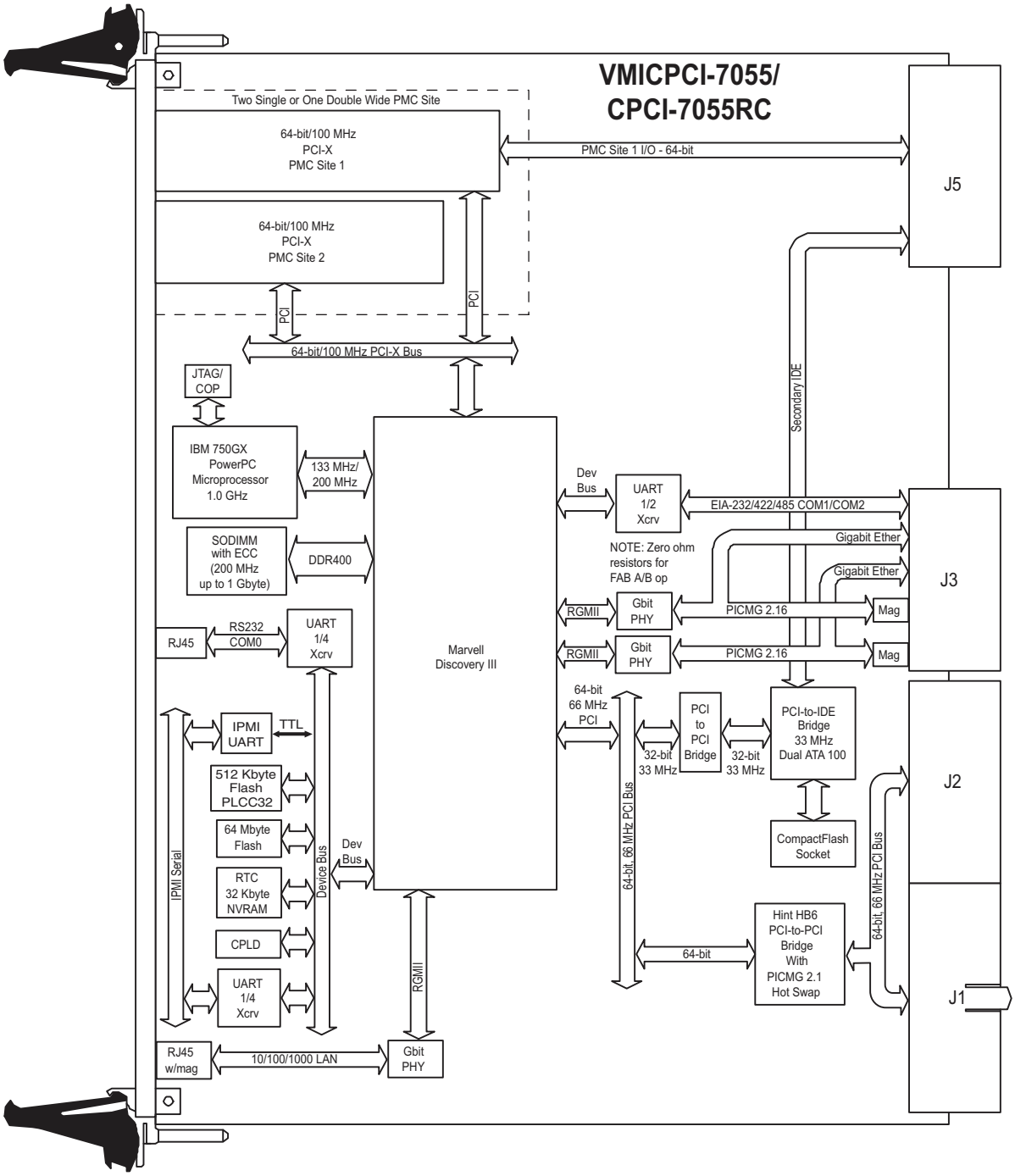
Marvell Discovery III (MV64460) Chipset

Revolutionary Architecture, Advanced Features

The Marvell Discovery™ III devices feature an advanced high performance crossbar switch architecture with any-to-any connectivity. With up to 100 Gigabits per second (Gbit/s) of aggregate throughput, the crossbar fabric supports non-blocking concurrent connections among peripherals at full bus speeds, delivering break-through performance for advanced Internet infrastructure equipment.

The Discovery III system controllers are highly integrated and offer leading-edge peripherals on-chip, including up to three Gigabit Media Access Controllers (MACs), up to two PCI-X interfaces and DDR memory support. In addition, the Discovery III device offers an integrated 2 MBit of cache coherent SRAM that resides on the processor interface unit to provide low latency storage for descriptors and packets.

Figure 1 VMICPCI-7055/CPCI-7055RC Block Diagram



NOTE

IPMI is no longer supported. Older boards may have IPMI.

References

IBM PowerPC 750FX/GX RISC Microprocessor

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY 12533-6351
www.ibm.com or
www-3.ibm.com/chips/

Marvell MV64460/1/2 System Controller for PowerPC

Marvell Semiconductor
700 First Ave.
Sunnyvale, CA 94089
(408) 222-2500
www.marvell.com

PCI Local Bus Specification, Rev. 2.2

Marvell Semiconductor
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

PCI 6150 PCI-to-PCI Bridge Chip (IDE)

PLX Technology, Inc.
870 Maude Ave.
Sunnyvale, CA 94085 USA
Tel: 1-800-759-3735
Tel: 1-408-774-9060
Fax: 1-408-774-2169
Email: info@plxtech.com
Web Site: www.plxtech.com

PLX PCI-6254 (HB6) Dual Mode Universal PCI-to-PCI Bridge Datasheet

PLX Technology Inc.
870 Maude Ave.
Sunnyvale, CA 94085
www.plxtech.com

CMC Specification, P1386/Draft 2.0 from:

IEEE Standards Department
Copyrights and Permissions
445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331

PMC Specification, P1386.1/Draft 2.0 from:

IEEE Standards Department
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Piscataway, NJ 08855-1331
445 Hoes Lanes, P.O. Box 1331
Piscataway, NJ 08855-1331, USA

For a detailed description and specification of the CompactPCI bus, please refer to:

CompactPCI Specification PICMG 2.0 R3.0

IEEE Standards Department
PCI Industrial Computer Manufacturers' Group
301 Edgewater Place
Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 (FAX)
www.picmg.org

Packet Switching Backplane Specification PICMG 2.16 R1.0

PCI Industrial Computer Manufacturers' Group
301 Edgewater Place
Suite 220
Wakefield, MA 01880
(617) 224-1100
(617) 224-1239 (FAX)
www.picmg.org

The following is useful information related to the operation of the I^2C controllers:

The I^2C Specification version 2.0

Philips Semiconductor
811 East Arques Ave.
Sunnyvale, CA 94088-3409
(800) 234-7381
www.semiconductors.philips.com

1 • Handling and Installation

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the VMICPCI-7055/CPCI-7055RC.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Customer Care.

1.2 Handling Precaution

Electronic assemblies use devices that are sensitive to static discharge. Observe anti-static procedures when handling these boards. All products should be in an anti-static plastic bag or conductive foam for storage or shipment. Work at an approved anti-static workstation when unpacking boards.

1.3 Hardware Setup

The VMICPCI-7055/CPCI-7055RC are factory populated with user-specified options as part of the VMICPCI-7055/CPCI-7055RC ordering information. The RAM size is not user-upgradable. To change RAM size, contact Customer Care to receive a Return Material Authorization (RMA).

The VMICPCI-7055/CPCI-7055RC are tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the SBC are illustrated in Figure 1-1 on page 19. The definitions of the SBC board jumpers and connectors are included in Table 1-1 through Table 1-3. Please note that the VMICPCI-7055/CPCI-7055RC offer two PMC sites designated PMC #1 and PMC #2 as shown in Figure 1-1 on page 19.



CAUTION

All jumpers marked *User Configurable* in the following tables may be changed or modified by the user. All jumpers marked factory configured should not be modified by the user.

Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper not marked *User Configurable* will void the Warranty and may damage the unit. Tables with bold text indicates that this is the default setting.

Figure 1-1 VMICPCI-7055/CPCI-7055RC PMC Sites and Jumper Locations

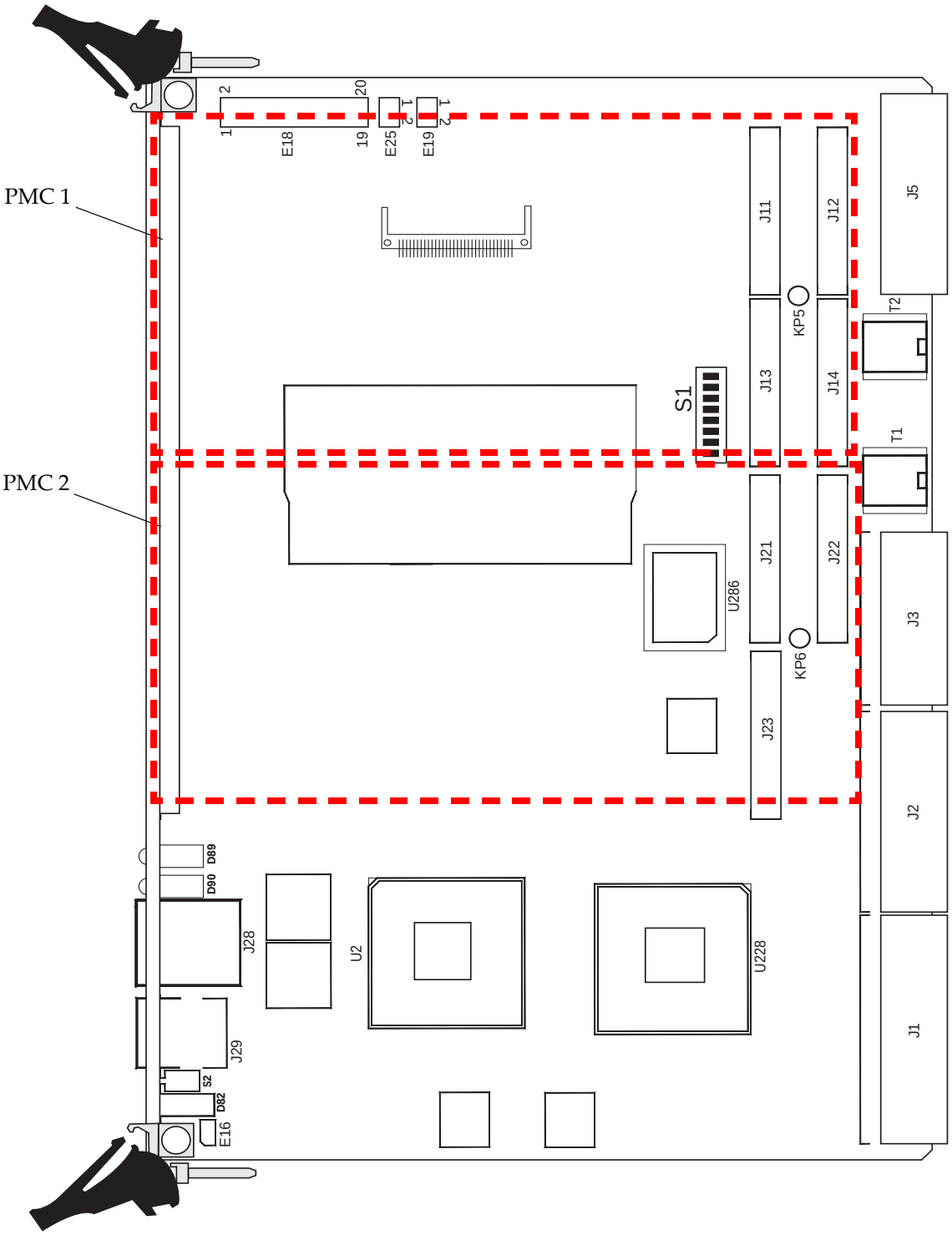


Table 1-1 Board Connectors, Headers, Switches and Jumpers

Connectors, Header, Jumpers and Switches	Function
J1, J2, J3 and J5	CompactPCI Backplane Connectors
J11, J12, J13, J14	PMC Slot 1
J21, J22, J23	PMC Slot 2
J28	LAN 0
J29	COM 0
D82	Front Panel Status Indicators
D89	Ethernet Port 2 Status LEDs
D90	Ethernet Port 1 Status LEDs
E16	Hotswap Switch Header
E18	JTAG Header
E19	Bridge Mode Jumper
E25	Reset Enable Jumper
S1	System Controller Switch
S2	Board Reset Switch
KP5	PMC Site#1 Keypin (5V VIO)
KP6	PMC Site#2 Keypin (5V VIO)

Table 1-2 CompactPCI Bridge Mode (**User Configurable**) - Jumper (E19)

	Jumper Position	
CompactPCI Mode Enable	**Installed**	**Normal Mode**
	Omitted	Blade Mode

CompactPCI Bridge Mode Default: Normal operation mode.

Blade Mode: In this mode the VMICPCI-7055/CPCI-7055RC will turn off the bridge to the backplane. This allows the SBC to be inserted into any slot on the backplane, with or without a system controller. If the SBC is inserted in a chassis with a system controller the CPCI_RESET# will be ignored. PIGMG 2.16 will still be available on the backplane.

Table 1-3 CompactPCI Reset (**User Configurable**) - Jumper (E25)

	Jumper Position
Reset Active	**Installed**
Reset Ignore	Omitted

CompactPCI Reset (Default): With the jumper in installed, resets from the system controller will always be accepted.

Reset Ignore: With the jumper removed, a reset from the system controller will only be accepted until the boot done LED is turned off.

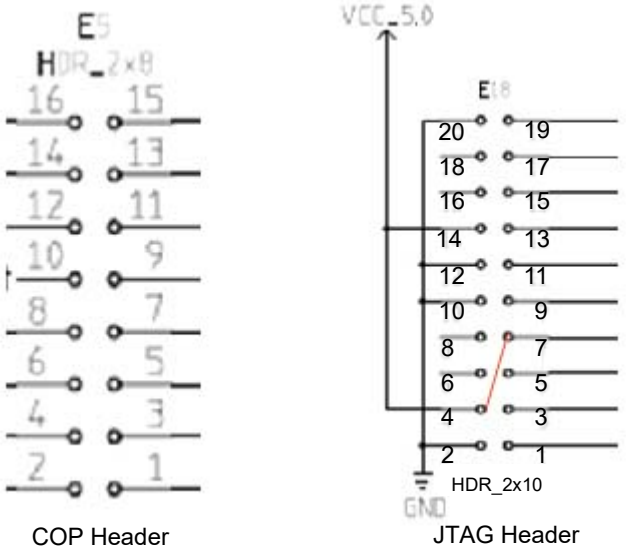
1.4 COP/ICE/Emulator

To use the COP/ICE/Emulator, there are two headers on the board that look similar. The location of both headers is shown in the diagram on the following page. It will be required for the user to access both headers (E5 and E18) in order to utilize the COP interface.

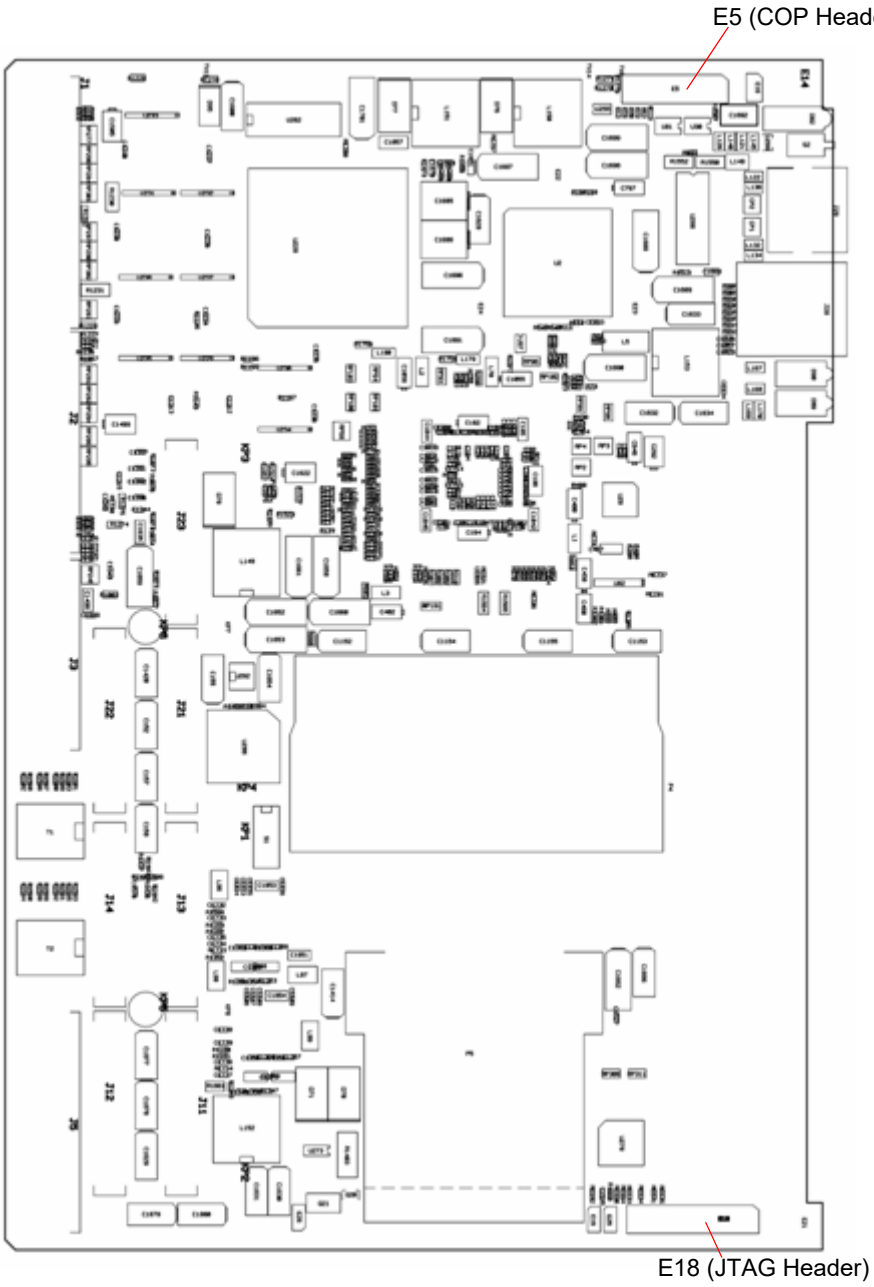
To use the COP port (E5)

1. Strap pin 4 to pin 7 on E18.
2. Connect emulator to E5.

Figure 1-2 COP Interface



COP Header JTAG Header

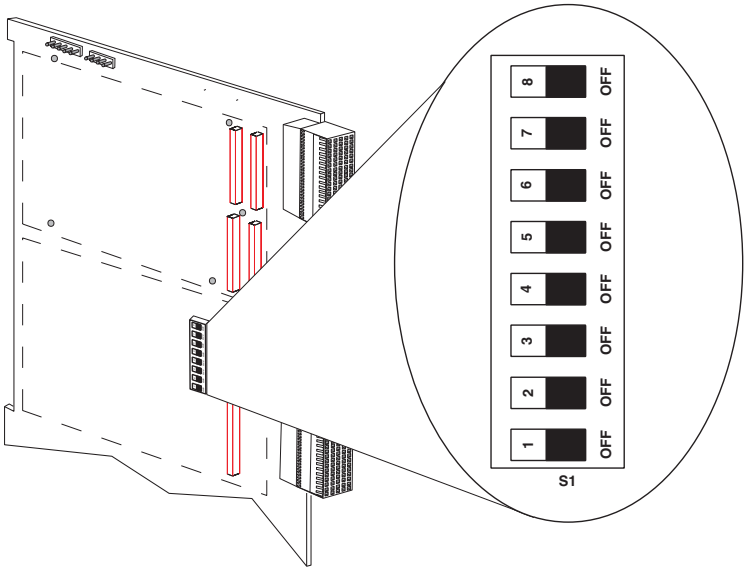

E5 (COP Header)
E18 (JTAG Header)

1.5 Switch S1

Table 1-4 CompactPCI Bus Switch S1 Configuration (Factory Default is “OFF” for All Positions)

Pin#	Position	Function
1	On	Boot from solder-down Flash (64 Mbyte)
	Off	**Boot from PLCC32**
2	On	Write protect all NVRAM and I^2C bus
	Off	**No write protection for NVRAM on I^2C bus**
3	On	Write protect all NVRAM on DEVbus
	Off	**No write protection for NVRAM on DEVbus**
4	On	COM Port 0 loopback
	Off	**COM Port 0 normal**
5	On	COM Port 1 (COM1) RS422/485 mode
	Off	**COM Port 1 (COM1) RS232 mode**
6	On	COM Port 1 loopback
	Off	**COM Port 1 normal**
7	On	COM Port 2 (COM2) RS422/485 mode
	Off	**COM Port 2 (COM2) RS232 mode**
8	On	COM Port 2 loopback
	Off	**COM Port 2 normal**

Figure 1-3 Location of Switch S1



NOTE

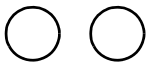
To configure the serial ports to loopback mode, S1 on the VMICPCI-7055/CPCI-7055RC will need pins 6 and 8 (relating to COM1 and COM2 respectively) placed in the ON position when used with the VMIACC-7055/ACC-7055RC Rear Transition Modules (RTMs).

1.6 Installation

The VMICPCI-7055/CPCI-7055RC conform to the CompactPCI physical specification for a 6U board. The VMICPCI-7055/CPCI-7055RC can be used for system control or as a peripheral board. It can be plugged directly into any standard chassis accepting either type of board. The following pictures illustrate the symbols used to identify the slots in a standard CompactPCI chassis.



This symbol identifies the System Controller slot



This symbol identifies Dual LAN Node slots



This symbol identifies peripheral slots

The following steps describe the recommended method for installation and powerup of the VMICPCI-7055/CPCI-7055RC:

1. If a PMC is to be used, install it on the VMICPCI-7055/CPCI-7055RC prior to board installation (as shown in Figure 1-5 on page 26). Refer to the Product Manual for the PMC module for configuration and setup.
2. The VMICPCI-7055/CPCI-7055RC must be installed in a designated slot of the CompactPCI backplane (see symbols above for selection of the correct slot).

NOTE
Air flow as measured at the output side of heatsink is to be greater than 400LFM.

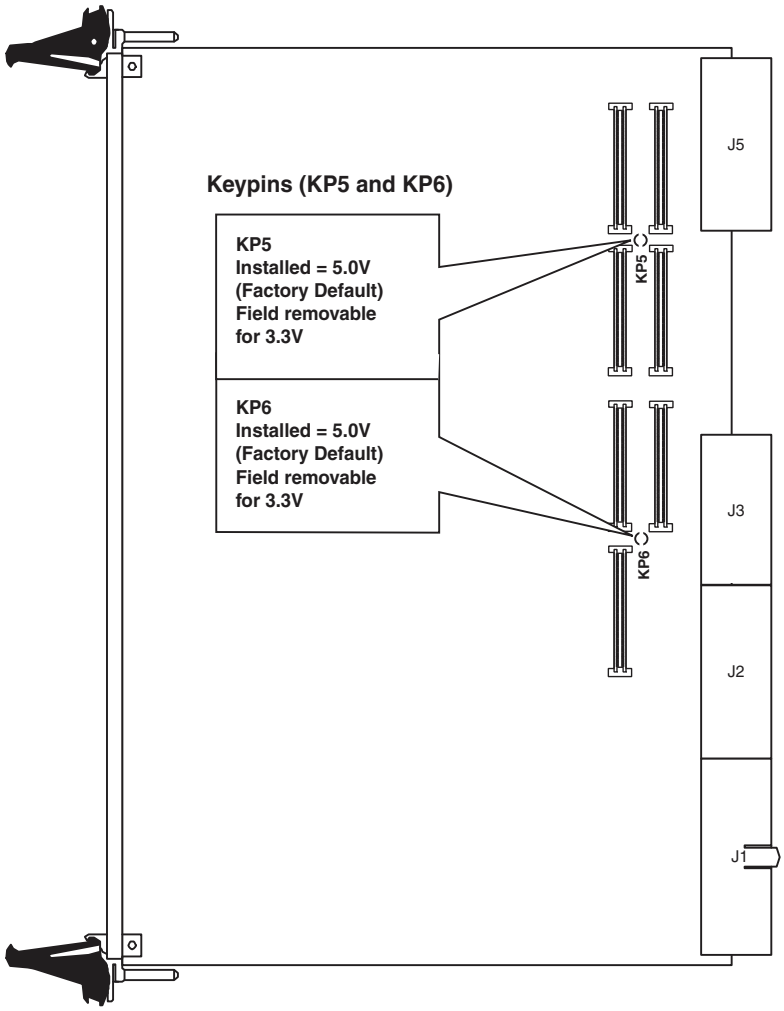
3. Insert the VMICPCI-7055/CPCI-7055RC into a CompactPCI chassis system controller or peripheral slot. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector. Use the ejector handles to firmly seat the board.
4. All needed peripherals can be accessed from the front panel or the rear I/O VMIACC-7055/ACC-7055RC RTMs. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A.
5. Connect an RS232 terminal to COM0 (see Figure 1-12 and "Using the Serial Port (Debug)" on page 33).

1.7 Installing PMCs

1.7.1 PMC Site (VIO)

VIO is the I/O voltage used for PCI bus termination. The PCI bus interface requires strong parallel (pull-up) termination. Initially, the voltage for the pull-ups was +5 V. Over time, with the need for power reduction and higher speeds, +3.3 V devices became prevalent. +3.3 V devices can easily drive TTL signaling. Higher speed PCI buses utilize +3 V termination.

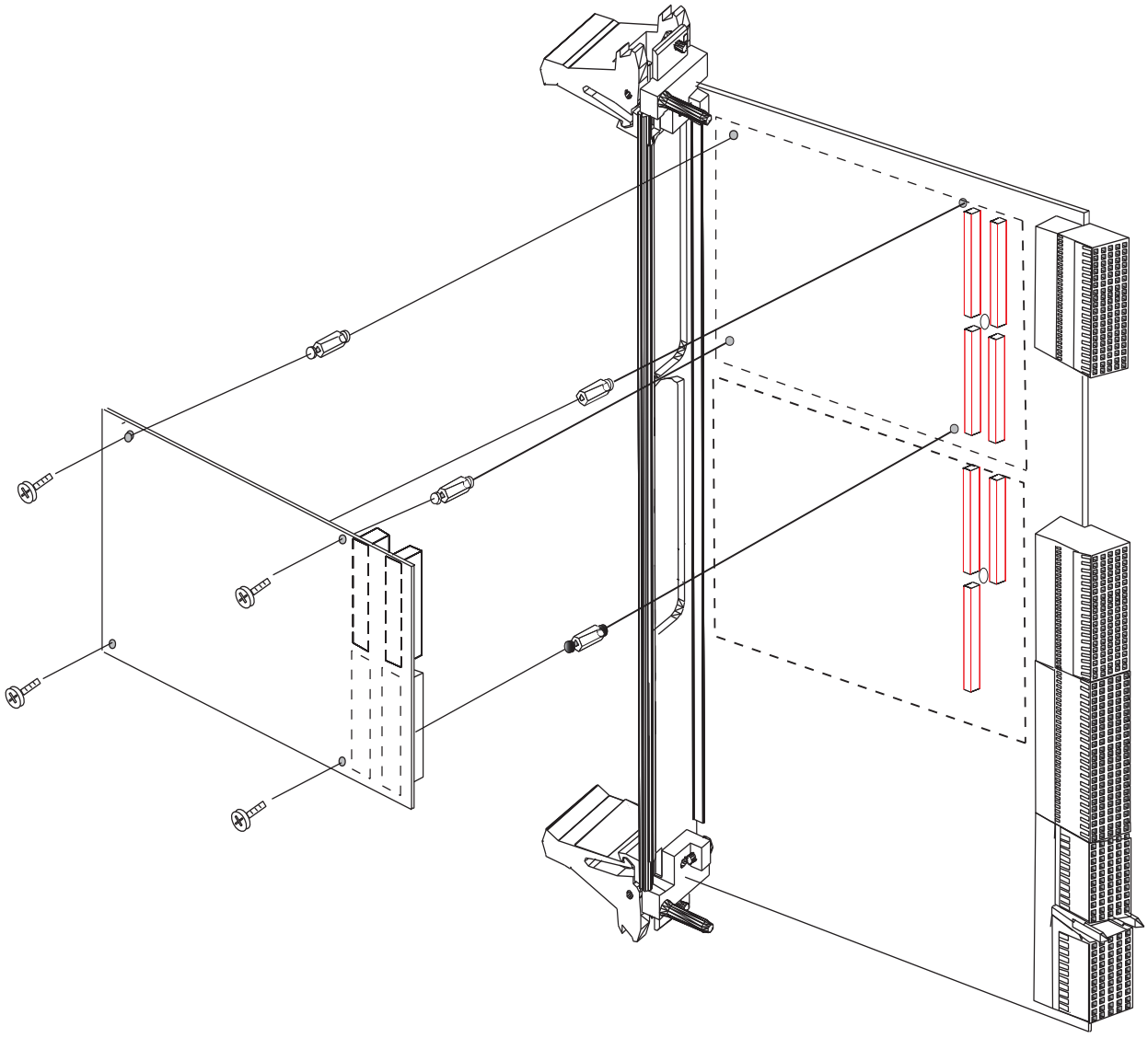
Figure 1-4 Keypin Installation and Setup



CAUTION

When Installing the keypins on the two PMC sites, the two keypins MUST be setup for the same voltage level (Either in the 5 V position (installed) or in the 3.3 V (removed) position). This is due to the keypins being on the same bus, if installed incorrectly this could cause damage.

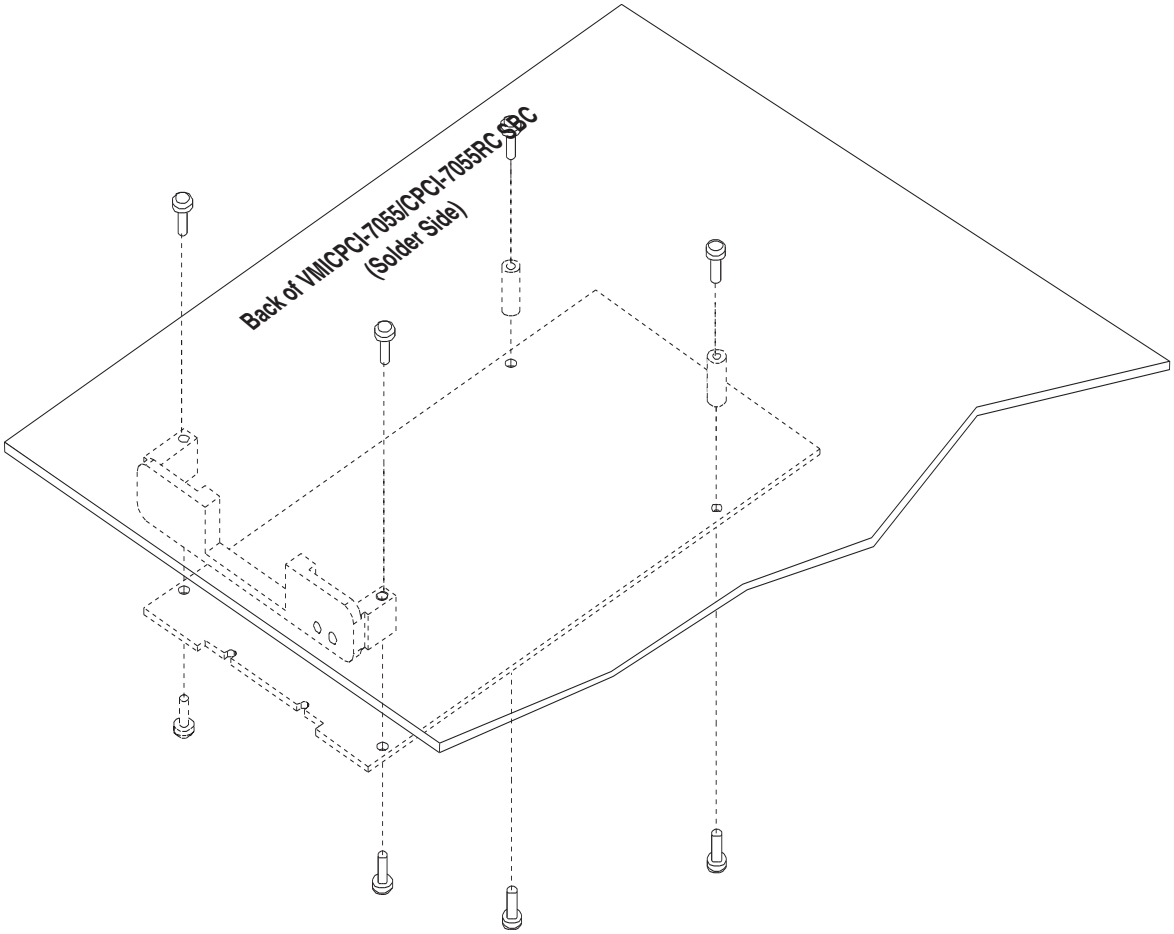
Figure 1-5 Installing a PMC on the VMICPCI-7055/CPCI-7055RC



CAUTION

When installing the keypins on the two PMC sites, the two keypins **MUST** be installed for the same voltage level (i.e., either in the 5 V position or in the 3.3 V position). This is due to the keypins being on the same bus, if installed incorrectly this could cause damage to the board.

Figure 1-6 VMICPCI-7055/CPCI-7055RC PMC Backside Mounting



1.8 Front/Rear Panel Connectors

The VMICPCI-7055/CPCI-7055RC provide front panel access for both PMC expansion sites, one Gigabit Ethernet port, one serial port, the manual reset switch and the status LEDs. A drawing of the VMICPCI-7055/CPCI-7055RC front panels are shown in Figure 1-7. The front panel connectors and indicators are labeled as follows:

LAN0	Gigabit Ethernet port LEDs
2/1	Gigabit Ethernet ports status LEDs (LAN1 and LAN2 rear I/O)
COM0	COM0 Serial Port LEDs
RST	Manual reset switch
S	Status LEDs
R	Reset LED
P	Backplane Power LED

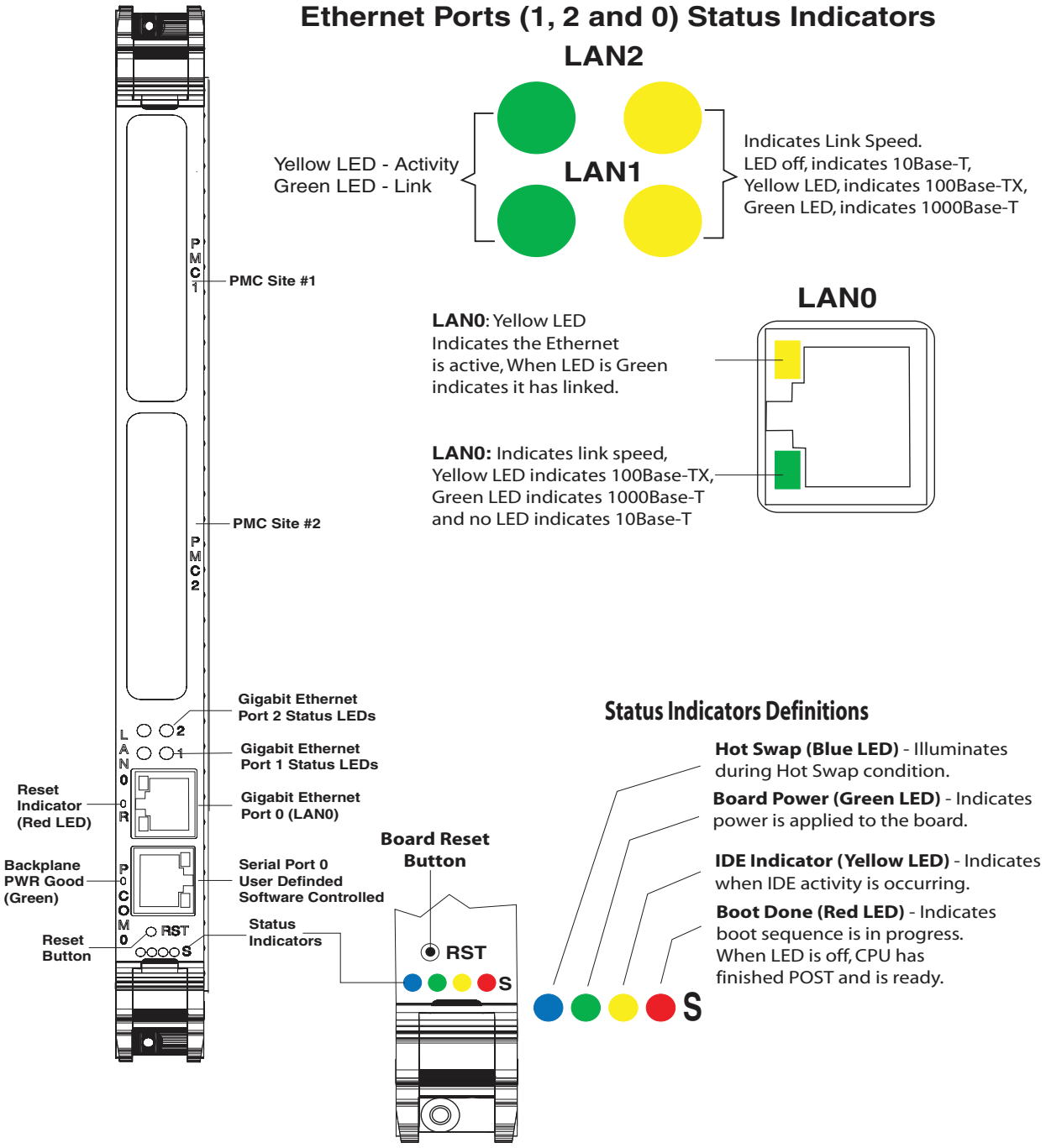
The VMICPCI-7055/CPCI-7055RC provide rear I/O support for the following: COM1, COM2, PMC I/O for one expansion site and IDE. These signals are accessed using the VMIACC-7055/ACC-7055RC RTMs, which terminate into industry standard connectors.

The front panel connectors, including connector pinouts and orientation, for the VMICPCI-7055/CPCI-7055RC are defined in Appendix A.

Rear panel connections are defined in the appropriate RTM Installation Guide. Contact Sales for compatible RTMs offered by Abaco.

1.9 LED Definition

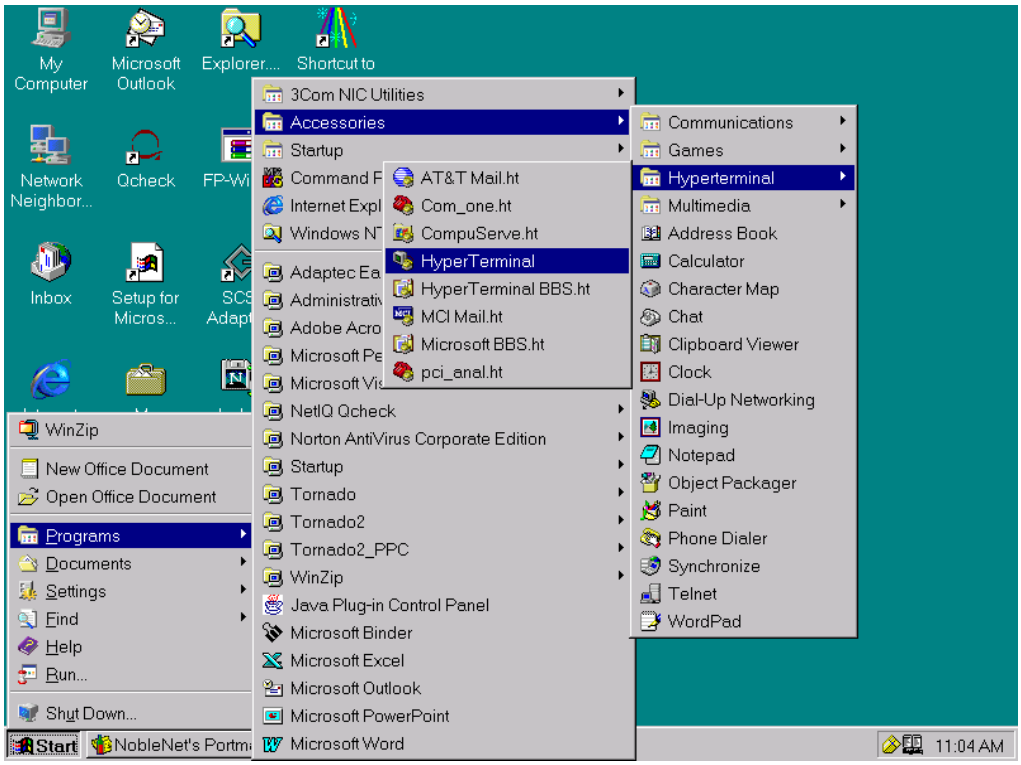
Figure 1-7 Front Panel LED Definitions



1.10 RS232 Serial Port (COM0)

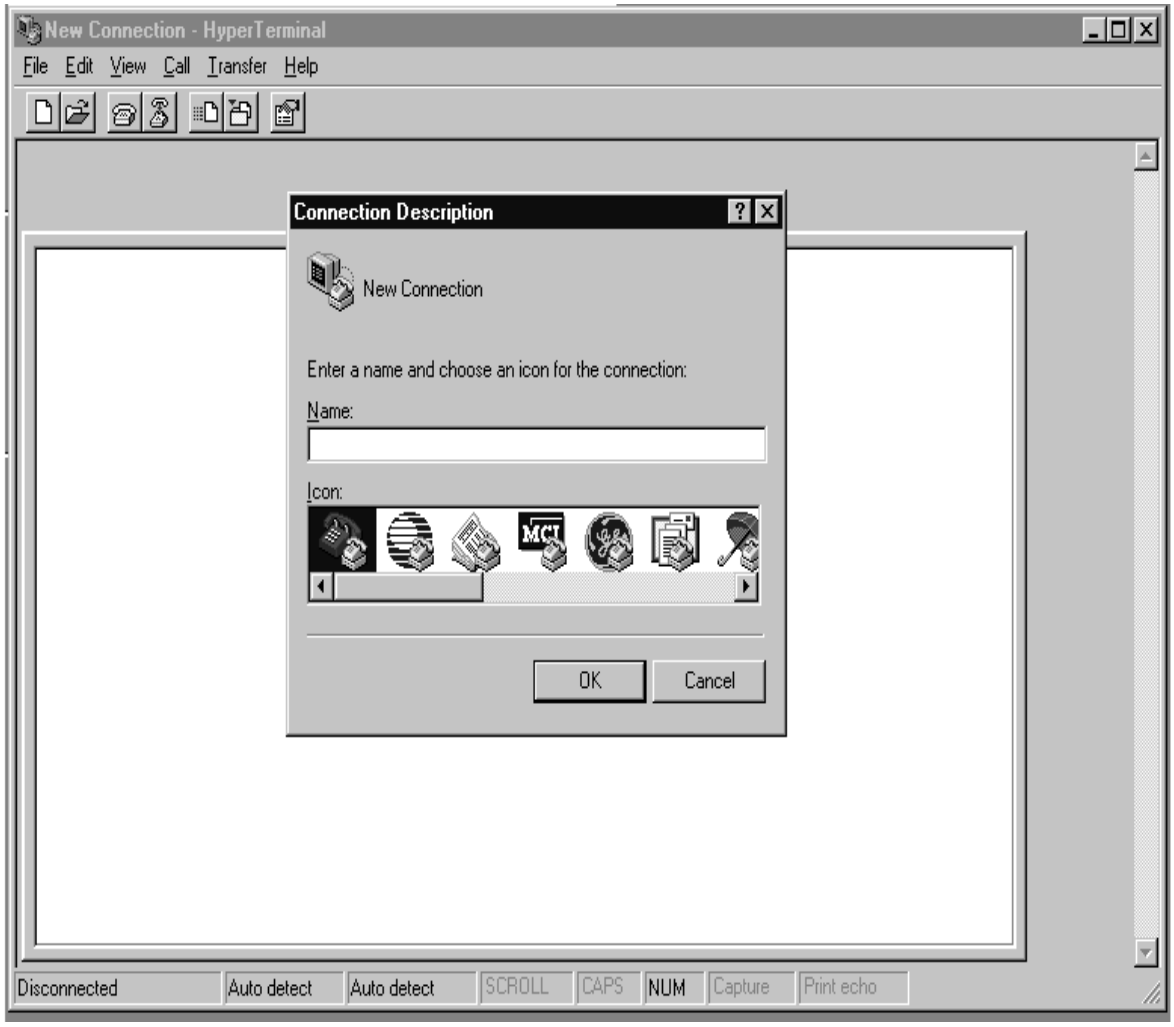
The serial port can be used to control, monitor and set up the VMICPCI-7055/CPCI-7055RC. Using a PC as a remote terminal with a Windows®-based OS, go to Accessories, then to Hyperterminal and click on *Hyperterminal*. When using a Linux-based OS, go to the root directory, at the command prompt and type in Minicom.

Figure 1-8 Serial Port Access Using Example: Desktop Windows-Based OS



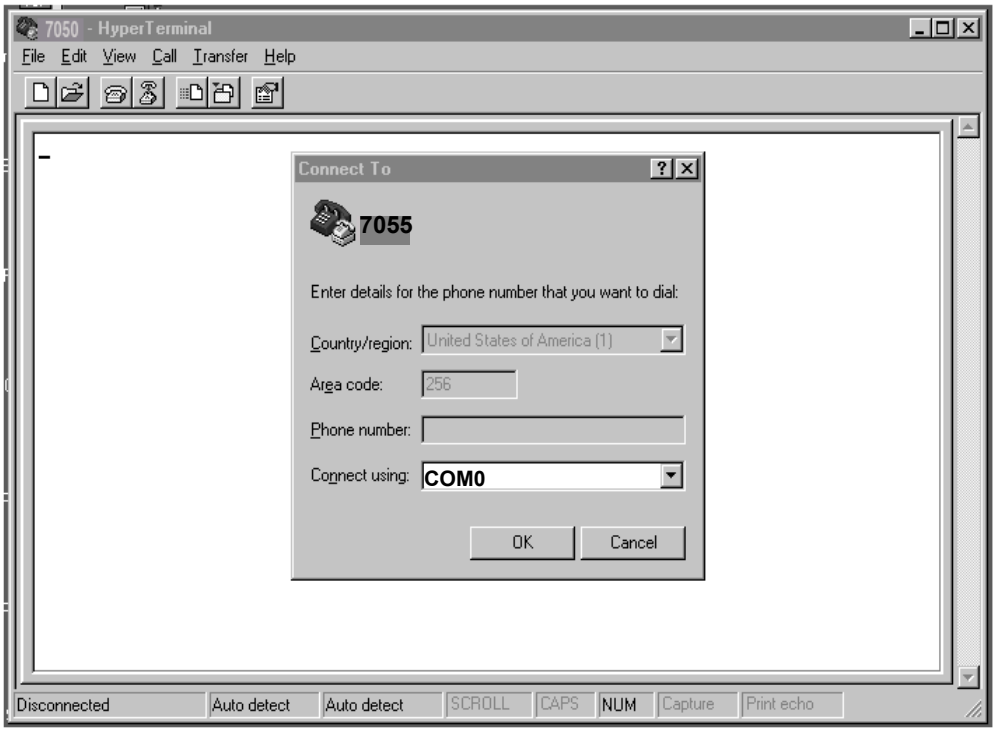
1. The following window will appear for Windows-based OS. From the Connection window, type in the name (7055). You can also choose an icon for the connection. Click OK.

Figure 1-9 Hyperterminal New Connection Window



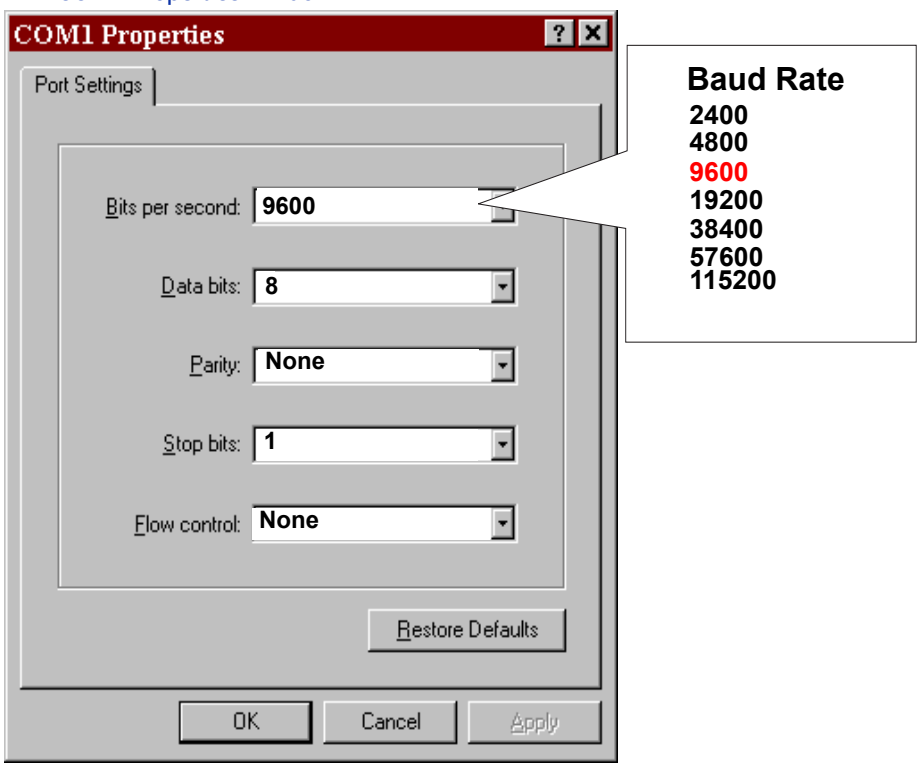
2. Select the COM port you will be using. After selecting the COM port click OK.

Figure 1-10 COM Port Window



3. The COM port properties window will appear. Select the Baud rate (bits per second). The default Baud rate for the VMICPCI-7055/CPCI-7055RC is 9600. Click OK.

Figure 1-11 COM1 Properties Window



Bits per second: 9600
Data bits: 8
Parity: None
Stop bits: 1
Flow control: None

1.11 Using the Serial Port (Debug)

The RS232 serial port is used to monitor and control the VMICPCI-7055/CPCI-7055RC. The VMICPCI-7055/CPCI-7055RC can be cabled to a standard PC with an available serial port. See Figure 1-12 below for an example of connecting the VMICPCI-7055/CPCI-7055RC with a PC using the RS232 serial port and cable.

Figure 1-12 VMICPCI-7055/CPCI-7055RC Serial Port Connection

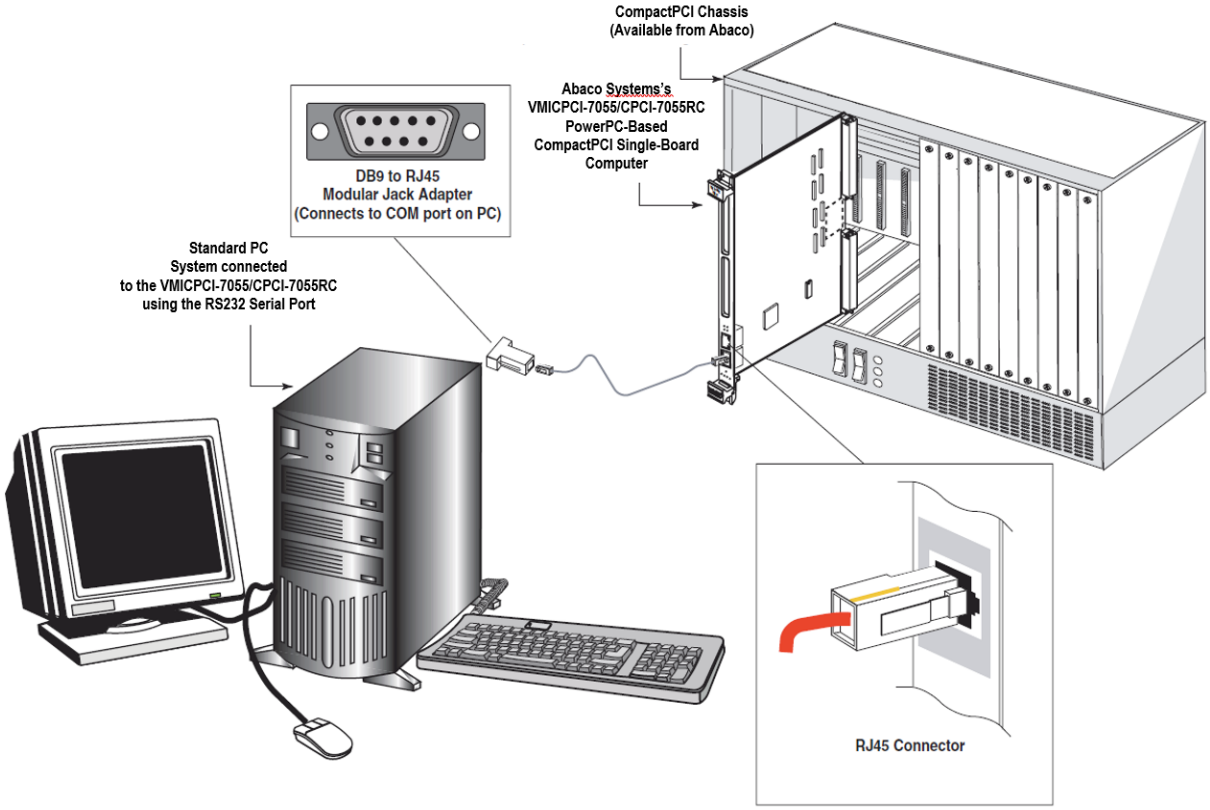


Table 1-5 RJ45 to Standard DB9 Adapter Pinout

RJ45 to DB9 COM Port Adapter	
PN#	Type
360-010030-002	DB9 Female (null modem cable)
42G7602-0002	DB9 Female (null modem cable) - RoHS Compliant

NOTE
One adapter (of the applicable type) is included with the VMICPCI-7055/CPCI-7055RC.

2 • Standard Features

The VMICPCI-7055/CPCI-7055RC are PowerPC-based single board computers compatible with modern industry standard desktop systems. The VMICPCI-7055/CPCI-7055RC therefore retain industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, IDE interface and Ethernet controller) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the VMICPCI-7055/CPCI-7055RC.

2.1 CPU

The VMICPCI-7055/CPCI-7055RC CPU is factory populated with an IBM PowerPC processor. The processor speed and Memory/CompactFlash size are user specified as part of the VMICPCI-7055/CPCI-7055RC ordering information.

To change memory size or CompactFlash size contact Customer Care to receive a Return Material Authorization (RMA).

2.2 Physical Memory

The VMICPCI-7055/CPCI-7055RC provides DDR Synchronous DRAM (SDRAM) as onboard system memory. Memory can be accessed as bytes, words or longwords.

The VMICPCI-7055/CPCI-7055RC accepts one 200-pin DDR SDRAM SODIMM with a maximum capacity of 1 GByte. The onboard DRAM is accessible to the CompactPCI bus through the PCI-to-PCI bridge and is addressable by the local processor.



NOTE

Memory capacity may change due to part availability.

2.3 PCI Device Interrupt Map

The PCI bus-based external devices include the PCI-to-PCI bus bridge, PMC site and the IDE controller. These external devices are mapped to the PCI Interrupt Request (PIRQx) lines of the MV64460. This mapping is defined in Table 2-1.

Table 2-1 PCI Device Interrupt Mapping

PCI-X Devices	PGNT	PREQ	IDSEL	IRQ	Vendor ID	Device ID
MV64460 PCI1	N/A	N/A	Px_AD[21]	Px_IRQA#	N/A	N/A
PMC Site 1	Px_GNT[0]#	Px_REQ[0]#	Px_AD[17]	Px_IRQA#	N/A	N/A
PMC Site 2	Px_GNT[1]#	Px_REQ[1]#	Px_AD[18]	Px_IRQB#	N/A	N/A
PCI Devices						
MV64460 PCI0	N/A	N/A	P_AD[21]	P_IRQA#	N/A	N/A
HINT HB6	P_GNT[0]#	P_REQ[0]#	P_AD[22]	P_IRQE#	10E3H	0513H
PCI-to-PCI Bridge	P_GNT[1]#	P_REQ[1]#	P_AD[20]	N/A	N/A	N/A
IDE Controller	P2_GNT[0]#	P2_REQ[0]#	P2_AD[23]	P2_IRQ[B]#	N/A	N/A

2.4 Integrated Peripherals

The VMICPCI-7055/CPCI-7055RC incorporate the Quad UART controller. The Quad UART controller provides the VMICPCI-7055/CPCI-7055RC with four 16554 UART-compatible serial ports. The Marvell MV64460 provides three independent Ethernet ports. One serial port and one Gigabit Ethernet port are available via the front panel, using an RJ45 connector for the serial port and an RJ45 connector for the Gigabit Ethernet connection. COM1 and COM2 are routed to the CompactPCI J3 connector.

The parallel IDE interface is provided by the PCI6150 PCI-to-PCI Bridge. The IDE interface supports two channels: primary and secondary. The primary channel is routed to an optional onboard CompactFlash socket. The secondary channel is routed out of the CompactPCI J5 backplane connector to an optional RTM that terminates into a standard 40-pin header. This channel can support a master and slave drive. The IDE interface on the VMICPCI-7055/CPCI-7055RC supports Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100 drives and automatically determines the proper operating mode based on the type of drive used. In order to properly function in the Ultra ATA/100 mode, a special 80 conductor cable must be used instead of the standard 40 conductor cable. This cable is typically available from the Ultra ATA/100 drive manufacturer.

2.5 Ethernet Controller

The network capability is provided by the Marvell MV64460 controller, with three independent channels. The VMICPCI-7055/CPCI-7055RC support 10BaseT, 100BaseTX and 1000BaseT Ethernet.

2.5.1 10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters.

2.5.2 100BaseTX

The VMICPCI-7055/CPCI-7055RC also support the 100BaseTX Ethernet. A network based on a 100BaseTX standard uses unshielded twisted-pair cables and an RJ45 connector. 100BaseTX has a maximum length of 100 meters.

2.5.3 1000BaseT

The VMICPCI-7055/CPCI-7055RC support 1000BaseT using the Marvell MV64460 controller. The interface uses shielded cables with four pairs of conductors, along with an RJ45 connector on the front panel and two channels routed to the CompactPCI J3 connector for use with the VMIACC-7055/ACC-7055RC RTMs. The Gigabit Ethernet is also available with the optional PICMG 2.16 routed to the CompactPCI backplane.



NOTE

Ethernet activity is monitored on the front panel LEDs by a blinking yellow LED. The yellow LED will be on continuously when the Ethernet port is linked but with no activity.



NOTE

If the PICMG 2.16 option is available on the VMICPCI-7055/CPCI-7055RC, then the Gigabit Ethernet can not be used with the VMIACC-7055/ACC-7055RC RTMs.

3 • Embedded PC/RTOS Features

The VMICPCI-7055/CPCI-7055RC feature additional capabilities beyond those of a typical desktop computer system. The unit provides standard general-purpose timers along with a programmable Watchdog Timer for synchronizing and controlling multiple events in embedded applications. The VMICPCI-7055/CPCI-7055RC also provide support for a CompactFlash disk system or PICMG 2.16 Ethernet over the CompactPCI backplane or rear I/O using the VMIACC-7055/ACC-7055RC RTMs. PICMG 2.9 support is available, which allows for compatibility with the most demanding CompactPCI applications. These features make the unit ideal for embedded applications, particularly where standard hard drives and floppy disk drives cannot be used.

3.1 CompactPCI Bus Bridge

The VMICPCI-7055/CPCI-7055RC incorporate a PLX PCI-6254 (Hint HB6AB) Universal Bridge device that performs universal PCI bridging functions for embedded and intelligent I/O applications. The PCI device acts as a gateway to an intelligent subsystem. As a peripheral controller it allows the local VMICPCI-7055/CPCI-7055RC processors to configure and control the onboard local subsystem independent from the CompactPCI bus host processor. The VMICPCI-7055/CPCI-7055RC local PCI subsystem is presented to the CompactPCI bus host as a single CompactPCI device. As a system controller, the bridge acts as a standard transparent PCI-to-PCI bridge. For detailed information concerning the embedded PCI bus bridge, consult the PLX PCI-6254 (Hint HB6) datasheet.

The VMICPCI-7055/CPCI-7055RC PCI bridge device provides the following features:

3.1.1 PCI Interface

- Full compliance with the PCI Local Bus Specification, Revision 2.2
- Supports 3.3 V or 5 V VIO operation
- Concurrent local (secondary) and CompactPCI (primary) bus operation

3.1.2 Buffer Architecture

- Queuing of multiple transactions in either direction
- 256 byte of posted write (data and address) buffering in each direction
- 256 byte of read data buffering in each direction
- Four delayed transaction entries in each direction

3.1.3 Blade Mode

This mode disables the bridge to the backplane. This results in the ability to be inserted into any slot on the backplane, with or without a system controller. All PCI signals from the chassis will be ignored. PIGMG 2.16 will still be available on the backplane.

3.2 PICMG 2.16 Ethernet

The VMICPCI-7055/CPCI-7055RC support three 10/100/1000 Ethernet LANs. 10BaseT, 100BaseTX, and 1000BaseT options are supported via a front panel RJ45 connector and through a PICMG 2.16 or CompactPCI J3 backplane connection (the PICMG 2.16 and the CompactPCI J3 are option dependent). Contact Sales for ordering information.



NOTE

The system backplane must support the PICMG 2.16 specification, and a PICMG 2.16 compatible switch is required for each Ethernet channel.

3.3 PICMG 2.9 Support

The VMICPCI-7055/CPCI-7055RC provide a Zircon PM peripheral management controller that supports a subset of IPMI 1.5 commands via PICMG 2.9. Refer to Appendix B for details of the IPMI capabilities of the onboard peripheral management controller.



NOTE

IPMI is no longer supported. Older boards may have IPMI.

A • Connectors and Pinouts

The VMICPCI-7055/CPCI-7055RC CompactPCI Universal SBCs have several connectors for their I/O ports. Wherever possible, the VMICPCI-7055/CPCI-7055RC use connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a CompactPCI bus chassis.

A.1 J1 Connector Pinout

The VMICPCI-7055/CPCI-7055RC utilize a high-density 110-pin, low inductance, controlled impedance connector. This connector meets the IEC-1076 international standard for CompactPCI connectors. An additional external metal shield is required. The large number of ground pins ensures adequate shielding and grounding for low ground bounce and reliable operation in noisy environments. The key prevents misalignment of the board when installing in the chassis. Figure below depicts the J1 connector and the connector pinout.

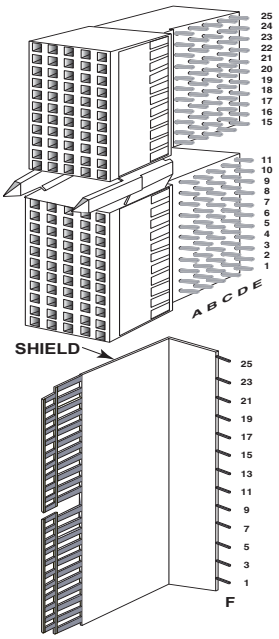


Table A-1 J1 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
25	VCC_5.0E	CPCI_REQ64#	CPCI_ENUM#	VCC_3.3E	VCC_5.0E	GND
24	CPCI_AD[1]	VCC_5.0E	CPCI_VIO_C24	CPCI_AD[0]	CPCI_ACK64#	GND
23	VCC_3.3E	CPCI_AD[4]	CPCI_AD[3]	CPCI_5V_D23	CPCI_AD[2]	GND
22	CPCI_AD[7]	GND	CPCI_3V_C22	CPCI_AD[6]	CPCI_AD[5]	GND
21	VCC_3.3E	CPCI_AD[9]	CPCI_AD[8]	CPCI_M66EN	CPCI_CBE[0]#	GND
20	CPCI_AD[12]	GND	VCC_VIO	CPCI_AD[11]	CPCI_AD[10]	GND
19	VCC_3.3E	CPCI_AD[15]	CPCI_AD[14]	GND	CPCI_AD[13]	GND
18	CPCI_SERR#	GND	VCC_3.3E	CPCI_PAR	CPCI_CBE[1]#	GND
17	VCC_3.3E	CPCI_IPMB_SCLH	CPCI_IPMB_SDAH	GND	CPCI_PERR#	GND
16	CPCI_DEVSEL#	CPCI_PCIXCAP	VCC_VIO	CPCI_STOP#	CPCI_LOCK#	GND
15	VCC_3.3E	CPCI_FRAME#	CPCI_IRDY#	CPCI_BDSEL#	CPCI_TRDY#	GND
12 through 14 are lost to the keying area						

Table A-1 J1 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
11	CPCI_AD[18]	CPCI_AD[17]	CPCI_AD[16]	GND	CPCI_CBE[2]#	GND
10	CPCI_AD[21]	GND	VCC_3.3E	CPCI_AD[20]	CPCI_AD[19]	GND
9	CPCI_CBE[3#]	CPCI_IDSEL	CPCI_AD[23]	GND	CPCI_AD[22]	GND
8	CPCI_AD[26]	GND	VCC_VIO	CPCI_AD[25]	CPCI_AD[24]	GND
7	CPCI_AD[30]	CPCI_AD[29]	CPCI_AD[28]	GND	CPCI_AD[27]	GND
6	CPCI_REQ#	CPCI_PCI_PRESENT#	CPCI_3V_C6	CPCI_CLK	CPCI_AD[31]	GND
5	N/C	N/C	CPCI_RST#	GND	CPCI_GNT#	GND
4	CPCI_IPMB_PWR	CPCI_HEALTHY#	CPCI_VIO_C4	N/C	N/C	GND
3	CPCI_INTAR#	CPCI_INTBR#	CPCI_INTCR#	CPCI_5V_D3	CPCI_INTDR#	GND
2	CPCI_TCK	VCC_5.0E	CPCI_TMS	N/C	CPCI_TDI	GND
1	VCC_5.0E	VCC_-12.0E	CPCI_TRST#	VCC_12.0E	VCC_5.0E	GND

A.2 J2 Connector Pinout

The VMICPCI-7055/CPCI-7055RC J2 connector is a 2 mm “Hard Metric” CompactPCI connector, with five rows of 22 pins each. J2 is required for system slot SBCs. An additional external metal shield, labeled row F, is also used. This connector’s controlled impedance minimizes unwanted signal reflections. Figure below illustrates the J2 connector and the connector pinout.

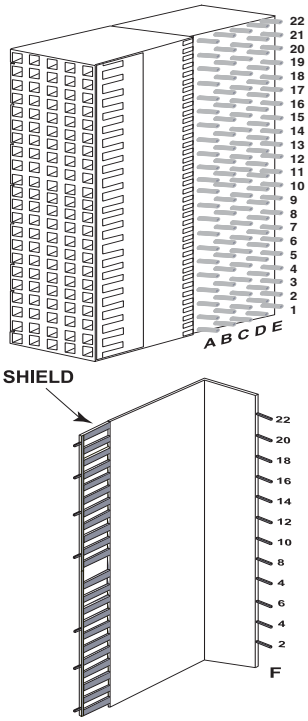


Table A-2 J2 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
22	VCC_3.3E	VCC_3.3E	VCC_3.3E	VCC_3.3E	VCC_3.3E	GND
21	CPCI_CLK 6	GND	N/C	N/C	N/C	GND
20	CPCI_CLK 5	GND	N/C	GND	N/C	GND
19	GND	GND	CPCI_SMB1_ SDA	CPCI_SMB1_ SCL	CPCI_SMB1_AL ERT#	GND
18	N/C	N/C	N/C	GND	N/C	GND
17	N/C	GND	BP_RST#	CPCI_REQ6#	CPCI_GNT6#	GND
16	N/C	N/C	CPCI_DEG#	GND	N/C	GND
15	N/C	GND	CPCI_FAL#	CPCI_REQ5#	CPCI_GNT5#	GND
14	CPCI_AD[3 5]	CPCI_AD[3 4]	CPCI_AD[33]	GND	CPCI_AD[32]	GND
13	CPCI_AD[3 8]	GND	VCC_VIO*	CPCI_AD[37]	CPCI_AD[36]	GND
12	CPCI_AD[4 2]	CPCI_AD[4 1]	CPCI_AD[40]	GND	CPCI_AD[39]	GND
11	CPCI_AD[4 5]	GND	VCC_VIO*	CPCI_AD[44]	CPCI_AD[43]	GND
10	CPCI_AD[4 9]	CPCI_AD[4 8]	CPCI_AD[47]	GND	CPCI_AD[46]	GND
9	CPCI_AD[5 2]	GND	VCC_VIO*	CPCI_AD[51]	CPCI_AD[50]	GND
8	CPCI_AD[5 6]	CPCI_AD[5 5]	CPCI_AD[54]	GND	CPCI_AD[53]	GND
7	CPCI_AD[5 9]	GND	VCC_VIO*	CPCI_AD[58]	CPCI_AD[57]	GND
6	CPCI_AD[6 3]	CPCI_AD[6 2]	CPCI_AD[61]	GND	CPCI_AD[60]	GND
5	CPCI_CBE[5]#	CPCI_64EN #	VCC_VIO*	CPCI_CBE[4] #	CPCI_PAR64	GND
4	VCC_VIO*	N/C	CPCI_CBE[7] #	GND	CPCI_CBE[6]#	GND
3	CPCI_CLK 4	GND	CPCI_GNT3#	CPCI_REQ4#	CPCI_GNT4#	GND
2	CPCI_CLK 2	CPCI_CLK3	SYSEN#	CPCI_GNT2#	CPCI_REQ3#	GND

Table A-2 J2 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
1	CPCI_CLK 1	GND	CPCI_REQ1#	CPCI_GNT1#	CPCI_REQ2#	GND
** VCC_VIO - The VMICPCI-7055/CPCI-7055RC are universal VIO designs. The VMICPCI-7055/CPCI-7055RC support a 64-bit CompactPCI bus.*						

A.3 J3 Connector Pinout

The J3 connector is a five row, 19 pins each, 2 mm "Hard Metric" CompactPCI connector. An additional external metal shield is also used, labeled row F. Figure below illustrates the J3 connector and the connector pinout. This connector is used to route the two serial ports and the two Gigabit Ethernet ports to the backplane rear I/O.

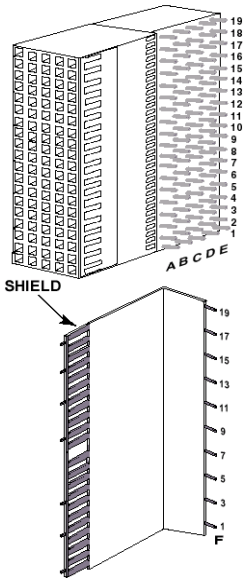


Table A-3 J3 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	GND	GND	GND	GND	GND
18	LPA_BI_DA+	LPA_BI_DA 2-	GND	LPA_BI_DC+	LPA_BI_DC-	GND
17	LPA_BI_DB+	LPA_BI_DB 2-	GND	LPA_BI_DD+	LPA_BI_DD-	GND
16	LPB_BI_DA+	LPB_BI_DA 2-	GND	LPB_BI_DC+	LPB_BI_DC-	GND
15	LPB_BI_DB+	LPB_BI_DB 2-	GND	LPB_BI_DD+	LPB_BI_DD-	GND
14	GND	GND	GND	GND	GND	GND
13	SP2_RTS	SP1_RI	SP2_DSR	SP2_DCD	SP2_CTS	GND
12	SP1_RTS	SP2_DTR	VCC_5.0	SP1_CTS	GND	GND
11	SP2_TXB	SP2_RXD	SP1_DTR	SP1_DCD	LPA_BI_DC-	GND
10	SP1_TXB	SP1_RXD	SP1_DSR	SP2_RI	LPA_BI_DD2 -	GND
9	GND	GND	N/C	GND	LPB_BI_DC2 -	GND
8	LPA_BI_DA2 +	LPA_BI_DA 2-	SP2_ACTIV E	LPA_BI_DC2+	LPB_BI_DD2 -]	GND
7	LPA_BI_DB2 +	LPA_BI_DB 2-	SP2_LOOPB ACK	LPA_BI_DD2+	GND	GND
6	LPB_BI_DA2 +	LPB_BI_DA 2-	SP2_R485/ 232	LPB_BI_DC2+	GND	GND
5	LPB_BI_DB2 +	LPB_BI_DB 2-	SP1_ACTIV E	LPB_BI_DD2+	N/C	GND
4	GND	GND	VCC_5.0	GND	VCC_3.3	GND
3	G1_Y_LINK1 00#	G1_G_LK10 00#	SP1_R485/ 232	GND	VCC_3.3	GND
2	G1_G_LINK1 0#	G1_Y_ACT	SP1_LOOPB ACK	G2_Y_LINK100 #	G2_G_LK10 00#	GND

Table A-3 J3 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
1	N/C	N/C	N/C	G2_G_LINK10#	G2_Y_ACT#	GND

NOTE

Backplane designs should route P3 signals straight through to rear J3. Then VMIACC-7055/ACC-7055RC boards can then be utilized. Although the two Gigabit Ethernet ports are available on the VMIACC-7055/ACC-7055RC, they can only be used when the VMICPCI-7055/CPCI-7055RC have a value of '1' in the options' D field, which allows for Ethernet via CompactPCI J3 (not PICMG 2.16 compatible). Contact Sales for ordering information.

A.4 J5 Connector Pinout

The VMICPCI-7055/CPCI-7055RC J5 connector is a 2 mm "Hard Metric" CompactPCI connector, with five rows of 22 pins each. An additional external metal shield is also used, labeled row F. This connector is used to route the I/O signals of PMC Site #1, and the IDE signals to the backplane I/O. This connector's controlled impedance minimizes unwanted signal reflections. Figure below illustrates the J5 connector and the connector pinout.

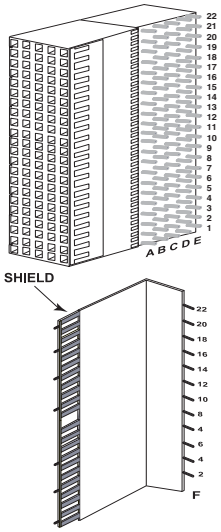


Table A-4 J5 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
22	PMC1_IO[5]	PMC1_IO[4]	PMC1_IO[3]	PMC1_IO[2]	PMC1_IO[1]	GND
21	PMC1_IO[10]	PMC1_IO[9]	PMC1_IO[8]	PMC1_IO[7]	PMC1_IO[6]	GND
20	PMC1_IO[15]	PMC1_IO[14]	PMC1_IO[13]	PMC1_IO[12]	PMC1_IO[11]	GND
19	PMC1_IO[20]	PMC1_IO[19]	PMC1_IO[18]	PMC1_IO[17]	PMC1_IO[16]	GND
18	PMC1_IO[25]	PMC1_IO[24]	PMC1_IO[23]	PMC1_IO[22]	PMC1_IO[21]	GND
17	PMC1_IO[30]	PMC1_IO[29]	PMC1_IO[28]	PMC1_IO[27]	PMC1_IO[26]	GND
16	PMC1_IO[35]	PMC1_IO[34]	PMC1_IO[33]	PMC1_IO[32]	PMC1_IO[31]	GND
15	PMC1_IO[40]	PMC1_IO[39]	PMC1_IO[38]	PMC1_IO[37]	PMC1_IO[36]	GND
14	PMC_IO[45]	PMC1_IO[44]	PMC1_IO[43]	PMC1_IO[42]	PMC1_IO[41]	GND
13	PMC1_IO[50]	PMC1_IO[49]	PMC1_IO[48]	PMC1_IO[47]	PMC1_IO[46]	GND
12	PMC1_IO[55]	PMC1_IO[54]	PMC1_IO[53]	PMC1_IO[52]	PMC1_IO[51]	GND
11	PMC1_IO[60]	PMC1_IO[59]	PMC1_IO[58]	PMC1_IO[57]	PMC1_IO[56]	GND
10	VCC_5.0	PMC1_IO[64]	PMC1_IO[63]	PMC1_IO[62]	PMC1_IO[61]	GND

Table A-4 J5 Connector and Pinout

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
9	IDE_DA[0]	GND	GND	IDE_DA[2]	N/C	GND
8	IDE_DA[1]	IDE_D[8]	IDE_IORDY #	IDE_D[0]	N/C	GND
7	IDE_DIOR#	IDE_D[9]	IDE_CS1#	IDE_D[1]	VCC_5.0	GND
6	IDE_DIOW#	IDE_D[10]	HD_ACTA #	IDE_D[2]	N/C	GND
5	UDMA_Sec_DETECT	IDE_D[11]	IDE_CS3#	IDE_D[3]	GND	GND
4	IDE_CBLIO#	IDE_D[12]	IDE_INTRQ	IDE_D[7]	N/C	GND
3	N/C	IDE_D[13]	IDE_DMACK#	IDE_D[6]	N/C	GND
2	N/C	IDE_D[14]	IDE_DMARQ	IDE_D[5]	VCC_3.3	GND
1	N/C	IDE_D[15]	IDE_RESET#	IDE_D[4]	N/C	GND

A.5 Ethernet Connector LAN0 (J28) and Pinout

The pinout and diagram for the RJ45 Gigabit Ethernet connector (J28) is shown in Figure A-1.

Figure A-1 Ethernet Connector and Pinout

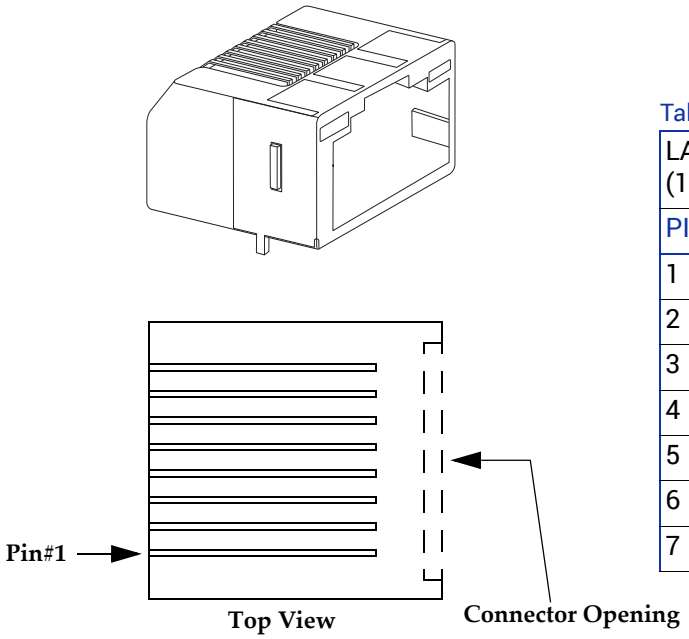


Table A-5 J28 Connector Pinout

LAN0 (J28) Ethernet Connector (1000 Mbit)	
PIN	Signal Name
1	MDI_0+
2	MDI_0-
3	MDI_1+
4	MDI_1-
5	MDI_2+
6	MDI_2-
7	MDI_3+

A.6 Serial Connector COM0 (J29) and Pinout

The COM0 serial port connector is a front panel mounted RJ45 connector as shown in the drawing in Figure A-2.

Figure A-2 Serial Connector and Pinout

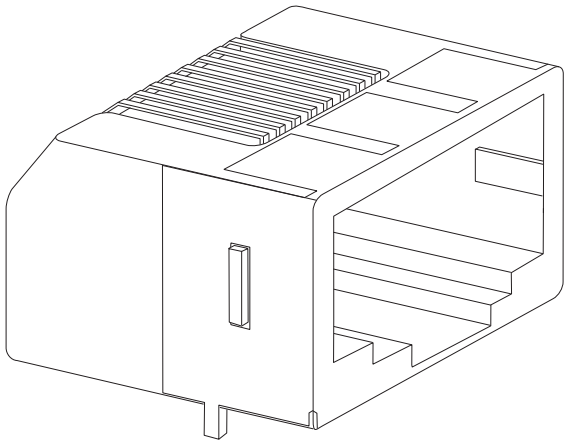


Table A-6 J29 Connector Pinout

COM0 SERIAL PORT CONNECTOR J29	
PIN	Assignment
1	DCD
2	RTS
3	GND
4	TXD
5	RXD
6	GND
7	CTS
8	DTR

NOTE
An RJ45 to DB9 adapter cable (Part Number 360-010030-002 (non-RoHS) or 42G7602-0002 (RoHS) is shipped with the VMICPCI-7055/CPCI-7055RC. The RJ45 pinout supports asynchronous RS232 mode only.

DB9	Assignment
1	DCD
2	RXD
3	TXD
4	DTR
5	GND
6	NC
7	RTS
8	CTS
9	NC

A.7 PMC Connectors and Pinouts

A.7.1 PMC#1 (J11) and PMC#2 (J21) Connector and Pinout

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-7 through A-9 are the pinouts for the PMC connectors.

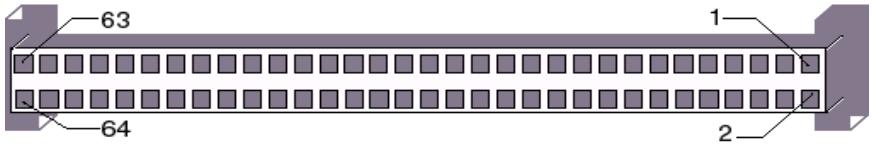


Table A-7 PMC#1 (J11) and PMC#2 (J21) Connector Pinout

PMC Connector (J11/J21)				PMC Connector (J11/J21)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12 V	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5.0 V
7	PMC1_PRSNT	8	+5.0 V	39	PCIXCAP	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	PMC1_SB0#
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	Px_VIO	46	AD[15]
15	GND	16	GNT[0]#	47	AD[12]	48	AD[11]
17	REQ0#	18	+5.0 V	49	AD[9]	50	+5.0 V
19	Px_VIO	20	AD[31]	51	GND	52	C/BE#[0]
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE#[3]	57	Px_VIO	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5.0 V	61	AD[0]	62	+5.0 V
31	Px_VIO	32	AD[17]	63	GND	64	REQ64#

A.7.2 PMC#1 (J12) and PMC#2 (J22) Connector and Pinout

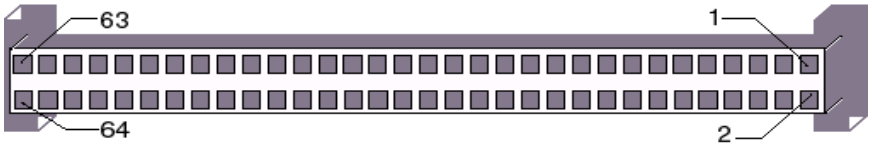


Table A-8 PMC#1 (J12) and PMC#2 (J22) Connector Pinout

PMC Connector (J12/J22)				PMC Connector (J12/J22)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	Px_VIO	33	GND	34	N/C
3	GND	4	N/C	35	TRDY#	36	+3.3 V
5	Px_VIO	6	GND	37	GND	38	STOP#
7	GND	8	N/C	39	PERR#	40	GND
9	N/C	10	N/C	41	+3.3 V	42	SERR#
11	BMODE2#	12	+3.3 V	43	C/BE#[1]	44	GND
13	RESET#	14	GND	45	AD[14]	46	AD[13]
15	+3.3 V	16	GND	47	M66EN	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3 V
19	AD[30]	20	AD[29]	51	AD[7]	52	N/C
21	GND	22	AD[26]	53	+3.3 V	54	N/C
23	AD[24]	24	+3.3 V	55	N/C	56	GND
25	IDSEL	26	AD[23]	57	N/C	58	N/C
27	+3.3 V	28	AD[20]	59	GND	60	N/C
29	AD[18]	30	GND	61	ACK64#	62	+3.3 V
31	AD[16]	32	C/BE#[2]	63	GND	64	NC

A.8 PMC#1 (J13) and PMC#2 (J23) Connector and Pinout

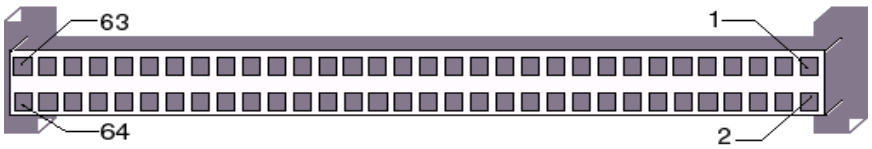


Table A-9 PMC#1 J13 Connector Pinout

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	AD[48]
3	GND	4	C/BE#[7]	35	AD[47]	36	AD[46]
5	C/BE#[6]	6	C/BE#[5]	37	AD[45]	38	GND
7	C/BE#[4]	8	GND	39	VIO	40	AD[44]
9	VIO	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	VIO	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	VIO	58	AD[32]
27	GND	28	AD[52]	59	N/C	60	N/C
29	AD[51]	30	AD[50]	61	N/C	62	GND
31	AD[49]	32	GND	63	GND	64	N/C

A.9 PMC#1 (J13) and PMC#2 (J23) Connector and Pinout

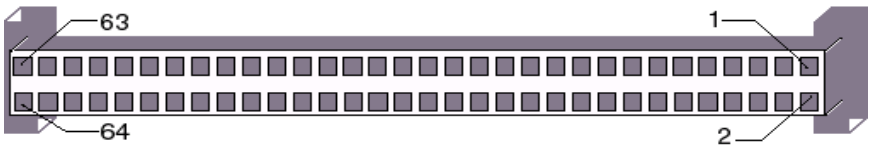


Table A-10 PMC#1 J13 Connector Pinout

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	GND	33	GND	34	AD[48]
3	GND	4	C/BE#[7]	35	AD[47]	36	AD[46]
5	C/BE#[6]	6	C/BE#[5]	37	AD[45]	38	GND
7	C/BE#[4]	8	GND	39	VIO	40	AD[44]
9	VIO	10	PAR64	41	AD[43]	42	AD[42]
11	AD[63]	12	AD[62]	43	AD[41]	44	GND
13	AD[61]	14	GND	45	GND	46	AD[40]
15	GND	16	AD[60]	47	AD[39]	48	AD[38]
17	AD[59]	18	AD[58]	49	AD[37]	50	GND
19	AD[57]	20	GND	51	GND	52	AD[36]
21	VIO	22	AD[56]	53	AD[35]	54	AD[34]
23	AD[55]	24	AD[54]	55	AD[33]	56	GND
25	AD[53]	26	GND	57	VIO	58	AD[32]
27	GND	28	AD[52]	59	N/C	60	N/C
29	AD[51]	30	AD[50]	61	N/C	62	GND
31	AD[49]	32	GND	63	GND	64	N/C

A.10 PMC#1 (J14) Connector and Pinout

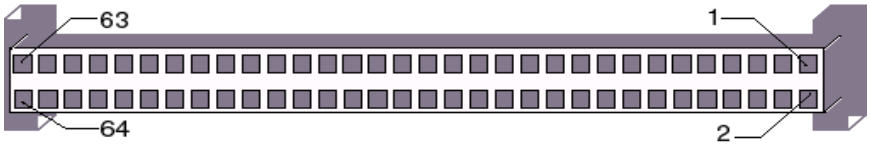


Table A-11 PMC#1 J14 Connector Pinout

PMC Connector (J14)				PMC Connector (J14)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	PMC1_IO[1]	2	PMC1_IO[2]	33	PMC1_IO[33]	34	PMC1_IO[34]
3	PMC1_IO[3]	4	PMC1_IO[4]	35	PMC1_IO[35]	36	PMC1_IO[36]
5	PMC1_IO[5]	6	PMC1_IO[6]	37	PMC1_IO[37]	38	PMC1_IO[38]
7	PMC1_IO[7]	8	PMC1_IO[8]	39	PMC1_IO[39]	40	PMC1_IO[40]
9	PMC1_IO[9]	10	PMC1_IO[10]	41	PMC1_IO[41]	42	PMC1_IO[42]
11	PMC1_IO[11]	12	PMC1_IO[12]	43	PMC1_IO[43]	44	PMC1_IO[44]
13	PMC1_IO[13]	14	PMC1_IO[14]	45	PMC1_IO[45]	46	PMC1_IO[46]
15	PMC1_IO[15]	16	PMC1_IO[16]	47	PMC1_IO[47]	48	PMC1_IO[48]
17	PMC1_IO[17]	18	PMC1_IO[18]	49	PMC1_IO[49]	50	PMC1_IO[50]
19	PMC1_IO[19]	20	PMC1_IO[20]	51	PMC1_IO[51]	52	PMC1_IO[52]
21	PMC1_IO[21]	22	PMC1_IO[22]	53	PMC1_IO[53]	54	PMC1_IO[54]
23	PMC1_IO[23]	24	PMC1_IO[24]	55	PMC1_IO[55]	56	PMC1_IO[56]
25	PMC1_IO[25]	26	PMC1_IO[26]	57	PMC1_IO[57]	58	PMC1_IO[58]
27	PMC1_IO[27]	28	PMC1_IO[28]	59	PMC1_IO[59]	60	PMC1_IO[60]
29	PMC1_IO[29]	30	PMC1_IO[30]	61	PMC1_IO[61]	62	PMC1_IO[62]
31	PMC1_IO[31]	32	PMC1_IO[32]	63	PMC1_IO[63]	64	PMC1_IO[64]

B • IPMI Firmware and OEM Extensions

The IPMI firmware provides all the mandatory standard commands specified in the IPMI 1.5 framework. The firmware also provides functionality beyond that of a normal Peripheral Manager, by implementing several commands in the OEM range (per IPMI spec).

NOTE
IPMI is no longer supported. Older boards may have IPMI.

B.1 Standard IPMI Commands

The Abaco IPMI firmware implements all "Required" commands for a Peripheral Manager per the IPMI 1.5 spec, as well as some of the "Optional" commands.

B.1.1 Get Device ID

This command is used to retrieve the Intelligent device's Hardware Revision, Firmware/Software Revision, and Sensor and Event Interface Command specification revision information.

Table B-1 NetFn 0x06, Cmd 0x01

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	
	2	00	Device ID	Unspecified
	3	00	Device Revision	Unspecified
	4	02[1]	Firmware Revision byte 1	Firmware revision 1.08
	5	11[1]	Firmware Revision byte 2	
	6	51	IPMI Version	IPMI version 1.5
	7	2b	Additional device support	The following bits are set: [5] IPMB Event Generator [3] FRU Inventory Device [1] SDR Repository Device [0] Sensor Device
	8:10	CO 33 00	Manufacturer ID	
	11:12 [2]	0878	Product ID	

1. Depends on the version of firmware installed on the board.
2. Depends on the type of device.

B.1.2 Cold Reset

This command performs a “Cold Reset” of the IPMI subsystem. This causes default setting of interrupt enables, event message generation, sensor scanning, threshold values and other “power up default” states to be restored.

Table B-2 NetFn 0x06, Cmd 0x02

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	

B.1.3 Warm Reset

While there are two commands, one for a cold reset, and one for a warm reset, the firmware does not distinguish between them and always performs a cold reset.

Table B-3 NetFn 0x06, Cmd 0x03

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	

B.1.4 Get Self-Test Results

This command returns the results of the Power-On Self Test.

Table B-4 NetFn 0x06, Cmd 0x04

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	
	2	55h 56h 57h 58h FFh All other	No error. All Self-Tests Passed. Self-Test not implemented in this controller. Corrupted or inaccessible data or devices. Fatal hardware error. Reserved. Device-specific 'internal' failure.	
	3	XXh	If byte 2 is 55h, 56h or FFh, then 00h. If byte 2 is 58h or All other, then device specific. If byte 2 is 57h, then Self-test error bit field. 1b means 'failed', 0b means 'unknown'. [7] 1b = cannot access SEL device [6] 1b = cannot access SDR repository [5] 1b = cannot access FRU device [4] 1b = IPMB signal lines do not respond [3] 1b = SDR repository empty [2] 1b = Internal use area of FRU corrupted [1] 1b = controller update 'boot block' firmware corrupted [0] 1b = controller operational firmware corrupted	

B.1.5 Set ACPI Power State

This command is used to set the platform management subsystem to a particular power state. The firmware does not support the ACPI power state, instead it can be used to turn off/on power to the board.

Table B-5 NetFn 0x06, Cmd 0x06

	Byte	Value	Data Field	Comments
Request-data	1	XXh	ACPI System power state	The Abaco IPMI does not have control over the system power state. Therefore, this byte is ignored.
	2	XXh	ACPI Device power state [7] – 1b = set device power state 0b = don't change device power state [6:0] – device power state 00h – Fully on 03h – Power off	
Response-data	1	XXh	Completion Code	

B.1.6 Get ACPI Power State

This command is used to get the platform management subsystem's power state. The firmware does not support the ACPI power state, instead it only returns whether the board has its power turned off/on.

Table B-6 NetFn 0x06, Cmd 0x07

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00	Completion code	
	2	2Ah	ACPI System Power State [7] – reserved [6:0] – System power state 2Ah – unknown	The Abaco IPMI subsystem does not have control over the system power.
	3	XXh	ACPI Device Power State 00h – Fully on 03h – Power off 2Ah – unknown, power state has not been initialized or device lost track of power state.	

B.1.7 Get Device GUID command

This command returns a Globally Unique ID (GUID) for the management controller. The format of the ID follows that specified in Attachment A of the *Wired for Management Baseline, Version 2.0 specification*. The ID can be used to uniquely identify an instance of a management controller. This information can be used in conjunction with the SDR information to verify that a particular controller is still present in the system.

Table B-7 NetFn 0x06, Cmd 0x08

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00h	Completion code	
	2	XXh	node	
	3	XXh	node	
	4	XXh	node	
	5	XXh	node	
	6	XXh	node	
	7	XXh	node	MS byte
	8	XXh	clock seq low	
	9	XXh	clock seq high and reserved	MS byte
	10	XXh	time high and version	
	11	XXh	time high and version	MS byte
	12	XXh	time mid	
	13	XXh	time mid	MS byte
	14	XXh	time low	
	15	XXh	time low	
	16	XXh	time low	
	17	XXh	time low	MS byte

B.1.8 Broadcast Get Device ID

This is a broadcast version of the "Get Device ID" command that is provided for the discovery of Intelligent Devices on the IPMB. It is only specified for use on the IPMB.

The response for a *Broadcast 'Get Device ID'* is the same as that returned for a *'Get Device ID'* command.

B.1.9 Master-Write-Read

This command can be used for low-level I^2C/SMBus write, read, or write-read accesses to the IPMB or private buses behind the management controller.

Table B-8 NetFn 0x06, Cmd 0x52

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Bus ID: [7:4] channel number [3:1] bus ID, 0-based [0] bus type 0 = public (IPMB) 1 = private bus	This byte can take one of the following three values, depending on which bus will be used: 0x0 = I2C0 (IPMB) 0x3 = I2C1 (CPCI-SMB) 0xf = I2C2 Local I^2C
	2	XXh	Slave Address [0] - reserved	
	3	XXh	Read count – number of bytes to read 1 based, 0 = no bytes to read.	
	4:N		Data to write	
Response-data	1	XXh	Completion code 00h – if successful 81h – Lost Arbitration 82h – Bus Error 83h – NAK on Write 84h – Truncated Read	
	2:M		Bytes read from the specified slave address.	

B.1.10 Set Event Receiver

This command sets the slave address and the LUN of the Event Receiver, which will receive the Event Messages generated by the Abaco IPMI subsystem.

Table B-9 NetFn 0x04, Cmd 0x00

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Event Receiver Slave Address. 0FFh disables Event message generation [7:1] - IPMB (I^2C) slave address [0] - 0	
	2	XXh	[7:2] – reserved [1:0] – Event receiver LUN	
Response-data	1	00	Completion code	

For a list of platform events generated by the Abaco IPMI subsystem see *"Platform Events" on page 65*.

B.1.11 Get Event Receiver

This command gets the current setting for the Event Receiver slave address and LUN.

Table B-10 NetFn 0x04, Cmd 0x01

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	XXh	Completion code	
	2	XXh	Event Receiver Slave Address. 0FFh disables Event message generation [7:1] - IPMB (I^2C) slave address [0] - 0	
	3	XXh	[7:2] – reserved [1:0] – Event receiver LUN	

B.1.12 Get Sensor Reading

This command returns the present reading for the sensor. Sensors are periodically scanned, and the last reading will be immediately returned in response to this command.

Table B-11 NetFn 0x04, Cmd 0x2D

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Sensor Number (FFh reserved)	
Response-data	1	00h	Completion code	
	2	XXh	Sensor reading	
	3	XXh	[7] – 0b =All event messages disabled for this sensor [6] - 0b = sensor scanning disabled [5] – 1b =Initial update in progress. [4-0] – reserved	
	4	XXh	For threshold-based sensors, present threshold comparison status. For discrete reading sensors, State 0-7 assert condition.	
	5	XXh	State 8-14 assert condition	Optional for discrete reading sensors

The Abaco IPMI subsystem contains several sensors. They provide the voltages and temperature reading of the system. The various sensor settings like threshold, hysteresis, event enable, etc., are statically configured in the Sensor Data Records.

Sensor No	Type	Comments
0x41	3.3 V	Switched on/off by hotswap controller, *BDSEL etc.
0x42	5 V	Switched on/off by hotswap controller, *BDSEL etc.
0x43	3.3 V IN backplane	
0x44	5 V IN backplane	
0x60	Temp Sensor	
0x61	Temp Sensor	

The sensor readings returned are in their "raw" values; to convert them to actual values use the following formulas below.

a. For 3.3 V sensors

$V_a = (V_r / 256) * (3.3 / 2.5) * 3.3$

Where V_a = actual voltage

V_r = "raw" sensor reading

e.g.: if sensor 0x41 says 0xC0 (192 decimal), the actual voltage is (192/256) * 3.3/2.5 * 3.3 = 3.267 V.

b. For 5 V sensors

$V_a = (V_r / 256) * 3.3 * 2$

Where V_a = actual voltage

V_r = "raw" sensor reading

e.g.: if sensor 0x44 says 0xC3 (195 decimal), the actual voltage is (195/256) * 3.3 * 2 = 5.027 V.

c. For Temp sensors

$T_a = T_r$

Where T_a = actual temperature in ^oC

T_r = "raw" sensor reading

e.g.: if sensor 0x61 says 0x1f (31 decimal), the actual temperature is 31^oC.

B.1.13 FRU Inventory Area Info

This command is used to obtain information about the size and access method of the FRU Inventory data in the device.

Table B-12 NetFn 0x0A, Cmd 0x10

	Byte	Value	Data Field	Comments
Request-data	1	XXh	FRU device ID. FFh reserved.	
Response-data	1	00h	Completion code	
	2	XXh	FRU inventory area size in bytes, LS Byte.	
	3	XXh	FRU inventory area size in bytes, MS Byte.	
	4	XXh	[7:1] – reserved [0] – 0b = accessed by bytes 1b = accessed by words	

B.1.14 Read FRU Data

This command returns the specified data from the FRU Inventory Info area. No parsing of the FRU data is performed by the IPMI subsystem; system management software is responsible for interpreting the FRU data.

Table B-13 NetFn 0x0A, Cmd 0x11

	Byte	Value	Data Field	Comments
Request-data	1	XXh	FRU device ID. FFh reserved.	
	2	XXh	FRU Inventory offset to read. LS Byte.	
	3	XXh	FRU Inventory offset to read. MS Byte.	Offset is in words or bytes per device access type returned in the FRU Inventory Area Info command.
	4	XXh	Count to read – 1 based	
Response-data	1	00	Completion code	
	2	XXh	Count returned – 1 based	
	3:2+N		Requested data	

The FRU data conforms to the *IPMI FRU Information Storage Definition v 1.0* specification. All Abaco IPMI-enabled boards come with the FRU data preloaded; the specific data is documented in *"FRU Data Specification" on page 64*.

B.1.15 Write FRU Data

This command writes the specified byte or word to the FRU Inventory Info area. No parsing of the FRU data is performed by the IPMI subsystem; system management software is responsible for creating valid FRU data structures and writing the data to the FRU area.

Table B-14 NetFn 0x0A, Cmd 0x12

	Byte	Value	Data Field	Comments
Request-data	1	XXh	FRU device ID. FFh reserved.	
	2	XXh	FRU Inventory offset to write. LS Byte.	
	3	XXh	FRU Inventory offset to write. MS Byte.	
	4:3+N		Data to write	
Response-data	1	XXh	Completion code 00h – successful 80h – Write protected	
	2	XXh	Count written – 1 based	

B.1.16 Get SDR Repository Info

This command returns the SDR command version for the SDR Repository.

Table B-15 NetFn 0x0A, Cmd 0x20

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00h	Completion code	
	2	51h	SDR Version.	
	3	XXh	Record count LS Byte.	
	4	XXh	Record count MS Byte.	
	5:6	XXXXh	Free space in bytes. LS Byte first. 000h indicates 'full' FFFEh indicates 64KB-2 or more, FFFFh indicates 'unspecified'.	
	7:10	00000000h	Most recent addition timestamp. LS Byte first.	Add SDR or Partial-Add SDR command not supported, always returns 00000000.
	11:14	00000000h	Most recent erase (delete or clear) timestamp. LS Byte first.	Delete SDR or Clear SDR command not supported, always returns 00000000.
	15	02h	Operation Support [7] – Overflow flag =1	Only Reserve SDR Repository command supported.

B.1.17 Reserve SDR Repository Command

This command is used to set the present 'owner' of the repository, as identified by the 'Software ID' or by the Requester's Slave Address from the command. The reservation process provides a limited amount of protection on repository access from the IPMB when records are being incrementally read.

Table B-16 NetFn 0x0A, Cmd 0x22

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	00h	Completion Code.	
	2	XXh	Reservation ID, LS Byte.	
	3	XXh	Reservation ID, MS Byte.	

B.1.18 Get SDR Command

This command returns the sensor record specified by 'Record ID'. The command also accepts a 'byte range' specification that allows just a selected portion of the record to be retrieved. The Requester must first reserve the SDR Repository using the 'Reserver SDR Repository' command in order for an incremental read to an offset other than 0000h to be accepted.

If 'Record ID' is specified as 0000h, this command returns the Record Header for the 'first' SDR in the repository. FFFFh specifies that the 'last' SDR in the repository should be listed. If 'Record ID' is non-zero, the command returns the information from the matching record, and the Record ID for the *next* SDR in the repository.

Table B-17 NetFn 0x0A, Cmd 0x23

	Byte	Value	Data Field	Comments
Request-data	1	XXh	Reservation ID, LS Byte.	Only required for partial reads with a non-zero 'Offset into record' field. Use 0000h otherwise.
	2	XXh	Reservation ID, MS Byte.	
	3	XXh	Record ID of record to Get, LS Byte.	
	4	XXh	Record ID of record to Get, MS Byte.	
	5	XXh	Offset into record.	
	6	XXh	Bytes to read, FFh means read entire record.	
Response-data	1	XXh	Completion Code	
	2	XXh	Record ID for next record, LS Byte.	
	3	XXh	Record ID for next record, MS Byte.	
	4:3+N	XXh	Record Data	

B.2 FRU Data Specification

Abaco boards have data pre-loaded into the FRU area to provide basic information about the board. The FRU data conforms to the '*Platform Management FRU Information Storage Definition'*, Revision 1.1. Please refer to this document, available from Intel®, for the exact meaning of the various fields.

Only the Board Info and Product Info areas are utilized. An example of the entire contents of the FRU EEPROM is given below:

```
0000  01 00 00 01 00 00 00 FE-01 09 00 E8 44 41 D9 47  DA.G
0010  45 20 46 41 4E 55 43 20-45 6D 62 65 64 64 65 64  Abaco
0020  20 53 79 73 74 65 6D 73-CC 56 4D 49 43 50 43 49  Systems.CPCI
0030  2D 37 38 30 36 C5 31 30-30 30 31 CE 33 35 30 2D   -7055.10001.350-
0040  36 35 37 38 30 36 2D 32-31 30 C0 C1 00 00 00 B1   657055-000......
0050  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0060  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0070  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0080  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
0090  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00A0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00B0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00C0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00D0  00 00 00 00 00 00 00 00-00 00 00 00 00 00 00 00   ................
00E0  CA 45 54 F3 90 B6 80 49-94 B0 0B F8 C2 78 47 FD   .ET....I.....xG.
00F0  C0 33 00 06 78 00 00 00-00 00 00 00 00 00 00 00   .3..x...........
```

B.3 Platform Events

The Abaco IPMI subsystem contains several sensors for reading the voltages and temperature of the system. Each sensor is configured with a threshold, hysteresis, and nominal value. When the value of a sensor crosses a threshold, a platform event is sent to the "Event Receiver".

The following events are generated by the Abaco IPMI Subsystem:

- Threshold Events – Events of this type are generated if the sensors exceed their threshold settings. Threshold events are either an Assertion Event or a De-Assertion Event.

Table B-18 NetFn 0x04, Cmd 0x02

	Byte	Value	Data Field	Comments
Request-data	-	-	Generator ID (RqSA, RqLun)	
	1	03h	EvMRev	IPMB v 1.0 message
	2	XXh	Sensor Type	02h = voltage sensors 01h = temperature sensors
	3	XXh	Sensor #	Sensor numbers will be one of 41h, 42h, 43h, 44h, 60h or 61h
	4	XXh	[7] - Event Dir 0b = Assertion Event 1b = De-assertion Event [6:0] - Event Type	Event Type indicates the type of threshold crossing that produced the event.
	5	XXh	Event Data 1 [7:6] – 01b = trigger reading in byte2 [5:4] – 01b = trigger threshold value in byte3 [3:0] - offset from Event/ Reading code for threshold event	
	6	XXh	Event Data 2	Sensor reading
	7	XXh	Event Data 3	Threshold value that triggered event.
Response-data	1	XXh	Completion Code	

The Generator ID field is a required element of an Event Request Message. For IPMB messages, this field is equated to the Requestor's Slave Address and LUN fields. Thus, the Generator ID information is not carried in the data field of an IPMB request message.

B.4 Chassis Control

All Abaco IPMI-enabled boards include extra circuitry to enable the IPMI controller to monitor and control certain CompactPCI signals. These functions are controlled by sending IPMI packets from the VMICPCI-7055/CPCI-7055RC processor cards to the controller.

B.4.1 Get Geographical Address

This command returns the Slave Address based on the Geographical Slot the board is inserted into.

Table B-19 NetFn 0x30, Cmd 0x01

	Byte	Value	Data Field	Comments
Request-data	-	-		
Response-data	1	XXh	Completion code	
	2	XXh	Geographical address	

B.5 BMC Functions

The Abaco IPMI firmware can perform some of the functions of a Baseboard Management Controller. The firmware can send IPMI commands to other targets on the IPMB on behalf of the VMICPCI-7055/CPCI-7055RC and return the responses to the VMICPCI-7055/CPCI-7055RC. It can also forward any platform events it receives to the VMICPCI-7055/CPCI-7055RC.

B.5.1 IPMB Relay

This command allows the VMICPCI-7055/CPCI-7055RC, connected to the Zircon's I^2C1 bus, to have the Zircon send a command on its I^2C0 bus (which is connected to the IPMB pins on the backplane), and for the Zircon to send the response to that command back to the VMICPCI-7055/CPCI-7055RC on I^2C1.

NOTE
The Zircon will accept an IPMB Relay request on its I^2C0 bus, but it will always send the response to the I^2C1 bus. Therefore, any device on the IPMB that sends an IPMB Relay request to the Zircon will not receive a response.

If the request is successfully sent, then the response will be the actual response from the target system, with only a few header bytes changed to have it sent back to the VMICPCI-7055/CPCI-7055RC.

If the request cannot be relayed (due to a device not responding, or the Zircon is temporarily out of memory), the response to this command will use the NetFn and Cmd for IPMB Relay, and a completion code only.

Table B-20 NetFn 0x32, Cmd 0x00

	Byte	Value	Data Field	Comments
Request-Data	1	XXh	[7:1] – Target slave address [0] – 0	
	2	XXh	[7:6] – 0 [5:0] – NetFn	
	3	XXh	[7:2] – 0 [1:0] – LUN	
	4	XXh	Command	
	5:N	XXh	Optional Data	
Response-data	1	XXh	Completion code	
	2:N	XXh	Optional response data	See examples below

B.5.2 Forwarding of Platform Events

A chassis may contain other IPMI devices, such as an alarm card, which will generate Platform Events. The alarm card would send the event to the I^2C slave address that was provided by a "Set Event Receiver" command. The Abaco IPMI firmware will immediately acknowledge any Platform Event it receives then forward the packet to the slave address provided by a "Set Platform Event Forwarding Address" command.

The VMICPCI-7055/CPCI-7055RC should not send a response for the Platform Event to the Zircon nor to the originating device, as the Zircon has already responded.

Software on the VMICPCI-7055/CPCI-7055RC should set the forwarding address first then use IPMB relay to send a "Set Event Receiver" command to the alarm cards or other IPMI devices in the chassis.

B.5.3 Set Platform Event Forwarding Address

This command sets the slave address and the LUN of the Event Receiver to which the Platform Events are forwarded.

Table B-21 NetFn 0x32, Cmd 0x80

	Byte	Value	Data Field	Comments
Request-data	1	XXh	[7:1] – I^2C slave address [0] – always 0	
	2	XXh	[7:2] – 0 [1:0] – LUN	
Response-data	1	XXh	Completion code	

If the forwarding address is 0 (by default, or deliberately set), events will not be forwarded.

In all cases, any Platform Events will be acknowledged back to the original sender. The VMICPCI-7055/CPCI-7055RC should not acknowledge the forwarded event back to the IPMI controller.

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