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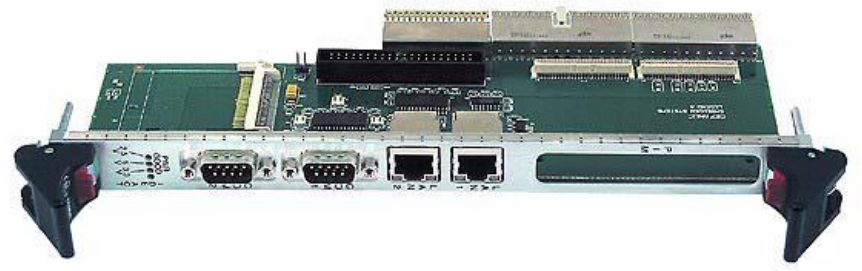
Hardware Reference Manual

VMIACC-7055*/ACC-7055RC*

CompactPCI Rear Transition Module for the VMICPCI-7055*/CPCI-7055RC*

THE VMIACC-7055/ACC-7055RC ARE DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTIONS OF HAZARDOUS SUBSTANCE (RoHS) DIRECTIVE (2015/863) CURRENT REVISION.

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Document History

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This manual may use the following types of notice:



WARNING

Warnings alert you to the risk of severe personal injury.



CAUTION

Cautions alert you to system danger or loss of data.



NOTE

Notes call attention to important features or instructions.



TIP

Tips give guidance on procedures that may be tackled in a number of ways.



LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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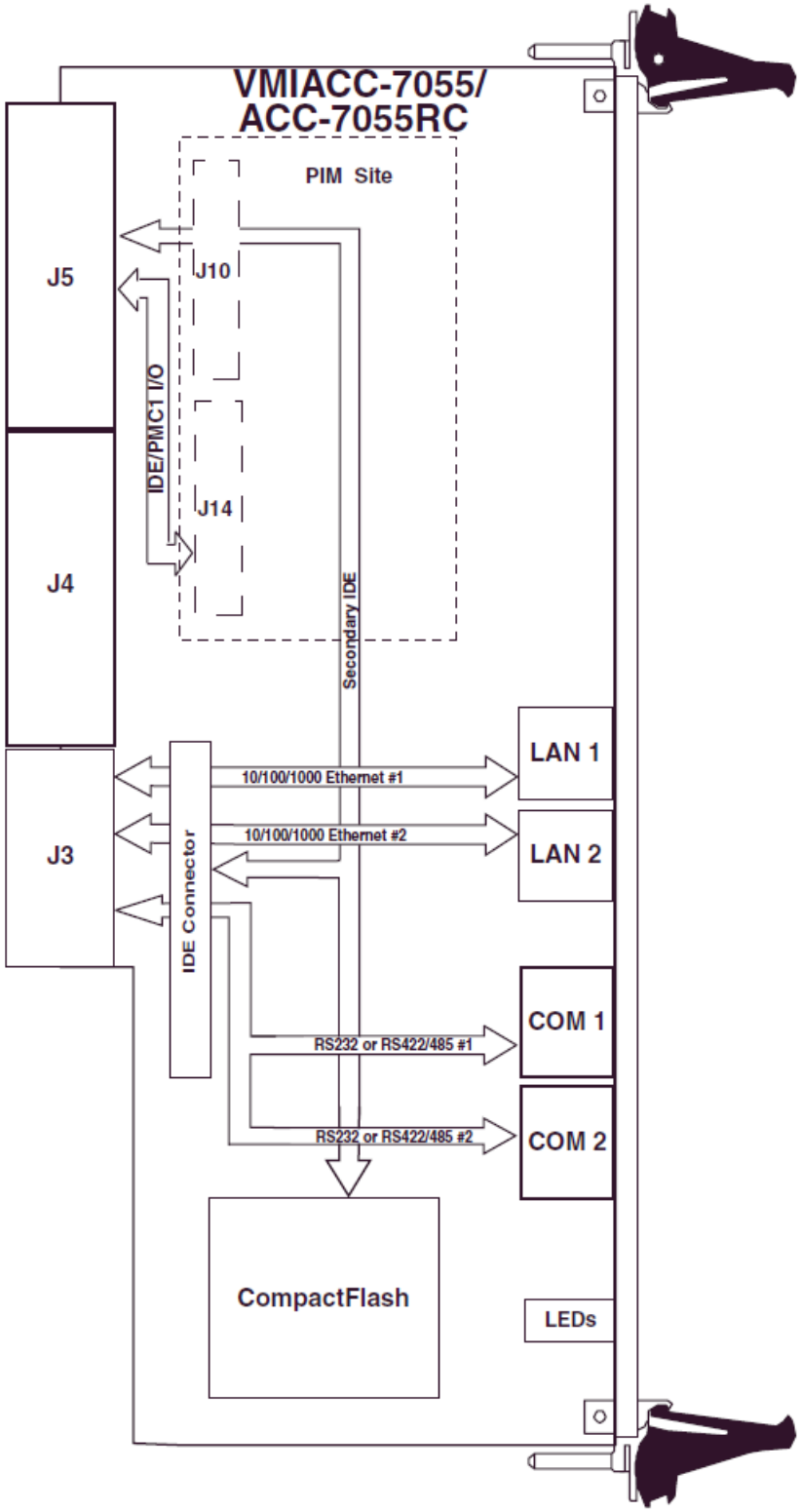
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1 • Installation

The VMIACC-7055*/ACC-7055RC* rear transition modules (RTMs) are designed to be used with the VMICPCI-7055*/CPCI-7055RC* single board computers (SBCs). The RTM is mounted in the rear I/O area of the chassis and provides associated signals to the front mounted SBC. The signals are routed to the backplane through the J3 and J5 connectors. The J4 connector is used for alignment only and has no electrical connections.

The VMIACC-7055/ACC-7055RC boards are full 6U form factor boards with a CompactFlash connector, an internal IDE header, two COM ports, two LAN ports (option dependent), and one PIM site.

Figure 1-1 VMIAC-7055/ACC-7055RC Rear Transition Module

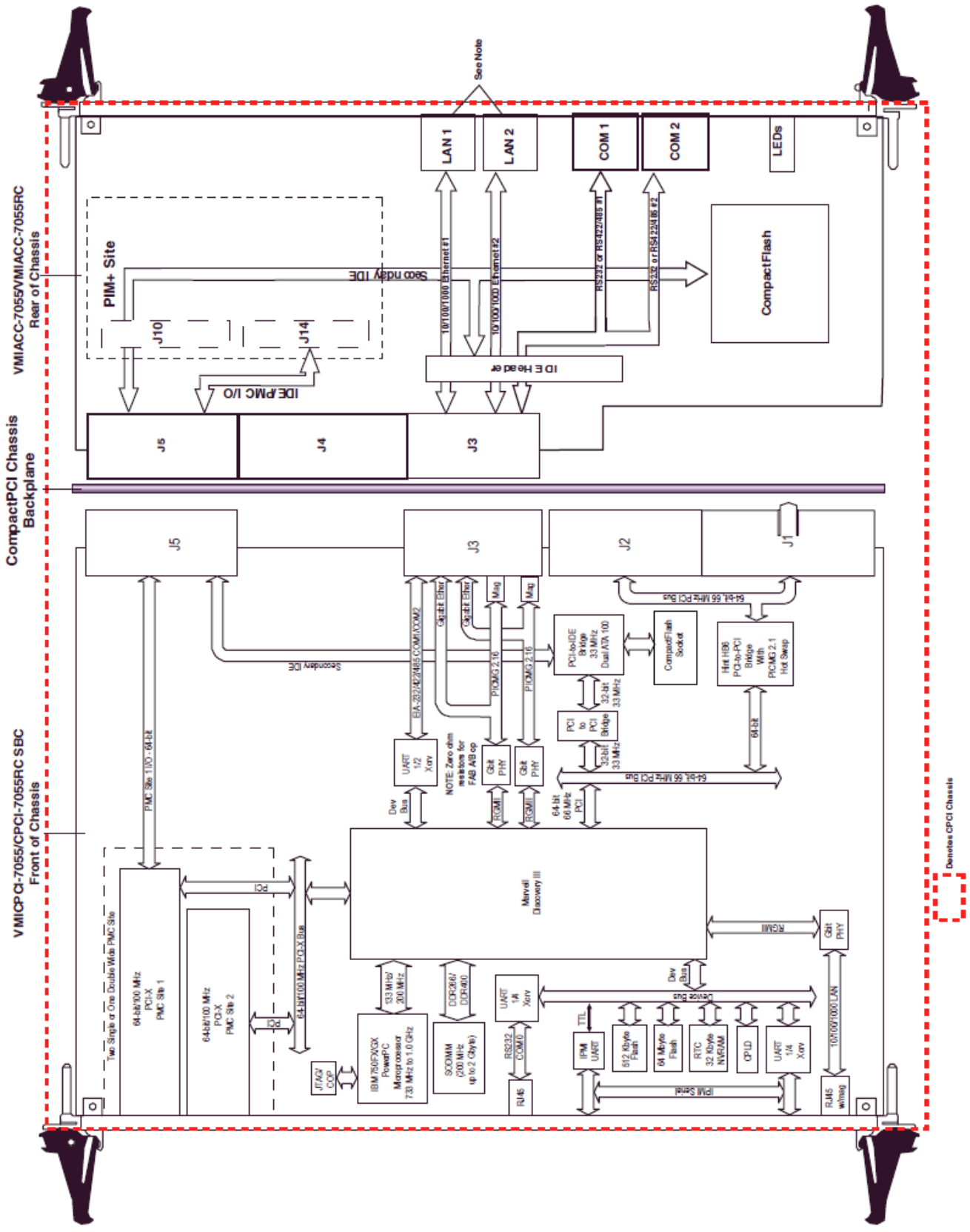


1.1 Installation of the RTM

The RTM installs in the rear I/O portion of the CompactPCI® chassis using the J4 connector as a guide. Installation of the VMIACC-7055/ ACC-7055RC is shown in Figure 1-2.

The Gbit Ethernet ports are only accessible with certain options of the VMIPCI-7055/CPCI-7055RC boards, contact Sales for more details.

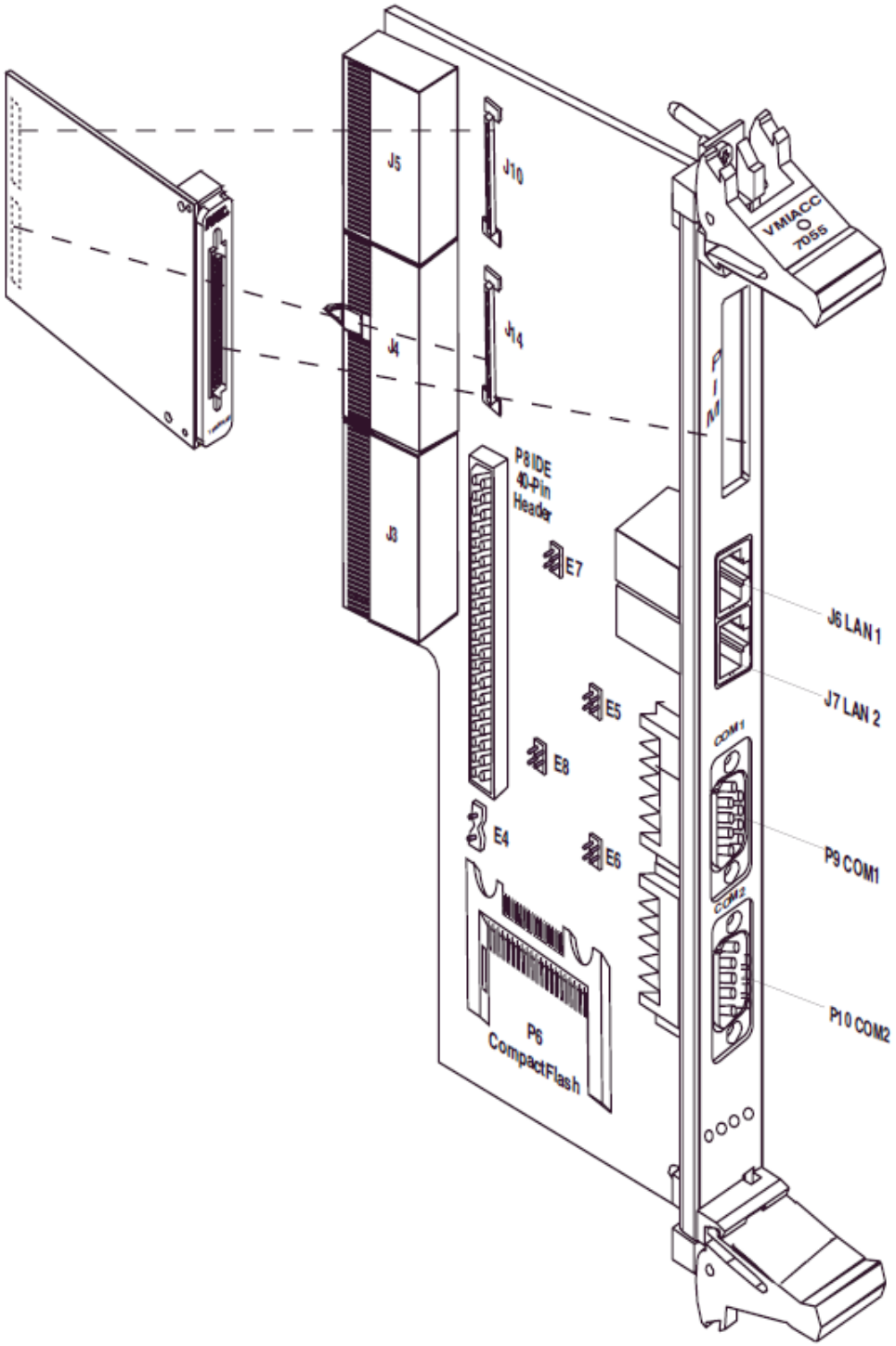
Figure 1-2 Installation of the VMIPCI-7055/CPCI-7055RC RTM with a VMICPCI-7055/CPCI-7055RC SBC



1.2 Installation of the PIM

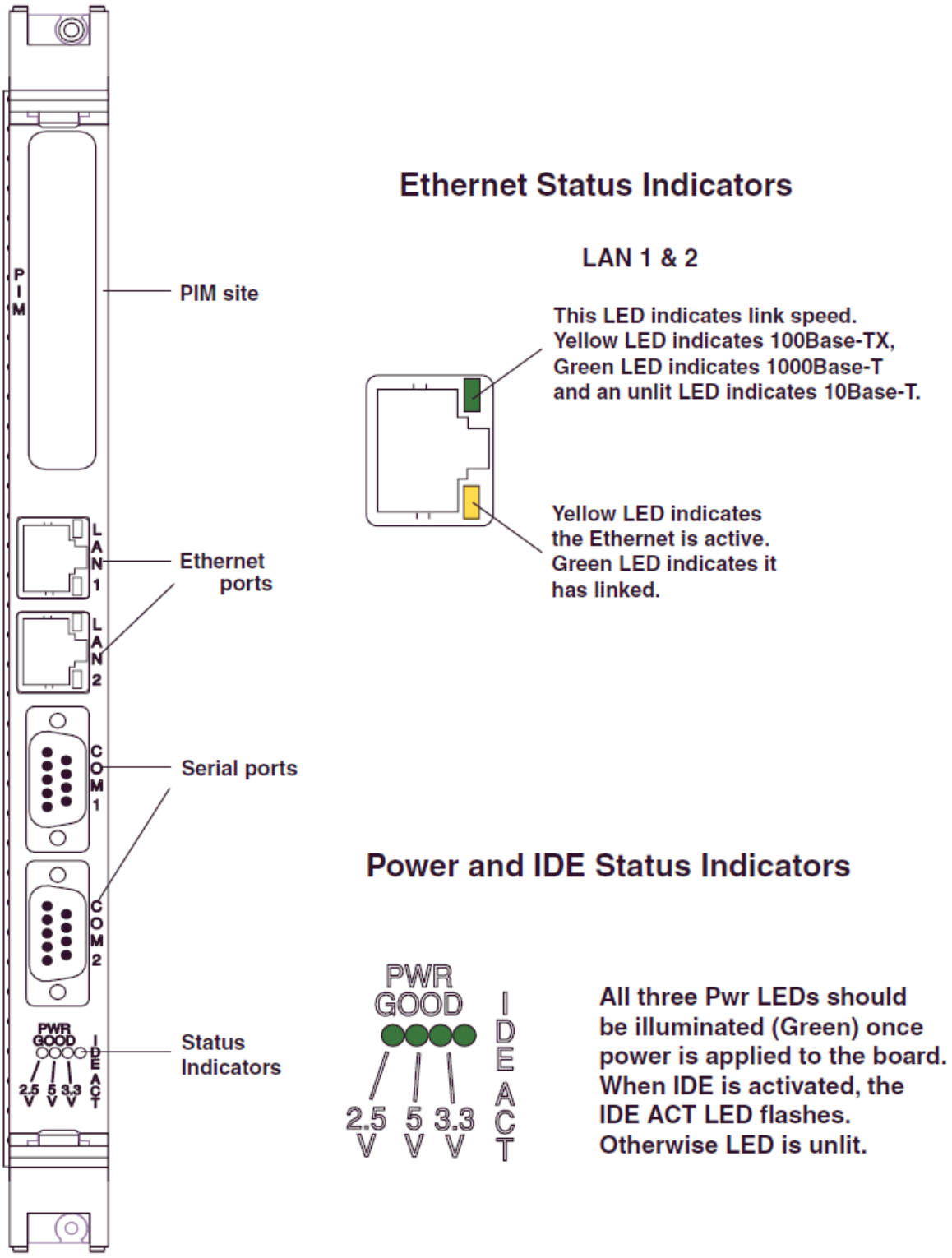
The PIM installs on the VMIACC-7055/ ACC-7055RC's PIM site using the J10 and J14 connectors.

Figure 1-3 Installing the PIM on the VMIACC-7055/ ACC-7055RC



2 • LED Definitions

Figure 2-1 LED Definitions



3 • Connectors and Headers

There is one internal IDE 40-pin header, one PIM site consisting of two 64-pin connectors, two COM ports, one CompactFlash connector and two Gigabit Ethernet ports available on the VMIACC-7055/ACC-7055RC. The J3, J4 and J5 connectors are standard CompactPCI backplane connectors. Jumpers E5, E6, E7 and E8 are used to set the mode for the COM ports. Jumper E4 is used to configure the CompactFlash for master or slave mode.

3.1 40-Pin IDE Header

When an IDE drive is connected to P8, and a CompactFlash is loaded on the P6 connector, one of them must be set as a slave. See Section 3.5.1, "CompactFlash Master and Slave Jumper (E4)" for instructions on how to set the CompactFlash as a master/slave.

NOTE

An 80-conductor cable is required for IDE interfaces above Ultra ATA/66.

Figure 3-1 P8 40-pin IDE Header (Internal)

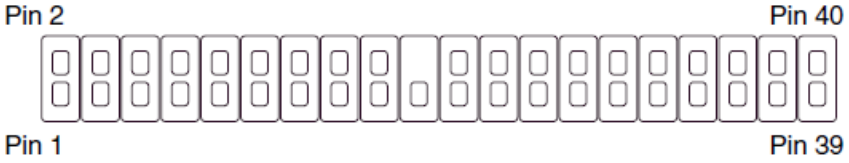


Table 3-1 40-pin IDE Header Pinout

Pin	Signal	Pin	Signal
1	IDES_RESET#	2	GND
3	IDES_ D[7]	4	IDES_D[8]
5	IDES_ D[6]	6	IDES_D[9]
7	IDES_D[5]	8	IDES_D[10]
9	IDES_D[4]	10	IDES_D[11]
11	IDES_D[3]	12	IDES_D[12]
13	IDES_D[2]	14	IDES_D[13]
15	IDES_D[1]	16	IDES_D[14]
17	IDES_D[0]	18	IDES_D[15]
19	GND	20	Key
21	IDES_DMARQ	22	GND
23	IDES_DIOW#	24	GND
25	IDES_DIOR#	26	GND
27	IDES_IORDY	28	GND
29	IDES_DMACK #	30	GND

Pin	Signal	Pin	Signal
31	IDES_INTRQ	32	5V
33	IDES_DA1	34	IDES_CBLIO#
35	IDES_DA0	36	IDES_DA2
37	IDES_CS1#	38	IDES_CS3#
39	HD_ACTA#	40	GND

3.2 PIM Site Connector and Pinout (J10)

Figure 3-2 PIM Site (J10) Connector

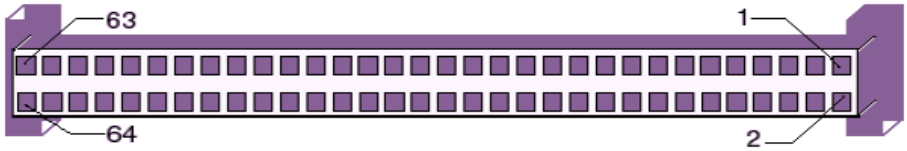


Table 3-2 PIM Site (J10) Connector Pinout

PIM Connector (J10) Left Side		PIM Connector (J10) Right Side		PIM Connector (J10) Left Side		PIM Connector (J10) Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N/C	2	N/C	33	N/C	34	GND
3	N/C	4	N/C	35	N/C	36	N/C
5	5.0VDC	6	N/C	37	5.0VDC	38	N/C
7	N/C	8	N/C	39	N/C	40	N/C
9	N/C	10	3.3VDC	41	N/C	42	3.3VDC
11	N/C	12	N/C	43	N/C	44	N/C
13	GND	14	N/C	45	GND	46	N/C
15	N/C	16	N/C	47	N/C	48	N/C
17	N/C	18	GND	49	N/C	50	GND
19	N/C	20	N/C	51	N/C	52	N/C
21	5.0VDC	22	N/C	53	5.0VDC	54	N/C
23	N/C	24	N/C	55	N/C	56	N/C
25	N/C	26	3.3VDC	57	N/C	58	3.3VDC
27	N/C	28	N/C	59	N/C	60	N/C
29	GND	30	N/C	61	N/C	62	N/C
31	N/C	32	N/C	63	N/C	64	N/C

3.3 PIM Site Connector and Pinout (J14)

Figure 3-3 PIM Site (J14) Connector

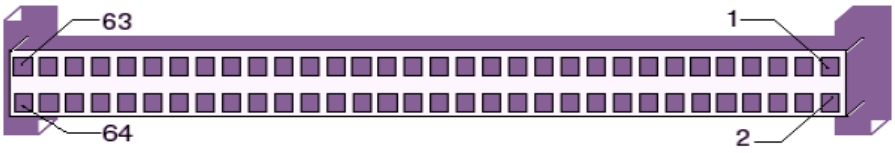


Table 3-3 PIM Site (J14) Connector Pinout

PIM Connector (J14) Left Side		Right Side		PIM Connector (J14) Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	PMC1_IO[1]	2	PMC1_IO[2]	33	PMC1_IO[33]	34	PMC1_IO[34]
3	PMC1_IO[3]	4	PMC1_IO[4]	35	PMC1_IO[35]	36	PMC1_IO[36]
5	PMC1_IO[5]	6	PMC1_IO[6]	37	PMC1_IO[37]	38	PMC1_IO[38]
7	PMC1_IO[7]	8	PMC1_IO[8]	39	PMC1_IO[39]	40	PMC1_IO[40]
9	PMC1_IO[9]	10	PMC1_IO[10]	41	PMC1_IO[41]	42	PMC1_IO[42]
11	PMC1_IO[11]	12	PMC1_IO[12]	43	PMC1_IO[43]	44	PMC1_IO[44]
13	PMC1_IO[13]	14	PMC1_IO[14]	45	PMC1_IO[45]	46	PMC1_IO[46]
15	PMC1_IO[15]	16	PMC1_IO[16]	47	PMC1_IO[47]	48	PMC1_IO[48]
17	PMC1_IO[17]	18	PMC1_IO[18]	49	PMC1_IO[49]	50	PMC1_IO[50]
19	PMC1_IO[19]	20	PMC1_IO[20]	51	PMC1_IO[51]	52	PMC1_IO[52]
21	PMC1_IO[21]	22	PMC1_IO[22]	53	PMC1_IO[53]	54	PMC1_IO[54]
23	PMC1_IO[23]	24	PMC1_IO[24]	55	PMC1_IO[55]	56	PMC1_IO[56]
25	PMC1_IO[25]	26	PMC1_IO[26]	57	PMC1_IO[57]	58	PMC1_IO[58]
27	PMC1_IO[27]	28	PMC1_IO[28]	59	PMC1_IO[59]	60	PMC1_IO[60]
29	PMC1_IO[29]	30	PMC1_IO[30]	61	PMC1_IO[61]	62	PMC1_IO[62]
31	PMC1_IO[31]	32	PMC1_IO[32]	63	PMC1_IO[63]	64	PMC1_IO[64]

3.4 Serial Port Connectors and Pinouts (P9 and P10)

Figure 3-4 Serial Port Connectors (P9 and P10)

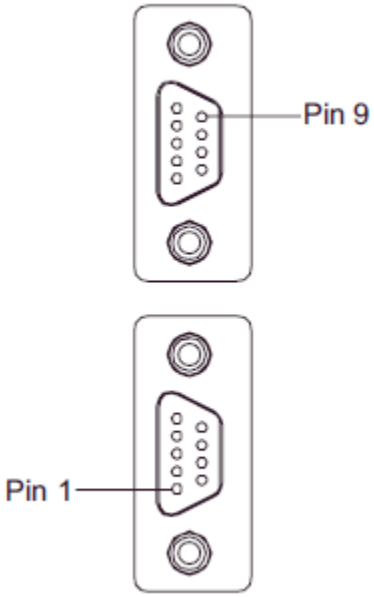


Table 3-4 Serial Port (P9/P10) Pinout

RS232		RS422/485	
Pin	Name	Pin	Name
1	DCD	1	RXD-
2	RXD	2	RXD+
3	TXD	3	TXD+
4	DTR	4	RTS-
5	GND	5	GND
6	DSR	6	CTS-
7	RTS	7	RTS+
8	CTS	8	CTS+
9	RI	9	TXD-

3.4.1 Jumper Configuration for Different Serial Modes

Each COM port can be set to one of two different modes, RS232 or RS422/485, and are independent of each other. The table below describes the various jumper configurations needed to obtain each mode. Along with the jumper configuration, switch (S1) on the VMICPCI-7055/CPCI-7055RC (Product Manual, Document Number 500-657055-000 for details) must be set accordingly as well.

NOTE

Defaults are in **bold**.

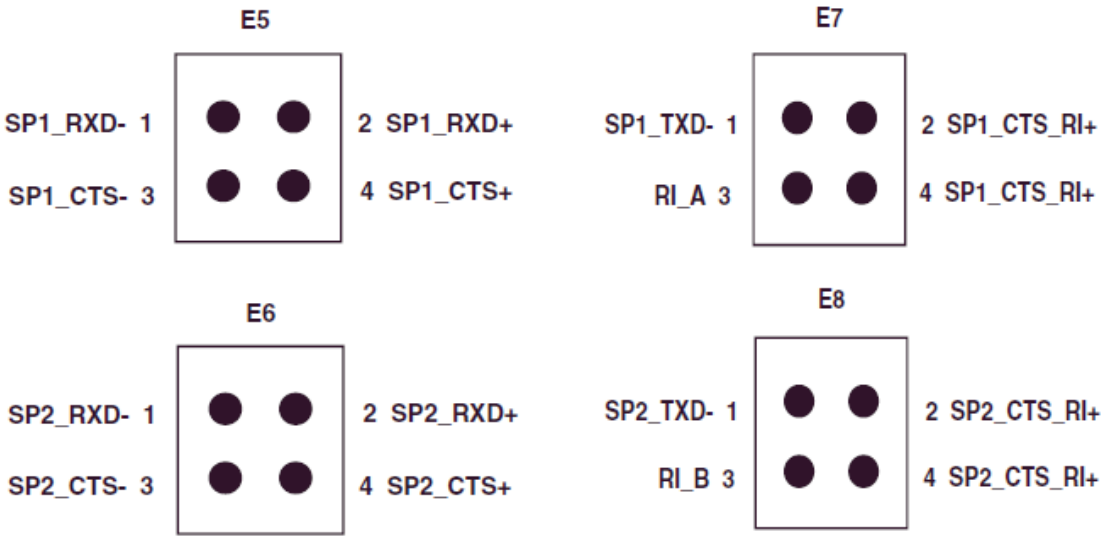
Table 3-5 Jumper Configuration for Different Serial Modes

COM Port	Mode Selection	S1 Pin#	S1 Pin Position	E5	E6	E7	E8
1	**RS232**	**5**	**OFF**	**OMIT**	**NA**	**3-4**	**NA**
	RS422/485	5	ON	1-2, 3-4	NA	1-2	NA
2	**RS232**	**7**	**OFF**	**NA**	**OMIT**	**NA**	**3-4**
	RS422/485	7	ON	NA	1-2, 3-4	NA	1-2

NOTE

To configure the serial ports for loopback mode, S1 on the VMICPCI-7055/CPCI-7055RC (Product Manual, Document Number 500-657055-000 for details) will need pins 6 and 8 (relating to COM 1 and COM 2 respectively) placed in the ON position.

Figure 3-5 Serial Header Signals



3.5 CompactFlash Connector and Pinout (P6)

Figure 3-6 CompactFlash Connector (P6)

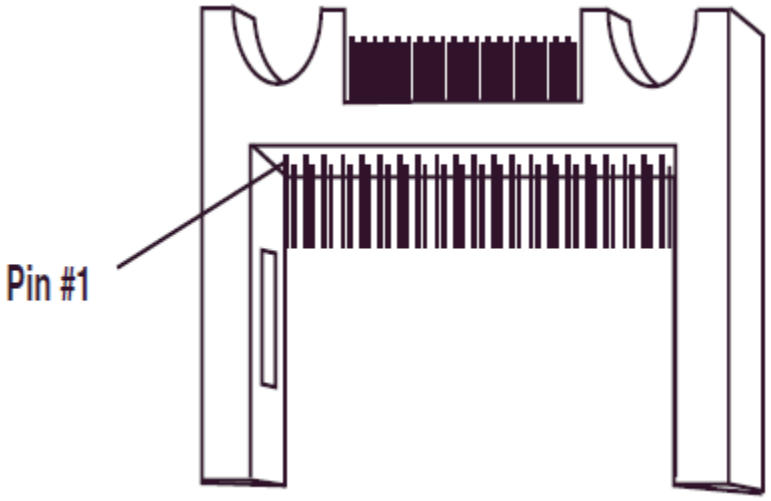


Table 3-6 CompactFlash (P6) Pinout

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	GND	14	GND	27	IDES_D[11]	40	N/C
2	IDES_D[3]	15	GND	28	IDES_D[12]	41	IDES_RESET#
3	IDES_D[4]	16	GND	29	IDES_D[13]	42	IDES_IORDY
4	IDES_D[5]	17	GND	30	IDES_D[14]	43	IDES_DMARQ
5	IDES_D[6]	18	IDES_DA2	31	IDES_D[15]	44	IDES_DMACK #
6	IDES_D[7]	19	IDES_DA1	32	IDES_CS3#	45	HD_ACTA#
7	IDES_CS1#	20	IDES_DA0	33	N/C	46	IDES_CBLIO#
8	GND	21	IDES_D[0]	34	IDES_DIOR#	47	IDES_D[8]
9	GND	22	IDES_D[1]	35	IDES_DIOW#	48	IDES_D[9]
10	GND	23	IDES_D[2]	36	5 VDC	49	IDES_D[10]
11	GND	24	N/C	37	IDES_INTRQ	50	GND
12	GND	25	N/C	38	5 VDC	51	GND
13	V5.0	26	N/C	39	CF_MASTER #	52	GND

3.5.1 CompactFlash Master and Slave Jumper (E4)

When the IDE drive and CompactFlash are installed at the same time, one of them must be set as a slave.

NOTE

Defaults are in **bold**.

Figure 3-7 CompactFlash Master and Slave Jumper (E4)

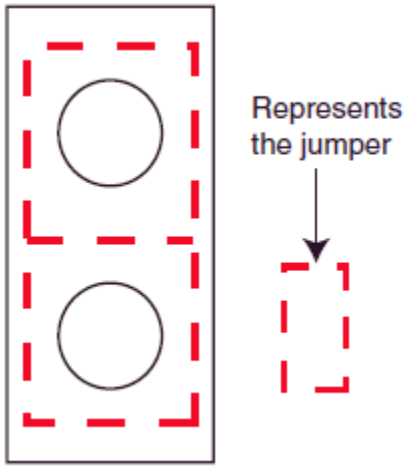


Table 3-7 CompactFlash Master and Slave Jumper (E4)

	Master	Slave
E4	**Installed**	Omitted

3.6 Gigabit LAN Port Connectors and Pinouts (J6 and J7)

Although the two Gigabit Ethernet connectors are available on the VMIACC-7055/ACC-7055RC, they can only be used when the VMICPCI-7055/ CPCI-7055RC has a value of '1' in the options' D field, which allows for Ethernet via CompactPCI J3 (not PICMG 2.16 compatible).

Figure 3-8 Ethernet Connector

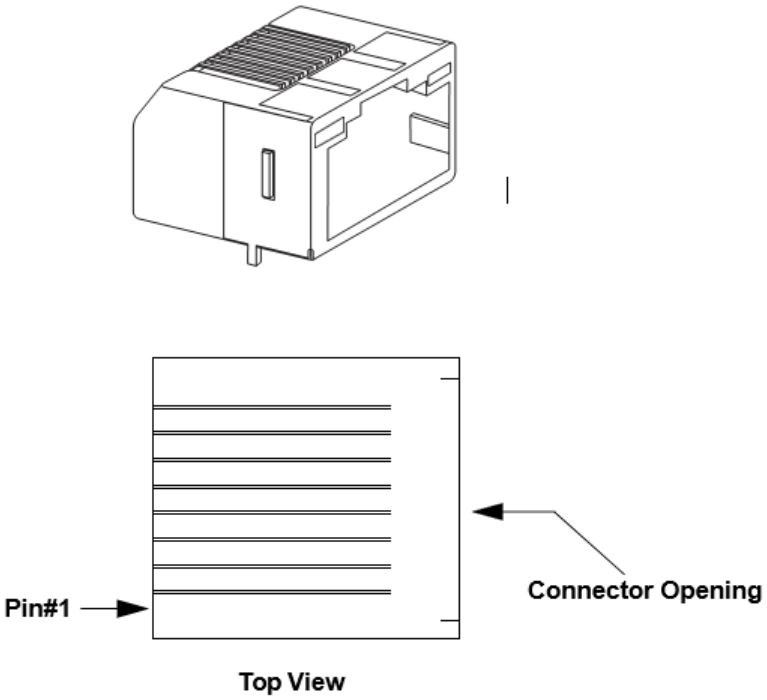


Table 3-8 Ethernet Connectors LAN1 and LAN2 Pinouts

LAN1 and LAN2	
Pin	Name
1	MDI[0]+
2	MDI[0]-
3	MDI[1]+
4	MDI[2]+
5	MDI[2]-
6	MDI[1]-
7	MDI[3]+
8	MDI[3]-

3.7 J3 Connector Pinout

The J3 connector is a 5 row, 19 pins each, 2 mm “Hard Metric” CompactPCI connector. An additional external metal shield is also used, labeled row F. The Figure 3-9 and Table 3-9 illustrate the J3 connector and the connector pinout. This connector is used to route the serial and Ethernet signals to the backplane I/O.

Figure 3-9 J3 Connector

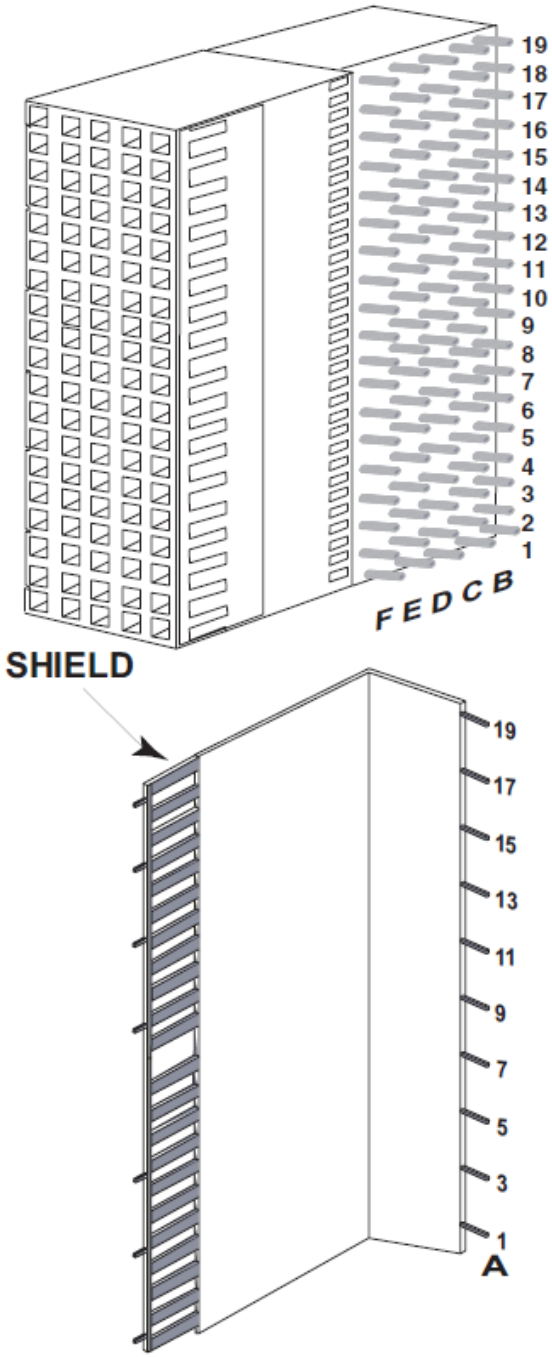


Table 3-9 J3 Connector Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
19	GND	GND	GND	GND	GND	GND
18	LPA_BI_DA+	LPA_BI_DA2-	GND	LPA_BI_DC+	LPA_BI_DC-	GND
17	LPA_BI_DB+	LPA_BI_DB2-	GND	LPA_BI_DD+	LPA_BI_DD-	GND
16	LPB_BI_DA+	LPB_BI_DA2-	GND	LPB_BI_DC+	LPB_BI_DC-	GND
15	LPB_BI_DB+	LPB_BI_DB2-	GND	LPB_BI_DD+	LPB_BI_DD-	GND
14	GND	GND	GND	GND	GND	GND
13	SP2_RTS	SP1_RI	SP2_DSR	SP2_DCD	SP2_CTS	GND
12	SP1_RTS	SP2_DTR	VCC_5.0	SP1_CTS	GND	GND
11	SP2_TXB	SP2_RXD	SP1_DTR	SP1_DCD	LPA_BI_DC-	GND
10	SP1_TXB	SP1_RXD	SP1_DSR	SP2_RI	LPA_BI_DD2-	GND
9	GND	GND	N/C	GND	LPB_BI_DC2-	GND
8	LPA_BI_DA2+	LPA_BI_DA2-	SP2_ACTIVE	LPA_BI_DC2+	LPB_BI_DD2-]	GND
7	LPA_BI_DB2+	LPA_BI_DB2-	SP2_LOOPBACK	LPA_BI_DD2+	GND	GND
6	LPB_BI_DA2+	LPB_BI_DA2-	SP2_R485/232	LPB_BI_DC2+	GND	GND
5	LPB_BI_DB2+	LPB_BI_DB2-	SP1_ACTIVE	LPB_BI_DD2+	N/C	GND
4	GND	GND	VCC_5.0	GND	VCC_3.3	GND
3	G1_Y_LINK100#	G1_G_LK1000#	SP1_R485/232	GND	VCC_3.3	GND
2	G1_G_LINK10#	G1_Y_ACT	SP1_LOOPBACK	G2_Y_LINK100#	G2_G_LK1000#	GND
1	N/C	N/C	N/C	G2_G_LINK10#	G2_Y_ACT#	GND

3.8 J5 Connector Pinout

The J5 connector is a 5 row, 22 pins each, 2mm “Hard Metric” CompactPCI connector. An additional external metal shield is also used, labeled row F. The figure and table below illustrate the J5 connector and the connector pinout. The 64-bit PMC I/O is routed through the J5 to a PIM connector and the IDE signals.

Figure 3-10 J5 Connector

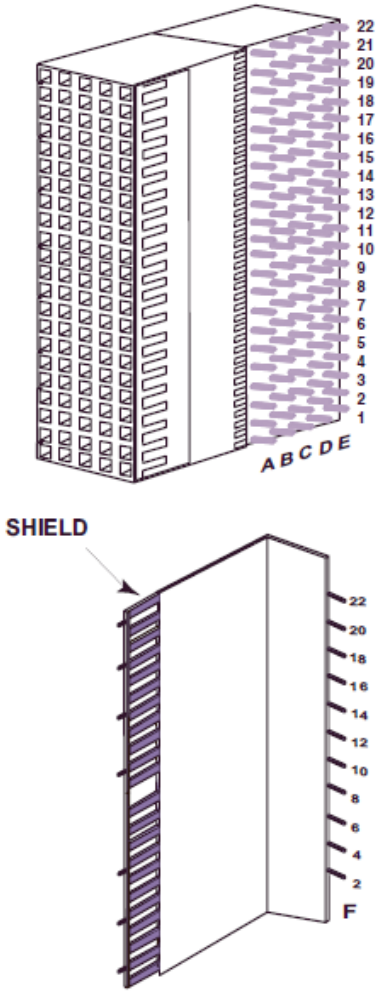


Table 3-10 J5 Connector Pinout

Pin	Row A	Row B	Row C	Row D	Row E	Row F
22	PMC1_IO[5]	PMC1_IO[4]	PMC1_IO[3]	PMC1_IO[2]	PMC1_IO[1]	GND
21	PMC1_IO[10]	PMC1_IO[9]	PMC1_IO[8]	PMC1_IO[7]	PMC1_IO[6]	GND
20	PMC1_IO[15]	PMC1_IO[14]	PMC1_IO[13]	PMC1_IO[12]	PMC1_IO[11]	GND
19	PMC1_IO[20]	PMC1_IO[19]	PMC1_IO[18]	PMC1_IO[17]	PMC1_IO[16]	GND
18	PMC1_IO[25]	PMC1_IO[24]	PMC1_IO[23]	PMC1_IO[22]	PMC1_IO[21]	GND
17	PMC1_IO[30]	PMC1_IO[29]	PMC1_IO[28]	PMC1_IO[27]	PMC1_IO[26]	GND
16	PMC1_IO[35]	PMC1_IO[34]	PMC1_IO[33]	PMC1_IO[32]	PMC1_IO[31]	GND
15	PMC1_IO[40]	PMC1_IO[39]	PMC1_IO[38]	PMC1_IO[37]	PMC1_IO[36]	GND
14	PMC1_IO[45]	PMC1_IO[44]	PMC1_IO[43]	PMC1_IO[42]	PMC1_IO[41]	GND

Pin	Row A	Row B	Row C	Row D	Row E	Row F
13	PMC1_IO[50]	PMC1_IO[49]	PMC1_IO[48]	PMC1_IO[47]	PMC1_IO[46]	GND
12	PMC1_IO[55]	PMC1_IO[54]	PMC1_IO[53]	PMC1_IO[52]	PMC1_IO[51]	GND
11	PMC1_IO[60]	PMC1_IO[59]	PMC1_IO[58]	PMC1_IO[57]	PMC1_IO[56]	GND
10	VCC_5.0	PMC1_IO[64]	PMC1_IO[63]	PMC1_IO[62]	PMC1_IO[61]	GND
9	IDES_DA0	GND	GND	IDES_DA2	N/C	GND
8	IDES_DA1	IDES_D[8]	IDES_IORDY	IDES_D[0]	N/C	GND
7	IDES_DIOR#	IDES_D[9]	IDES_CS1#	IDES_D[1]	VCC_5.0	GND
6	IDES_DIOW#	IDES_D[10]	HD_ACTA#	IDES_D[2]	N/C	GND
5	N/C	IDES_D[11]	IDES_CS3#	IDES_D[3]	GND	GND
4	IDES_CBLIO#	IDES_D[12]	IDES_INTRQ	IDES_D[7]	N/C	GND
3	N/C	IDES_D[13]	IDES_DMACK#	IDES_D[6]	N/C	GND
2	N/C	IDES_D[14]	IDES_DMARQ	IDES_D[5]	VCC_3.3	GND
1	N/C	IDES_D[15]	IDES_RESET#	IDES_D[4]	N/C	GND

4 • Safety Notices

4.1 Summary

Observe the following general safety precautions during operation, service and repair of this equipment. Failure to comply with these precautions or with specific Warnings and/or Cautions elsewhere in this manual violates safety standards of design, manufacture and intended use of this equipment. Abaco Systems assumes no liability for the user's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Abaco is aware. Take note of these warnings and take all other safety precautions necessary for the safe operation of the equipment in your operating environment.

4.2 Equipment Grounding

To minimize electric shock hazard, connect the equipment chassis and rack/enclosure to an electrical ground. If AC power is supplied to the rack/enclosure, the power jack and mating plug of the power cable must meet International Electrotechnical Commission (IEC) safety standards.

4.3 Power Supplies



WARNING

Use extreme caution when handling, testing and adjusting this equipment. Refer to warnings contained in associated system equipment manuals before operating these devices. Follow instructions contained within all warnings.

You should also employ all other safety precautions that are deemed necessary for the safe operation of the equipment in your operating environment.

Ensure that all power to the system is removed before installing these devices.

4.4 Flammability

Abaco circuit boards are manufactured by UL-recognized manufacturers and have a flammability rating of 94V-1.

4.5 EMI/EMC Regulatory Compliance

CAUTION

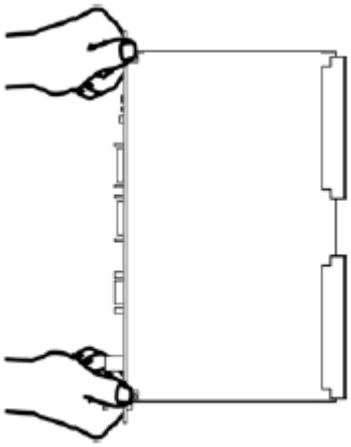
This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to EMI if not installed and used in a cabinet with adequate EMI protection.

Abaco's boards are designed using good EMC practices and, when used in a suitably EMC-compliant chassis, should maintain the compliance of the total system.

4.6 Handling Precautions

Proper handling of the board or module is critical to ensure proper operation and long term reliability. When unpacking the board, and whenever handling it thereafter, be sure to handle the board by the front panel as shown. Do not handle the board by the circuit card edges, the heat sink or the connectors, unless handling a conduction-cooled version. Conduction-cooled boards do not have a front panel and will need to be handled carefully by the front edge.

Figure 4-1 Handling the Board



CAUTION

Handle the board by the front edge (if no front panel) or front panel only.

4.7 Handling the Board

- Ensure that both the person handling the board and the surrounding area are protected from ESD.
- Carefully remove the board or module from the shipping carton by grasping it by the front panel and the connectors.
- Place the board, in its antistatic bag, flat, down on a suitable surface.
- Remove the board from the antistatic bag by tearing the ESD warning labels.

5 • Unpacking

5.1 Unpacking Procedures

On receipt of the shipping container, check for any evidence of physical damage. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Technical Support, see Technical Support Contact Information.

Electronic assemblies use devices that are sensitive to static discharge. Observe antistatic procedures when handling these boards. All products should be in an antistatic plastic bag or conductive foam for storage or shipment. Work at an approved antistatic workstation when unpacking boards.

5.2 Identifying Your Board

The board is identified by labels at strategic positions. These can be cross-checked against the Advice Note provided with your delivery.

Identification labels attached to the shipping box and the antistatic bag give identical information: product code, product description, equipment number, and board revision. On the board within the antistatic bag, there is an identifying label attached to the PCB.

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