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Hardware Reference Manual

VME-2131* 64-bit Current Source/Sink Driver MEGAMODULE*

Publication No: 500-012131-000 Rev. E.0

abaco SYSTEMS

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Document History

Revision	Date	Description
D	October 2013	
E.0	September 2016	Reformatting

Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case-by-case basis. A WEEE management fee may apply.

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About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when “k”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.


NOTE
When describing transfer rates, “k”, “M” and “G” mean $x10^3$, $x10^6$ and $x10^9$ *not* $x2^{10}$, $x2^{20}$ and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.


LINK
www.abaco.com/products/vme-2131-driver-board

Third-party Documents

For detailed explanation of the VMEbus and its characteristics, refer to the VMEbus Specification ANSI/IEEE 1014-1987 and ANSI/VITA 1.0-1994 available from:

VITA

VMEbus International Trade Association
7825 East Gelding Dr., No. 104
Scottsdale, AZ 85260
(602) 951-8866
FAX: (602) 951-0720
www.vita.com

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You can find technical assistance contact details on the website Embedded Support page.


LINK
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Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:


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support@abaco.com

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If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.

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Do not return products without first contacting the Abaco Repairs facility.

Additional Notes

The VME-2131 is capable of delivering sixty-four channels of high current output. These outputs can be current sourcing or current sinking. The VME-2131 is designed with a breakdown voltage of 35V minimum. A unique feature of the VME-2131 board is the Built-in-Test (BIT) logic, which allows the user, under software control, to verify the operation of each channel.

The VME-2131 is a member of Abaco's MEGAMODULE* family. It is designed with common programming features such that subsystems may be configured with continguous I/O addresses to conserve memory. Each of these boards (VME-1111, VME-2131, VME-2120 and VME-2510B) is designed with two sets of board address switches or jumpers to provide an efficient memory address map for Control and Status Register (CSR) and I/O addresses. CSR addresses may be set such that all CSRs among a variety of boards in the system may be mapped into contiguous memory locations separate from the I/O data addresses.

The MEGAMODULE product line is designed to support 8-, 16- and 32-bit data transfers and also features a front panel Fail LED that is illuminated at powerup or after a system reset and may be extinguished under program control upon successful completion of board level diagnostics. Specific hardware has been designed into the VME-2131 to support the BIT functions. The VME-2131 supports both offline and online fault detection and isolation.

Features

- 64 bits of high current outputs
- Outputs may be current sourcing/High-Z or current source/sinks
- Output transient protected
- High-breakdown voltage (35V minimum)
- Tri-state outputs
- Built-in-Test logic for fault isolation
- High reliability DIN type output connectors
- 8-, 16- or 32-bit transfers
- Double Eurocard form factor
- ±3.5 A peak output current (100msec, 10 percent duty cycle)
- 500 mA continuous current (fan cooled)
- Thermal shutdown protection
- Front panel software controlled Failed LED for Built-in-Test
- Separate user configurable address jumpers for the Control and Status Register and the Data Registers allow for contiguous data addressing when more than one I/O board is used in a VMEbus system.

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this Manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

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1 • Handling and Installation

This chapter describes the handling, installation, front panel and baseboard-to-backplane connectors of the VME-2131 board.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Systems Customer Care.

1.2 Handling Precaution

Electronic assemblies use devices that are sensitive to static discharge. Observe anti-static procedures when handling these boards. All products should be in an anti-static plastic bag or conductive foam for storage or shipment. Work at an approved anti-static workstation when unpacking boards.

1.3 Installation



CAUTION

DO NOT INSTALL OR REMOVE THE BOARDS WHILE POWER IS APPLIED.

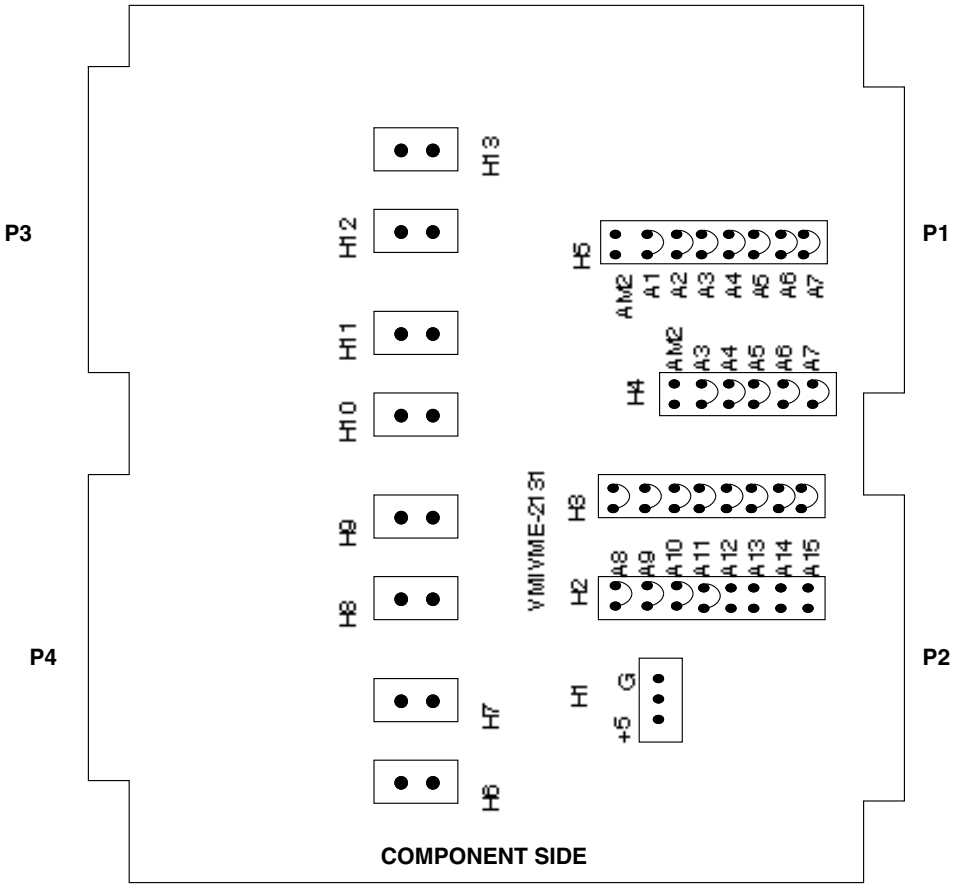
De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

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1.4 Jumper Locations

The physical positions of the jumpers described in this section are shown in *Figure 1-1*.

Figure 1-1 Jumper Locations Showing Factory Configuration

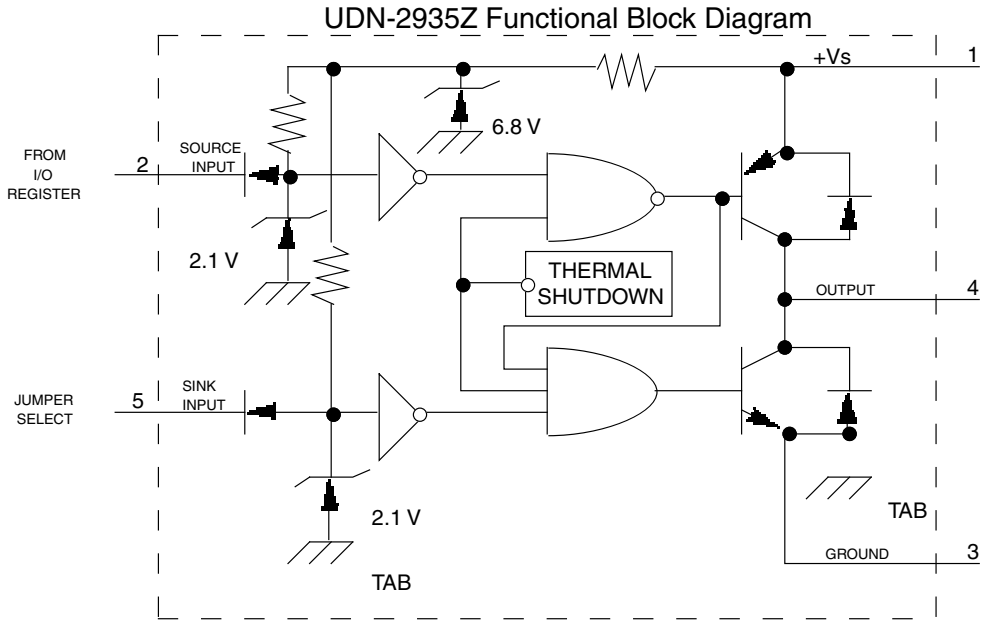


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1.5 Suppressor Diode Connections

The output drivers of the VME-2131 have built-in suppressor diodes for driving inductive loads. Thus, the user does not need to add diodes to his circuitry. A typical output driver stage is shown in *Figure 1-2*.

Figure 1-2 Typical Output Driver Stage



LOGIC TRUTH TABLE

DATA REGISTER INPUT, V_2	JUMPER SELECT INPUT, V_5	OUTPUT V_4
LOW	LOW	HIGH
LOW	HIGH	HIGH
HIGH	LOW	LOW
HIGH	HIGH	HIGH Z

1.6 Address Modifiers

The VME-2131 is configured at the factory to respond to short supervisory I/O access. This configuration can be changed to short nonprivileged I/O access by installing jumpers in position AM2 of the headers H4 and H5. H4 is for the Output Registers, and H5 is for the CSR.

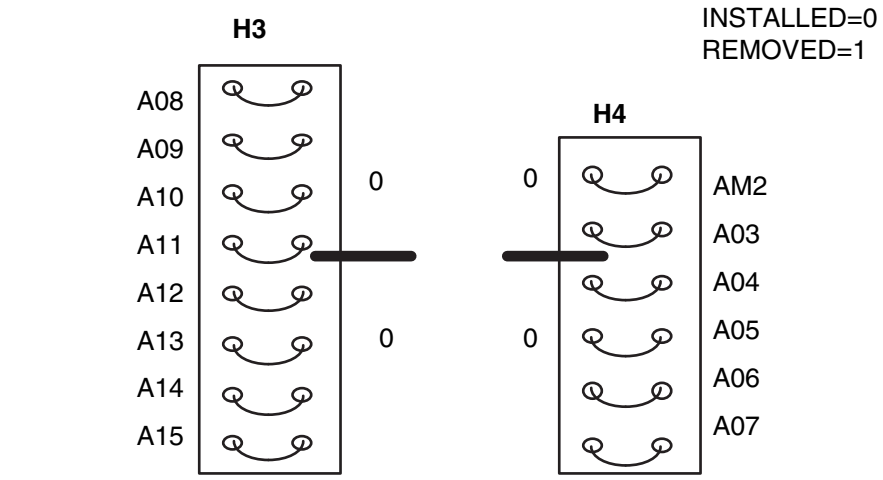
1.7 Address Selection Jumpers

The VME-2131 is designed with two banks of address select jumpers that specify the beginning board address for the Data Registers and the address of the CSR. The address selection jumpers are shown in *Figure 1-3* on page 13 and *Figure 1-4* on page 13. These jumpers are used like an address switch, installing a jumper

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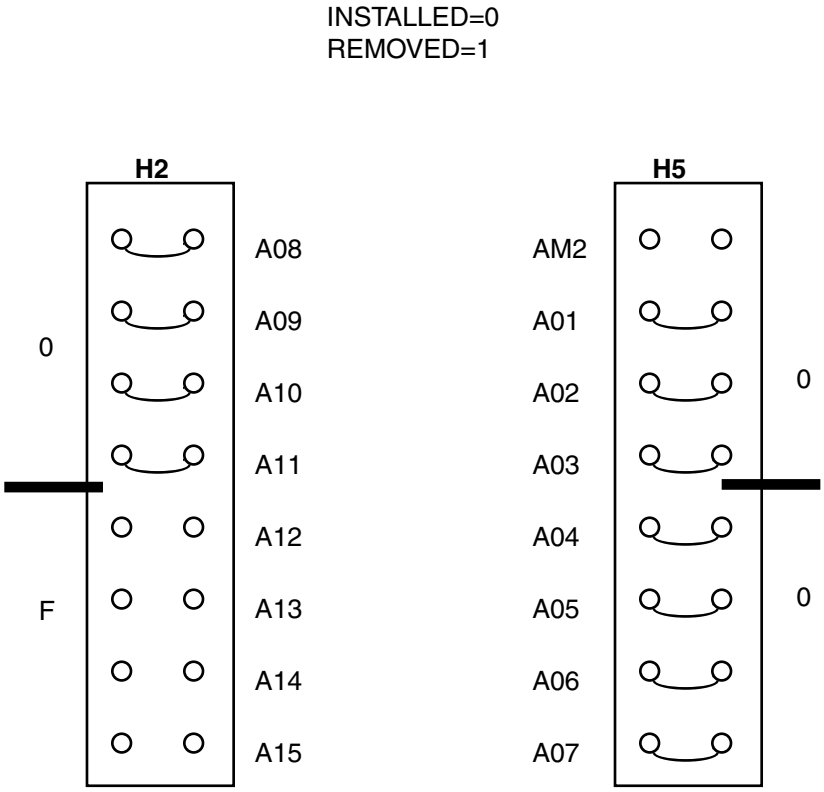
places the corresponding address bit to a logic “zero”. If the jumper is removed, then the corresponding address bit will be a logic “zero”. The VME-2131 is factory configured to respond to 0000 HEX for Data Registers and to F000 HEX for the CSR.

Figure 1-3 Data Register Base Address Select Jumpers



THE EXAMPLE SHOWN IS FOR BASE ADDRESS OF 0000 HEXADECIMAL

Figure 1-4 CSR Base Address Select Jumpers



THE EXAMPLE SHOWN IS FOR BASE ADDRESS OF F000 HEXADECIMAL

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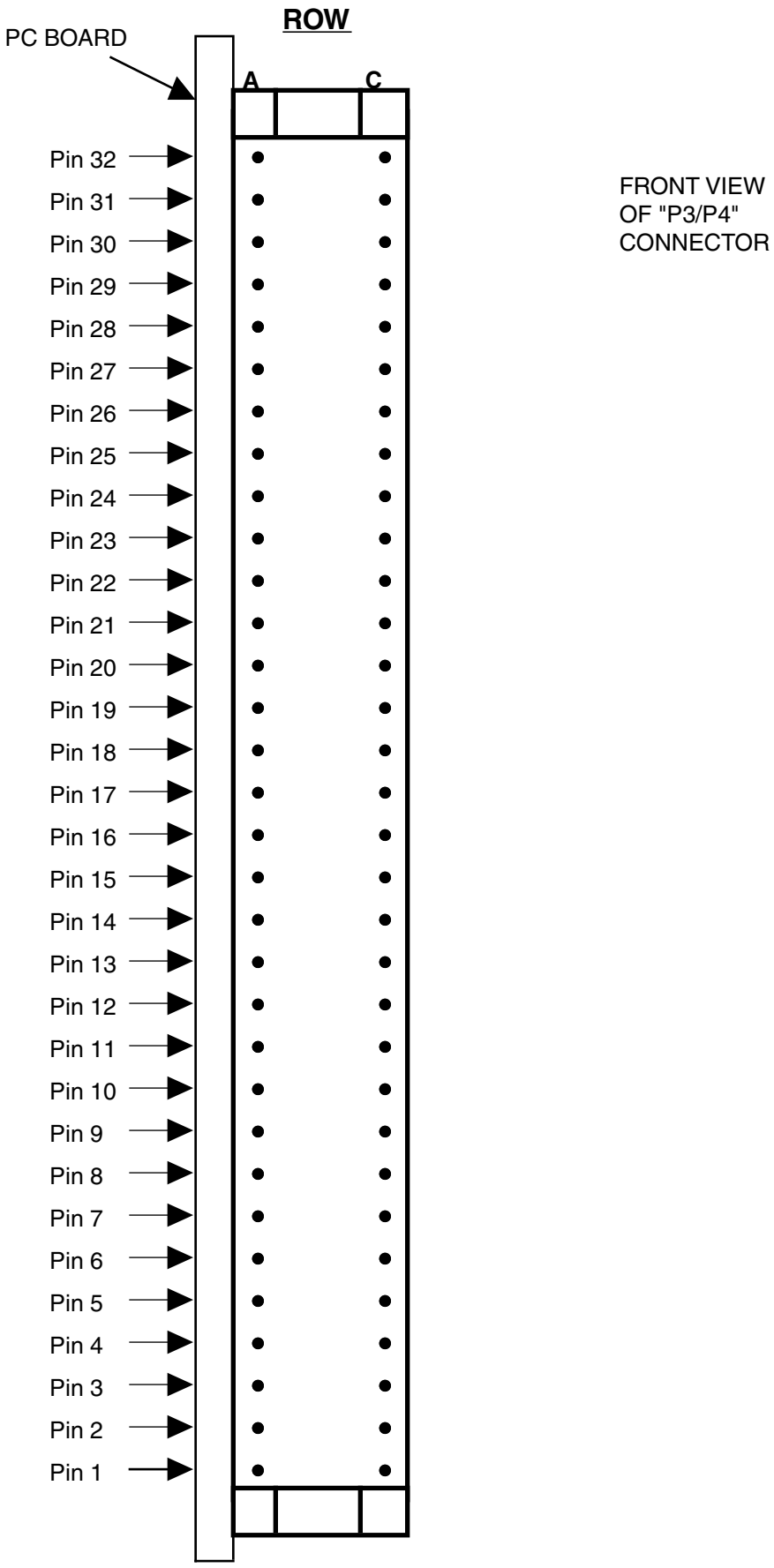
1.8 I/O Cable and Front Panel Connector Configuration

The output connectors (P3 and P4) on the VME-2131 are 64-pin DIN standard and were selected by Abaco Systems because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should contact Sales for additional information concerning the variety of possible cabling and connector types available.

Output connector pin configurations for P3 and P4 are shown in ***Figure 1-5*** on page 15. Connector pin assignments for the sixty-four output channels are shown in ***Table 1-1*** on page 16 and ***Table 1-2*** on page 17. The signals on row A of the connectors are used by two output drivers (as stated in the signal name). These power lines should be returned directly to the power source of the external circuitry. This is to help prevent excessive current from flowing in the backplane. A compatible flat-ribbon cable connector is ITW Pancon No. 120-964-435E. A compatible strain relief is ITW Pancon No. 100-000-032. Cable connector configuration is shown in ***Figure 1-6*** on page 16.

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Figure 1-5 P3/P4 Connector - Pin Configuration



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Figure 1-6 Cable Connector Configuration

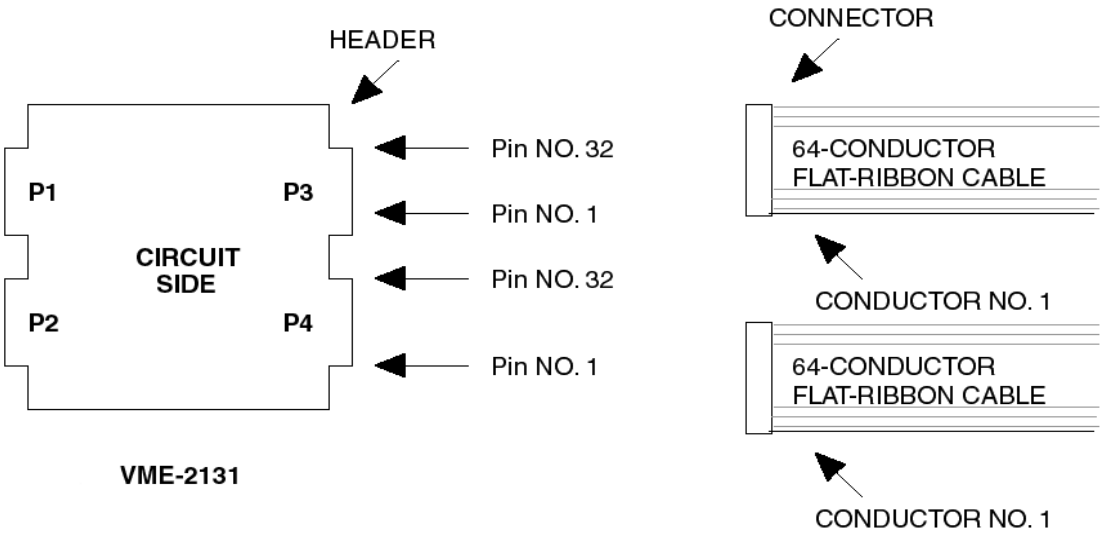


Table 1-1 Connector P4 Pin/Channel Assignments

Pin Number	Row A (Signal Usage)	Row C (Signal Usage)
1	CH00/01 VI	CH00 VO
2	GND	CH01 VO
3	CH01/03 VI	CH02 VO
4	GND	CH03 VO
5	CH04/05 VI	CH04 VO
6	GND	CH05 VO
7	CH06/07 VI	CH06 VO
8	GND	CH07VO
9	CH08/09 VI	CH08 VO
10	GND	CH09 VO
11	CH10/11 VI	CH10 VO
12	GND	CH11 VO
13	CH12/13 VI	CH12 VO
14	GND	CH13 VO
15	CH14/15 VI	CH14 VO
16	GND	CH15 VO
17	CH16/17 VI	CH16 VO
18	GND	CH17 VO
19	CH18/19 VI	CH18 VO
20	GND	CH19 VO
21	CH20/21 VI	CH20 VO
22	GND	CH21 VO
23	CH22/23 VI	CH22 VO
24	GND	CH23 VO
25	CH24/25 VI	CH24 VO
26	GND	CH25 VO
27	CH26/27 VI	CH26 VO
28	GND	CH27 VO
29	CH28/29 VI	CH28 VO
30	GND	CH29 VO
31	CH30/31 VI	CH30 VO
32	GND	CH31 VO

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Table 1-2 Connector P3 Pin/Channel Assignments

Pin Number	Row A (Signal Usage)	Row C (Signal Usage)
1	CH32/33 VI	CH32 VO
2	GND	CH33 VO
3	CH34/35 VI	CH34 VO
4	GND	CH35 VO
5	CH36/37 VI	CH36 VO
6	GND	CH37 VO
7	CH38/39 VI	CH38 VO
8	GND	CH39 VO
9	CH40/41 VI	CH40 VO
10	GND	CH41 VO
11	CH42/43 VI	CH42 VO
12	GND	CH43 VO
13	CH44/45 VI	CH44 VO
14	GND	CH45 VO
15	CH46/47 VI	CH46 VO
16	GND	CH47 VO
17	CH48/49 VI	CH48 VO
18	GND	CH49 VO
19	CH50/51 VI	CH50 VO
20	GND	CH51 VO
21	CH52/53 VI	CH52 VO
22	GND	CH53 VO
23	CH54/55 VI	CH54 VO
24	GND	CH55 VO
25	CH56/57 VI	CH56 VO
26	GND	CH57 VO
27	CH58/59 VI	CH58 VO
28	GND	CH59 VO
29	CH60/61 VI	CH60 VO
30	GND	CH61 VO
31	CH62/63 VI	CH62 VO
32	GND	CH63 VO



CAUTION

THE USER SHOULD USE THE CABLE GROUND LINES FOR THE EXTERNAL POWER SUPPLY RETURNS. THIS IS REQUIRED TO PREVENT EXCESSIVE CURRENT FROM FLOWING INTO THE VMEbus BACKPLANE. ALSO, THE USER SHOULD REMOVE POWER BEFORE THE CABLES ARE CONNECTED OR DISCONNECTED (FROM THE BOARD). THIS WILL PREVENT EXCESSIVE CURRENTS FROM DAMAGING THE P3/P4 CONNECTOR PINS.

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1.9 Jumper Functions

Jumper H1 is provided to invert the data written to the Control and Status Register (CSR). The jumper is configured at the factory such that the test software writes positive data to the CSR. The data polarity used by this board is controlled by the selection of data transceivers which interface with the VMEbus. For positive true data, the jumper H1 is placed in the +5 position, and for negative true data the jumper H1 is placed in the G position. Unless the option of the board is a -1XX then for positive true data, the jumper H1 is placed in the G position, and for negative true data the jumper H1 is placed in the +5 position.

Jumpers H6 through H13 are used to select the mode of operation for output drivers. If the jumper is not installed, the output devices operate in the current source mode. With the jumper installed, the associated output drivers will source as well as sink current (depending on output logic level). Please refer to the logic truth table in ***Figure 1-2*** on page 12 for the logical operation of these devices. This table is based on an impedance to ground.

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2 • Theory of Operation

2.1 Operational Overview

The VME-2131 is designed for a variety of applications such as:

- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Fiber-optic LED drivers

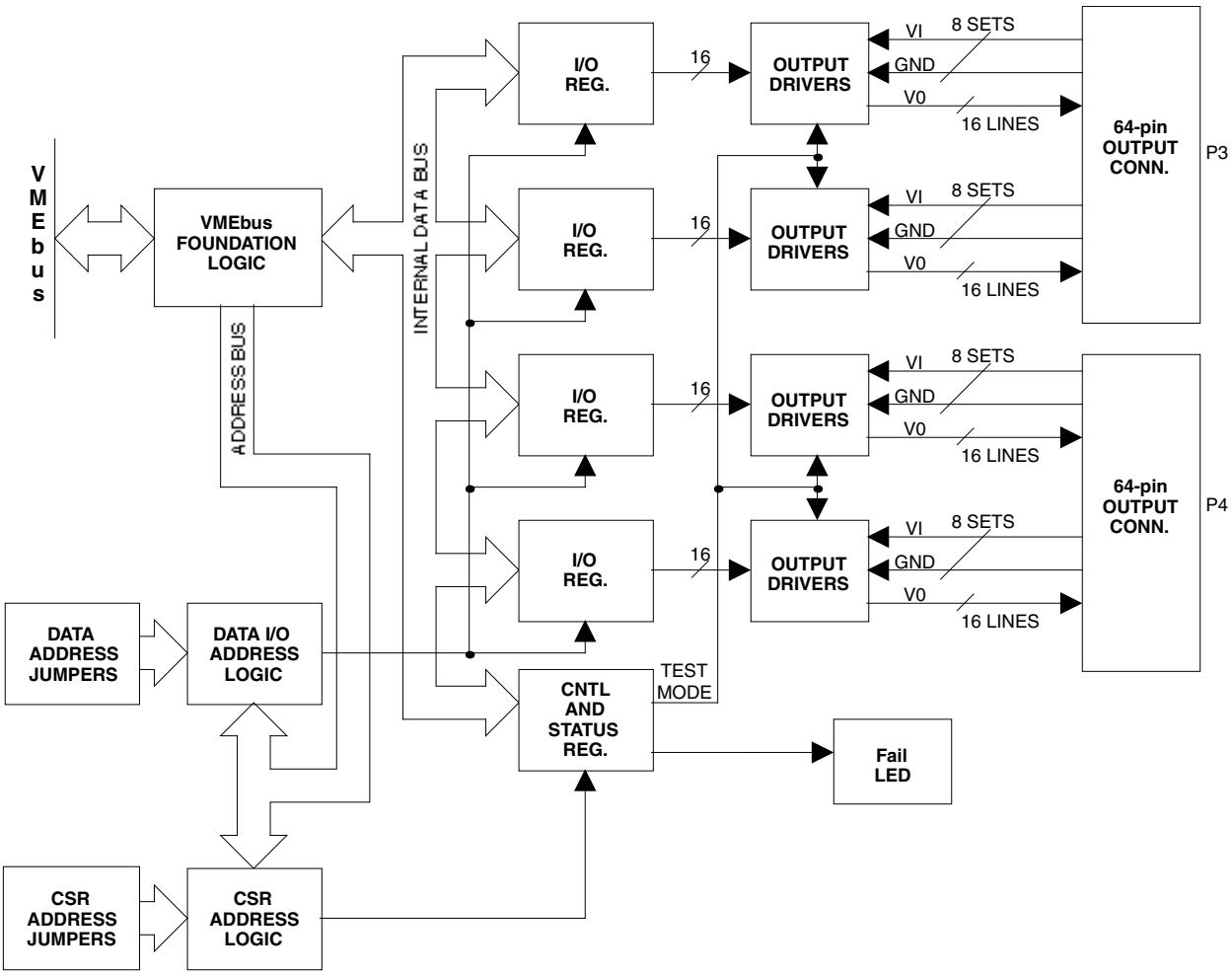
The design of the VME-2131 board, as shown in the functional block diagram in *Figure 2-1* on page 20, consists primarily of four sections which are:

- Device addressing
- VMEbus foundation logic
- Built-in-Test logic
- Output drivers

The board is designed using eight bi-directional 8-bit registers, a CSR, high performance output drivers, typical VMEbus foundation logic, and two device address jumper banks. The two jumper banks provide the user with the capability and flexibility to map I/O registers and CSRs into separate contiguous memory locations.

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Figure 2-1 VME-2131 Functional Block Diagram



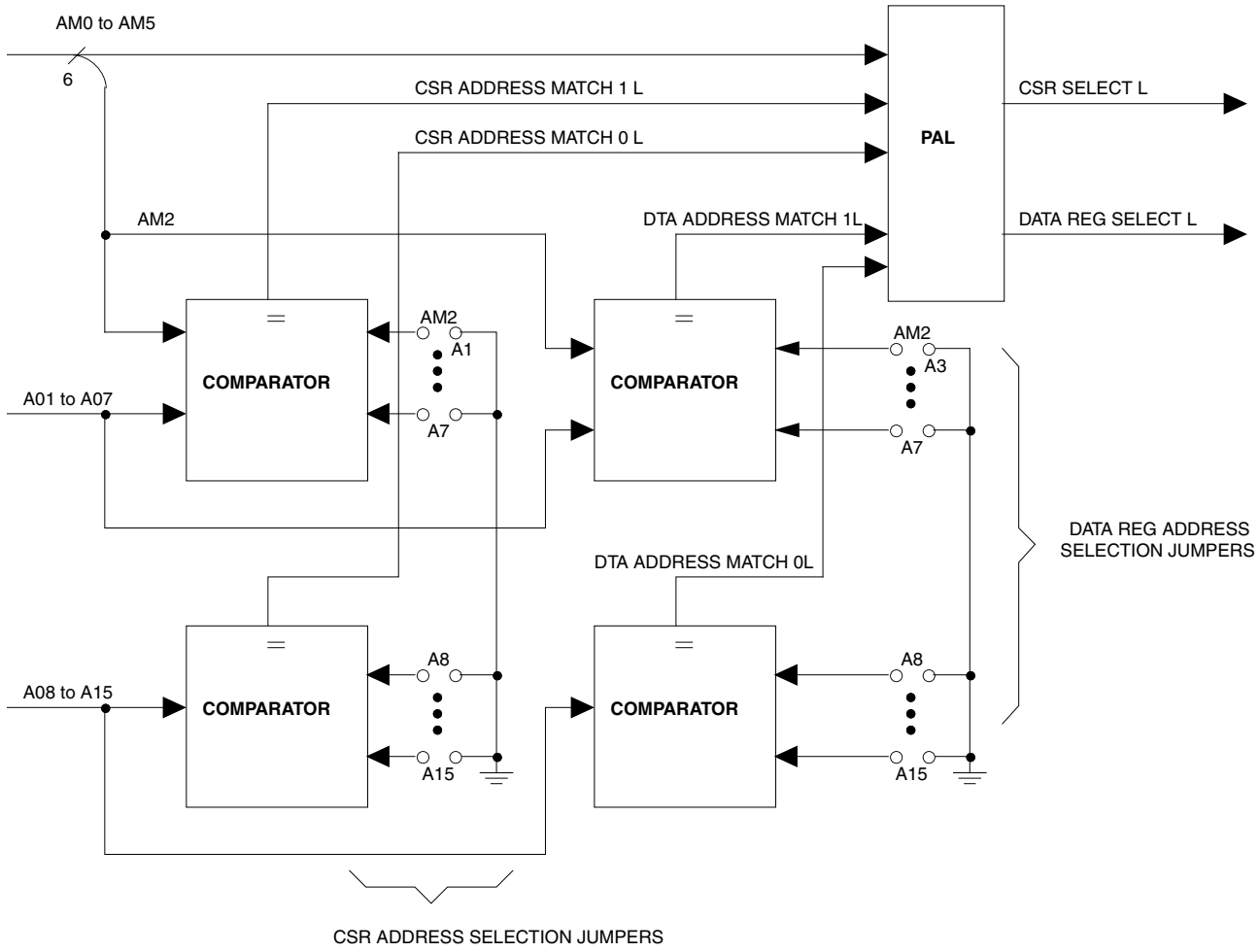
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2.2 Device Addressing

The VME-2131 is designed to support data transfers in supervisory or nonprivileged short I/O memory space. Jumpers are provided, as shown in ***Figure 2-2***, to allow user selection of either I/O access type. These jumpers are called AM2. There is one jumper for the Data Registers and one jumper for the CSR. The VME-2131 is factory configured (jumpers AM2 not installed) to respond to short supervisory I/O access.

The VME-2131 is designed with two sets of board select jumpers and decode logic as shown in ***Figure 2-2*** to provide an efficient memory address map for the CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into separate contiguous memory locations when configuring subsystems that require more than one board.

Figure 2-2 Address Selection Block Diagram

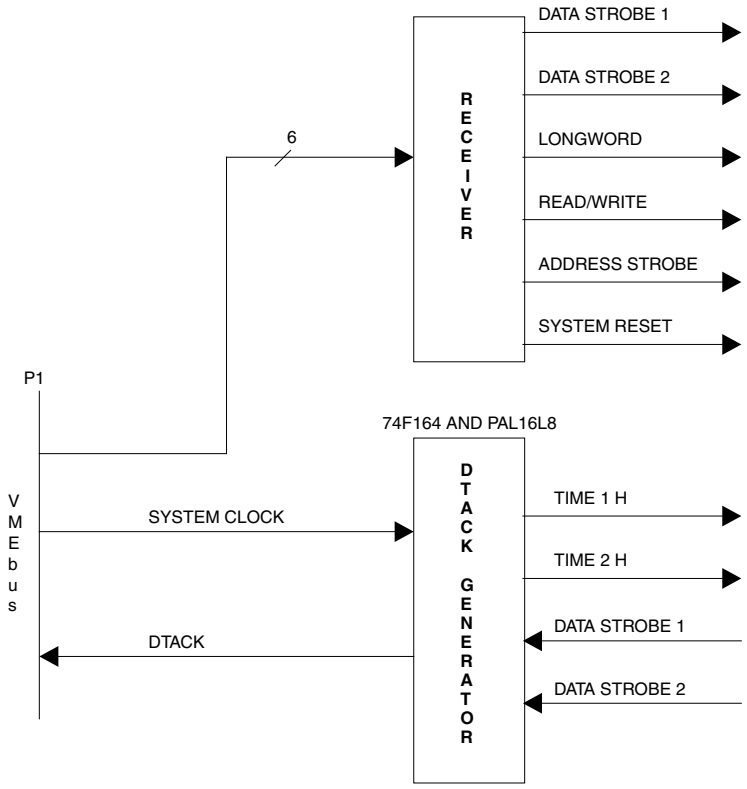


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2.3 VMEbus Foundation Logic

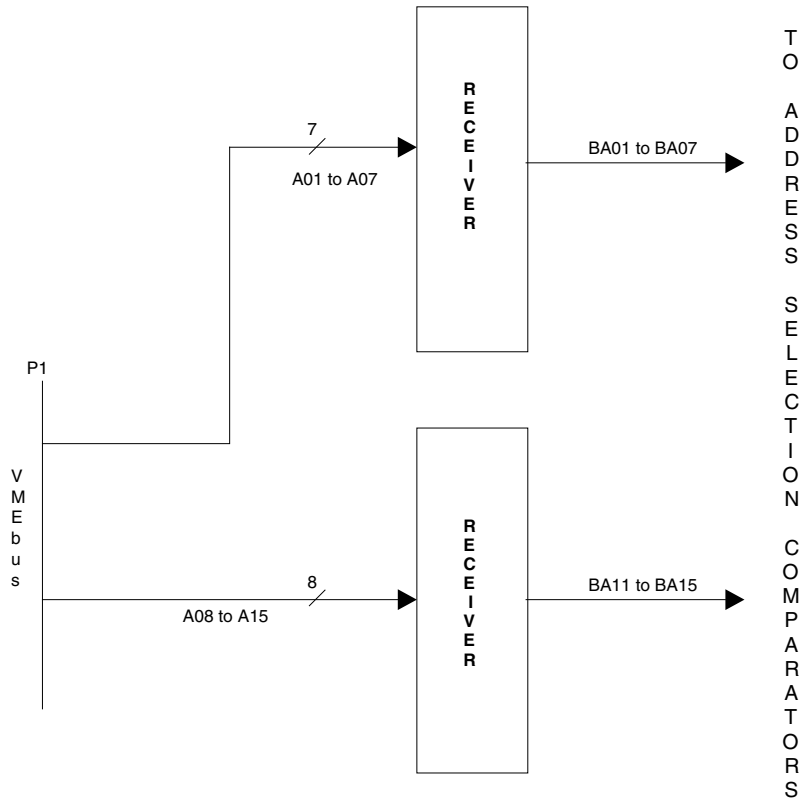
Typical VMEbus drivers, receivers, and control logic are shown in *Figure 2-2* on page 21, *Figure 2-3* below and *Figure 2-4* on page 23.

Figure 2-3 Control Section Block Diagram



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Figure 2-4 Address Section Block Diagram

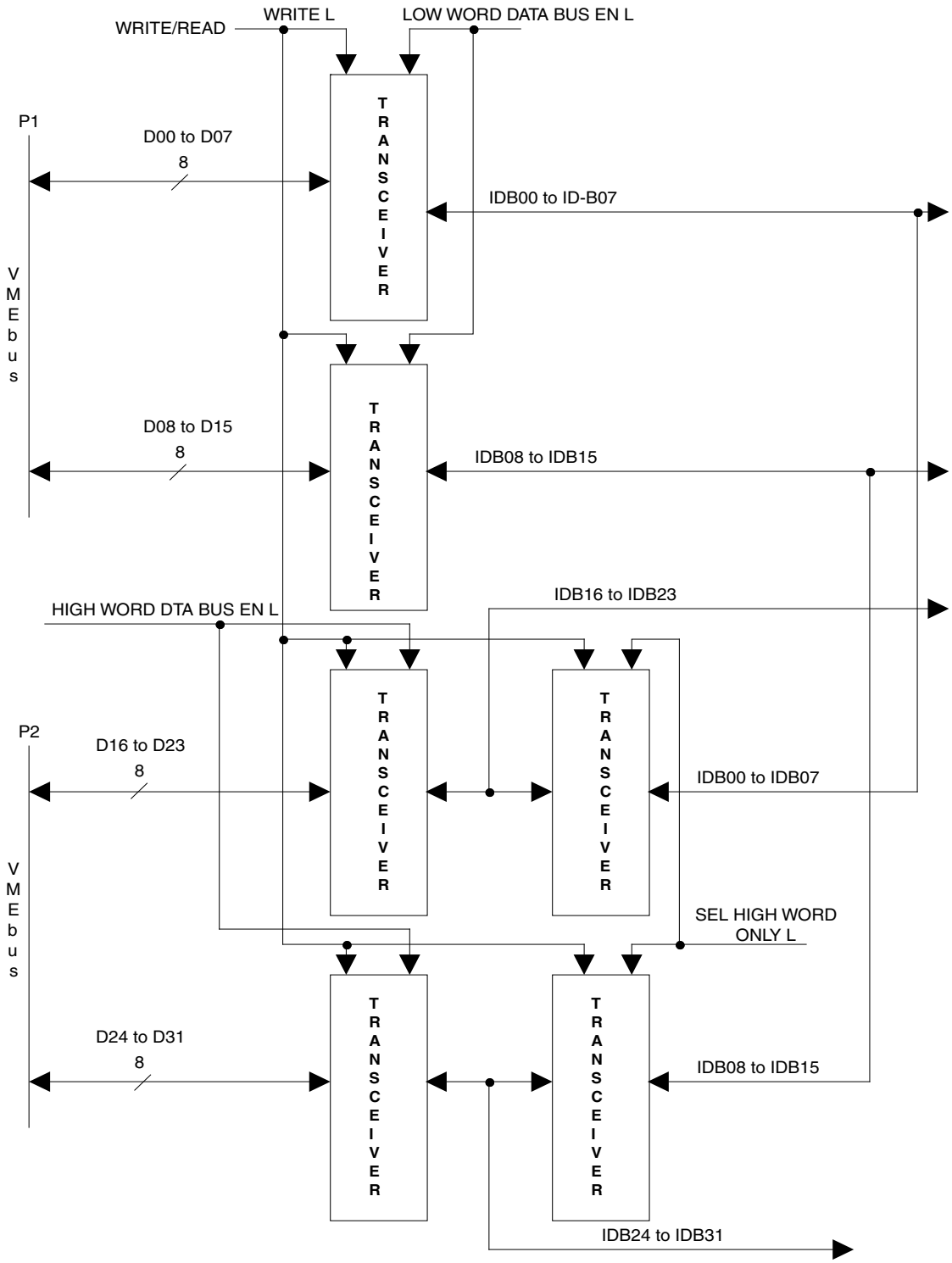


2.4 Data Transfers

Data transfer transceivers are shown in *Figure 2-5* on page 23. The data transceivers are designed to support write and read operations on 8-, 16-, and 32-bit boundaries. Thus, the sixty-four current source/sink outputs are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes.

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Figure 2-5 Data Transfer Block Diagram



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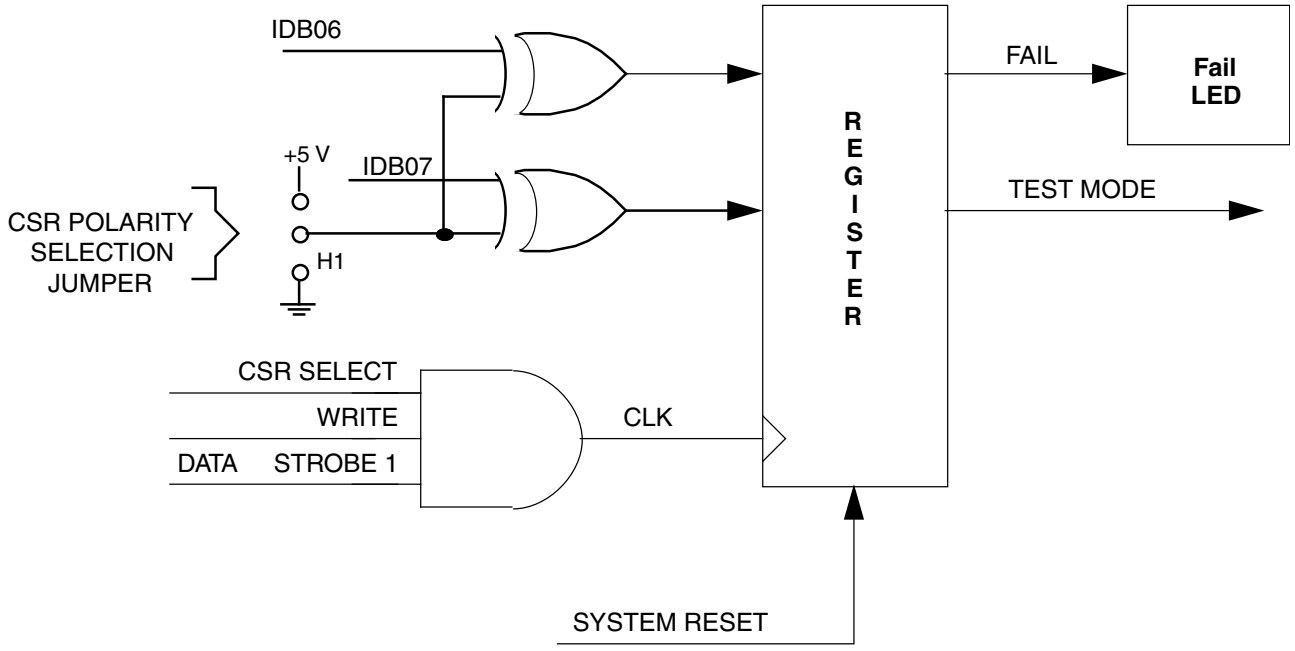
2.5 Register Control Logic

The register control logic for the VME-2131 board is designed to support write and read operations to and from the eight 8-bit bi-directional dual-port latches and write transfers to a CSR that controls the test mode and front panel LED. The control logic provides the capability to read or write 8, 16 or 32 bits of data. This control logic is implemented using programmable array logic (PAL) devices.

2.6 Control and Status Register (CSR)

The CSR is a write-only register that controls the Test Mode (TM) bit and the front panel Fail LED as shown in ***Figure 2-6***. The TM bit disables the output drivers to perform Built-in-Test functions. Both bits of the CSR are initialized active upon system reset or powerup such that the driver outputs are disabled and the front panel LED is illuminated. A jumper H1 is configured such that when writing a logic “one” to bits 6 and 7 of the CSR, the LED is illuminated and the output drivers are offline.

Figure 2-6 CSR Control Logic Block Diagram



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2.7 Built-in-Test

The Built-in-Test feature of the VME-2131 is enabled by asserting (setting to a logical “one”) the test mode bit in the CSR. As an aid to programming the VME-2131, a jumper (H1) is available to the user. This jumper can be used to invert the input data to the CSR of the VME-2131. It is used to permit existing software to control the VME-2131. If the program used writes “zeros” to the CSR, this jumper can be setup to invert this data (since the VME-2131 uses “ones” in the CSR). This way the H1 jumper can let the user run existing software without modifications.

While in Test Mode, data may written to any Output Data Register and read back on a following read operation. This way the data written can be compared to the data read and any action necessary can be initiated. While in Test Mode, writing to an output device will have no effect on the field equipment, because the output drivers are disabled during Test Mode operations.

The data loopback circuitry can be used even if TEST MODE is not active. Thus, the Built-in-Test feature of this product provides the user with the capability of performing real-time loopback testing with the output drivers connected to the field equipment.

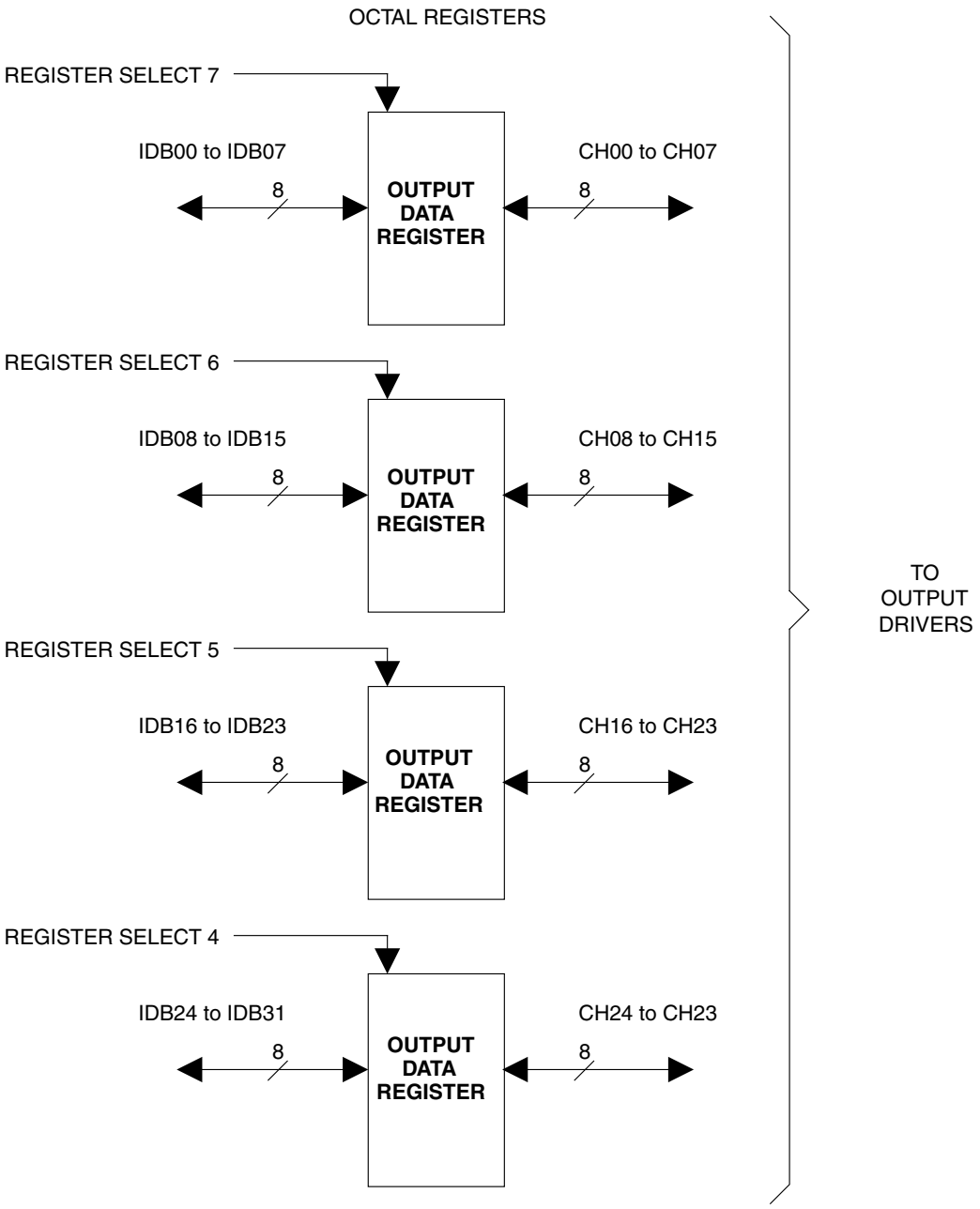
A front panel Fail LED is provided for quick fault isolation to the board level. The Fail LED is illuminated at powerup or system reset and is extinguished under software control by the user upon successful execution of a user-defined diagnostic program. The board is initialized in the Test Mode at powerup or upon system reset.

2.8 Octal Registers and Output Drivers

A block diagram of the eight 8-bit I/O registers is shown in *Figure 2-7* on page 27 and *Figure 2-8* on page 28. The Output Data Registers were selected as the primary building block of this design, because they have a unique feature that allows “read-back” of their input data, which is used by the Built-in-Test functions. In Test Mode, the Data Register outputs are tri-stated and the data read-back path is internal to the device. Whereas, during normal operation the data read-back path includes the output pins on the Output Data Register. Thus, during Test Mode all of the board’s circuitry is tested, except for the output drivers.

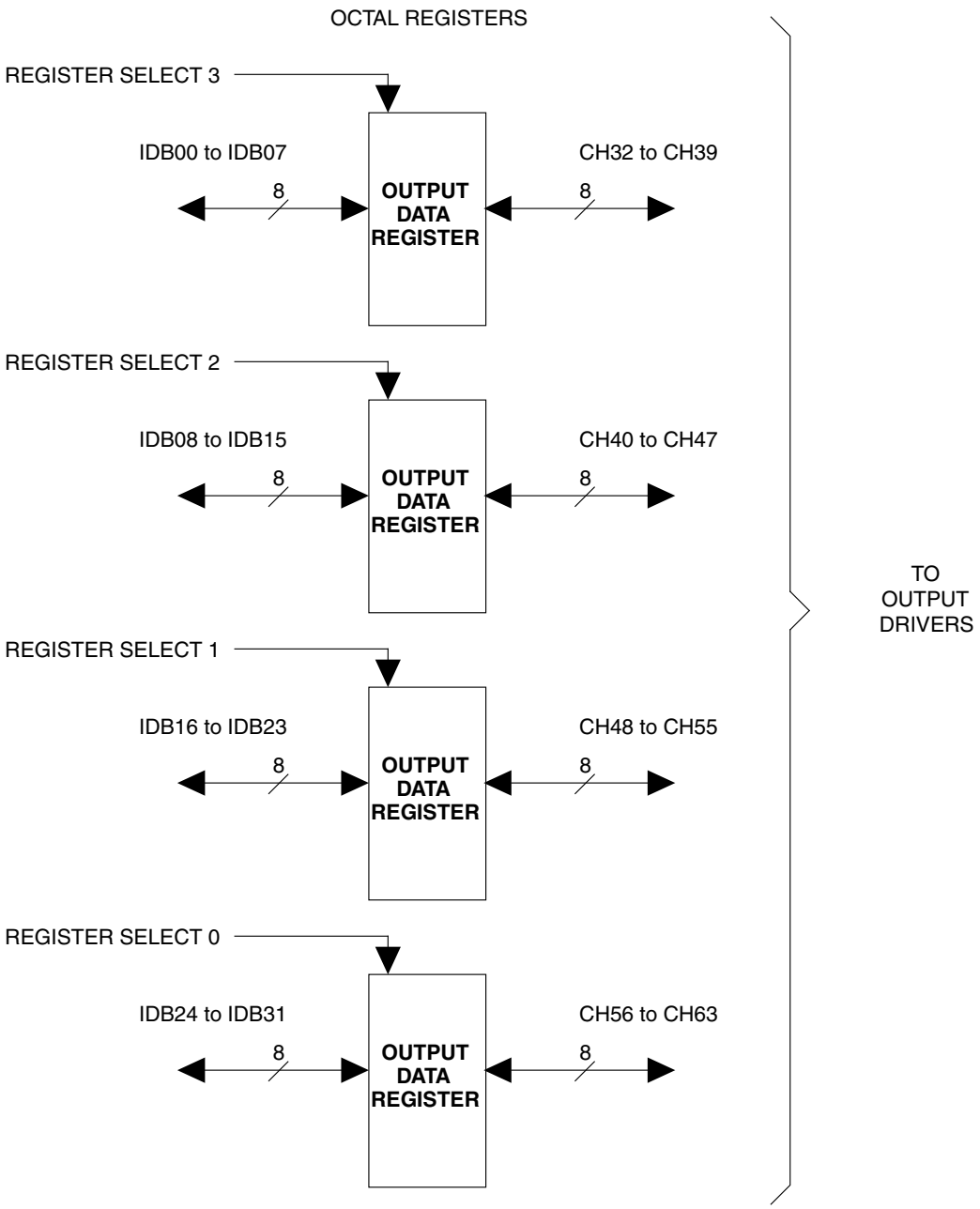
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Figure 2-7 I/O Registers Block Diagram



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Figure 2-8 I/O Registers Block Diagram Bank B



Due to the large output currents possible, each driver pair has a separate pin for their source voltage and ground. This voltage is independent on the TTL control voltage driving the output devices. Its maximum value is determined by the output devices (UDN-2935ZH), which is 35V.

CAUTION

The user should use the cable ground lines for the external power supply returns. This is required to prevent excessive current from flowing into the VMEbus backplane. Also, the user should remove power before the cables are connected or disconnected (from the board). This will prevent excessive currents from damaging the P3/P4 connector pins.

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3 • Programming

3.1 Register Map

The VME-2131 contains eight 8-bit Output Data Registers and an 8-bit Control and Status Register (CSR). These Output Data Registers allow access to sixty-four current source/sink output channels and are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes. The Output Data Registers also support bi-directional transfers, which is used for data validation or diagnostic testing. The CSR is addressable as a 16-bit word or as two 8-bit bytes. It is a write-only register.

3.2 Data Registers

Table 3-1 Output Data Registers

Relative Address	Mnemonic	Name/Function
$XXX0	DR0	DATA REGISTER 0
$XXX1	DR1	DATA REGISTER 1
$XXX2	DR2	DATA REGISTER 2
$XXX3	DR3	DATA REGISTER 3
$XXX4	DR4	DATA REGISTER 4
$XXX5	DR5	DATA REGISTER 5
$XXX6	DR6	DATA REGISTER 6
$XXX7	DR7	DATA REGISTER 7

XXX of the address is determined by data register address select jumpers as shown in *Section 1 • Handling and Installation* on page 10.

DR0 to DR7 are read/write registers.

3.3 CSR Registers

Table 3-2 Control and Status Register

Relative Address	Mnemonic	Name/Function
$YYY0	CSRU	CSR UPPER BYTE
$YYY1	CSRL	CSR LOWER BYTE

YYY of the address is determined by CSR address select jumpers as shown in *Section 1 • Handling and Installation* on page 10.

The CSR is a write-only register.

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3.4 Register Bit Definitions

The following *Table 3-3* and *Table 3-4* on page 31 will list and define the bits established by the output channels and the register that contain the bits as used by the VME-2131 board.

Table 3-3 Output Data Register Bit Definitions

$XXX0 DR0							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
----------OUTPUT DATA REGISTERS----------							
OD63	OD62	OD61	OD60	OD59	OD58	OD57	OD56
$XXX1 DR1							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
----------OUTPUT DATA REGISTERS----------							
OD55	OD54	OD53	OD52	OD51	OD50	OD49	OD48
$XXX2 DR2							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
----------OUTPUT DATA REGISTERS----------							
OD47	OD46	OD45	OD44	OD43	OD42	OD41	OD40
$XXX3 DR3							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
----------OUTPUT DATA REGISTERS----------							
OD39	OD38	OD37	OD36	OD35	OD34	OD33	OD32
$XXX4 DR4							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
----------OUTPUT DATA REGISTERS----------							
OD31	OD30	OD29	OD28	OD27	OD26	OD25	OD24
$XXX5 DR5							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
----------OUTPUT DATA REGISTERS----------							
OD23	OD22	OD21	OD20	OD19	OD18	OD17	OD16
$XXX6 DR6							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
----------OUTPUT DATA REGISTERS----------							
OD15	OD14	OD13	OD12	OD11	OD10	OD09	OD08
$XXX7 DR7							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
----------OUTPUT DATA REGISTERS----------							
OD07	OD06	OD05	OD04	OD03	OD02	OD01	OD00

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Table 3-4 CSR Bit Definitions

$YYY0 CSRU							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
----------NOT USED----------							
$YYY1 CSRL							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
TM = 1	FL = 1	----------NOT USED----------					

3.5 Detailed Programming

3.5.1 Output Data Transfers

As seen in the register map in ***Section 3.1 Register Map*** on page 29, DR0 to DR7 corresponds to output channels 63 to 0. By writing to these Data Registers, any output channel can be controlled.

3.5.2 Built-in-Test

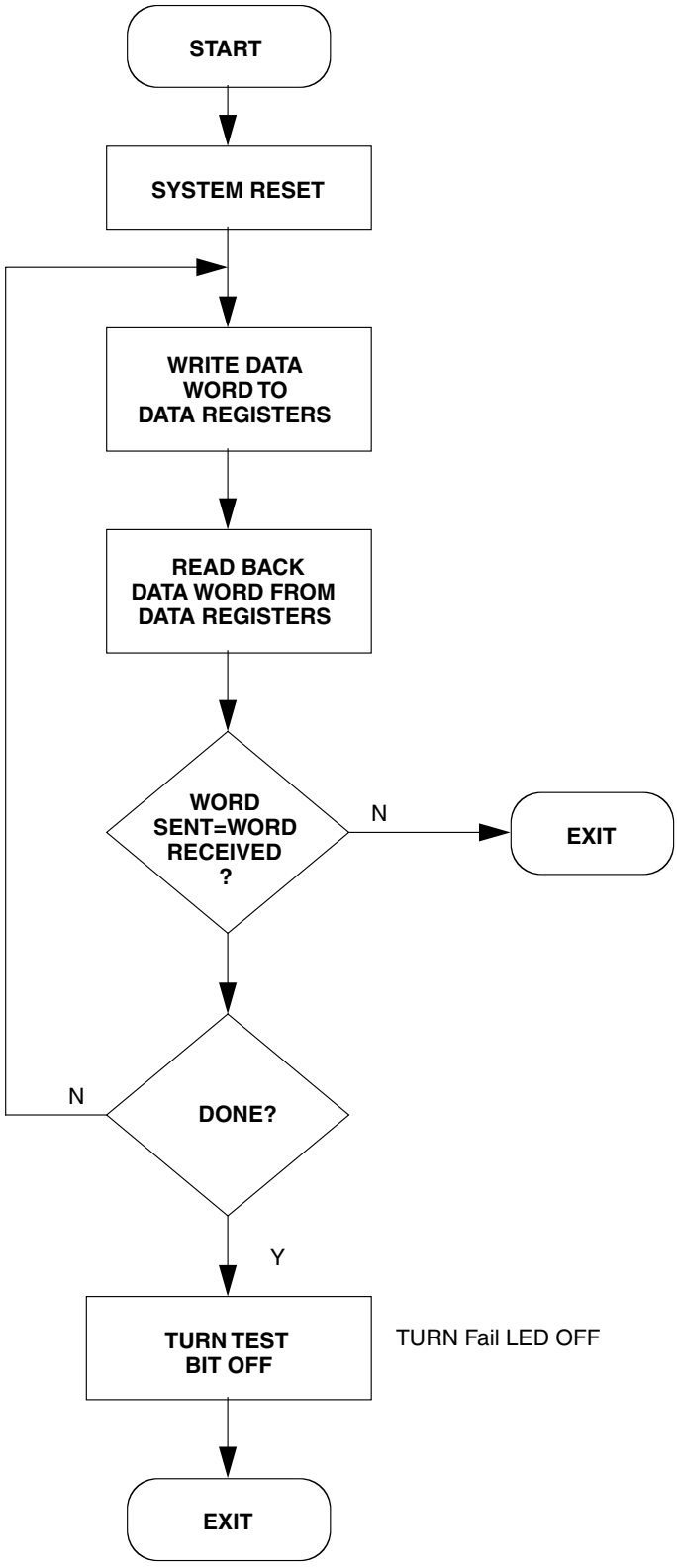
The Built-in-Test features of the VME-2131 provide the user with the capability of real-time loop-back data verification and offline diagnostic execution. The offline Built-in-Test feature is initiated by setting the TM bit in the CSR to a logic “one”. Test data may be written to the selected Data Register and read back on a read transfer.

At powerup or after a system reset, the Test Mode and Failed LED bits of the CSR are initialized active (a logic “one”). In Test Mode, the operator may perform diagnostic testing of the board’s logic and internal registers. At the end of the diagnostic testing, and assuming the board passes, the operator needs to negate (a logic “zero”) the CSR bits used to control Test Mode and the Fail LED. A simplified programming flowchart for Built-in-Test is shown in ***Figure 3-1*** on page 32 and ***Figure 3-2*** on page 33.

The H1 jumper is set at the factory so that Test Mode is active and the LED is illuminated when a logic “one” is written to the CSR. By altering the H1 jumper (moving from +5 V to ground or from ground to +5 V), the user program can activate Test Mode and illuminate the Fail LED by writing a logic “zero” to the CSR. The configuration of H1 is option dependent and is discussed in greater detail in ***Section 1.9 Jumper Functions*** on page 18.

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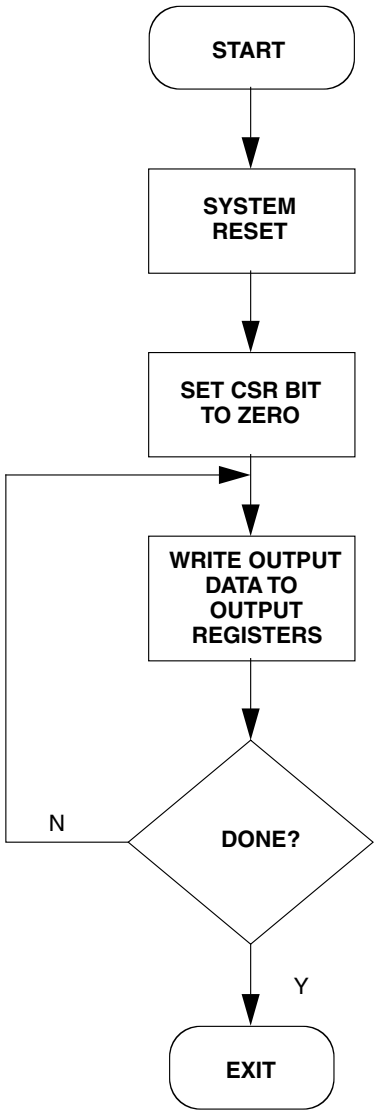
Figure 3-1 Programming Flowchart (Built-in-Test Active)



At system reset, the Fail LED is ON and the output drivers are disconnected.

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Figure 3-2 Programming Flowchart (Built-in-Test Not Active)



NOTE: At system reset, the output drivers are disconnected and the Fail LED is illuminated.

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