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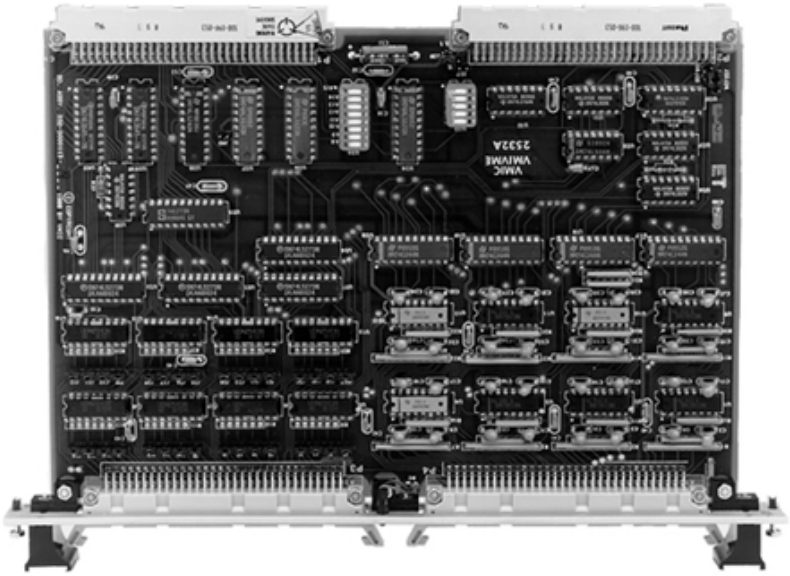
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Hardware Reference Manual

VME-2532A* High Voltage Digital I/O Board

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abaco SYSTEMS

Document History

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Waste Electrical and Electronic Equipment (WEEE) Returns



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About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when “k”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.


NOTE
When describing transfer rates, “k”, “M” and “G” mean $x10^3$, $x10^6$ and $x10^9$ *not* $x2^{10}$, $x2^{20}$ and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

Further Information

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www.abaco.com

Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.

LINK
www.abaco.com/products/vme-2532a-digital-inputoutput-board

The following Application and Configuration Guides are available from Abaco to assist the user in the selection, specification and implementation of systems based on Abaco's products.

Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

Third-party Documents

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA

LINK
www.vita.com/specifications

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Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

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Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.


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Do not return products without first contacting the Abaco Repairs facility.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this Manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

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1 • Introduction

1.1 Features

The VME-2532A is a VMEbus Compatible High Voltage Digital I/O Board with 32 channels of high voltage digital outputs and 32 channels of high voltage digital inputs. Its features include:

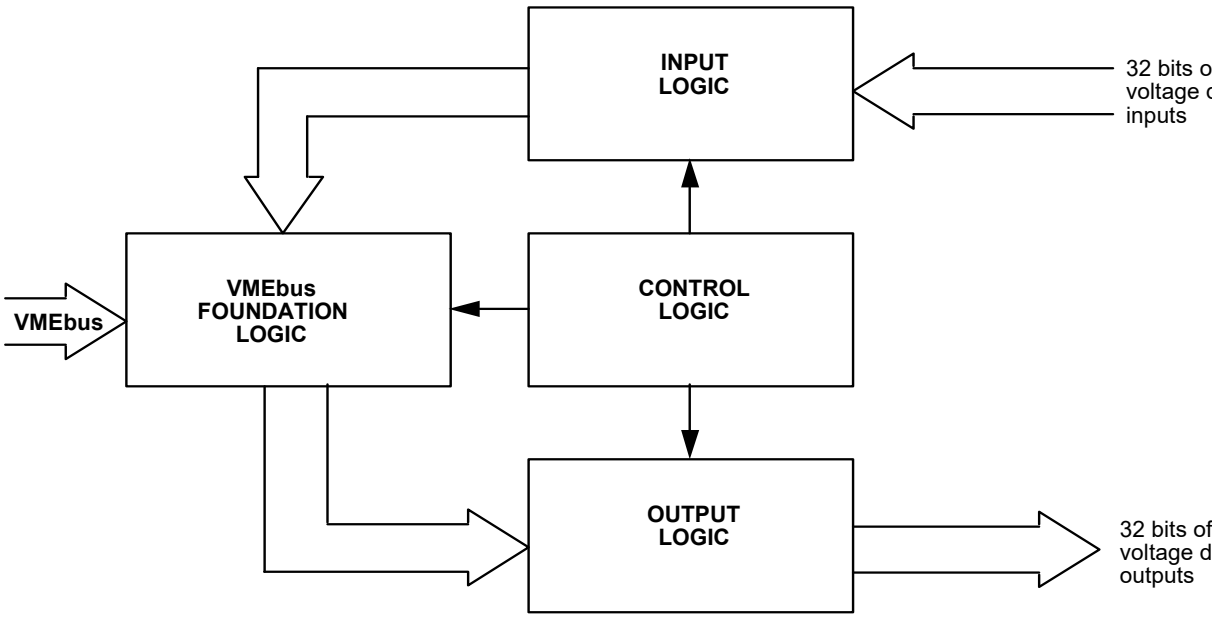
- 32 bits of high voltage outputs
- High current sink (600 mA)
- High breakdown voltage (70 V)
- Output voltage range options (5, 12, 24, 48 V, and TTL compatible)
- Output clamp diodes
- Outputs may be paralleled for higher drive capability
- 8- or 16-bit transfers
- 32 bits of high voltage inputs
- Input voltage range options (5, 12, 24, 48 V, and TTL compatible)
- Voltage sourcing or current sinking inputs
- Inputs have hysteresis and filtering options
- Built-in-test (off-line and real-time support)
- Front panel with Fail LED
- Jumper-selectable output test for 100 percent testing of output drivers
- Compatible with VME-9016 Intelligent I/O Controller

1.2 Functional Description

The 32-bit digital input/output (DIO) board transfers digital data from the VMEbus backplane to one of two 16-bit output registers that are interfaced to high voltage output drivers. It also reads one of two 16-bit banks of high voltage signal conditioned inputs and transfers the data to the VMEbus backplane for subsequent transfer to a CPU. ***Figure 1-1*** illustrates a simplified functional block diagram.

The high voltage DIO board is designed with a variety of manufacturing options to allow the user to specify board input and output configuration. Input signal conditioning electronics support voltage sourcing and current sinking configurations. A wide variety of input voltages, output voltages and output configurations are supported. The current sinking input configuration is normally used to detect open or closed contacts or the ON/OFF states of an electronic switch. Voltage source versions of the input signal conditioning are used to detect the presence or absence of a voltage connected to the board inputs. Voltage source inputs may be standard logic, mechanical switch contacts, or any other voltage source up to the absolute maximum voltage (e.g., 50 V for the 48 V option). The high voltage digital output configurations may be open collector, TTL compatible or electronic switch outputs.

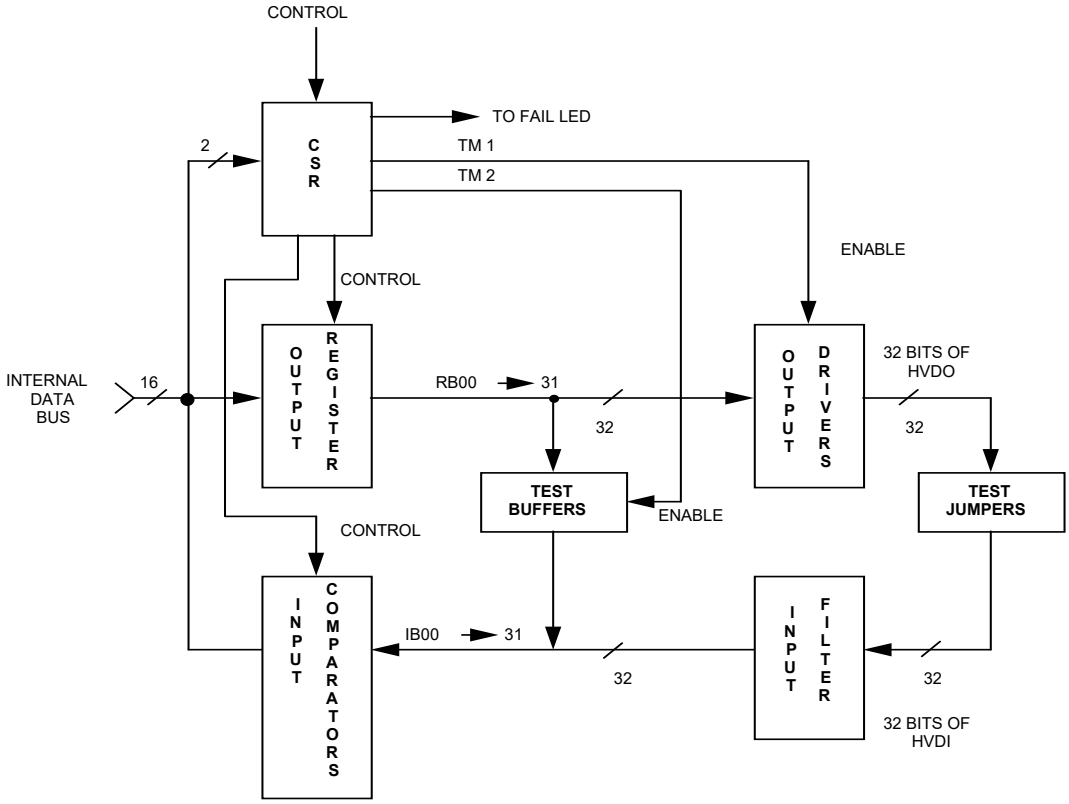
Figure 1-1 Basic Digital I/O Functions



The VME-2532A DIO Board is designed with extensive Built-in-Test electronics that enables the user to output data words to the output registers and read the contents from the input electronics. The board is also designed such that jumpers may be installed that connect each output driver to a selected input for 100 percent testing of the output circuits. In this mode, the digital inputs are not available for reading user input data.

A functional block diagram of the Built-in-Test features of the VME 2532A DIO Board is shown in ***Figure 1-2***.

Figure 1-2 Simplified Built-in Test Functional Block Diagram



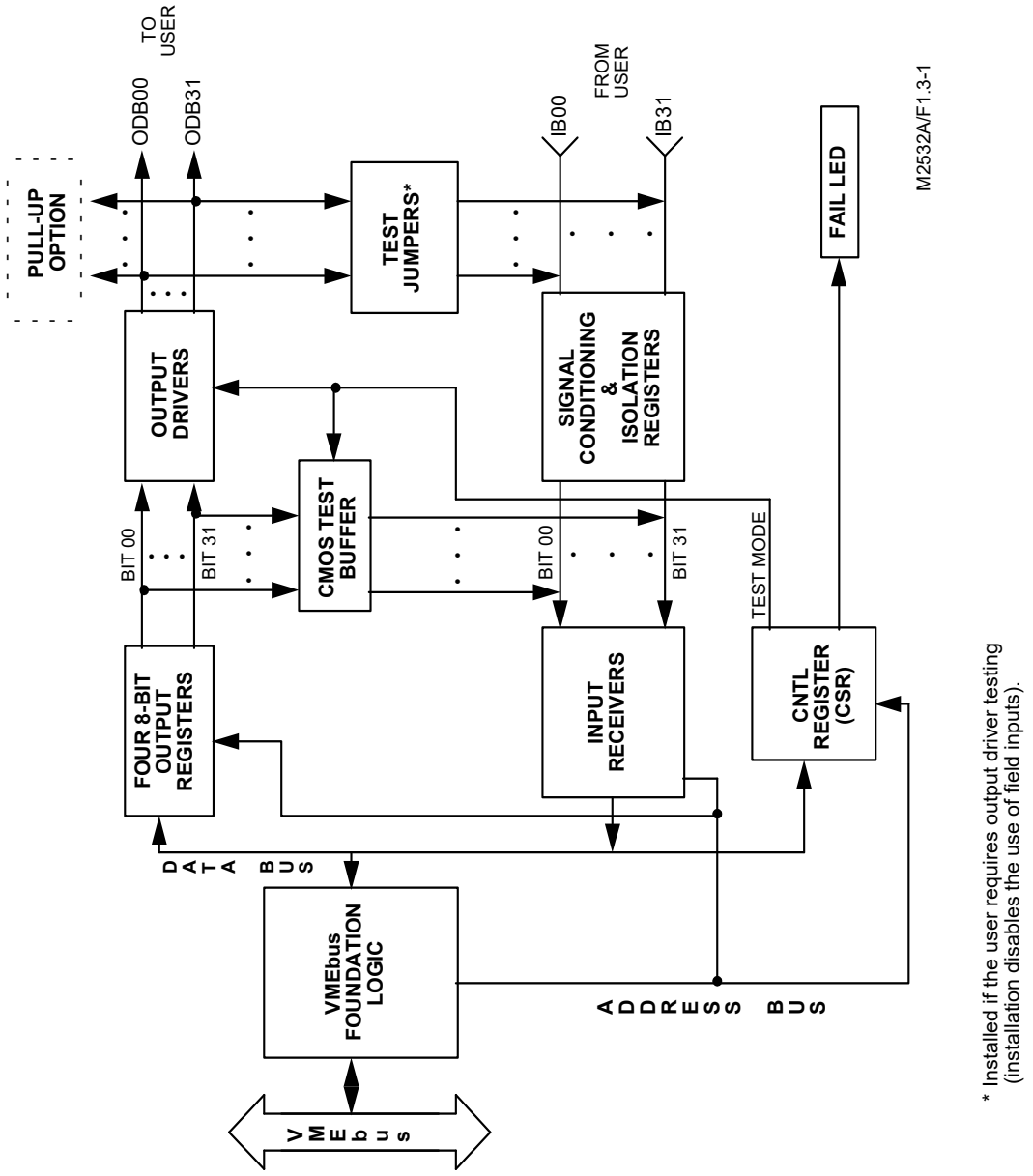
1.3 Functional Block Diagram

The VME-2532A High Voltage Digital I/O Board consists of VMEbus compatibility logic, four 8-bit output registers, four 8-bit input ports, a Control/Status Register, and Built-in-Test logic, as shown in ***Figure 1-3***.

The VMEbus compatibility logic controls data transfer allowing 8- or 16-bit VMEbus data transfers. Four 8-bit output registers latch 32 bits of output data, which drive high voltage output drivers to the field connector. The Control/Status Register (CSR) uses three bits. One bit controls the on-board Fail LED, while the other two bits control the test functions of the board.

Built-in-test logic enables output data to be read back through the input register without affecting incoming signals from the field. System reset or power up puts the board in test mode for immediate loopback testing.

Figure 1-3 Functional Block Diagram



2 • Theory of Operation

2.1 Introduction

This section of the manual presents information concerning the hardware operation of the board. The reader should refer to Abaco Document No. 825 000000-000 (Digital Input Board Application Guide) for a thorough understanding of voltage sourcing and current sinking concepts.

2.2 Operational Overview

The VME-2532A consists of five primary sections as illustrated in ***Figure 2-1***. These sections are described in detail in the following sections.

To perform output data transfer, data is written into output data registers, which latch the data. The latched data drives the output driver stage of the board.

High voltage digital inputs are converted to TTL levels by the input comparators, which compare incoming signals with a bias voltage. To perform input data transfers, data is read from the input comparators.

2.3 VMEbus Foundation Logic

A block diagram, shown in ***Figure 2-2, VMEbus Foundation Logic*** on page 14 illustrates the data transceivers, the DTACK generator, and the control signal bus receivers.

Data transfers to and from the VMEbus pass through the data transceivers, which provide buffering to the VME-2532A and proper drive and loading to the VMEbus. The direction of transfer is determined by the read/write control line.

Control lines from the VMEbus are received by bus receivers, which present minimum VMEbus loading and provide buffering to the board logic.

DTACK is the board's response to the VMEbus when its address has been selected and the board has stable data available or is prepared to accept data. The DTACK generator is designed to select the maximum data transfer speed.

Figure 2-1 Functional Block Diagram

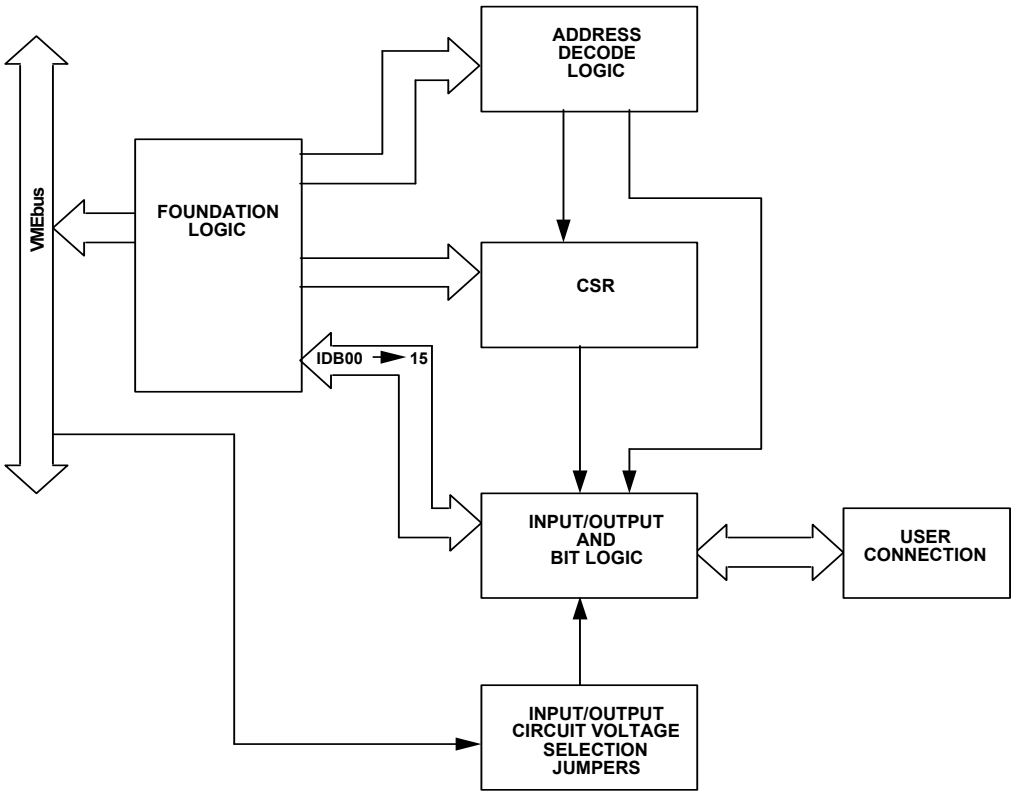
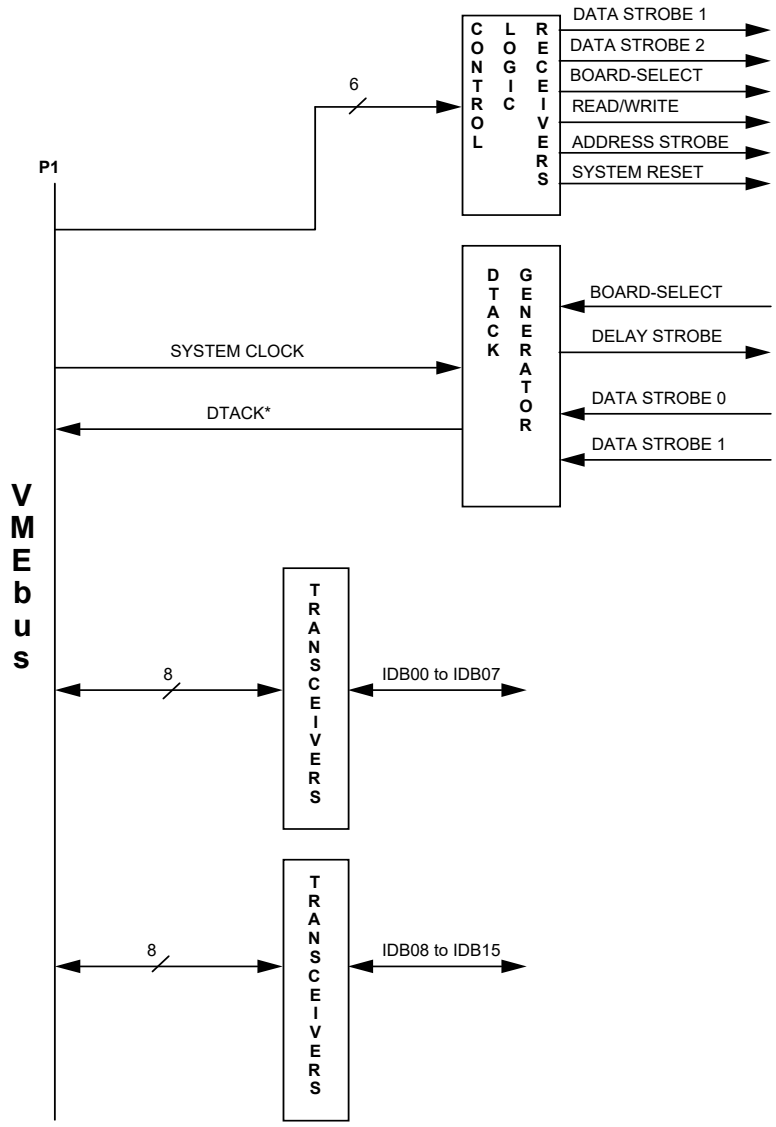


Figure 2-2 VMEbus Foundation Logic

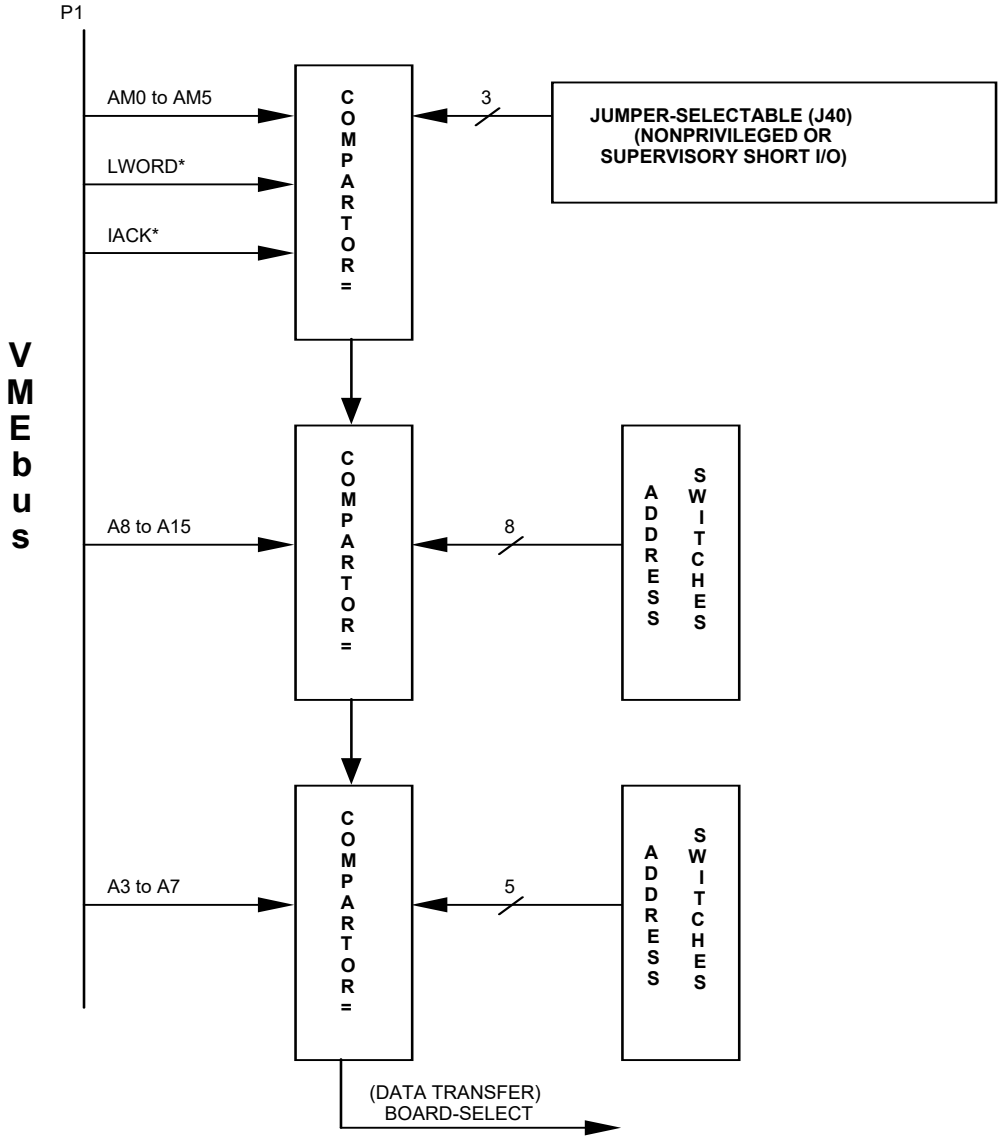


2.4 Device Addressing

The VME-2532A utilizes three magnitude comparator IC's that monitor address lines A3 through A15; address modifier lines AM0 through AM5, IACK* and LWORD*. When the monitored lines match the switch-selectable board address and jumper-selected address modifier, a DTBSL (Data Transfer Board Select) signal is generated.

The board is designed to support data transfers in supervisory or nonprivileged short I/O memory space. A jumper (J40) is provided as shown in ***Figure 2-3*** to allow user-selection of either I/O access type. The VME-2532A is factory configured (jumper J40 not installed) to respond to short supervisory I/O access.

Figure 2-3 Address Decode Block Program

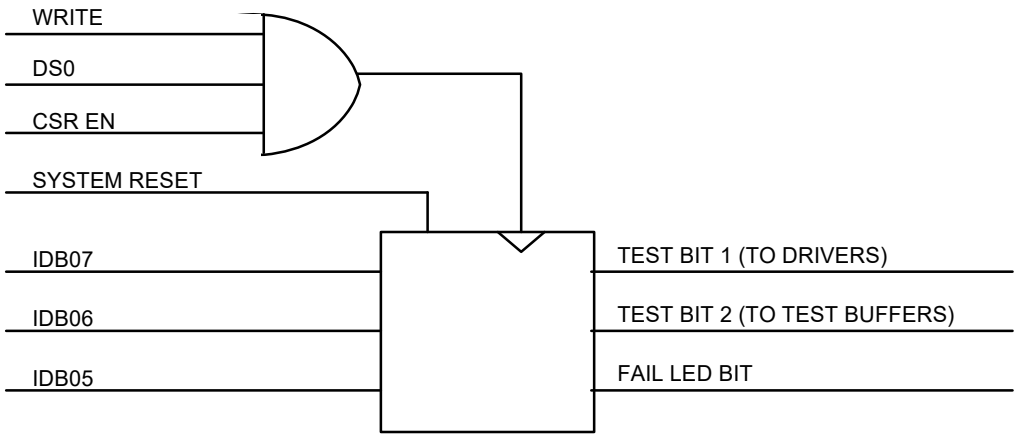


2.5 Control and Status Register (CRS)

The CSR is a write only register that controls the Test Mode (TM) bits and the front panel Fail LED as shown in *Figure 2-4*. TM bit 1 enables the output drivers, and TM bit 2 enables the test buffers. The CSR bits are initialized to logical "zero". This occurs after power-up or at system reset. In this state the board is in the off-line test mode with the output drivers disabled, the test buffers enabled, and the front panel Fail LED illuminated.

When writing to the CSR the data polarity must be taken into account. If the negative true data polarity option is selected, the data written to the CSR will be inverted by the data transceivers interfacing with the VMEbus. Thus, for a negative true data polarity option the data used to control the board (via the CSR) is inverted and the software must account for this.

Figure 2-4 CSR Block Diagram



2.6 Digital INPUT/OUTPUT and Built-in-Test (BIT) Description

The digital input/output and built-in-test section is comprised of the output data register, the output driver, the input comparator, and the test buffer. Both outputs and inputs are provided with various voltage level and logic type options, additionally the inputs are offered with various filtering options.

In the on-line (normal) mode of operation a write instruction initiates a data transfer from the VMEbus via the internal data bus to the output data register and hence to the output drivers and user connector P3. User data received at P4 is sensed at the input comparator and presented to the internal data bus and the VMEbus when a read data instruction is performed.

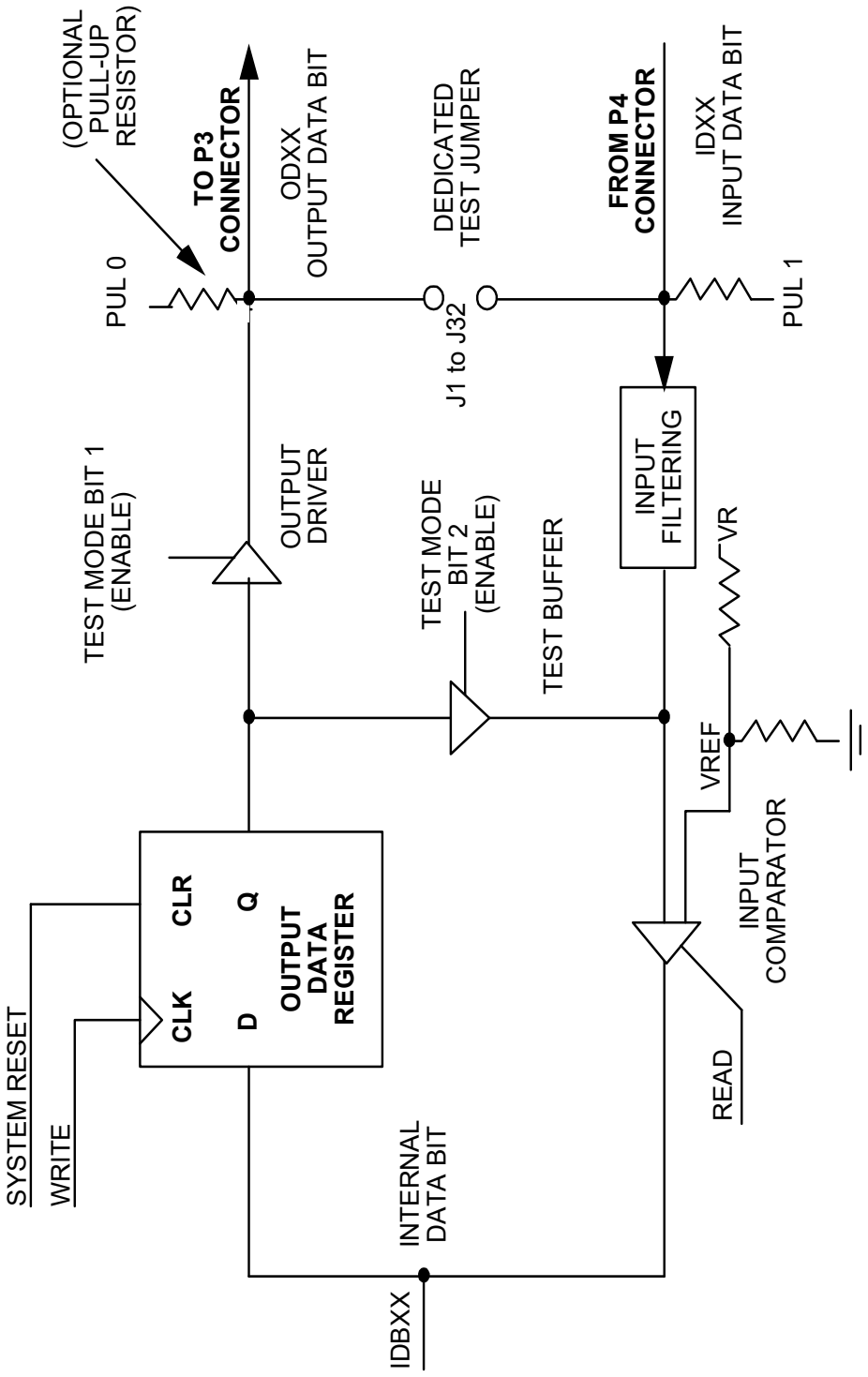
The VME-2532A test logic provides for three different modes of testing: an off-line test mode, an on-line test mode, and a dedicated on-line test mode. Upon system reset, the CSR register is cleared to all "zeroes" initializing the board in the off-line test mode. This mode of test disables all output drivers and enables all test buffers allowing a loop-back test of data without effecting off- board circuitry. Test mode bits 1 and 2 are reset.

The on-line test mode is initiated by enabling the output data drivers as well as the test buffers. This mode allows data that is latched in the output data register to be read back through the input comparators, while the output drivers are active. Test mode bit 1 is set; 2 is reset.

The dedicated on-line test mode is characterized by jumpering each output channel, jumpers J1 through J32 installed, to a paired input channel (same channel number). In this mode the input stage is dedicated to reading outputs and should not be connected to any field electronics. Test mode bit 1 and 2 are both set.

Both the on-line and off-line test modes do not affect incoming data from the field, while the dedicated on-line test mode assumes that the field inputs are not used. A detailed functional block diagram is shown in ***Figure 2-5*** that depicts a typical path for an I/O data bit.

Figure 2-5 Digital Input/ Output and BIT

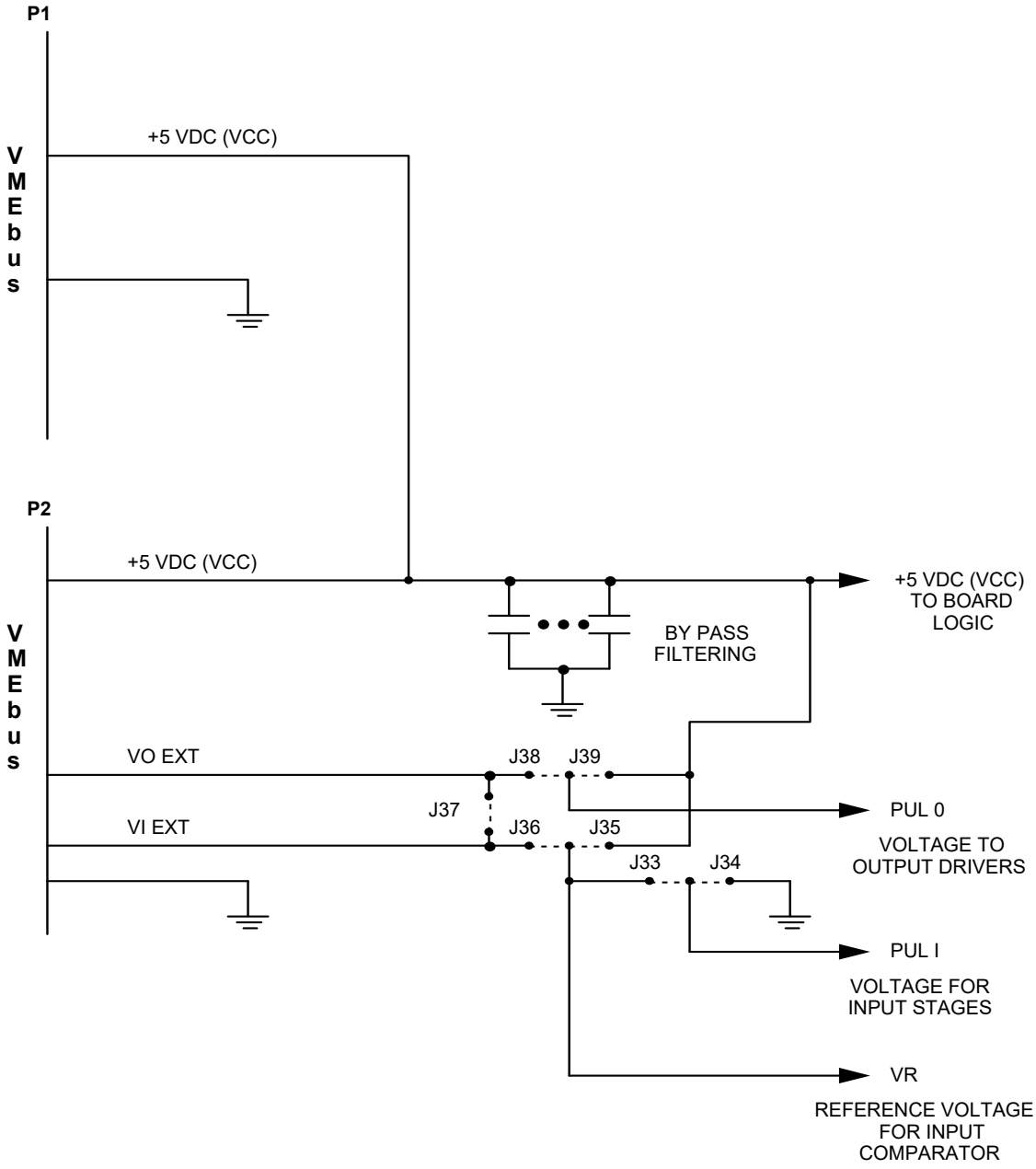


TYPICAL PATH FOR I/O DATA BIT

2.7 INPUT/OUTPUT Circuit External Voltage Selection

The VME-2532A is designed to operate with a wide variety of input and output voltages. A variety of jumpers are provided as shown in *Figure 2-6* to support these options.

Figure 2-6 External Voltage Selection Block Diagram



3 • Programming

3.1 Introduction

The VME-2532A performs output transfers by writing data to the appropriate output data registers. High voltage digital inputs are read by performing a read from input data registers. For programming simplicity the registers are mapped into the same address locations, therefore, the bits of each register correspond to an output channel when performing a write to that register, and to an input channel when performing a read cycle.

The base address required for accessing the VME-2532A is selected by the address switches U33 and U35 shown in ***Figure 4-2, Base Address Selection Switches*** on page 22. The on-board registers are selected by address bits A02, A01, and the data strobes.

3.2 Data Output

A data output operation is initiated when the CPU executes an instruction that sends a board address that causes selection of the board. When the CPU executes an instruction to store data, VMEbus control signals cause the board to store the output data as transferred from the VMEbus. The format of the output data and the board address is shown in ***Table 3-1, Register Address and Bit Definitions*** on page 20.

3.3 Data Input

A data input operation is initiated when the CPU executes an instruction that sends a board address that causes the selection of the board. When the CPU executes an instruction to read data, VMEbus control signals cause the board to place a data input word on the VMEbus for transfer to the computer. The format of the input data and the board address is shown in ***Table 3-1***.

3.4 Control and Status Register (CSR)

The CSR is a write only register that controls the Test Mode (TM) bits and the front panel Fail LED as shown in ***Figure 2-4, CSR Block Diagram*** on page 16. One of the TM bits enables the TRI-STATE outputs of four CMOS buffers, which are used to perform built-in-test functions. The other test mode bit is used to disable the output drivers, which supports off-line built-in-test functions. The format of the CSR data and address is shown in ***Table 3-1***. The CSR is initialized active upon system reset. Thus, the outputs are disabled, the CMOS buffer outputs enabled and the front panel Fail LED is illuminated.

Table 3-1 Register Address and Bit Definitions

HEX ADDRESS A15 TO A4			BINARY ADDRESS A3	A2	A1	A0								
							DATA PORT 0 (UPPER BYTE)							
X	X	X	X	0	0	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8
							I/O 31	I/O 30	I/O 29	I/O 28	I/O 27	I/O 26	I/O 25	I/O 24
							DATA PORT 1 (MIDDLE UPPER BYTE)							
X	X	X	X	0	0	1	IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0
							I/0 23	I/O 22	I/O 21	I/O 20	I/O 19	I/O 18	I/O 17	I/O 16
							DATA PORT 2 (MIDDLE LOWER BYTE)							
X	X	X	X	0	1	0	IDB 15	IDB 14	IDB 13	IDB 12	IDB 11	IDB 10	IDB 9	IDB 8
							I/O 15	I/O 14	I/O 13	I/O 12	I/O 11	I/O 10	I/O 9	I/O 8
							DATA PORT 3 (LOWER BYTE)							
X	X	X	X	0	1	1	IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0
							I/O 7	I/O 6	I/O 5	I/O 4	I/O 3	I/O 2	I/O 1	I/O 0
							BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
X	X	X	X	1	0	0	NOT USED							
							CONTROL AND STATUS REGISTER							
							IDB 7	IDB 6	IDB 5	IDB 4	IDB 3	IDB 2	IDB 1	IDB 0
X	X	X	X	1	0	1	TM1*	TM2*	FAIL*	NOT USED	NOT USED			
X	X	X	X	1	1	0	NOT USED							
X	X	X		1	1	1	NOT USED							
ADDRESS SELECTION SWITCHES														

CSR BIT DEFINITIONS

TM1* Set to a "zero" to disable output drivers. Set to a "one" to enable output drivers.

TM2* Set to a "zero" to enable test buffers. Set to a "one" to disable test buffers.

FAIL* Fail mode LED bit. FAIL LED is on if the bit is "zero", off if it is a "one".

*For the I/O true data ordering option - 00 (neg true inputs and neg true outputs): invert the data for these three bits (they are active LOW)

4 • Configuration and Installation

4.1 Unpacking Procedures

CAUTION

Some of the components assembled on Abaco's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes as shipped. When the board is to be laid on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Systems Customer Care.

4.2 Physical Installation

CAUTION

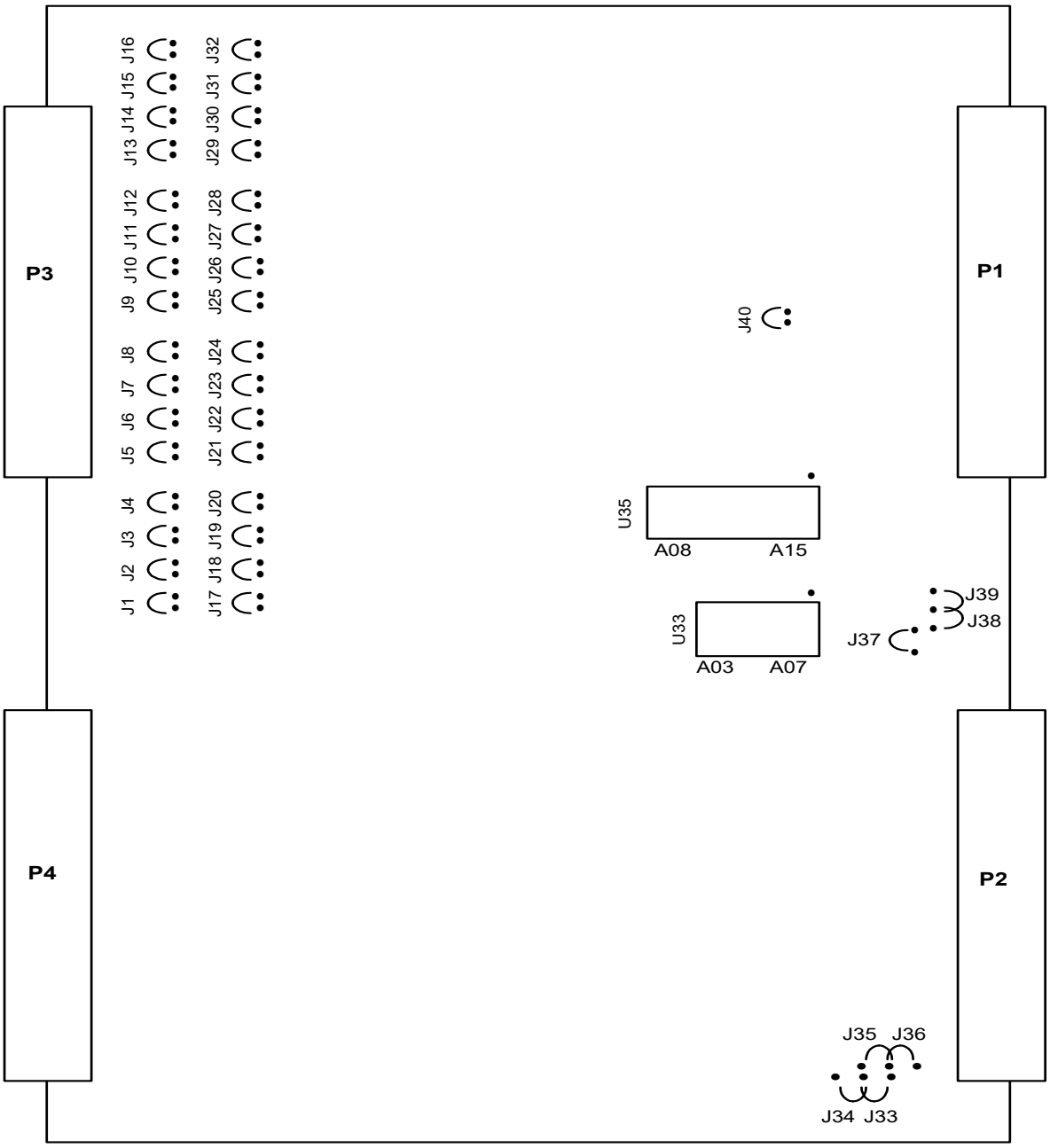
Do not install or remove boards while power is applied unless power-up replacement is selected.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

4.3 Dedicated Online Test Configuration

Dedicated on-line testing is characterized by jumpering each output channel to a paired input channel (one with the same channel number). In this mode, the input stage is dedicated to reading the outputs and should not be connected to the field inputs. The output stages are jumpered directly to their corresponding input stages by installing jumpers J1 through J32. See ***Figure 4-1*** for the jumper locations.

Figure 4-1 Jumper and Switch Locations



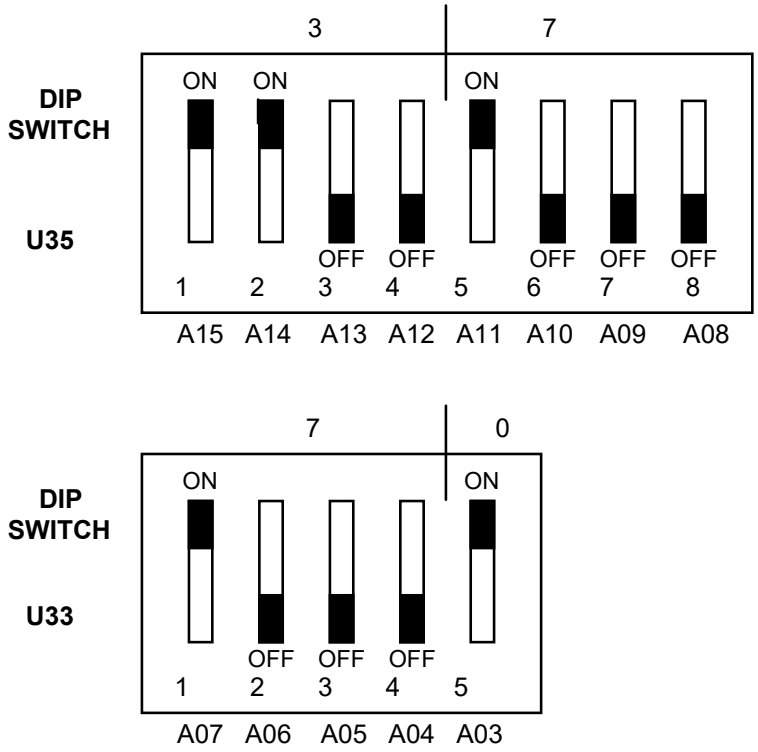
4.4 Address Modifiers

The VME-2532A Board is configured at the factory to respond to short supervisory I/O access. This configuration can be changed by installing jumper J40 as shown in ***Figure 4-1***. With J40 installed the board will respond to short nonprivileged I/O access.

4.5 Board Base Address

The VME-2532A Board occupies 8 bytes of the VMEbus short I/O address space. *Figure 4-2* shows the base address DIP (dual in-line packaged) switches. The physical location of the switches are shown in *Figure 4-1*.

Figure 4-2 Base Address Selection Switches



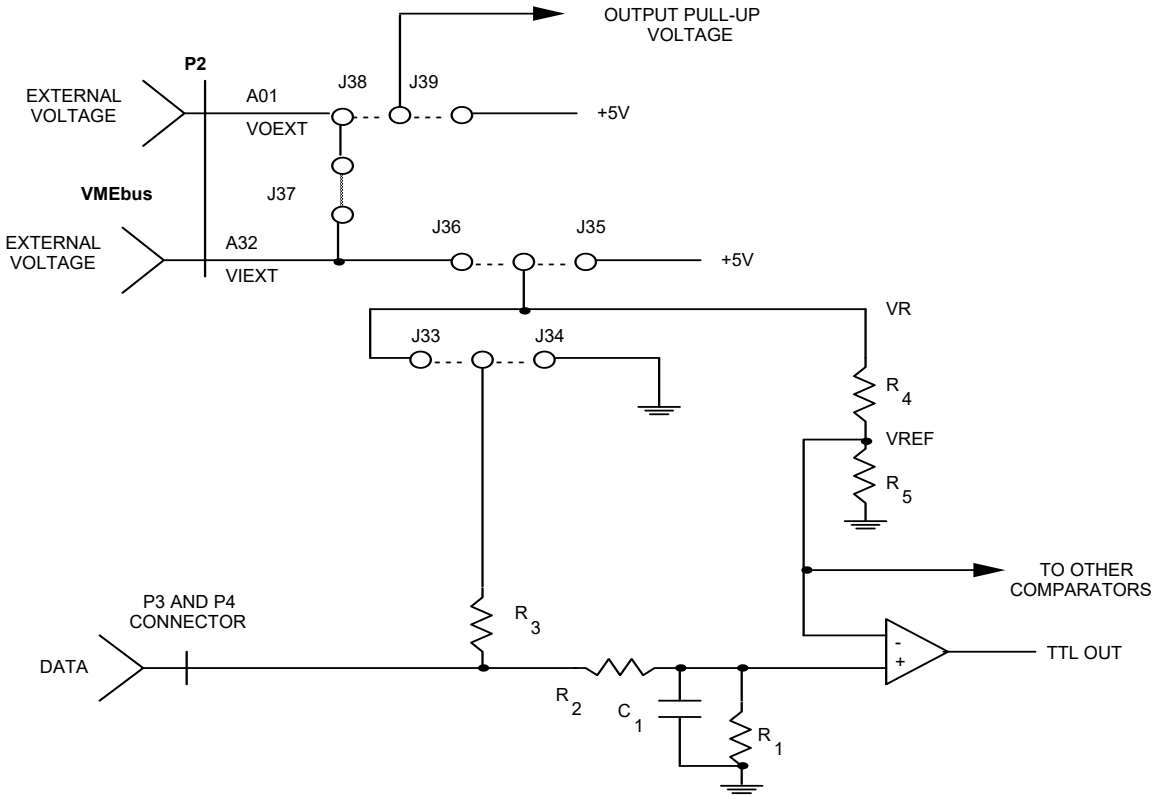
Example: Hex Base Address = $3770 = 0011 0111 01110

4.6 Current Sink, Voltage Source Selection

For the specified voltage ranges for each board option, jumpers J33 and J34 can be installed to select between a current sink configuration or a voltage source configuration.

The board is configured for current sink with jumper J33 installed or for voltage source with jumper J34 installed as shown in *Figure 4-3*. The physical location of jumpers J33 and J34 is shown in *Figure 4-1*.

Figure 4-3 Signal Conditioning Configuration Selection



4.7 Output/ Input Pull-up Voltage

A pull-up voltage, if required, can be supplied through an external source via the P2 connector on pin A32 for input pull-up (J36 installed) or through the P2 connector pin A1 for output pull-up (J38 installed). The current demand on these lines should not exceed 1 A to prevent damage to the VMEbus backplane. The user can also select the pull-up voltage from the onboard +5 V voltage source by installing J39 for output and J35 for input. Jumper J37 allows a common connection of the selected input and output pull-up voltage.

The reader should refer to ***Figure 4-3*** for jumper configuration, to ***section 1.2, Functional Description*** on page 9 for optional input voltage requirements, and ***section 4.9, External Pull-up Voltage/ Suppressor Diode Connections*** on page 27 for output pull-up/suppressor DIODE connections.

4.8 I/O Cable and Front Panel Connector Configuration

The I/O connectors (P3 and P4) are 64-pin DIN standard and were selected by Abaco because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to ***Technical Support Contact Information*** on page 4 for additional information concerning the variety of possible cabling and connector types available.

Details concerning input connections are shown in ***Figure 4-4***. This figure has conductor No. 1 shown at the bottom of the connector as it plugs into the header, due to pin No. 1 of P3 and P4 being mounted as shown.

Connector pin assignments for the 64 I/O channels of the VME-2532A are shown in ***Table 4-1*** and ***Table 4-2***. The I/O connector pin configurations for P3 and P4 are shown in ***Figure 4-5*** on page 25. Details concerning connector P2 user I/O pins and the use of the external voltage input are shown in ***Table 4-3, P2 Connector Pin Assignments*** on page 26 and ***Figure 4-6, P1/P2 Connector Pin Layout*** on page 26.

The board is designed with a high quality ground plane that is connected to the VMEbus ground and to alternate pins on connectors P3 and P4 to provide enhanced noise immunity and more reliable operation.

A compatible flat-ribbon cable connector for the VME-2532A is Panduit No. 120-964-455E, and the strain relief is Panduit No. 100-000-032.

Figure 4-4 Cable Connector Configuration

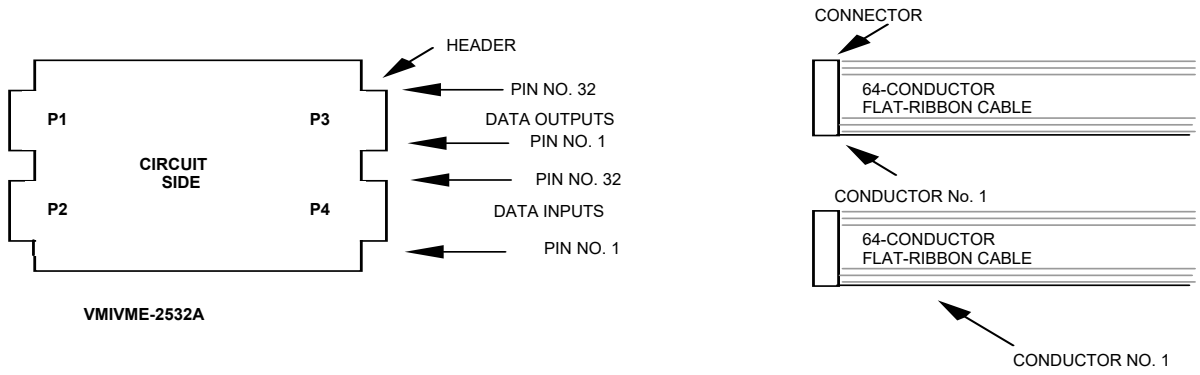


Table 4-1 P3 Output Connector Channel Assignment

P3*		P3*	
Row A Pin#	Channel No.	Row A Pin#	Channel No.
32	31	16	15
31	30	15	14
30	29	14	13
29	28	13	12
28	27	12	11
27	26	11	10
26	25	10	09
25	24	09	08
24	23	08	07
23	22	07	06
22	21	06	05
21	20	05	04
20	19	04	03
19	18	03	02
18	17	02	01
17	16	01	00
*All pins on Row C pins are grounded			

Table 4-2 P4 Input Connector Channel Assignment

P4*		P4*	
Row A Pin#	Channel No.	Row A Pin#	Channel No.
32	31	16	15
31	30	15	14
30	29	14	13
29	28	13	12
28	27	12	11
27	26	11	10
26	25	10	09
25	24	09	08
24	23	08	07
23	22	07	06
22	21	06	05
21	20	05	04
20	19	04	03
19	18	03	02
18	17	02	01
17	16	01	00
*All pins on Row C pins are grounded			

Figure 4-5 P3/P4 Connector Pin Layout

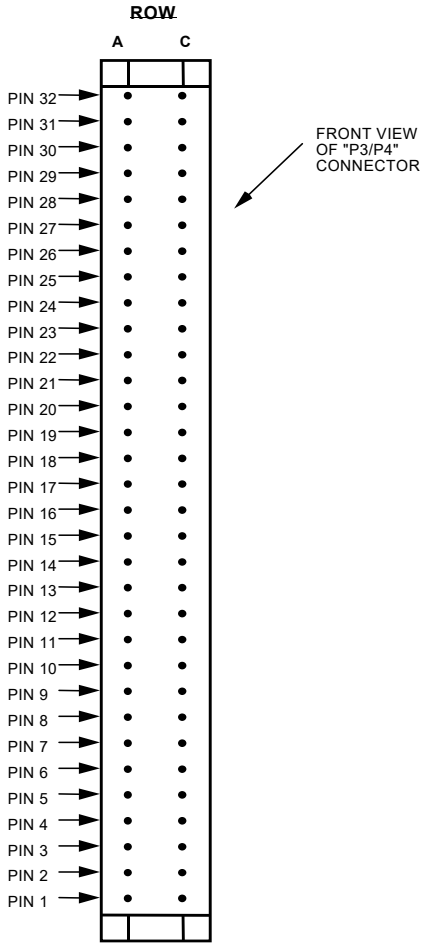
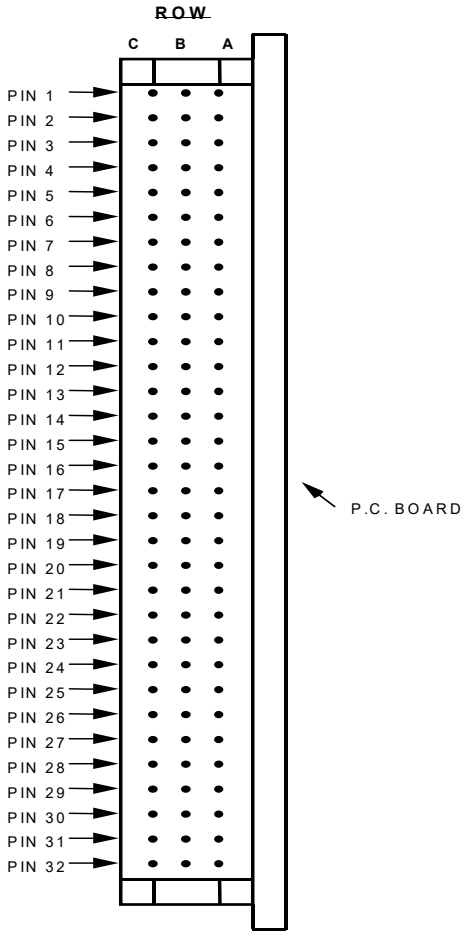


Table 4-3 P2 Connector Pin Assignments

P2			
Pin #	Row A[1]	Row B[2]	Row C
1	VOEXT	+5 V	
2		GND	
3 -11			
12		GND	
13		+5V	
14 - 21			
22		GND	
23 - 30			
31		GND	
32	VIEXT	+5V	

1. External Voltage is supplied by the user.
2. Inputs to Board - not required

Figure 4-6 P1/P2 Connector Pin Layout



4.9 External Pull-up Voltage/ Suppressor Diode Connections

The output drivers of the VME-2532A have built in suppressor diodes for driving inductive loads. If the user requires operation for a relay driver or a similar application, the coil voltage must be connected to the VME-2532A via connector P2 pin A1. ***Figure 4-3, Signal Conditioning Configuration Selection*** on page 23 and ***Table 4-3, P2 Connector Pin Assignments*** on page 26 show the configuration and the required external voltage connection. Signal PULO is routed to all 32 output channels.

In addition to supplying inductive flyback suppression diodes with voltage, the PULO signal supplies optional pull-up resistors with pull-up voltage for current source applications.

The on-board 5 VDC supply can be jumpered to the PULO signal if +5 VDC is to be used for a pull-up voltage.

If the total load current exceeds 1 A, it is important that the grounded conductors be connected to any power supply (GND Return) associated with these signal loads, in order to prevent excessive currents (DC or Noise) from flowing through the VMEbus backplane.

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