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Find the *Abaco Systems / VMIC VMIVME-3115-010* at our website: ***Click HERE***

VMIVME-3115

2 MHz 12-bit Analog Input Board with Simultaneous Sample-and-Hold Inputs, Dual Analog Outputs, and 16-bit Digital I/O

ANALOG INPUTS

- High throughput; aggregate scan rates to 2 MHz
- Four sample-and-hold, differential analog input channels
- 12-bit analog-to-digital converter (ADC), with range options of 0 to +5 V and ±5 V, or 0 to +10 V to ±10 V
- Simultaneous sampling of all inputs
- Dual 256 Kbyte data buffers
- Continuous or synchronous sequencing
- Multiboard or independent synchronizing
- Program-controlled bus interrupter
- No programming required in software transparent operating mode
- MTBF: 32,800 hrs. (217E)

ANALOG OUTPUTS

- Dual 12-bit (10 mA) analog outputs
- Output ranges of 0 to +10 V, ±5 V, and ±10 V

DIGITAL INPUT/OUTPUT

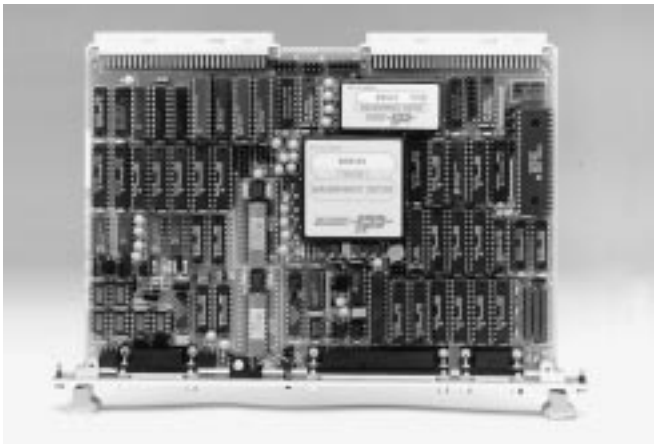
- Dual 8-bit TTL I/O ports, program controlled as inputs or outputs

GENERAL DESCRIPTION — The VMIVME-3115 is a high throughput ,12-bit Analog Input/Output (AIO) board which provides four analog inputs, two analog outputs, and dual 8-bit bi-directional digital input/output ports for VMEbus system applications. Dual-ported data memory, on-board timers, and a program-controlled bus interrupter enables the VMIVME-3115 board to support extensive analog input and output traffic with minimum involvement of the host processor.

Sample-and-hold input amplifiers provide "snapshot" simultaneous sampling of all analog inputs at aggregate sample rates up to 2 MHz, and virtually eliminate time skewing between input channels. The VMIVME-3115 supports both independent and multiboard synchronization. Dual analog outputs enable the board to "close the loop" in system servo applications. The VMIVME-3115 functional block diagram is shown in Figure 1.

Analog input data is stored sequentially in dual 256 Kbyte buffer memories. The host controls which one of the two buffers will reside in VMEbus memory through a single toggle bit in the Control and Status Register (CSR). The host can also direct the board to generate an interrupt when a scanning sequence is completed.

Analog inputs can be sequenced either continuously, single block synchronously, or multiboard synchronously. In the continuous mode, sequencing executes continuously until stopped by the host processor. In the single block synchronous mode, a preselected block of data is transferred, after which



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ORDERING INFORMATION

October 13, 1997 800-003115-000 C		A	B	C	–	D	E	F
VMIVME-3115	–			0	–			

A = Front Panel Connector Options
0 = 15-pin "D-Sub" Analog Input Connector
1 = Four BNC Analog Input Connectors

B = Input Voltage Range and Sampling Rate Selection
0 = 0 to +5 V and ±5 V Option with 2, 1, .5, .25, .125, .0625, .03125, .01563 M channels/s
1 = 0 to 10 V and ±10 V Option with 2, 1, .5, .25, .125, .0625, .03125, .01563 M channels/s
2 = 0 to +5 V and ±5 V Option with 2, 1, .5, .4, .2, .1, .05, .025 M channels/s
3 = 0 to +10 V and ±10 V Option with 2, 1, .5, .4, .2, .1, .05, .025 M channels/s

C = 0 (Option reserved for future use)

I/O CONNECTOR DATA (*)

Typical Connecting Component	P2 (Panduit)	P3 (**) (AMP)	P4 (AMP)	P5 (AMP)
Compatible Mating Connector	120-964-435E	747945-5	747949-5	747943-5
Strain Relief	100-000-032	1747580-8	1-747579-0	747579-8
PC Board I/O Connector	101-096-033A (96-pin DIN)	747841-3 (15-pin Plug)*	747843-3 (37-pin Plug)	747840-3 (9-pin Plug)*

* P3, P4, and P5 are standard D-Subminiature connectors.
** P3 is replaced with four BNC connectors if Option A = 1 is specified.

For Ordering Information, Call:
1-800-322-3616 or 1-205-880-0444 • FAX (205) 882-0859
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sequencing halts. Multiboard synchronization can be applied to either the continuous or single block modes, with a designated board controlling other VMIVME-3115 boards.

Each buffer memory appears as 256 Kbytes of VMEbus memory. To simplify automatic system configuring, the buffer is disabled during power up and reset operations. To support multiple VMIVME-3115 boards without requiring additional memory space, the buffer can be removed from the VMEbus memory entirely through a control bit in the I/O space CSR. The buffer is jumper locatable on any 4 0000 byte (HEX) boundary in the VMEbus memory space. Block Mode D16 data transfers (BLT) are supported.

Dual analog output channels can drive 10 mA loads over the maximum output range of ±10 V. On-line or off-line (disconnected) operation is program controlled. Each analog output is controlled directly by a single 16-bit word in the VMEbus short I/O space.

FUNCTIONAL CHARACTERISTICS

Sequence Initiation: Scanning can be programmed to commence either upon direct command from the host, or by an external TTL trigger event. Scan rate for the analog inputs is program controlled.

The external trigger line also can be used to synchronize multiple VMIVME-3115 boards for simultaneous sampling of large arrays of analog signals. For multiboard sychronization, a specific VMIVME-3115 board is designated the synchronous master, while the remaining boards are designated as slaves. The master then controls the sequencing of all slave boards.

Digital I/O Ports: 16-bit parallel digital input and output capability is provided by dual 8-bit TTL data ports. Each port can be program configured as either an input or output port, and is accessible in the short I/O space in which the Control Registers for the board are located.

I/O Addressing: Addressable as 16 contiguous 16-bit registers, located on any 16-word boundary within the short supervisory or short nonprivileged I/O space.

Memory Addressing: The Analog-to-Digital Converter (ADC) buffer appears as conventional memory to the VME host. Total memory space occupied by the board is 256 Kbytes, and can be program located on any 4 0000 byte (HEX) boundary in the VMEbus memory space. The VMIVME-3115 buffers can be removed (masked) from VMEbus memory by a CSR control bit.

I/O Address Selection: Board address in the short I/O space is selected by on-board field selectable jumpers. Operation is supported in any slot except slot 1.

Access Privilege: Address modifiers are decoded to support either supervisory, nonprivileged, or both accesses. Jumpers are provided to support this feature, and are factory configured for either access. Decoded modifier codes include 09, 0A, 0B, 0D, 0E, 0F, 2D, 29, 39, 3A, 3B, 3D, 3E, and 3F.

VMEbus Interrupt: The VMIVME-3115 can be programmed to generate an IRQ1 to IRQ7 when either buffer is full. The interrupt response vector is controlled by an on-board Interrupt Vector Register.

Board Identification: The Board Identification Register (BIR) contains the VMIVME-3115 identification code.

Transparent Operation: The following default conditions are established at RESET:

Independent continuous operation
Maximum block size (256 Kbytes)
15.625 kHz scan rate
Analog outputs off
Digital ports as inputs

VMEbus Compliance: Complies with the VMEbus Specification Rev. C.1
A32/A24/A16:D16/D08 (EO) DTB Slave:BLT
D16 Slave
Interrupter I(1) to I(7) ROAK (DYN)
Interrupt Vector: D08 (O) (DYN)
6U form factor

Interrupt Event: Either buffer full

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ELECTRICAL SPECIFICATIONS AT 25 °C

Analog Inputs:

Number of Input Channels: Four differential channels; jumper-selectable

Converter Channels: Two

Sample-and-Hold Amplifiers: Eight (two per input channel)

Resolution: 12 bits

Voltage Ranges: 0 to +5 V, ±5 V (options X-0-X and X-2-X), or 0 to +10 V, ± 10 V (options X-1-X and X-3-X)

Input Sampling: Simultaneous sampling of all analog inputs

Interchannel Phase Skew: Less than 0.1° at 20 kHz

Scan Rate(1): Program controlled from 15.625 kCPS to 2 MCPS. See the Ordering Information.

Acquisition Time: Same as conversion cycle. See Note 2.

Conversion Cycle (Settling Plus Conversion): 1 µsec x 2,000,000/SCAN RATE. See Note 3.

Data Coding: Two's complement, binary or offset binary

Gain Error: ±0.05 percent maximum

Input Offset: ±5 mV maximum

Input Impedance: 4 kΩ, differential; 8 kΩ with 10 V input options

Input Protection: ±25 V; ±40 V with 10 V input options

Maximum Sampling Rate: 1.0 MCPS (2 channels) or 0.5 MCPS (4 channels), jumper-selectable

Common-Mode Rejection: 72 dB at 1 kHz; differential mode

Common-Mode Range: ±10 V (options X-0-X and X-2-X)
± 20 V (options X-1-X and X-3-X)

Crosstalk Rejection: 72 dB at 1 kHz

Analog Outputs:

Number of Output Channels: Two independent analog outputs

Resolution: 12 bits

Monotonicity: 12 bits, over operating temperature range

Output Modes: On-line (outputs connected to I/O connector) or off-line (outputs disconnected from I/O connector)

Voltage Ranges: 0 to +10 V, ±5 V, ±10 V, jumper-selectable

Output Impedance: Less than 0.5 Ω

Data Coding: Two's complement, binary, or offset binary

Settling Time: 25 µs maximum, to 0.02 percent

Linearity Error: ±0.03 percent maximum

Output Offset: ±5 mV maximum

Load Current: ±10 mA maximum, over full output range of ±10 V

Load Capacitance: 5,000 pFd, no oscillation

Output Protection: Continuous short to ground; ±25 V for one second

Off-line Output Leakage: 50 nA maximum

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1. MCPS = Million Channels per Second; kCPS = /Thousand Channels per Second
2. Each input is "pipelined" with two Sample-and-Hold amplifiers. Sample acquisition occurs while the previously acquired sample is digitized.
3. An effective conversion cycle of 500 ns (2 MCPS) is obtained by digitizing two channels simultaneously.

BUFFER MEMORIES

Buffer Size (Each of 2 Buffers): 4 bytes to 256 Kbytes, 8 ratios of 4:1; program controlled

VMEbus Access: D8 or D16 random access; D16 block mode (BLT)

VMEbus Access Location: Jumper-locatable on any 4 0000 byte (HEX) boundary from 0000 0000 to FF FC 0000 (HEX)

Control: Disabled at power up and during reset operations. Enabled or disabled through the short I/O space CSR.

Mean Access Time (From Data Strobe):*
Block Mode: 460 ns at 2 MCPS; 320 ns at or below 500 kCPS

Operating Modes: Continuous or single block

Synchronization:
Independent: Continuous or synchronized single block
Multiboard: Synchronized continuous or synchronous single block

DIGITAL I/O PORTS

Organization: Dual 8-bit bi-directional ports

Logic Levels: Standard TTL levels with no inversions

VMEbus Access: Single 16-bit register in short I/O space, D8 or D16 access

Control: Each port is program selected as either an input port or an output port

Access time is defined as the time between DSX active (low state) to DTACK* active (low state).

PHYSICAL/ENVIRONMENTAL

Ambient Temperature: 0 to +55 °C, operating -40 to +85 °C, storage

Relative Humidity: 10 to 80 percent, noncondensing

Altitude: Operation to 10,000 ft

Dimensions: Standard VME double height board, 160 x 233.35 mm

VME Connectors: Extended ground pins on P1 and P2

Input/Output Connectors (P3, P4, P5, J1 to J4): Refer to the Ordering Information

Electrical Power: +5.0 VDC +0.25/-0.125 VDC at 5.7 A (typical), 7.1 A (maximum)

APPLICATIONS —

Voltage Measurement and Stimulus
High-Speed Data Acquisition
Industrial Instrumentation
Digital Signal Processing
Development and Research
Closed Loop Control Systems
Digital Input and Output
Phase Coherent Analog Sampling
Trainers and Simulators

REFERENCE MATERIAL LIST — For a detailed explanation of the VMEbus and its characteristics, the publication “The VMEbus Specification” is available from:

VITA
VMEbus International Trade Association
7825 East Gelding Drive
Suite No. 104
Scottsdale, AZ 85260-3415
Phone: (602) 951-8866
Fax: (602) 951-0720
Internet: www.vita.com

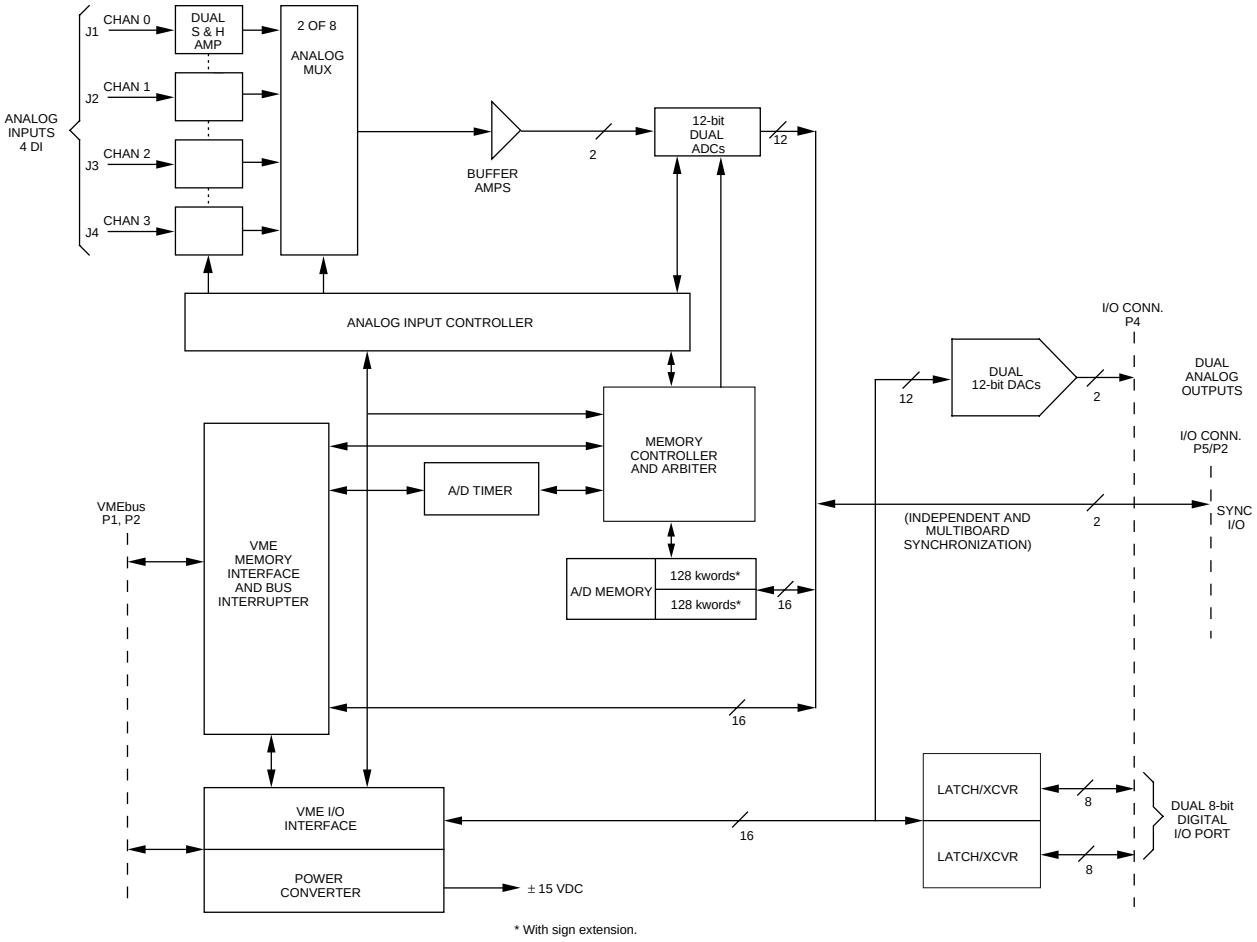


Figure 1. VMIVME-3115 High Throughput Analog I/O Board Block Diagram (2 MHz Sample Rate with 4-Channel Simultaneous Sample-and-Hold Analog Inputs)

APPLICATION AND CONFIGURATION GUIDES — The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products.

Title	Document No.
Digital Input Board Application Guide	825-000000-000
Change-of-State Board Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006
Data Acquisition Noise Reduction Application Guide	825-000000-026

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