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VMIVME-3118
SCANNING 16-bit ANALOG-TO-DIGITAL CONVERTER BOARD WITH PROGRAMMABLE GAIN

INSTRUCTION MANUAL

DOCUMENT NO. 500-003118-000 E

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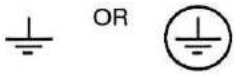
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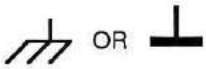
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Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

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The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

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TABLE OF CONTENTS

Page

SECTION 1. GENERAL DESCRIPTION

1.1 INTRODUCTION 1-1
1.2 FUNCTIONAL DESCRIPTION 1-3
1.3 REFERENCE MATERIAL LIST 1-5

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

SECTION 3. PRINCIPLES OF OPERATION

3.1 INTRODUCTION 3-1
3.2 INTERNAL FUNCTIONAL ORGANIZATION 3-1
3.3 CONTROL INTERFACE 3-2
3.3.1 Board Selection 3-2
3.3.2 Read/Write Operations 3-2
3.3.3 Bus Interrupter 3-2
3.3.4 Interval Timer and Channel Counter 3-4
3.4 DATA BUFFER MEMORY 3-4
3.4.1 Organization and Control 3-4
3.4.2 Data Storage and Retrieval 3-4
3.5 OPERATING MODES 3-5
3.6 ANALOG INPUT MULTIPLEXING, SAMPLING, AND DIGITIZING 3-6
3.6.1 Input Configuration 3-6
3.6.2 Gain Control 3-6
3.6.3 Sampling and Digitizing 3-8
3.6.4 Analog-to-Digital Conversion 3-8
3.7 POWER CONVERTER 3-8

SECTION 4. PROGRAMMING

4.1 INTRODUCTION TO CONTROLLING THE VMIVME-3118 BOARD 4-1
4.2 GENERAL CONTROL FEATURES 4-1

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TABLE OF CONTENTS (Continued)

Page

SECTION 4. PROGRAMMING (Concluded)

4.2.1 Addressing Modes and Board Location....4-1
4.2.2 Data Transfers....4-1
4.2.3 Reset Operations and Initialization....4-2
4.2.4 Conventions....4-2
4.3 CONTROL REGISTERS....4-2
4.3.1 Board Identification Register (BID)....4-3
4.3.2 Control and Status Register (CSR)....4-3
4.3.3 Buffer Control Register (BCR)....4-5
4.3.4 Interrupter Registers....4-5
4.3.5 Timer/Counter Registers....4-5
4.3.6 Converter Data Register (CDR)....4-5
4.4 DATA ORGANIZATION AND CONTROL....4-5
4.4.1 Data Word....4-5
4.4.2 Scaling and Coding....4-5
4.4.3 Data Block....4-5
4.4.4 Data Buffer/RAM....4-8
4.4.5 Gain Selection....4-8
4.4.6 Gain Initialization Preload....4-8
4.5 OPERATING MODES....4-8
4.5.1 Continuous Scanning....4-8
4.5.2 Single Channel Random Access....4-10
4.5.3 Timed Burst....4-10
4.5.4 Locally Triggered Burst....4-10
4.5.5 Remotely Triggered Burst....4-10
4.5.6 Synchronizing Multiple VMIVME-3118 Boards....4-10
4.5.7 Gain Loading....4-10
4.6 SCAN MONITORING....4-11
4.6.1 Data Ready Flag and Interrupt....4-11
4.6.2 Data Counter and Interrupt....4-11
4.7 BUS INTERRUPTER....4-11
4.7.1 Interrupt Control Register....4-11
4.7.2 Interrupt Vector Register....4-12
4.8 TIMER/COUNTER CONTROL....4-12
4.8.1 General Characteristics....4-12
4.8.2 Scan Interval Timer....4-14
4.8.3 Data Counter Control....4-16
4.9 TYPICAL PROGRAMMING EXAMPLES....4-16
4.9.1 Example C Header File....4-17
4.9.2 Example C Program....4-18

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TABLE OF CONTENTS (Continued)

Page

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 BEFORE APPLYING POWER: CHECKLIST 5-1
5.4 OPERATIONAL CONFIGURATION 5-2
5.4.1 Factory-Installed Jumpers 5-2
5.4.2 Access Modes 5-2
5.4.3 Board Location in Short I/O or Memory Space 5-6
5.4.4 Analog Input Gain 5-6
5.4.5 Converter Voltage Range 5-6
5.4.6 Input Voltage Range 5-6
5.4.7 External Triggering 5-6
5.4.8 Input Configurations 5-7
5.4.9 Internal Ground Connections 5-7
5.5 CALIBRATION 5-7
5.5.1 Equipment Required 5-7
5.5.2 Calibration Procedure 5-10
5.5.3 Functional Verification 5-11
5.6 CONNECTOR DESCRIPTIONS 5-12
5.6.1 Connector Functions 5-12
5.6.2 Input Modes 5-12
5.6.3 Input Cables 5-14
5.6.4 External Synchronization 5-14
5.7 SYSTEM CONSIDERATIONS 5-14
5.7.1 Applications with Signal Conditioning Boards 5-14
5.7.2 Operation with Direct Analog Inputs 5-14

SECTION 6. MAINTENANCE

6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1

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TABLE OF CONTENTS (Concluded)

LIST OF FIGURES

Figure		Page
1.1-1	Photograph of the VMIVME-3118 Analog Input Board	1-2
1.2-1	VMIVME-3118 Functional Block Diagram	1-4
3.3.1-1	VMEbus Interface Logic	3-3
3.6.1-1	Analog Multiplexers and PGA	3-7
3.6.3-1	Pipelined A/D Conversion	3-9
4.8.2-1	VMIVME-3118 Timer Functional Block Diagram	4-14
5.4-1	VMIVME-3118 Jumper Locations	5-3
5.5-1	Locations of Test Points and Adjustments	5-9
5.6.1-1	P1 to P4 Connector Pin Configuration	5-15

LIST OF TABLES

Table		Page
4.3-1	VMIVME-3118 Board Register Map	4-3
4.3.2-1	Control and Status Register (CSR) Functions	4-4
4.3.3-1	Buffer Control Register (BCR)	4-6
4.4.2-1	ADC Data Format and Coding	4-7
4.5-1	Operating Mode Selection	4-9
4.7-1	Interrupt Registers Organization	4-12
4.7.1-1	Interrupt Control Register Functions	4-13
4.8.1-1	Timer/Counter Data Transfer Sequences	4-15
5.4-1	Programmable Jumper Functions	5-4
5.4-2	Typical Jumper Configurations	5-5
5.4.8-1	Input Configuration Selection	5-8
5.5.3-1	Input/Output Connector Pin Assignments	5-13

APPENDIX

A Assembly Drawing, Parts List, and Schematics

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TABLE OF CONTENTS (Concluded)

LIST OF TABLES

Table		Page
4.3-1	VMIVME-3118 Board Register Map	4-3
4.3.2-1	Control and Status Register (CSR) Functions	4-4
4.3.3-1	Buffer Control Register (BCR)	4-6
4.4.2-1	ADC Data Format and Coding	4-7
4.5-1	Operating Mode Selection	4-9
4.7-1	Interrupt Registers Organization	4-12
4.7.1-1	Interrupt Control Register Functions	4-13
4.8.1-1	Timer/Counter Data Transfer Sequences	4-15
5.4-1	Programmable Jumper Functions	5-4
5.4-2	Typical Jumper Configurations	5-5
5.4.8-1	Input Configuration Selection	5-8
5.5.3-1	Input/Output Connector Pin Assignments	5-13

APPENDIX

A Assembly Drawing, Parts List, and Schematics

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SECTION 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The VMIVME-3118 Board (Figure 1.1-1) is a member of VMIC's extensive family of analog input/output products for the VMEbus. With 16-bit digitizing resolution, program controlled gain, and automatic scanning of 64 differential or single-ended analog inputs, the VMIVME-3118 Board provides exceptional dynamic range and analog input channel density. Various operating modes are supported, including continuous scanning, data bursts, external synchronization, and single channel operation. This board is designed to interface directly with VMIC's line of signal conditioning boards for digitizing the outputs from thermocouples, RTDs, and strain gages.

Individual channel gains are downloaded for selection in real-time during scanning operations, or the board can be configured with a fixed gain that is common to all channels. Multiple boards can be synchronized together to enable as many as 16 boards to initiate each scan simultaneously. An interval timer, bus interrupter, channel counter, and midscan/endscan flag simplify the monitoring of data within the dual port data buffer.

The broad range of system applications that can benefit from the VMIVME-3118 capabilities include factory automation, process control, data acquisition systems, training simulators, and laboratory instrumentation. The following brief overview of principal features illustrates the flexibility and performance that is available with the VMIVME-3118 Board:

a. 64 differential or single-ended analog inputs
b. 16-bit A/D conversion
c. 52 kHz scanning rate
d. Program-selectable gains of x1, x10, or x100
e. A/D converter ranges of ±2.5 V, ±5 V, ±10 V, 0 to +5 V, 0 to +10 V
f. Real-time automatic selection of individual channel gains
g. 16- to 1,024-word dual port data buffer
h. Operation in short I/O (A16) or standard (A24) data space
i. Program controlled channel block size and buffer size
j. Optional low pass input filters
k. Continuous, burst, and single channel operating modes
l. Free running operation or external/internal triggering
m. Bus interrupter for midscan or endscan indication
n. Program controlled interval timer for timed data bursts
o. Direct cabling from VMIC signal conditioning boards
p. Initializes after a reset in autoscan mode with gain = x1

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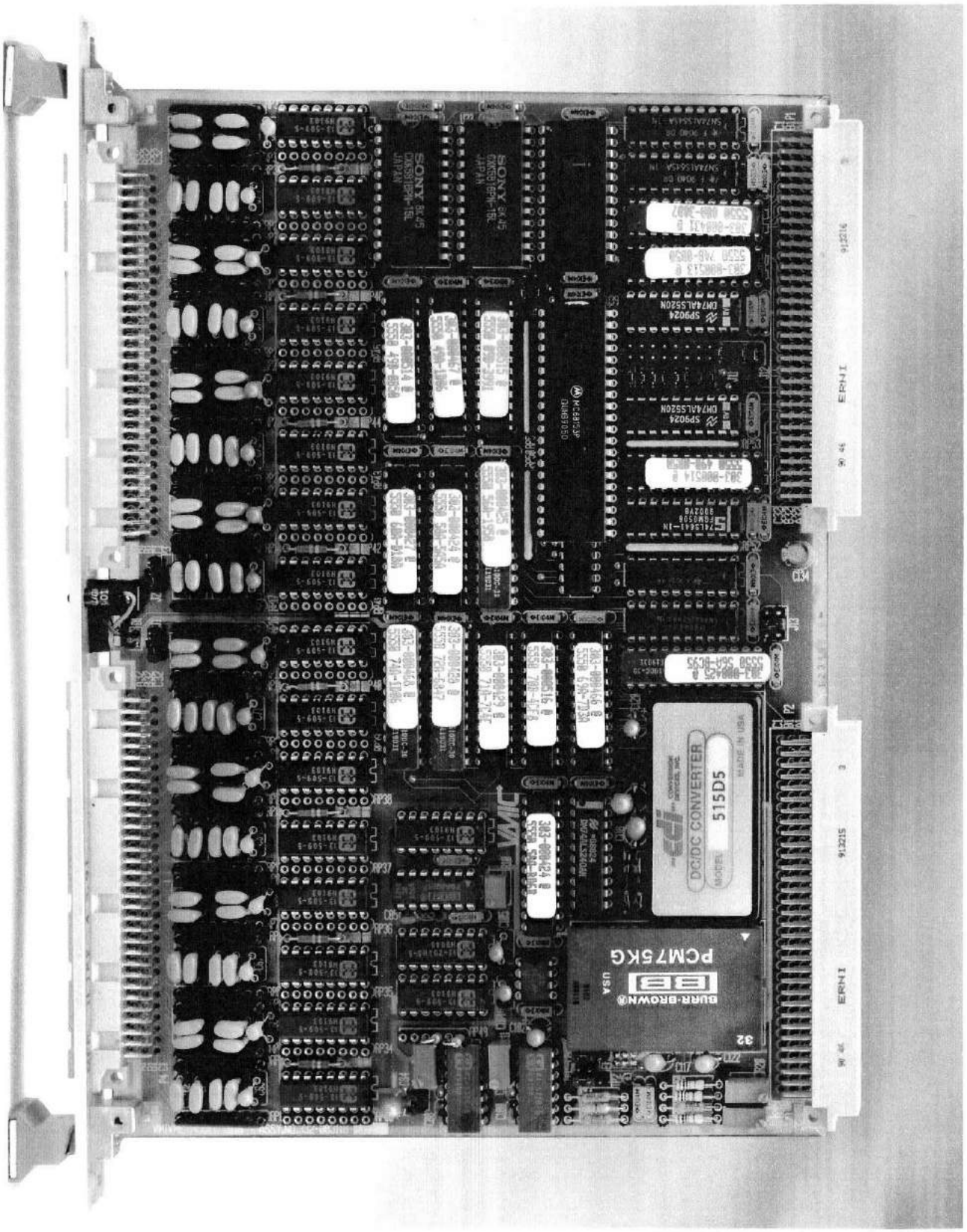


Figure 1.1-1. Photograph of the VMIVME-3118 Analog Input Board

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1.2 FUNCTIONAL DESCRIPTION

The VMIVME-3118 (Figure 1.2-1) is a high-resolution, 16-bit, 64-channel analog scanning and digitizing input board for VMEbus system applications. Dual ported data memory, on-board timers, automatically controlled gain, and a program controlled bus interrupter enable the VMIVME-3118 Board to support extensive analog input traffic, with minimum involvement of the host processor.

Analog inputs are scanned and digitized sequentially in blocks of 16 to 64 channels, and the digital values are stored in a dual port data buffer which can be accessed at any time from the VMEbus. The gain of each channel can be program controlled individually in real-time from an on-board gain buffer, or can be jumper-configured for a fixed gain that is common to all channels. Channel gain is software or jumper-selectable as x1, x10, or x100. A/D converter voltage ranges are jumper-selectable from ±2.5 V, ±5 V, ±10 V, 0 to 5 V, 0 to 10 V.

When a system or program reset occurs, the board initializes in the 64-channel continuous scanning mode, and if automatic gain control has been selected, all channel gains are initialized to unity (x1). After a reset operation, the program can select the timed burst, triggered burst or random access single channel modes, and can modify the block size, buffer size, and channel gains as necessary. The channel block is adjustable as 16, 32, 48 or 64 channels, and the data buffer size can be selected from 16 to 1,024 data words in six equal ratios of 2:1.

Timed data bursts are controlled by an interval timer which can provide repetitive or single-shot burst intervals of up to 536 s. A burst can consist of from 16- to 1,024-channel samples. A data ready flag is available at the middle or end of a scan, and an interrupt request can be generated simultaneously with the flag. The interrupt can also be initiated after a specific number of samples have been acquired.

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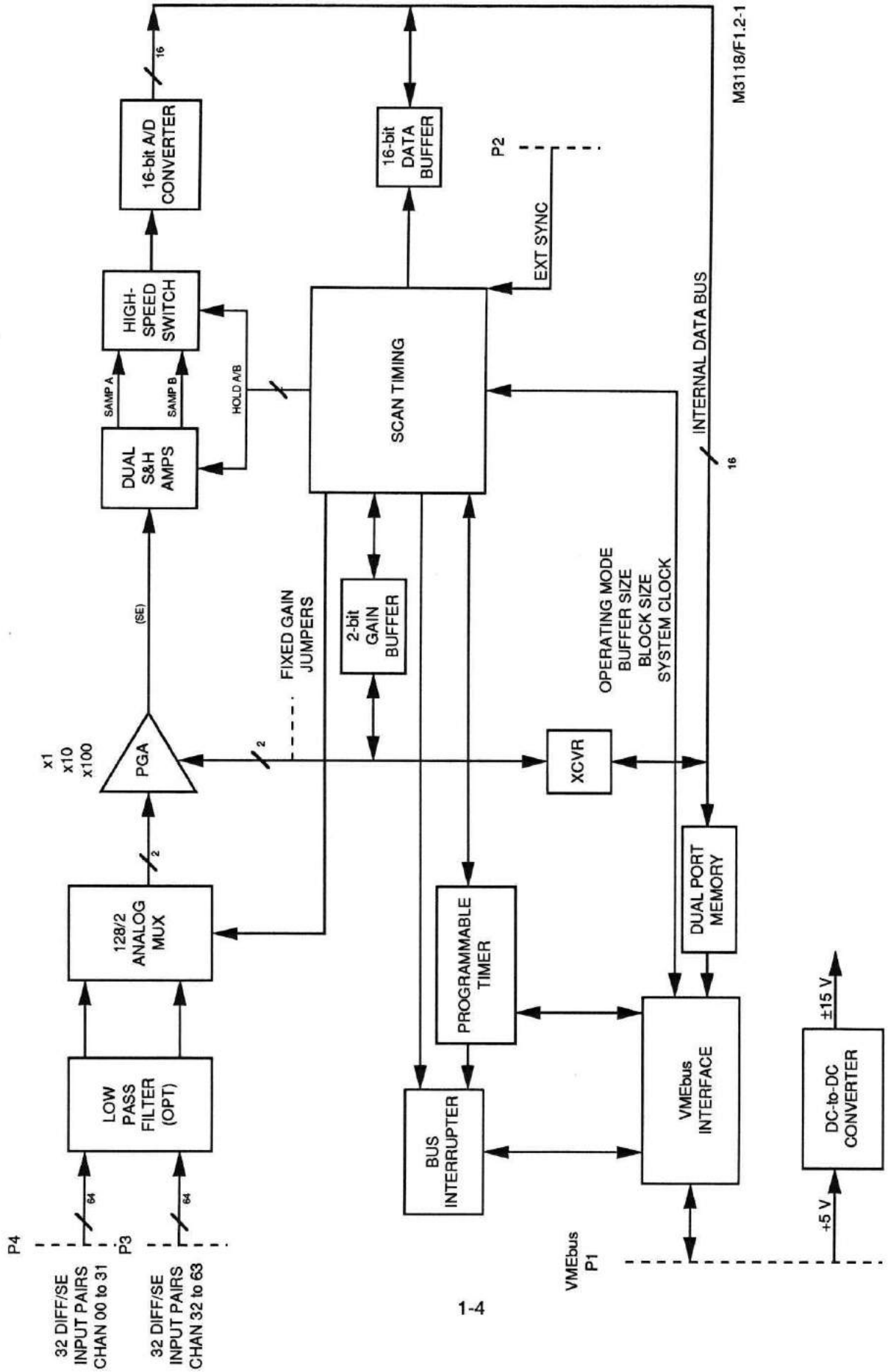


Figure 1.2-1. VMIVME-3118 Functional Block Diagram

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1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-in-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-in-Test) Configuration Guide	825-000000-005
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SECTION 2
PHYSICAL DESCRIPTION AND SPECIFICATIONS

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SECTION 3

PRINCIPLES OF OPERATION

3.1 INTRODUCTION

This section describes the internal organization of the VMIVME-3118 Board, and reviews the general principles of operation. Section 3.2 summarizes the major board functions, and the remainder of Section 3 addresses each function individually. The information in this section is supplemented by programming details in Section 4 and by the schematic diagrams in Appendix A.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-3118 Board contains the following principal hardware functions, as shown in Figure 1.2-1 of Section 1:

a. Analog input multiplexing and digitizing
b. VMEbus interface
c. Scan timing and control
d. Data and gain buffers
e. Interval timer and channel counter
f. Bus interrupter
g. Power converter

An analog multiplexer, a programmable amplifier, and a 16-bit A/D converter digitize the analog input channels, and the digitized values are stored in a dual ported data buffer for access from the VMEbus. ***Low pass input filters*** minimize the effects of system noise and eliminate high frequency signal components which would otherwise cause aliasing problems. Dual ***sample-and-hold amplifiers*** pipeline alternate odd and even channels, to obtain maximum throughput by acquiring each channel while the preceding channel is digitized. The conversion rate is constant at 19 µs for all operating modes except the single scan random access mode (Section 3.5). Operating modes are described in detail in Section 4.5. Regulated ±15 VDC power for the analog networks is obtained from the 5 VDC bus through a DC-to-DC converter.

A separate ***gain buffer*** permits the input gain of each channel to be assigned individually. Gain codes ($0 = x1, $1 = x10, $2 = x100) are first loaded into the gain buffer from the bus, and the gain for each channel is then used during the scanning process. Programmable ***fixed gain jumpers*** provide a fixed gain for all channels if software programmable gain is not required.

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Control signals and data transfers take place through the VMEbus P1 connector. ***VMEbus interface logic*** controls data transfers through the P1 interface, and latches the operating mode parameters. Status monitoring and sequence timing are supported by a ***bus interrupter*** and ***programmable timer***, both of which are controlled from the bus. Scan timing logic controls the analog input scanning process, uses the gain buffer to adjust input gain, and routes digitized channel data to the data buffer.

3.3 CONTROL INTERFACE

3.3.1 Board Selection

VMEbus data transfer requests are accepted when the **board-selection comparator** detects a match between the on-board selection jumpers shown in Figure 3.3.1-1, and the address and address modifier lines from the backplane. When a match is detected, the board responds with a data transfer, after which the open collector DTACK interface signal is asserted (LOW). DTACK returns to the negated (HIGH) state when the transfer has been completed. During an interrupt response, DTACK is provided by the interrupt controller.

3.3.2 Read/Write Operations

Data Bus lines D00 through D15 are bi-directional and move data to or from the board through a 16-bit ***data transceiver*** in response to control signals from ***interface timing and control logic***. The data transceiver isolates the VMEbus data lines from the ***internal data bus***. Address lines **A12** through **A23** map the board into either the short I/O A16 space or the standard A24 space. Data transfer control signals from the VMEbus determine whether data is moved to the board (Write) or from the board (Read). Both D8 (EO) and D16 transfers are supported.

The Control and Status Register (***CSR***) establishes the operational mode of the board and selects the input channel during random access A/D conversions. The Buffer Control Register (***BCR***) controls the size of the data buffer and the number (block) of channels being scanned.

3.3.3 Bus Interrupter

Access to the VMEbus interrupt structure is provided through a ***bus interrupter***. If the interrupt is enabled, an interrupt is generated in response to a request either by the scan timing logic as a data ready flag, or by the channel counter after a specific number of buffer locations have been updated. The interrupt function is implemented with a Motorola MC68153 Bus Interrupter Module (BIM). Details of the interrupter capabilities are described in Section 4.

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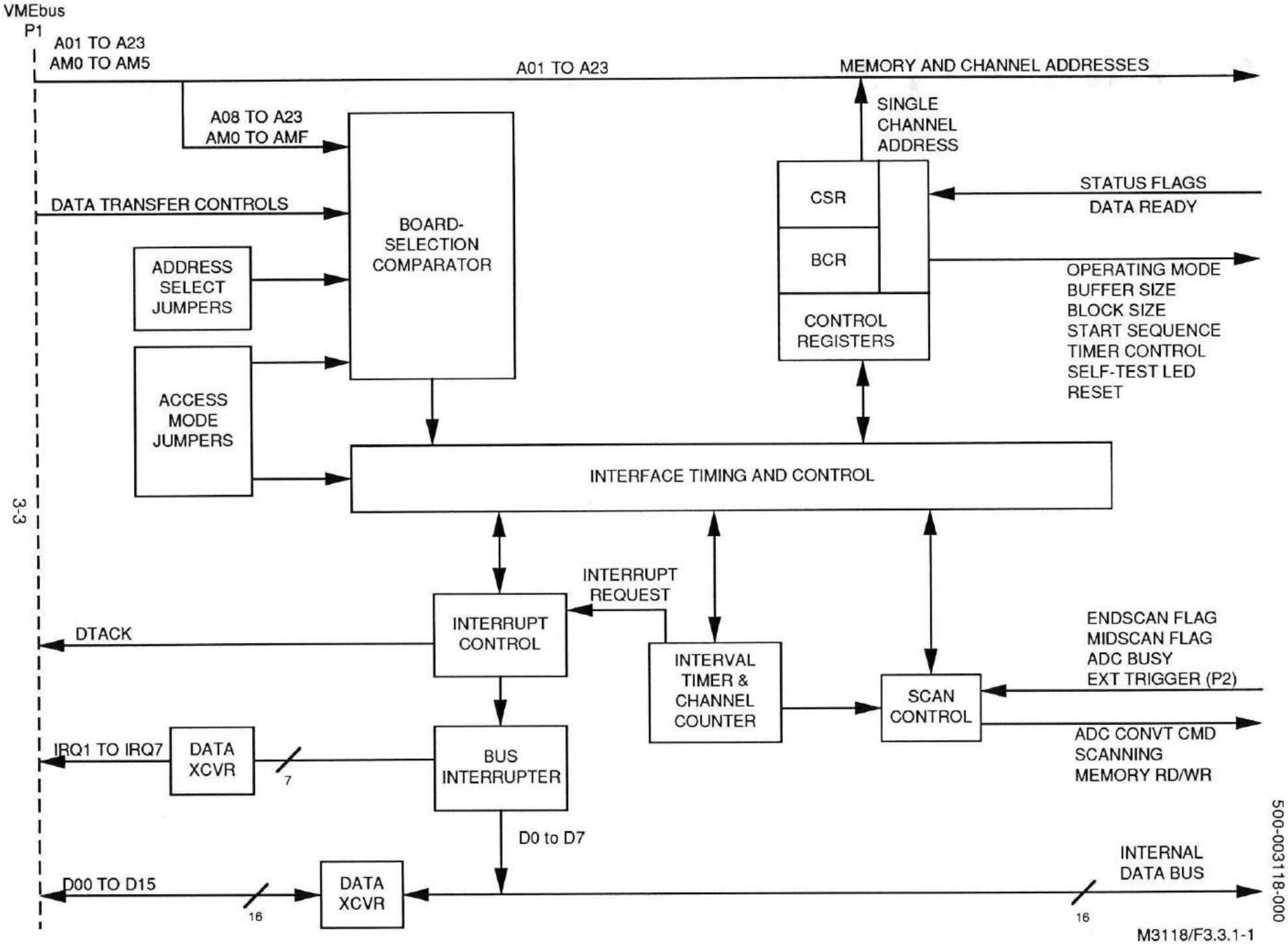


Figure 3.3.1-1. VMEbus Interface Logic

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3.3.4 Interval Timer and Channel Counter

A triple 16-bit counter device contains the ***interval timer*** and ***channel counter***. Two of the counter sections are driven from an 8 MHz clock, and can be cascaded as a 32-bit timer for delays up to 536 sec. Timed data acquisition bursts (Sections 3.6 and 4.5) occur periodically at the interval programmed into the interval timer. The channel counter can be programmed to generate an interrupt after a programmed number of data buffer locations have been updated, or can be read directly to serve as a data pointer.

3.4 DATA BUFFER MEMORY

3.4.1 Organization and Control

Digitized inputs are stored in a 16-bit ***data buffer***, the size of which can be software configured from 16 data words to 1,024 data words. Data in the buffer is organized into consecutive ***channel blocks***, each of which represents a complete scan of all active channels. Both buffer size and block size are controlled by the ***BCR***. The input channels are sampled consecutively, starting with Channel 00 located at the bottom (lowest address) of each block in the buffer, and proceeding through the highest channel at the top of the block.

Total data memory buffer size is 2,048 words. The remaining memory that is not used for storage of scanning input data may be used as on-board scratch pad memory.

3.4.2 Data Storage and Retrieval

The data buffer can be loaded or read from the bus at any time. ***Arbitration*** for the buffer occurs at the beginning of an update from the A/D converter. If the converter has control of the memory when a bus transfer is initiated, the transfer will be extended by approximately 250 nsec while the buffer update is completed.

If a bus transfer is in progress when a converter access is requested, the bus transfer will proceed normally and the converter access will take place after the transfer has been completed. Because the converter access must be completed before the scanning sequence can continue, a long data transfer (greater than 600 nsec) may extend the 19 µsec channel update period.

A ***data ready flag*** is set at the top, or highest address, of the buffer, and can be programmed to occur also at the middle of the buffer. The data ready flag can initiate an interrupt request, or can be read from the bus as a status flag.

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3.5 OPERATING MODES

All operating modes available with the VMIVME-3118 are controlled through the CSR and BCR. Operating modes are described in detail in Section 4, and are summarized here as:

a. Continuous scanning
b. Single scan random access
c. Timed burst
d. Locally triggered burst
e. Remotely triggered burst
f. Gain loading

Continuous scanning is selected by clearing both mode control bits in the CSR (Section 4.3), and is the default selection after a reset operation. All active channels are scanned continuously in this mode. A single channel can be selected at random for conversion in the ***single channel random access mode***. The resulting digitized value is read from a dedicated Converter Data Register (CDR).

Three operating modes acquire data in bursts, with each burst representing an entire update of the data buffer. ***Timed burst*** data is acquired in a single data scan, or burst, of all buffer locations when the interval timer times out. A single burst can be acquired at the end of the programmed interval, or the process can be repetitive. In the repetitive mode, a burst is acquired at the end of each interval until either a different mode is selected, or the interval timer is disabled by clearing CSR bit D09. Timer control is described in Section 4.8.

Two "triggered burst" modes generate a single burst each time a trigger occurs. In the ***locally triggered burst*** mode, the trigger occurs when the "start sequence" control bit in the CSR is set (Section 4.3). In the ***remotely triggered burst*** mode, the trigger occurs at the falling edge of the EXT STRT L digital input at the P2 connector.

Remotely triggered burst capability permits multiple boards to be synchronized. All boards will begin each scan simultaneously together. Multiboard synchronization is obtained by connecting the TRIG OUT L output from P2 of a synchronizing "master" to the EXT STRT L input of all slave boards. As many as 16 boards in a single chassis can be synchronized together.

If automatic selection of channel gain (autogain) is required, the gain code for each channel is loaded into the gain buffer while operating in the ***gain loading*** mode (see Section 3.2 for more information).

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3.6 ANALOG INPUT MULTIPLEXING, SAMPLING, AND DIGITIZING

3.6.1 Input Configuration

Analog inputs from connectors P3 and P4 are routed through low pass ***input filters*** to the input multiplexers shown in Figure 3.6.1-1. Channels 00 to 31 are connected through P4 and Channels 32 to 63 are connected through P3.

To provide at least one ground in each of the input connectors, the LOW inputs for Channels 31 and 63 can be jumpered individually to either AGND or COMM, or can be left ungrounded (Sections 5.4 and 5.6). AGND is the internal analog ground, and COMM is a bus which connects all center row (B row) pins together on P3 and P4. The COMM bus provides a return connection for all channels if 96-wire cables are used for the analog inputs.

The ***analog multiplexers*** route one of each group of eight channels to the PGA multiplexers, which in turn selects an input to route to the PGA. Input address lines A0, A1, and A2 control the input multiplexer, and A3, A4, and A5 select the PGA multiplexer input.

Crosstalk and common mode errors are minimized by discharging the multiplexer node between input channel selections. As each channel is selected, any residual charge left on the node capacitance, ***Cn***, from the preceding channel would produce a small error voltage across the input filter capacitor. The ***multiplexer discharge switch*** is closed for approximately 1.5 µs between channel selections, and removes the residual charge before a new channel is selected.

At high scanning rates, the node capacitance appears as a pure resistance to the analog inputs, and the resistance is inversely proportional to the scan repetition rate. When operating in the **continuous scan** mode with a 64-channel block size, node capacitance in the VMIVME-3118 produces an effective input resistance of approximately 15 mΩ.

3.6.2 Gain Control

The Programmable Gain Amplifier (***PGA***) applies a gain of x1, x10, or x100 to the differential channel from the PGA multiplexer, and produces a single-ended output. PGA gain is selected by the GAIN A0 and A1 control lines which originate either from the gain buffer, or from fixed gain jumpers (Section 3.2).

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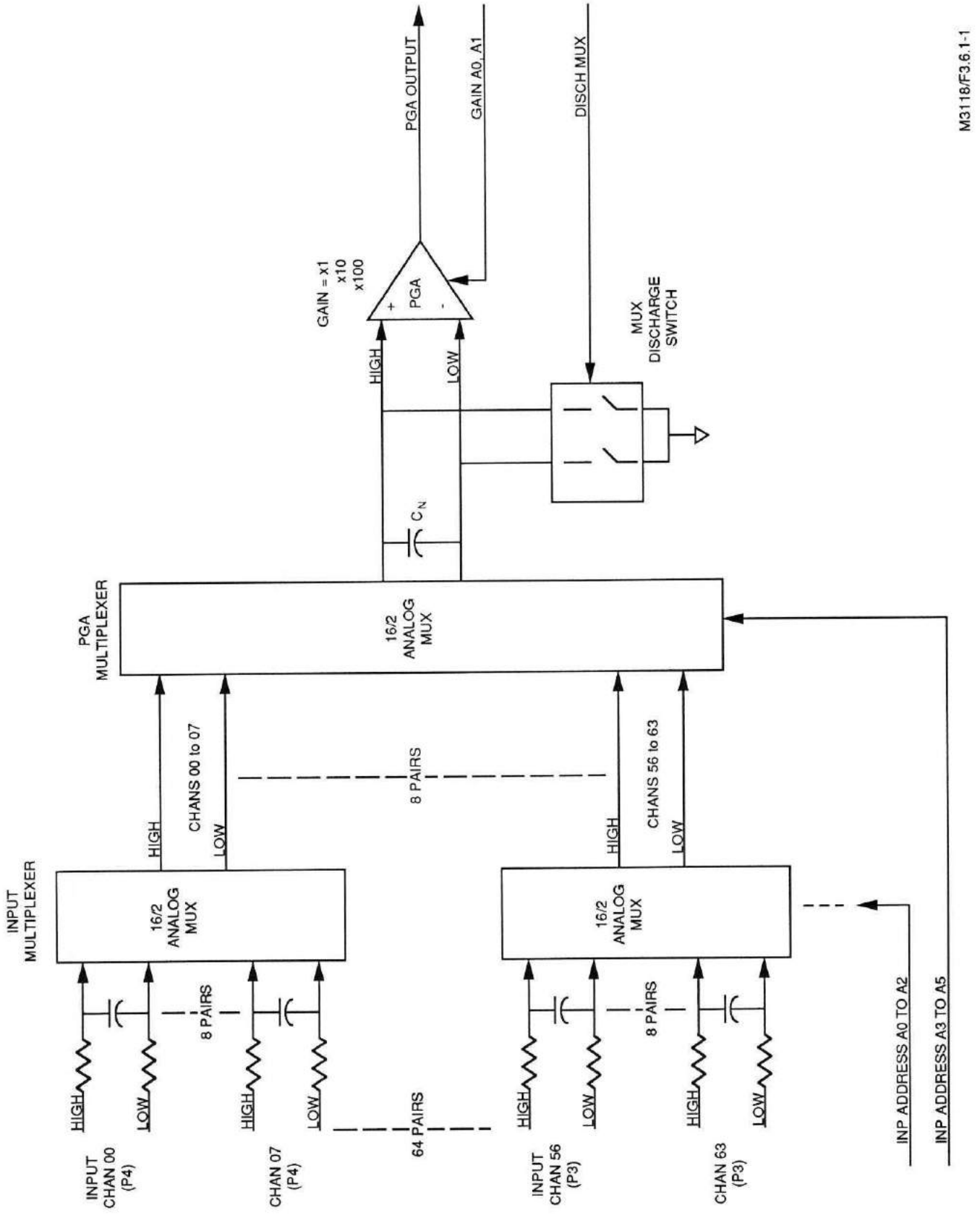


Figure 3.6.1-1. Analog Multiplexers and PGA

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3.6.3 Sampling and Digitizing

Dual ***sample-and-hold (S&H) amplifiers*** shown in Figure 3.6.3-1a provide the pipelined sampling that is required in order to use the maximum conversion rate available with the A/D converter. While one of the two amplifiers holds a sample for the converter, the other amplifier acquires the next channel to be converted. ***Analog switches*** select the output from the amplifier which is in the "hold" state, and a fast ***unity gain buffer*** provides the low source impedance required by the converter.

Figure 3.6.3-1b shows the VMIVME-3118 pipeline timing. The S&H amplifiers and the analog switches are controlled by the complementary ***Hold A*** and ***Hold B*** lines which alternate as each successive channel is digitized. A ***convert command*** is issued shortly after each transition of the Hold A/B lines. After the conversion is completed, a ***read ADC*** strobe stores the digitized value in the data buffer.

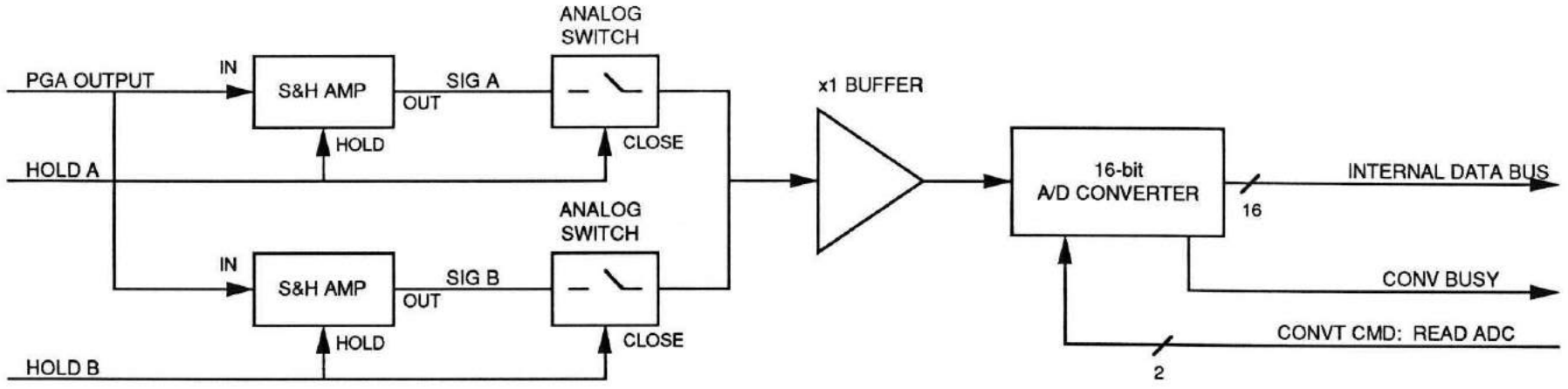
3.6.4 Analog-to-Digital Conversion

The output of the unity gain buffer is digitized by the 16-bit successive approximation ***A/D converter*** shown in Figure 3.6.3-1a. Each conversion is initiated by the convert command, and the ***Read ADC*** strobe writes the digitized value to the data buffer through the ***internal data bus***. Total conversion time is 17 µs. The additional 2 µs in each 19 µs conversion cycle is used for housekeeping operations such as starting and reading the converter.

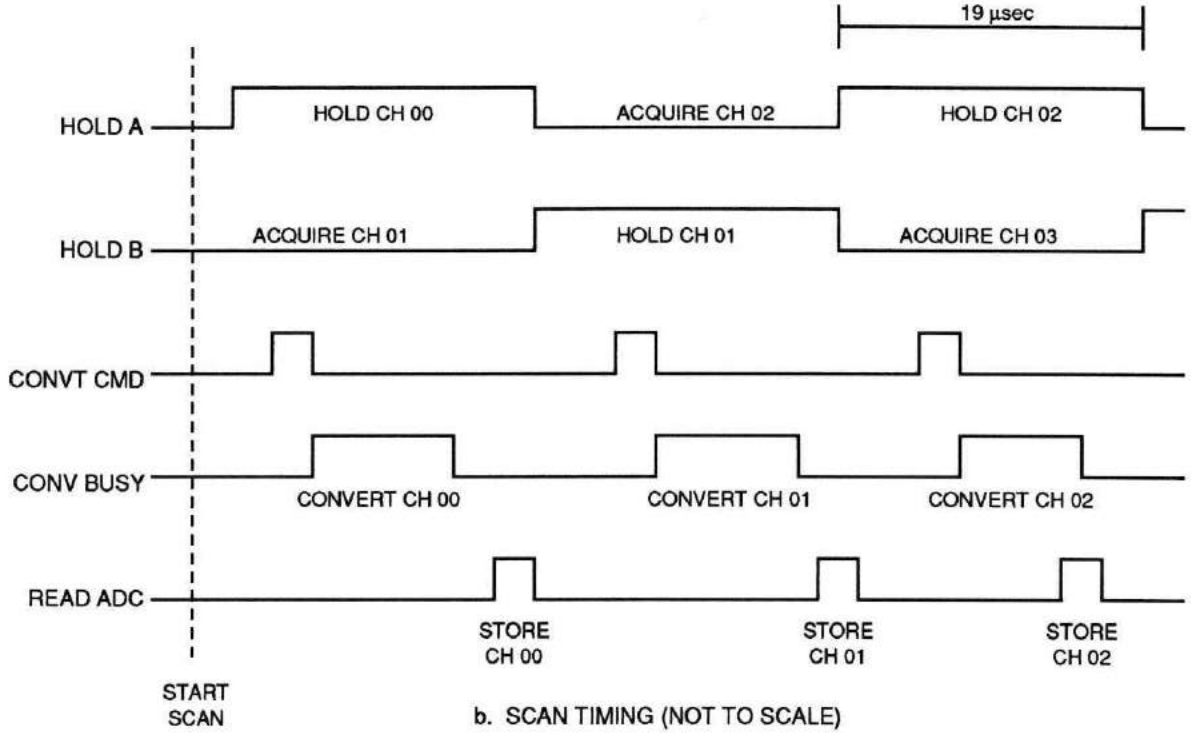
3.7 POWER CONVERTER

Electrical power for the analog networks is supplied by a single DC-to-DC converter which converts 5 VDC logic power from the VMEbus into isolated and regulated ±15 VDC. This method is used so that this product does not require the optional ±12 V on the VMEbus backplane.

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a. ANALOG SAMPLING AND DIGITIZING



b. SCAN TIMING (NOT TO SCALE)

M3118/F3.6.3-1

Figure 3.6.3-1. Pipelined A/D Conversion

500-003118-000

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SECTION 4

PROGRAMMING

4.1 INTRODUCTION TO CONTROLLING THE VMIVME-3118 BOARD

VMEbus communication takes place through Control, Status, and Data Registers which can be jumper-located in either the A16 short I/O space or the A24 standard address space. A resident bus interrupter is under program control and can be configured to generate any interrupt request from IRQ1 through IRQ7.

Digitized input data is accumulated in a dual port data buffer which consists of from 16 to 1,024 data words, where each data word contains the 16-bit digitized value of a single analog input channel. Data accumulates in the buffer in blocks of from 16 to 64 input channels. Buffer size and block size both are under program control, and the buffer can be read at any time without affecting the scanning sequence.

Data scaling is adjustable with jumper-controlled voltage ranges, and with either jumper-controlled or program-controlled channel gain. A Data Ready flag can be programmed to occur when the buffer is either filled or half-filled. An interrupt can be generated simultaneously with the Data Ready flag, or after a specific number of samples have been acquired.

The analog inputs can be scanned continuously or in triggered data bursts. Bursts (single scans) can be acquired automatically at intervals up to 536 sec, or can be triggered by an external event. Single channel random access is also supported.

References to programming jumpers are made throughout this section. Jumper installation requirements are described in Section 5.

4.2 GENERAL CONTROL FEATURES

4.2.1 Addressing Modes and Board Location

Programmable address jumpers permit the VMIVME-3118 Board to be located in either the short I/O (A16) space or the standard address (A24) space. The board can be located on any 4,096-word boundary. Board operation is jumper-configured in either program space or data space. Access privilege is jumper-designated as either short supervisory, short nonprivileged, or both.

4.2.2 Data Transfers

Registers at addresses $0000 to $0026 respond to both D8 and D16 data transfers, within the limitations described in Section 4.3. Data buffer locations can be *read* with either D8 (EO) or D16 transfers, but *should be written* with D16 transfers.

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Any register or buffer location can be accessed at any time without affecting the existing scanning sequence, although data transfers longer than 600 ns may extend conversion times.

4.2.3 Reset Operations and Initialization

All Control Registers are reset either by a system reset operation or by setting the software reset control bit D14 in the CSR. Either reset operation initializes the board to the following configurations:

a. Continuous scanning operating mode
b. 64-channel block size
c. 64 data word buffer size
d. Automatic gain set to x1
e. Offset binary data coding
f. Self-test LED ON
g. Data Ready flag at end-of-buffer
h. Interrupt disabled

The automatic gain codes for all channels will be initialized to "zero" (gain = x1) after a reset operation, as described in Section 4.4.6. If the automatic gain mode has been jumper-selected, channel gains other than x1 must be initialized as described in Section 4.5.7.

4.2.4 Conventions

a. Hexadecimal Notation: To be consistent with conventional VMEbus development system nomenclature, hexadecimal numbers throughout this document are indicated with the prefix "$" unless otherwise indicated, and are expressed in byte "$XX", word "$XXXX" or longword "$XXXX XXXX" formats. Decimal numbers are presented without a designating prefix.

b. Logic States: This document uses the convention that a data bit or control line is "SET" when it is in the "one", or HIGH state, and is "CLEARED" when "zero" or LOW.

4.3 CONTROL REGISTERS

Register designations and locations are summarized in Table 4.3-1.

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Table 4.3-1. VMIVME-3118 Board Register Map

REGISTER ADDRESS (HEX)	REGISTER DESIGNATION	DESIG	ACCESS	NOTES
$0000	BOARD IDENTIFICATION	BIR	R	2
$0002	CONTROL AND STATUS	CSR	R/W	
$0004	BUFFER CONTROL	BCR	R/W	3
$0006 to $000E	(RESERVED)			
$0010	INTERRUPT CONTROL	ICR	R/W	3
$0012 to $0016	(RESERVED)			
$0018	INTERRUPT VECTOR	IVR	R/W	3
$001A to $001E	(RESERVED)			
$0020	INTERVAL TIMER 0	TR0	R/W	3
$0022	INTERVAL TIMER 1	TR1	R/W	3
$0024	DATA COUNTER	DCR	R/W	3
$0026	TIMER/COUNTER CONTROL	TCR	R/W	3
$0028 to $007E	(RESERVED)			
$0080 to $087E	DATA BUFFER	BUFF	R/W	4,5
$0880 to $0FFE	SCRATCH PAD MEMORY	RAM	R/W	

M3118/T4.3-1

NOTES:
1. Unless indicated otherwise, all registers are 16-bit words.
2. D08 to D15.
3. D00 to D07.
4. Buffer location $0080 is replaced with the Gain Code Buffer Register when operating in the gain loading mode, or the Converter Data Register when operating in the random access mode.
5. See Section 4.4.4.

4.3.1 Board Identification Register (BID)

The Board Identification Register (BID) contains the board identification code ($24XX HEX) for the VMIVME-3118 Board, and occupies the upper eight data bits at board relative location $0000. This code can be used during system configuration to identify the board as a VMIVME-3118.

4.3.2 Control and Status Register (CSR)

CSR functions are summarized in Table 4.3.2-1. All control register bits are mapped directly to the Status Register. The CSR can be accessed with either D8 or D16 data transfers, and provides control and monitoring of the following board functions:

a. Random access channel selection
b. Operating mode
c. Scan sequence start
d. Timer and flag control
e. Data Ready flag
f. Data coding
g. Board reset
h. Self-test LED

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Table 4.3.2-1. Control and Status Register (CSR) Functions

MSB LSB

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

CONTROL and STATUS REGISTER (CSR) DATA FORMAT

CONTROL and STATUS BIT	NAME	FUNCTION
D00	INP A0 H	D0 to D5 select an input channel for random access.
D01	INP A1 H	
D02	INP A2 H	
D03	INP A3 H	
D04	INP A4 H	
D05	INP A5 H	
D06	MODE 0 H	D06 and D07 select the operating sequence mode as:
D07	MODE 1 H	

D07	D06	Operating Mode
0	0 *	Auto Scanning
0	1	Random Access to any channel for conversion
1	0	Single Scan of data buffer
1	1	Gain Loading of AUTOGAIN channel-gain codes

D08	START SEQUENCE H	RANDOM ACCESS or SINGLE SCAN operation initiates when D08 is SET. D08 has no effect if either D09 or D10 is SET. D08 is CLEARED automatically after sequence initiation.
D09	ENABLE INTERVAL TIMER H	The AUTOSCAN interval timer operates when D09 is SET, and is disabled when D09 is CLEARED. The selected operating sequence is initiated at the end of each interval. D09 has no effect if D10 is SET.
D10	ENABLE EXTERNAL START H	When D10 is SET, the selected operating sequence is initiated by the falling edge of the EXTERNAL START input at P2. D10 permits multiple VMIVME-3118 Boards to be synchronized together to a single external signal.
D11	ENABLE MIDSCAN FLAG H	D11 controls the occurrence of the DATA READY flag (D12) in the Single Scan and Auto Scan operating modes.
D12	DATA READY H (Status only)	D12 is SET according to: (a) the selected operating mode, (b) the ENABLE MIDSCAN FLAG (D11), and (c) the status of the scanning sequence. An interrupt can be programmed to occur when DATA READY is SET. D12 is CLEARED automatically by the first data register access.

OPERATING MODE	D11	D7	D6	CONDITION FOR SETTING DATA READY
Random Access	X	0	1	End-of-Conversion
Single or Auto Scan *	0	X	0	Data Buffer filled
Single or Auto Scan	1	X	0	Data Buffer half-filled
Gain Loading	X	1	1	DATA READY not active

D13	TWO'S COMPLEMENT H	Digitized input data is presented in offset binary format if D13 is CLEARED, or in two's complement format if D13 is SET.
D14	SOFTWARE RESET H	All board functions are reset when D14 is SET. D14 is cleared automatically when reset has been completed.
D15	SELF-TEST LED L	The "SELF-TEST" LED is OFF if D15 is SET, or is ON if D15 is CLEARED.

M3118/T4.3.2-1

* Default mode at RESET.

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4.3.3 Buffer Control Register (BCR)

Block size and data buffer size are controlled by the BCR, as shown in Table 4.3.3-1. The BCR also controls the size of the interval timer as either 16 or 32 bits, and determines whether an interrupt will be generated by the data ready flag or by the channel counter.

4.3.4 Interrupter Registers

The Interrupter Control and Vector Registers are used to establish the interrupt parameters, and to enable or disable the interrupt. The Interrupter Registers are described in Section 4.7.

4.3.5 Timer/Counter Registers

The Timer/Counter Registers control three 16-bit counters, two of which are available for adjusting the time between scans in the timed-burst operating mode, and one of which can provide an interrupt at a specific data word count. These registers are described in Section 4.8.

4.3.6 Converter Data Register (CDR)

A/D converter data is read from the CDR when the board is operating in the **random access** mode (Section 4.5.2).

4.4 DATA ORGANIZATION AND CONTROL

4.4.1 Data Word

The contents of each word location in the data buffer is a ***data word***, and represents the 16-bit digitized value of a single analog input channel.

4.4.2 Scaling and Coding

Table 4.4.2-1 shows the data word scaling and coding for all three available channel gains of x1, x10, and x100. Data bit D15 is the most significant bit and D00 is the least significant bit. Coding is straight binary or offset binary if CSR bit D13 is cleared, and is two's complement if CSR bit D13 is set.

4.4.3 Data Block

A complete set of digitized values for all active input channels is a ***data block***, and it can consist of 16, 32, 48, or 64 channels. Block size is controlled by bits D00 and D01 in the BCR, as shown in Table 4.3.3-1. Data words within a block are organized with Channel 00 at the lowest address in the block, and with the highest numbered channel at the highest address.

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Table 4.3.3-1. Buffer Control Register (BCR)

D00 to D01 **INPUT BLOCK SIZE (Number of Active Channels)**

D01	D00	BLOCK SIZE	ACTIVE INPUT CHANNELS
0	0	* 64 Channels	00 to 63
0	1	48	00 to 48
1	0	32	00 to 31
1	1	16	00 to 15

D02 to D04 **INPUT BUFFER SIZE (Total Data Storage)**

D04	D03	D02	BUFFER SIZE (dec)
0	0	0	* 64 Words
0	0	1	16
0	1	0	32
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1,024

D05 **INTERVAL TIMER SELECT (Number of Cascaded 16-bit Timers)**

D05	NUMBER OF TIMERS
0	*1
1	2

D06 **INTERRUPT SOURCE CONTROL**

D06	INTERRUPT SOURCE
0	*DATA READY Flag (CSR)
1	Channel Counter

D07 **Not used**

M3118/T4.3.3-1

* Default mode at RESET.

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Table 4.4.2-1. ADC Data Format and Coding

MSB LSB

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00

ADC DATA FORMAT

ADC DATA CODING (Gain = x1)			
	UNIPOLAR RANGE	**STRAIGHT BINARY**	
INPUT	0 to +10 V	D15	D00
+FS-1 LS	+9.99985 V	1111 1111 1111 1111	
+1/2 FS	+5.00000 V	1000 0000 0000 0000	
+1 LSB	+0.00015 V	0000 0000 0000 0001	
	BIPOLAR RANGE	**OFFSET BINARY**	
INPUT	±10 V	D15	D00
+FS-1 LSB	+9.99969 V	1111 1111 1111 1111	
+1/2 FS	+5.00000 V	1100 0000 0000 0000	
+1 LSB	+0.00031 V	1000 0000 0000 0001	
ZERO	0.00000 V	1000 0000 0000 0000	
-1 LSB	-0.00031 V	0111 1111 1111 1111	
-FS+1 LSB	-9.99969 V	0000 0000 0000 0001	
-FS	-10.00000 V	0000 0000 0000 0000	
	BIPOLAR RANGE	**TWO'S COMPLEMENT**	
INPUT	±10 V	D15	D00
+FS-1 LSB	+9.99969 V	0111 1111 1111 1111	
+1/2 FS	+5.00000 V	0100 0000 0000 0000	
+1 LSB	+0.00031 V	0000 0000 0000 0001	
ZERO	0.00000 V	0000 0000 0000 0000	
-1 LSB	-0.00031 V	1111 1111 1111 1111	
-FS+1 LSB	-9.99969 V	1000 0000 0000 0001	
-FS	-10.00000 V	1000 0000 0000 0000	

	LSB BIT WEIGHT VERSUS INPUT GAIN		
INPUT RANGE	**Gain = x1**	**x10**	**x100**
0 to +5 V, ±2.5V	76.2939 µV	7.62939 µV	0.762939 µV
0 to +10 V, ±5 V	152.588 µV	15.2588 µV	1.52588 µV
±10 V	305.176 µV	30.5176 µV	3.05176 µV

M3118/T4.4.2-1

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4.4.4 Data Buffer/RAM

The ***data buffer*** contains from 1 to 64 data blocks, and is located at board address $0080. The size of the buffer is controlled by the Input Buffer Size bits D02 to D04 in the BCR. The buffer can be adjusted from 16 to 1,024 data words in six equal ratios of 2:1. A single update of all locations in the buffer is a ***data scan***, and is executed at the maximum A/D conversion rate of 52 kHz. Data blocks within the buffer are organized with the first block located at the lowest word address in the buffer, and with the data word in the last block located at the highest address.

Total on-board RAM size is 2,048 words. Memory locations $0880 through $0FFE may be used as scratch pad memory. Also, memory not used for storage of scanning input data may be used as on-board scratch pad memory.

4.4.5 Gain Selection

A fixed channel gain of x1, x10, or x100 can be jumper-selected for all channels, or can be assigned individually for each channel. A jumper-selected gain applies to all channels and cannot be modified by the program. The automatic gain mode provides program control of the gain of each channel.

For automatic gain control, a gain code for each channel is loaded into board memory while operating in the Gain Loading mode (Section 4.5.7). The gain is adjusted automatically as each channel is selected and digitized. Gain codes for all channels are initialized to "zero" (gain = x1) automatically after a reset operation.

4.4.6 Gain Initialization Preload

Directly after each reset operation, an automatic initialization sequence presets all gain codes to "zero", and establishes a gain of x1 for all channels. The sequence is approximately 1.2 msec in length and is completed when the data ready flag (CSR bit D12) is set at the end of the first buffer scan. During this initialization interval, the gain buffer should not be accessed from the VMEbus and the Enable Midscan Flag control bit (CSR D11) should not be set.

4.5 OPERATING MODES

The VMIVME-3118 Board can be programmed to scan the input channels continuously, to read input channels individually, or to acquire data in timed or synchronized bursts. Table 4.5-1 summarizes the various operating modes, all of which are described in this section.

4.5.1 Continuous Scanning

This ***default*** operating mode is selected by a reset operation, or by clearing both CSR Mode control bits. All active channels are scanned continuously in this mode, and any channel can be read at any time without affecting the scanning operation. (See also Section 4.2.3.)

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Table 4.5-1. Operating Mode Selection

OPERATING MODE	CSR CONTROL BITS D10	D09	D08	D07	D06	CSR CODE (Note 1)	INITIATION	TERMINATION
CONTINUOUS SCANNING (Note 2)	0	0	0	0	0	$8000	Select Mode	Change mode
RANDOM ACCESS	0	0	1	0	1	$8140	Set CSR D08 (Note 3)	Automatic (single sample)
TIMED BURSTS	0	1	0	1	0	$8280	Timer zero	Reset or change mode
LOCALLY TRIGGERED BURST	0	0	1	1	0	$8180	Set CSR D08 (Note 3)	Automatic (single scan)
REMOTELY TRIGGERED BURST	1	0	0	1	0	$8480	Ext trigger	Automatic (single scan)
GAIN LOADING (Note 5)	0	0	0	1	1	$80C0	Select Mode (Note 4)	Reset or change mode

NOTES:

1. The indicated CSR code also establishes the following conditions:

a. Self-test LED is OFF.	Subtract $8000 to turn the LED ON.
b. Data coding is binary.	Add $2000 for two's complement coding.
c. Data Ready Flag occurs at end-of-scan.	Add $0400 for a midscan flag.
d. Random access channel is 00.	Add the channel HEX code for any other channel, e.g.: $001A for channel 26.

2. Continuous Scanning is the default mode after a reset operation.
3. CSR D08 clears automatically after sequence initiation.
4. Input sampling and conversion are disabled in the gain loading mode.
5. Automatic channel gain is initialized to unity (x1) at reset, and is specified with a gain code as:

GAIN CODE	CHANNEL GAIN
$00	x1
$01	x10
$02	x100
$03	Invalid Code.

M3118/T4.5-1

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4.5.2 Single Channel Random Access

In this mode, the digitized channel value is read from the Converter Data Register (CDR) at board address $0080. Each input channel is accessed individually by loading the channel number into CSR control bits D00 to D05, and by setting the Start Sequence bit (CSR D08). The Start Sequence bit clears automatically when the sample is initiated, and the Data Ready flag (CSR D12) is set when the digitized value is available in the CDR.

4.5.3 Timed Burst

Timed burst data is acquired in a single data scan, or burst, of all buffer locations when the interval timer times out. A single burst can be acquired at the end of the programmed interval, or the process can be repetitive. In the repetitive mode, a burst is acquired at the end of each interval until either a different mode is selected, or the interval timer is disabled by clearing CSR bit D09. Timer control is described in Section 4.8.

4.5.4 Locally Triggered Burst

An acquisition burst, or data scan, is produced each time the Start Sequence bit (CSR D08) is set. The Start sequence bit clears automatically when the burst is initiated.

4.5.5 Remotely Triggered Burst

This mode is similar to the **locally triggered burst** mode, except that the burst is initiated by a HIGH to LOW transition on the EXT STRT L input at the P2 connector.

4.5.6 Synchronizing Multiple VMIVME-3118 Boards

Multiple VMIVME-3118 Boards can be synchronized together by connecting the TRIG OUT L output from P2 of a synchronizing "master" to the EXT STRT L input of all slave boards. As many as 16 boards in a single chassis can be synchronized in this manner, thereby providing up to 1,024 synchronized input channels and the simultaneous sampling of like numbered channels on all boards.

4.5.7 Gain Loading

If the **automatic gain** mode has been jumper-selected (Section 4.4.5), the gain codes for channels with gains other than unity (x1) must be loaded into board memory after each reset operation. Gain loading is performed by first selecting the **gain loading** mode, and by then loading the gain code for each channel into the gain buffer, as listed in Table 4.5-1.

Selection of the **gain loading** mode replaces the first word of the data buffer with the ***gain buffer*** register. A gain code for each channel is loaded into the Gain Buffer Register, by selecting the channel in the CSR.

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The address for each gain value is loaded into the CSR as the input address INPA0H to INPA5H (D00 to D05). After all gain codes have been initialized, the **scanning** mode can be selected and the gain for each channel will be adjusted automatically.

The gain codes for all channels are initialized to "zero" (gain = x1) directly after a reset operation. The gain buffer should not be accessed during this initialization interval. The Data Ready flag is set when initialization is complete and the board may be accessed normally.

4.6 SCAN MONITORING

4.6.1 Data Ready Flag and Interrupt

CSR bit D12 is the Data Ready flag, and is set to "one" at the end of a scan if CSR D11 is "zero", or at the middle of a scan if CSR D11 is "one". The data ready flag clears automatically when any buffer location is accessed from the VMEbus.

If the interrupt is enabled and the BCR control bit D06 (Table 4.3.3-1) is "zero", an interrupt will be generated when the Data Ready flag is set.

4.6.2 Data Counter and Interrupt

The Data Counter Register (DCR) can be programmed to provide a data word count directly, or to generate an interrupt when a specific number of A/D conversions have occurred. Control of the DCR is described in Section 4.8.

4.7 BUS INTERRUPTER

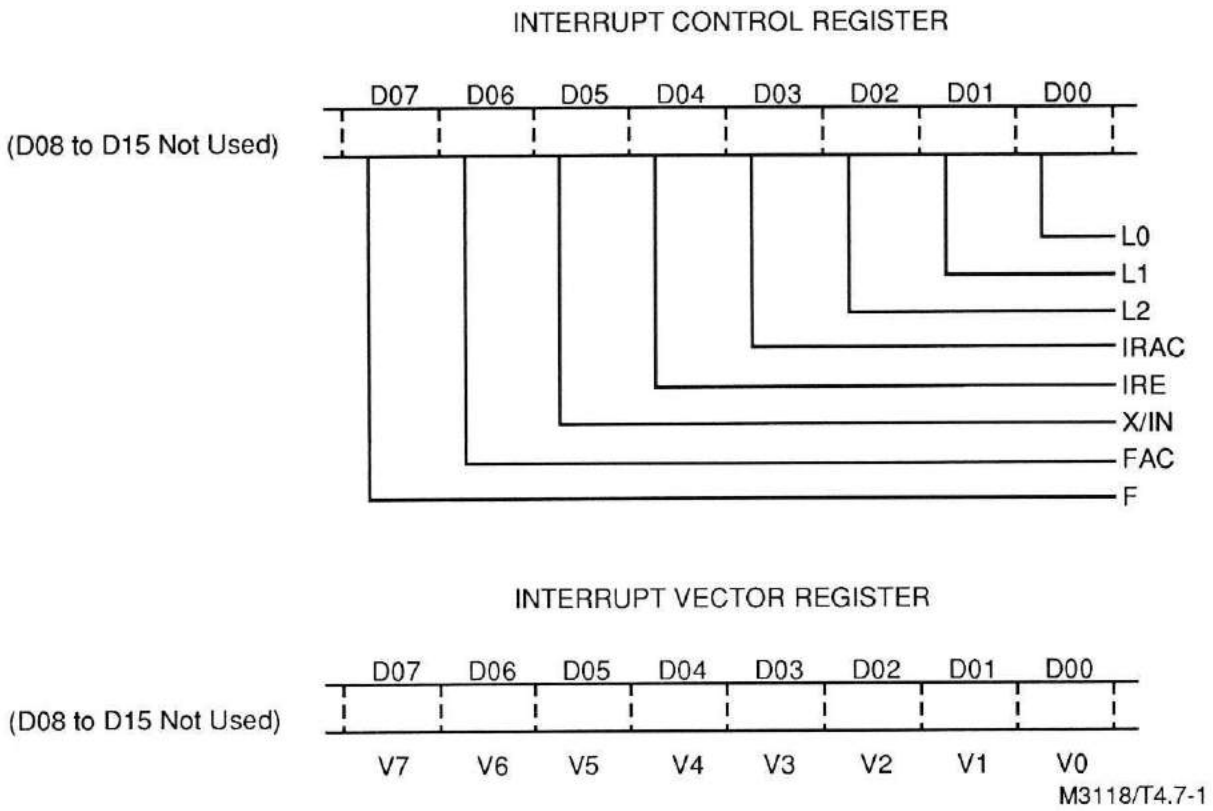
An interrupt can be generated when the data buffer is filled or half-filled, or after a specific number of A/D conversions have been completed (Section 4.6). The interrupt response is established through the INTERRUPT CONTROL and INTERRUPT VECTOR registers which are shown in Table 4.7-1. During board reset or system reset operations, the INTERRUPT CONTROL register is cleared to "$00" and the INTERRUPT VECTOR register is preset to "$0F".

4.7.1 Interrupt Control Register

The INTERRUPT CONTROL register controls the interrupt level, as well as enabling or disabling the interrupt. The function of each control bit is described in Table 4.7.1-1.

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Table 4.7-1. Interrupt Registers Organization



4.7.2 Interrupt Vector Register

Contents of the INTERRUPT VECTOR register are supplied as a data byte (D07 through D00) on the data bus during the board's **interrupt acknowledge cycle**. The function of the vector is determined by the system user.

4.8 TIMER/COUNTER CONTROL

4.8.1 General Characteristics

Interval timing and data counting capabilities are provided by a triple 16-bit programmable timer/counter which is controlled by the Timer/Counter Registers at board addresses $0020 to $0026 (Table 4.3-1). Interval Timer Register TR0 is driven by an 8 MHz clock, and TMR1 is driven by the output of TMR0.

The Data Counter Register (DCR) operates independently of the two timers, and is used to monitor the progress of data through the buffer. Operating modes and data transfers for all three counters are controlled by the Timer/Counter Register (TCR).

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Table 4.7.1-1. Interrupt Control Register Functions

INTERRUPT LEVEL (L2, L1, L0, Bits D02, D01, D00):

Determines the level at which an interrupt will occur:

REGISTER BIT L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

INTERRUPT ENABLE (IRE, Bit D04):

When this bit is set HIGH, the bus interrupt is enabled; the interrupt is disabled if IRE is LOW.

INTERRUPT AUTO-CLEAR (IRAC, Bit D03):

If the IRAC bit is set HIGH, the interrupt enable bit (IRE) is cleared during the interrupt acknowledge cycle which responds to the request. The IRE bit must then be set HIGH again to enable the interrupt.

EXTERNAL/INTERNAL (X/IN, Bit D05):

This control bit has no valid function on the VMIVME-3118 Board, and *MUST* be cleared LOW at all times.

FLAG (F, Bit D07):

This control bit has no effect on the operation of the VMIVME-3118 Board, and is available for use by the controlling processor as a utility flag.

FLAG AUTO-CLEAR (FAC, Bit D06):

If "FAC" is set HIGH, the flag bit "F" is automatically cleared during an interrupt acknowledge cycle.

M3118/T4.7.1-1

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All timer/counter data transfers are eight bits wide and use data bits D0 to D7. Two data transfers are required to read or write each 16-bit counter, with the least significant byte transferred first and the most significant byte transferred second. The control word determines the type of transfer, and must be written to the timer/counter before each data transfer. Table 4.8.1-1 lists the data transfer sequences for the timers and counter.

4.8.2 Scan Interval Timer

By operating in the "timed burst mode", the data buffer can be scanned (filled) repetitively at specific intervals, or a single scan can be initiated after the first interval. The **timed burst** mode is selected as follows:

a. Operating Mode 2 — CSR D07 = 1, CSR D06 = 0

b. Interval Timer enabled — CSR D09 = 1

When operating in this mode, a buffer scan will occur at the end of the time interval programmed into the timer.

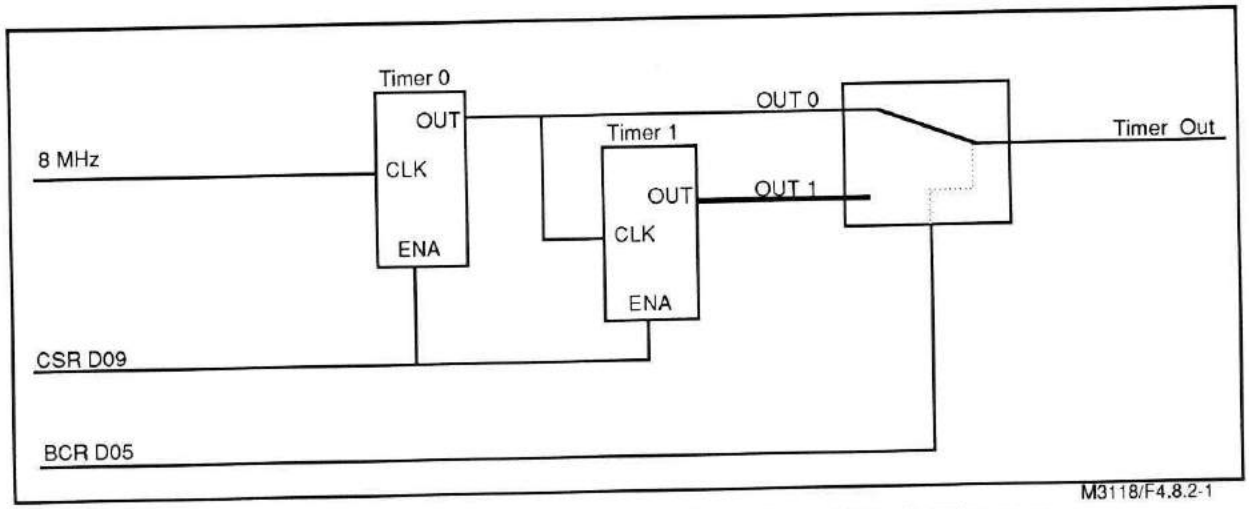


Figure 4.8.2-1. VMIVME-3118 Timer Functional Block Diagram

If BCR D05 is cleared, Timer 0's output is selected as the timer's output and the product of the timer's output will be:

Formula for 16-bit Timer: Time/.125 = T0

If BCR D05 is set, then Timer 1's output is selected as the timer's output and the output of Timer 0 is used as the clock for Timer 1. The period of the timer's output will be:

Formula for 2 Cascaded 16-bit Timers: Time/.125 = T1 X T0

Where:
Time = Period of Timer out in µs up to 536.8454 s.
T0 = Timer 0's 16-bit value in decimal (1 to 6535).
T1 = Timer 1's 16-bit value in decimal (1 to 65535).

See Figure 4.8.2-1 for a functional block diagram of the interval timer circuitry.

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Table 4.8.1-1. Timer/Counter Data Transfer Sequences

OPERATION	LOAD SEQUENCE	REGISTER ADDRESS	REGISTER NAME	TRANSFERRED DATA, D00-D07(Note 2)	XFR MODE
LOAD TIMER 0	1	$26	Control Word	$34 (Select Timer)	WRITE
	2	$20	TMR 0 LS Byte	Least Significant Byte	WRITE
	3	$20	TMR 0 MS Byte	Most Significant Byte	WRITE
LOAD TIMER 1 (Note 1)	1	$26	Control Word	$74 or $78 (Note 3)	WRITE
	2	$22	TMR 1 LS Byte	Least Significant Byte	WRITE
	3	$22	TMR 1 MS Byte	Most Significant Byte	WRITE
LOAD DATA COUNTER	1	$26	Control Word	$B4	WRITE
	2	$24	CNTR LS Byte	Least Significant Byte	WRITE
	3	$24	CNTR MS Byte	Most Significant Byte	WRITE
READ TIMER 0	1	$26	Control Word	$00 (Latch Timer Value)	WRITE
	2	$26	Control Word	$34 (Select Timer)	WRITE
	3	$20	TMR 0 LS Byte	Least Significant Byte	READ
	4	$20	TMR 0 MS Byte	Most Significant Byte	READ
READ TIMER 1 (Note 1)	1	$26	Control Word	$40	WRITE
	2	$26	Control Word	$74 or $78 (Note 3)	WRITE
	3	$22	TMR 1 LS Byte	Least Significant Byte	READ
	4	$22	TMR 1 MS Byte	Most Significant Byte	READ
READ DATA COUNTER	1	$26	Control Word	$80	WRITE
	2	$26	Control Word	$B4	WRITE
	3	$24	CNTR LS Byte	Least Significant Byte	READ
	4	$24	CNTR MS Byte	Most Significant Byte	READ

M3118/T4.8.1-1

NOTES:

1. BCR control bit D05 must be set to "one" to include Timer 1 in the interval timer (See text). The 32-bit timer is configured as:

	TIMER 1 (BITS 31 to16)		TIMER 0 (BITS 15 to 00)		
MSB	MS BYTE	LS BYTE	MS BYTE	LS BYTE	LSB

2. Timer values $0001 0000, $0001 0001, and $0001 are invalid.
3. A Timer 1 control word of $0074 will produce repetitive data bursts at the programmed interval. A control word of $0078 will limit the acquisition to a single data burst at the end of the first interval. The single burst can be repeated by reloading the timer 1 load sequence.

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Programmed timer intervals less than the time required to fill the buffer can cause unpredictable operation and should be avoided. The time, in microseconds, required to fill a buffer is 19 times the buffer word size. For example, a 64-word buffer fills in 1,216 µs.

4.8.3 Data Counter Control

The data counter can generate an interrupt after a predetermined number of data words have been stored in the buffer. The counter can be read directly to monitor the data count. To use the counter to generate an interrupt:

a. Load the data counter with the required data count (Table 4.8.1-1)

b. Set the source control bit D06 in the BCR (Table 4.5-1) to "one". (This disables the midscan/endscan interrupt.)

c. Enable the interrupt as described in Section 4.7

d. Initiate the scanning operation

Table 4.8.1-1 shows the sequence required for reading the data counter directly. The data counter can be accessed at any time, regardless of which operating mode is selected. Because the counter counts down, the value read is the ***remaining*** data count.

4.9 TYPICAL PROGRAMMING EXAMPLES

The following examples of VMIVME-3118 programming illustrate typical applications for various operating modes.

We assume the following conditions:

a. Type 68010 or later system processor
b. Automatic gain
c. Short I/O location $FBFF 0000
d. Offset binary data coding

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4.9.1 Example C Header File

```
/*-------------------------------------------------------------------------*/
/*  3118.H  3118 HEADER FILE                                               */
/*-------------------------------------------------------------------------*/

/*  DEFINE  Bytes, Words AND Longs  FROM C DATA SIZES.                     */

typedef unsigned char  Byte;        /* BYTES ARE UNSIGNED CHAR'S          */
typedef unsigned short Word;        /* WORDS ARE UNSIGNED SHORT'S         */
typedef unsigned int   Long;        /* LONGS ARE UNSIGNED INT'S           */
typedef struct v3118_reg Reg3118;   /* 3118 register type                 */
typedef struct v3118_buf Buf3118;   /* 3118 ram buff type                 */


struct v3118_reg
{
  Word reg3118[20];           /* 3118 REGISTERS ARE AN ARRAY OF 20 WORDS  */
};


struct v3118_buf
{
  Word  adc3118[1024];        /* 3118 ADC MEMORY IS AN ARRAY OF 1024 WORDS*/
};


/*  REGISTER OFFSET (ARRAY) DEFINITIONS                                    */

#define   BID           00          /* BOARD ID REGISTER (1 word)         */
#define   CSR           01          /* CONTROL STSTUS REGISTER            */
#define   BCR           02          /* BUFFER CONTROL REGISTER            */
#define   ICR           08          /* INTERRUPT CONTROL REGISTER         */
#define   IVR           12          /* INTERRUPT VECTOR  REGISTER         */
#define   TR0           16          /* INTERVAL TIMER REGISTER 0          */
#define   TR1           17          /* INTERVAL TIMER REGISTER 1          */
#define   DCR           18          /* DATA COUNTER REGISTER              */
#define   TCR           19          /* TIMER/COUNTER CONTROL REGISTER     */

/*-------------------------------------------------------------------------*/
```


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4.9.2 Example C Program

```
/*-------------------------------------------------------------------------*/
/*  EXAMPLE C ROUTINES FOR THE VMIVME - 3118 64 CHANNEL ANALOG INPUT BOARD  */
/*-------------------------------------------------------------------------*/
/*-------------------------------------------------------------------------*/
/*  INCLUDE NEEDED SUPPORT CODE                                            */
/*-------------------------------------------------------------------------*/
#include  <stdio.h>                  /* STANDARD I/O HEADER FILE           */
#include  "3118.h"                   /* VMIVME-3118 HEADER FILE            */

/*-------------------------------------------------------------------------*/
/*  SETUP MEMORY POINTERS AND STORAGE                                      */
/*-------------------------------------------------------------------------*/

void init_gain( Reg3118 *board, Buf3118 *buffer, Word gain ) ;
void set_gain( Reg3118 *board, Buf3118 *buffer, Word channel, Word gain ) ;
void auto_scan( Reg3118 *board, Buf3118 *buffer, Word num_of_scans ) ;
void timed_scan( Reg3118 *board, Buf3118 *buffer, Word num_of_scans ) ;
void local_burst( Reg3118 *board, Buf3118 *buffer ) ;
void remote_burst( Reg3118 *board, Buf3118 *buffer, Word num_of_scans ) ;

struct
{
  Word storage[1024] ;
} memory ;

Word  loop, oldcsr, gain, channel, num_of_scans, num_done;

main()
{
  Reg3118 * brd_base = ((Reg3118 *) 0xFBFF0000) ;
  Buf3118 * buf_base = ((Buf3118 *) 0xFBFF0080) ;

  gain = 0x0001;              /* GAIN SET EQUAL TO X10                      */
  channel = 0x0005;           /* CHANNEL SELECTED IS CHANNEL 5              */
  num_of_scans = 0x0100;      /* NUMBER OF SCANS IS EQUAL TO 100 HEX BUFFERS */

  init_gain( brd_base, buf_base, gain ) ;
  set_gain( brd_base, buf_base, channel, gain ) ;
  auto_scan( brd_base, buf_base, num_of_scans ) ;
  timed_scan( brd_base, buf_base, num_of_scans ) ;
  locally_burst( brd_base, buf_base ) ;
  remote_burst( brd_base, buf_base, num_of_scans ) ;
}

/*-------------------------------------------------------------------------*/

void init_gain( Reg3118 *board, Buf3118 *buffer, Word gain )
{
  oldcsr = board->reg3118[CSR] ;
  for( loop = 0x0000; loop < 0x0040; loop++ )
  {
    board->reg3118[CSR] = (0x80c0 + loop) ;  /* 80C0 = GAINLOAD MODE       */
```


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```
    buffer->adc3118[00] = gain ;
  }
  board->reg3118[CSR] = oldcsr ;
}

/*-------------------------------------------------------------------------*/

void set_gain( Reg3118 *board, Buf3118 *buffer, Word channel, Word gain )
{
    oldcsr = board->reg3118[CSR] ;
    board->reg3118[CSR] = (0x80c0 + channel) ;  /* 80C0 = GAINLOAD MODE      */
    buffer->adc3118[00] = gain ;
    board->reg3118[CSR] = oldcsr ;
}

/*-------------------------------------------------------------------------*/

void auto_scan( Reg3118 *board, Buf3118 *buffer, Word num_of_scans )
{
  oldcsr = board->reg3118[CSR] ;
  num_done = 0x0000 ;
  board->reg3118[BCR] = 0x001C ; /* 64 CHANNELS, 1024 WORDS                  */
  board->reg3118[CSR] = 0x8800 ; /* AUTO SCAN, MIDSCAN ENABLED               */
  do
  {
    if( board->reg3118[CSR] = = 0x9800 ) /* CHECK FOR DATA READY FLAG       */
    {
      for( loop = 0x0000; loop < 0x0400; loop ++ )
 {
      memory.storage[ loop ] = buffer->adc3118[ loop ] ;
      }
      num_done++ ;
    }
  } while ( num_done < num_of_scans ) ;
  board->reg3118[CSR] = oldcsr ;
}

/*-------------------------------------------------------------------------*/

void timed_scan( Reg3118 *board, Buf3118 *buffer, Word num_of_scans )
{
  oldcsr = board->reg3118[CSR] ;
  num_done = 0x0000 ;

  board->reg3118[TCR] = 0x0034 ;  /* SELECT TIMER 0                          */
  board->reg3118[TR0] = 0x00E8 ;  /* WRITE TR0 LSB                           */
  board->reg3118[TR0] = 0x0003 ;  /* WRITE TR0 MSB                           */
  board->reg3118[TCR] = 0x0074 ;  /* SELECT TIMER 1                          */
  board->reg3118[TR1] = 0x0040 ;  /* WRITE TR1 LSB                           */
  board->reg3118[TR1] = 0x001F ;  /* WRITE TR1 MSB                           */
  board->reg3118[BCR] = 0x003C ;  /* 64 CHANNELS, 1024 WORDS, TR1 ENABLED    */
  board->reg3118[CSR] = 0x8280 ;  /* TIMER ENABLED, SINGLE SCAN              */

  do
```


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```
  {
    if( board->reg3118[CSR] = = 0x9280 ) /* CHECK FOR NEW DATA READY FLAG      */
    {
      for( loop = 0x0000; loop < 0x0400; loop ++ )
      {
        memory.storage[ loop ] = buffer->adc3118[ loop ] ;
      }
    num_done++ ;
    }
  } while ( num_done < num_of_scans ) ;
  board->reg3118[CSR] = oldcsr ;
}



/*-------------------------------------------------------------------------*/

void local_burst( Reg3118 *board, Buf3118 *buffer )
{
  oldcsr = board->reg3118[CSR] ; /* STORE CSR FOR FUTURE USE                 */
  board->reg3118[BCR] = 0x001C ; /* 64 CHANNELS, 1024 WORDS                  */
  board->reg3118[CSR] = 0x8080 ; /* SINGLE SCAN                              */
  board->reg3118[CSR] = 0x8180 ; /* TRIGGER BURST                            */
  for( loop = 0x0000; loop < 0x0400; loop ++ )
  {
    memory.storage[ loop ] = buffer->adc3118[ loop ] ;
    num_done++ ;
  }
  board->reg3118[CSR] = oldcsr ;
}

/*-------------------------------------------------------------------------*/

void remote_burst( Reg3118 *board, Buf3118 *buffer, Word num_of_scans )
{
  oldcsr = board->reg3118[CSR] ;
  num_done = 0x0000 ;
  board->reg3118[BCR] = 0x001C ; /* 64 CHANNELS, 1024 WORDS                  */
  board->reg3118[CSR] = 0x8480 ; /* WAIT REMOTE TRIGGER                      */
  do
  {
    if( board->reg3118[CSR] = = 0x9480 )
    {
      for( loop = 0x0000; loop < 0x0400; loop ++ )
      {
        memory.storage[ loop ] = buffer->adc3118[ loop ] ;
      }
      num_done++ ;
    }
  } while ( num_done < num_of_scans ) ;
  board->reg3118[CSR] = oldcsr ;
}

/*-------------------------------------------------------------------------*/
```


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SECTION 5
CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
**********
*  CAUTION  *
**********
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC'S PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE, AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC DISCHARGE. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC, together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
**********
*  CAUTION  *
**********
```

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis, while ensuring that the board is properly aligned and oriented in the supporting card guides. Slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before applying power to the VMEbus chassis in which the board is installed, execute the following checklist to ensure that the board has been correctly prepared for operation.

a. Verify that the sections pertaining to programming and configuration, Section 4 and 5, have been reviewed and applied to system requirements. _____

b. Review Section 5.4 and Table 5.4-1 to verify that all jumpers are configured correctly for the application. _____

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c. Verify that the I/O cables are properly terminated for the input/output connectors. Refer to Section 5.6 for connector descriptions. _____

d. Physical installation should have been completed as described in Section 5.2. _____

e. Ensure that all system cable connections are correct. _____

5.4 OPERATIONAL CONFIGURATION

VMEbus access modes and analog input configurations are controlled by field replaceable jumpers. This section describes the use of these jumpers, and their effects on board performance. Locations and functions of all VMIVME-3118 jumpers are shown in Figure 5.4-1 and Table 5.4-1. Typical jumper configurations are summarized in Table 5.4-2.

5.4.1 Factory-Installed Jumpers

Each VMIVME-3118 Board is configured at the factory with the specific jumper arrangement shown in Table 5.4-1. The ***factory configuration*** establishes the following functional baseline for the VMIVME-3118 Board, and ensures that all essential jumpers are installed.

a. Board Identification is located at *$0000* in the ***short I/O space***, with either ***supervisory or nonprivileged*** access

b. Automatic gain control
c. ±10 V range
d. Differential inputs
e. External trigger I/O is enabled
f. Input COMM bus is connected to analog return (AGND)
g. LOW inputs for Channels 31 and 63 are disconnected from COMM and AGND

5.4.2 Access Modes

Supervisory (privileged) access is selected by installing J11-3,4, and user (nonprivileged) access is selected by installing J11-5,6. Installing both J11-3,4 and J11-5,6 selects either supervisory ***or*** user access. J11 also permits memory operation in the A24 memory space to be designated for either ***data access*** (J11-7, 8 installed) or ***program access*** (J11-7,8 removed).

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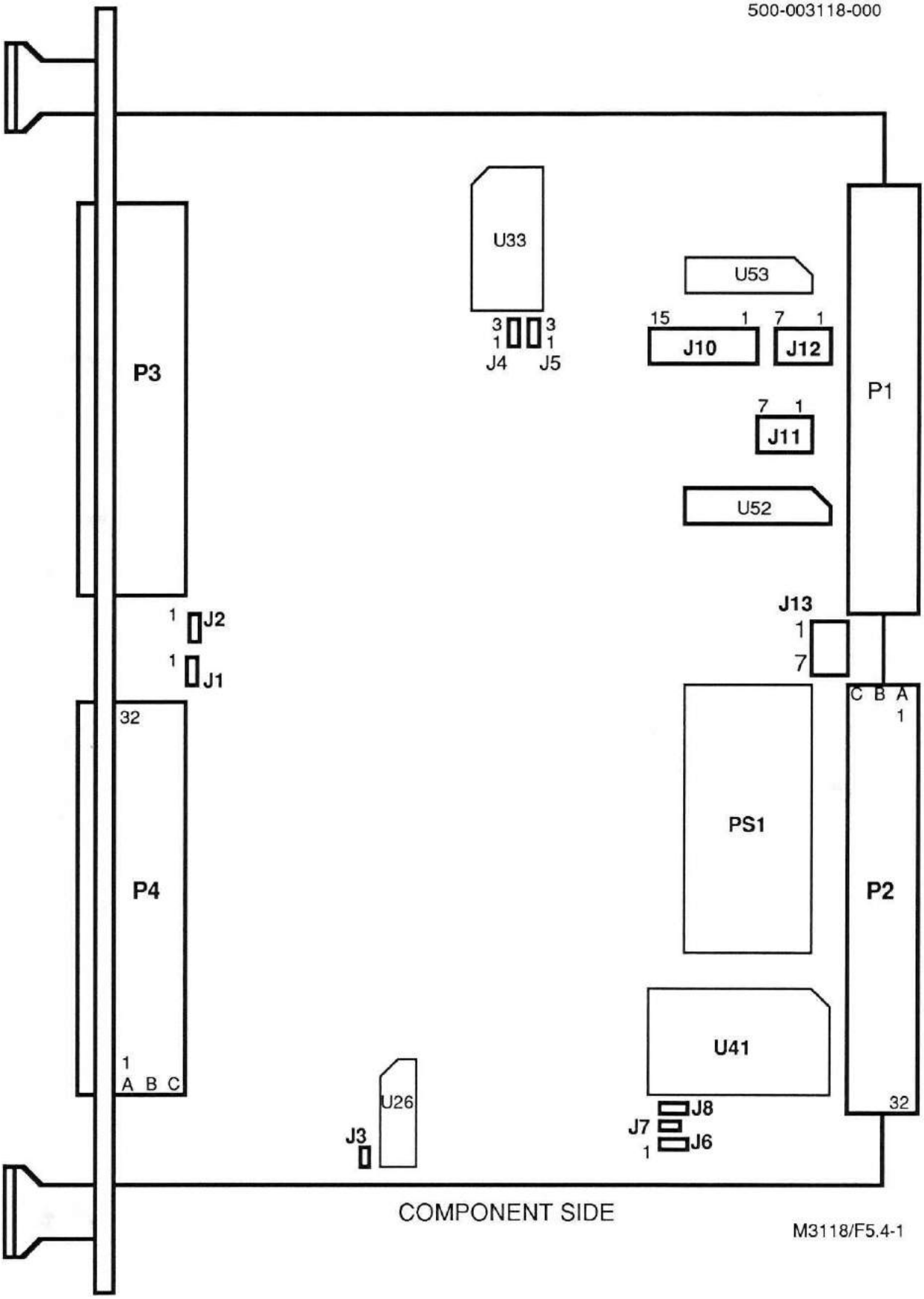


Figure 5.4-1. VMIVME-3118 Jumper Locations

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Table 5.4-1. Programmable Jumper Functions

JUMPER IDENT	FUNCTION (Installed)	FACT CONFIG
J11-1,2	Short I/O Operation	Installed
J11-3,4	Supervisory (Supervisory) Access	Installed
J11-5,6	User (Nonprivileged) Access	Installed
J11-7,8	Data Access	Installed
J12-1,2	Address Bit A12 = 0	Installed
J12-3,4	Address Bit A13 = 0	Installed
J12-5,6	Address Bit A14 = 0	Installed
J12-7,8	Address Bit A15 = 0	Installed
J10-1,2	Address Bit A16 = 0	Installed
J10-3,4	Address Bit A17 = 0	Installed
J10-5,6	Address Bit A18 = 0	Installed
J10-7,8	Address Bit A19 = 0	Installed
J10-9,10	Address Bit A20 = 0	Installed
J10-11,12	Address Bit A21 = 0	Installed
J10-13,14	Address Bit A22 = 0	Installed
J10-15,16	Address Bit A23 = 0	Installed
J4-1,2	Gain A1 = 0	Removed
J4-2,3	Gain A1 = Automatic	Installed
J5-1,2	Gain A0 = 0	Removed
J5-2,3	Gain A0 = Automatic	Installed
J6-1,2	Bipolar Analog Inputs	Installed
J6-2,3	Unipolar Analog Inputs	Removed
J7	±2.5 V or 0 to +5 V Ranges	Removed
J8-1,2	±10 V Range	Installed
J8-2,3	±2.5 V, 0 to +5 V, ±5 V, 0 to +10 V Ranges	Removed
J13-1,2	External Trigger Enabled	Installed
J13-3,4	External Trigger Enabled	Installed
J13-5,6	External Trigger Enabled	Installed
J3	Input COMM Grounded to AGND	Installed
J1-1,2	Ch 31 LOW Input Conn to AGND	Removed
J1-2,3	Ch 31 LOW Input Conn to COMM	Removed
J2-1,2	Ch 63 LOW Input Conn to AGND	Removed
J2-2,3	Ch 63 LOW Input Conn to COMM	Removed

M3118/T5.4-1

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Table 5.4-2. Typical Jumper Configurations

EXAMPLE OF J10 TO J12 CONFIGURATION

for: **Standard Memory Access;**
Supervisory Only;
Data Space.
Address $00D1 F000

JUMPER	STATE	POSITION *
J11-1,2	STD MEMORY	REMOVED
J11-3,4	SPVSR	INSTALLED
J11-5,6	USER	REMOVED
J11-7,8	DATA	INSTALLED
J12-1,2	A12=1	REMOVED
J12-3,4	A13=1	REMOVED
J12-5,6	A14=1	REMOVED
J12-7,8	A15=1	REMOVED
J10-1,2	A16=1	REMOVED
J10-3,4	A17=0	INSTALLED
J10-5,6	A18=0	INSTALLED
J10-7,8	A19=0	INSTALLED
J10-9,10	A20=1	REMOVED
J10-11,12	A21=0	INSTALLED
J10-13,14	A22=1	REMOVED
J10-15,16	A23=1	REMOVED

	INPUT GAIN			
JUMPER	x1	x10	x100	AUTO
J4	1,2	1,2	REM	2,3
J5	1,2	REM	1,2	2,3

	ADC VOLTAGE RANGE *				
JUMPER	±10 V	±5 V	±2.5 V	0 TO +10 V	0 TO +5 V
J6	1,2	1,2	1,2	2,3	2,3
J7	REM	REM	INS	REM	INS
J8	1,2	2,3	2,3	2,3	2,3

	EXTERNAL TRIGGER *	
JUMPER	ENABLED	DISABLED
J13 (All)	INS	REM

M3118/T5.4-2

* "INS" = Jumper installed, "REM" = Jumper removed.

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NOTE

TO BE CONSISTENT WITH CONVENTIONAL VMEbus DEVELOPMENT SYSTEM NOMENCLATURE, HEXADECIMAL NUMBERS IN THIS DOCUMENT ARE DESIGNATED A "$" PREFIX UNLESS OTHERWISE INDICATED. DECIMAL NUMBERS ARE PRESENTED WITHOUT A PREFIX.

5.4.3 Board Location in Short I/O or Memory Space

Jumper J11 selects operation in either the ***short I/O A16 space*** with J11-1, 2 installed, or in the ***standard A24 memory space*** with J11-1,2 removed (see Section 4.2). Jumper blocks J10 and J12 locate the board on any 4,096-word boundary in the A16 or A24 space.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit positions in jumper blocks J10 and J12, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A12 is the least significant address bit that can be jumper-selected, and has a weight of 4,096 words.

5.4.4 Analog Input Gain

Jumpers J4 and J5 control the ***analog input gain***, as shown in Table 5.4-2. Jumper-selected gains of x1, x10, and x100 are fixed and apply to all input channels. The AUTO gain configuration places the gain of each input channel under software control (Section 4.4).

5.4.5 Converter Voltage Range

The ***A/D Converter voltage range*** is controlled by jumpers J6, J7, and J8 as shown in Table 5.4-2.

5.4.6 Input Voltage Range

The input voltage range (full scale voltage at the input of each channel) is determined by both the ***analog input gain*** and the ***A/D converter voltage range***:

INPUT VOLTAGE RANGE = CONVERTER VOLTAGE RANGE ÷ INPUT GAIN

For example, an input gain of x10 combined with a converter voltage range of ±5 V produces an input voltage range of ±500 mV (±0.5 V).

5.4.7 External Triggering

The selection of either internal or external triggering of single scan is under software control (Section 4.5). Jumper block J13 connects the trigger signals at the P2 connector to the internal control logic, and usually is configured with all jumpers installed as shown in Table 5.4-1. If the application does not require external triggering, all J13 jumpers can be removed. If external triggering has been selected through software, and if all J13 jumpers are installed, a data scan begins at the HIGH to LOW transition of the EXT STRT L input at P2.

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5.4.8 Input Configurations

The analog inputs can be configured as single-ended, differential or pseudo-differential channels, as shown in Table 5.4.8-1. The configurations are selected in groups of four consecutive channels by the positions of jumpers J1, J2, and J3, and by the locations of SIP (single-in-line-package) resistor networks.

In pseudo-differential operation, the LOW input for Channels 31 or 63 acts as the external return. Input configurations can be mixed in groups of four channels with no restriction except that the pseudo-differential operation of any group commits either Channel 31 or 63 also as pseudo-differential.

5.4.9 Internal Ground Connections

All pins in the center "B" rows of both input connectors P3 and P4 are connected together as the COMM return, and provide a ground path and interchannel guards between differential input pairs when 96-wire 0.033-inch ribbon cables are used. The COMM return can be connected to the internal analog ground (AGND) by installing jumper J3.

The LOW input for Channel 31 or 63 can be connected to AGND by installing J1-1,2 (Channel 31) or J2-1,2 (Channel 63), or to the COMM return by installing J1-2,3 or J2-2,3. Installation of either of these jumpers configures the associated channel as a ***single-ended*** input. Each jumper must be removed entirely for differential operation of the associated channel.

5.5 CALIBRATION

Before delivery from the factory, the VMIVME-3118 Board is fully calibrated and conforms to all specifications listed in Section 2. Should recalibration be required, refer to Sections 5.5.1 through 5.5.3, and perform the indicated procedures in the order shown. The locations of test points and adjustments are shown in Figure 5.5-1.

5.5.1 Equipment Required

a. Digital Voltmeter (DVM) ..... 1.000 and 10.000 VDC ranges; 5 or more digits; ±0.003 percent of reading measurement accuracy; 10 MΩ minimum input impedance.

b. Digital Voltage Source..... 10.000 VDC ±0.001 VDC voltage source; ±0.003 percent setting resolution and accuracy. 10 Ω maximum source resistance.

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Table 5.4.8-1. Input Configuration Selection

P4 CHANNEL GROUP	INPUT CONFIGURATION (Note 1)								
	SINGLE-ENDED			DIFFERENTIAL			PSEUDO-DIFF		
	SIP POS (Note 2)	JUMPERS		SIP POS (Note 2)	JUMPERS		SIP POS (Note 2)	JUMPERS	
		J1	J2		J1	J2		J1	J2
00 to 03	RP33	1,2	---	RP1	---	---	RP33	2,3	---
04 to 07	RP34	1,2	---	RP3	---	---	RP34	2,3	---
08 to 11	RP35	1,2	---	RP5	---	---	RP35	2,3	---
12 to 15	RP36	1,2	---	RP7	---	---	RP36	2,3	---
16 to 19	RP37	1,2	---	RP9	---	---	RP37	2,3	---
20 to 23	RP38	1,2	---	RP11	---	---	RP38	2,3	---
24 to 27	RP39	1,2	---	RP13	---	---	RP39	2,3	---
28 to 31	RP40	1,2	---	RP15	REM	---	RP40	2,3	---
	Ch 31 is Sing-End						Return is Ch 31 LOW		

P3 CHANNEL GROUP	INPUT CONFIGURATION (Note 1)								
	SINGLE-ENDED			DIFFERENTIAL			PSEUDO-DIFF		
	SIP POS (Note 2)	JUMPERS		SIP POS (Note 2)	JUMPERS		SIP POS (Note 2)	JUMPERS	
		J1	J2		J1	J2		J1	J2
32 to 35	RP41	---	1,2	RP17	---	---	RP41	---	2,3
36 to 39	RP42	---	1,2	RP19	---	---	RP42	---	2,3
40 to 43	RP43	---	1,2	RP21	---	---	RP43	---	2,3
44 to 47	RP44	---	1,2	RP23	---	---	RP44	---	2,3
48 to 51	RP45	---	1,2	RP25	---	---	RP45	---	2,3
52 to 55	RP46	---	1,2	RP27	---	---	RP46	---	2,3
56 to 59	RP47	---	1,2	RP29	---	---	RP47	---	2,3
60 to 63	RP48	---	1,2	RP31	---	REM	RP48	---	2,3
	Ch 63 is Sing-End						Return is Ch 63 LOW		

M3118/T5.4.8.1

NOTES:

1. Jumper positions are indicated as:
   - 1,2 Shorting plug between pins 1 and 2.
   - 2,3 Shorting plug between pins 2 and 3.
   - REM Shorting plug removed.
   - --- "Don't care"; shorting plug can be installed or removed.
2. "SIP POS" = "Single-in-line-package position." The indicated position is one of two possible locations for the input SIP. Only one of the two locations is occupied. For example, the SIP for channel group 00 to 03 can be located as either RP33 or RP1.

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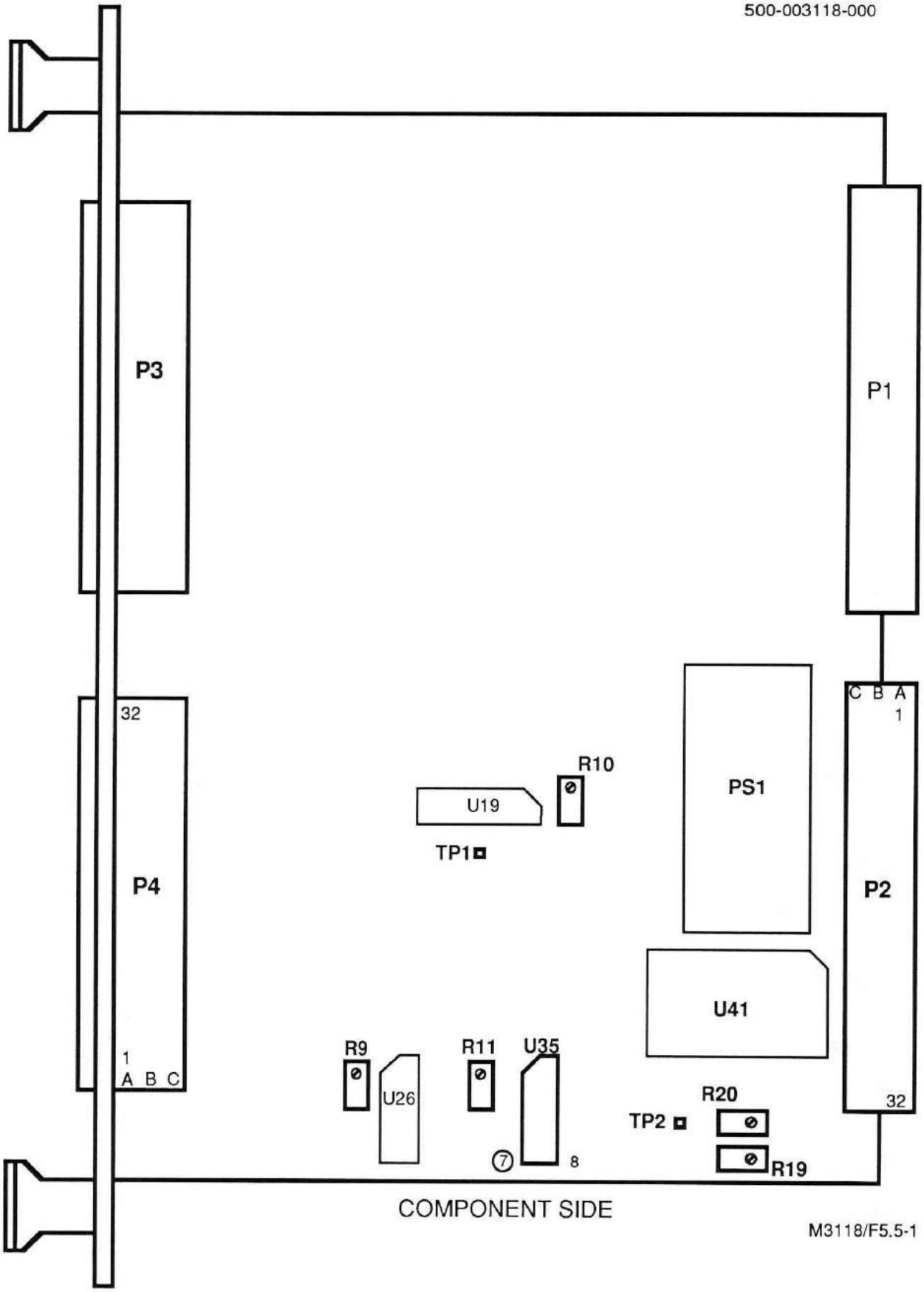


Figure 5.5-1. Locations of Test Points and Adjustments

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c. Chassis..... VMEbus backplane or equivalent, with J1 connector, 68000 Series master controller, +5 ±0.1 VDC, 7 A (reserve current) power supply. One slot allocated for testing the VMIVME-3118 Board.

d. Extender Board..... VMEbus extender board

```
**********
*  CAUTION  *
**********
```

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED TO THE SYSTEM.

5.5.2 Calibration Procedure

a. Restore all program jumpers to the factory configuration, as shown in Table 5.4-1.
b. Locate the board at an address that is compatible with the VME operating system. Install jumpers J4, and J5-1,2 to select a PGA gain of x1.
c. Install the VMIVME-3118 Board on an extender board in the VMEbus chassis
d. Apply power to the chassis backplane. Allow a minimum warmup interval of ten minutes before proceeding.
e. Connect the digital voltage source to the Channel 00 and Channel 01 input pins P4-A1, A2 (+) and P4-C1, C2 (-). Adjust the voltage source output to 0.0000 VDC.
f. Connect the digital voltmeter between TP1 (+) and TP2 (-)
g. Write the following data to the indicated board relative addresses:

ADDRESS	DATA	REGISTER	MODE
$0002	$C000	CSR	Reset
$0002	$8040	CSR	Random Access mode, multiplexer discharged

h. Adjust potentiometer R10 for a digital voltmeter indication of 0.0000 VDC ±0.0020 VDC
i. Move the voltmeter positive test lead to U35-7
j. Adjust R11 for a voltmeter indication of 0.0000 VDC ±0.0020 VDC
k. Remove the digital voltmeter test connection.
l. Write the following data to the indicated board relative addresses:

ADDRESS	DATA	REGISTER	MODE
$0002	$C000	CSR	Reset
$0002	$8000	CSR	Continuous scanning

m. Read and display board word locations $0080 repetitively, at 3 to 5 readings/sec.

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n. With the voltage source output adjusted to -9.9997 VDC, adjust R19 until the value displayed at location $0080 varies between $0000 and $0001.
o. With the voltage source output adjusted to +9.9997 VDC, adjust R20 until the value displayed at location $0080 varies between $FFFE and $FFFF.
p. Repeat steps *n* and *o* until both values are correct
q. With the voltage source output adjusted to 0.0000 VDC, adjust R19 until the value displayed at location $0080 varies between $7FFF and $8000.
r. With the voltage source output adjusted to 0.0000 VDC, adjust R9 until the value displayed at location $0082 varies between $7FFF and $8000.
s. Remove the J4 jumper. Verify that J5-1,2 is installed.
t. Adjust R10 until the value displayed at location $0080 varies between $7FFF and $8000
u. Calibration is completed. To perform the functional verification, retain the existing test configuration and proceed to Section 5.5.3.

5.5.3 Functional Verification

This procedure tests the Programmable Gain Amplifier (PGA), and verifies the integrity of all input channels. Steps *a* through *e* are identical to steps *a* through *e* in Section 5.5.2, and can be omitted if the calibration procedure has been performed within the previous hour, and if power has not been removed from the board.

a. Restore all program jumpers to the factory configuration, as shown in Table 5.4-1.
b. Locate the board at an address that is compatible with the VME operating system. Install jumpers J4-1,2 and J5-1,2 to select minimum PGA gain (x1).
c. Install the VMIVME-3118 Board on an extender board in the VMEbus chassis.
d. Apply power to the chassis backplane. Allow a minimum warmup interval of ten minutes before proceeding.
e. Connect the digital voltage source to the Channel 00 input pins P4-A1 (+) and P4-C1 (-). Adjust the voltage source output to 0.0000 VDC.
f. Write the following data to the indicated board relative addresses:

ADDRESS	DATA	REGISTER	MODE
$0002	$C000	CSR	Reset
$0002	$8000	CSR	Continuous scanning

g. Read and display board word location $0080 (input Channel 00) repetitively, at 3 to 5 readings /sec.
h. Verify that the J4 jumper is removed and that J5-1,2 is installed. Adjust the voltage source output to +99.219 mVDC, and verify that the displayed value is between $FED0 and $FF30.
i. Remove the J5 jumper. Install jumper J4-1,2 to select a gain of x10.
j. Adjust the voltage source output to +992.19 mVDC, and verify that the displayed value is between $FED0 and $FF30.

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k. Install jumper J5-1,2 to select a gain of x1. Verify that J4-1,2 is installed.
l. Adjust the voltage source output to +9.9219 VDC, and verify that the displayed value is between $FEFB and $FF05.
m. Refer to the P3 and P4 connector descriptions in Table 5.5.3-1 to determine the input pairs used in the remainder of this procedure.
n. Move the digital voltage source test leads to the Channel 01 input pins. Connect the positive test lead to the A row pin, and the negative test lead to the C row pin.
o. Change the address of the displayed data to $0082 (input Channel 01). Verify that the displayed value is between $FEFA and $FF06.
p. Repeat steps *n* and *o* for the remaining Channels 02 through 63. Increase the displayed address by $0002 for each successive channel, to a maximum address of $00FE for Channel 63.
q. Functional verification is completed. Remove power from the board. Remove all test connections. Restore the board to the factory configuration, as shown in Table 5.4-1.

5.6 CONNECTOR DESCRIPTIONS

5.6.1 Connector Functions

Electrical connections to the VMIVME-3118 Board are made through four 96-pin DIN connectors P1 through P4, all of which have the pin configuration shown in Figure 5.6.1-1.

P1 connects the VMIVME-3118 Board to the VMEbus backplane, and contains the address, data, and control lines, and all additional signals necessary to control VMEbus functions related to the board. P2 provides the user pins necessary for external synchronization of the board. User pin assignments are listed in Table 5.5.3-1.

5.6.2 Input Modes

Analog inputs are connected to the board through front panel connectors P3 and P4. P4 contains the input pins for Channels 00 to 31, and P3 contains the input pins for Channels 32 to 63. Pin assignments for P3 and P4 are summarized in Table 5.5.3-1. The center "B" rows in P3 and P4 are connected together to a COMM bus, which can be used as a guard bus for 96-wire cables. Refer to Section 5.4.8 and Table 5.4.8-1 for the selection of ***single-ended***, ***differential***, or ***pseudo-differential*** input configurations. Typical mating connectors for P3 and P4 are listed in Table 2.4-1.

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Table 5.5.3-1. Input/Output Connector Pin Assignments

P2 CONNECTOR USER PINS

PIN NUMBER	INPUT/OUTPUT SIGNAL ROW A	ROW C
01 to 26	N/C	N/C
27	EXT STRT L	N/C
28	EXT STRT RTN	N/C
29	TRIG OUT L	N/C
30	N/C	N/C
31	EN EXT STRT H	N/C
32	N/C	N/C

P4 CONNECTOR

PIN NUMBER	INPUT SIGNAL ROW A	ROW B	ROW C
01	CH 00 HIGH	COMM	CH 00 LOW
02	CH 01 HIGH	COMM	CH 01 LOW
03	CH 02 HIGH	COMM	CH 02 LOW
04	CH 03 HIGH	COMM	CH 03 LOW
05	CH 04 HIGH	COMM	CH 04 LOW
06	CH 05 HIGH	COMM	CH 05 LOW
07	CH 06 HIGH	COMM	CH 06 LOW
08	CH 07 HIGH	COMM	CH 07 LOW
09	CH 08 HIGH	COMM	CH 08 LOW
10	CH 09 HIGH	COMM	CH 09 LOW
11	CH 10 HIGH	COMM	CH 10 LOW
12	CH 11 HIGH	COMM	CH 11 LOW
13	CH 12 HIGH	COMM	CH 12 LOW
14	CH 13 HIGH	COMM	CH 13 LOW
15	CH 14 HIGH	COMM	CH 14 LOW
16	CH 15 HIGH	COMM	CH 15 LOW
17	CH 16 HIGH	COMM	CH 16 LOW
18	CH 17 HIGH	COMM	CH 17 LOW
19	CH 18 HIGH	COMM	CH 18 LOW
20	CH 19 HIGH	COMM	CH 19 LOW
21	CH 20 HIGH	COMM	CH 20 LOW
22	CH 21 HIGH	COMM	CH 21 LOW
23	CH 22 HIGH	COMM	CH 22 LOW
24	CH 23 HIGH	COMM	CH 23 LOW
25	CH 24 HIGH	COMM	CH 24 LOW
26	CH 25 HIGH	COMM	CH 25 LOW
27	CH 26 HIGH	COMM	CH 26 LOW
28	CH 27 HIGH	COMM	CH 27 LOW
29	CH 28 HIGH	COMM	CH 28 LOW
30	CH 29 HIGH	COMM	CH 29 LOW
31	CH 30 HIGH	COMM	CH 30 LOW
32	CH 31 HIGH	COMM	CH 31 LOW*

P3 CONNECTOR

PIN NUMBER	INPUT SIGNAL ROW A	ROW B	ROW C
01	CH 32 HIGH	COMM	CH 32 LOW
02	CH 33 HIGH	COMM	CH 33 LOW
03	CH 34 HIGH	COMM	CH 34 LOW
04	CH 35 HIGH	COMM	CH 35 LOW
05	CH 36 HIGH	COMM	CH 36 LOW
06	CH 37 HIGH	COMM	CH 37 LOW
07	CH 38 HIGH	COMM	CH 38 LOW
08	CH 39 HIGH	COMM	CH 39 LOW
09	CH 40 HIGH	COMM	CH 40 LOW
10	CH 41 HIGH	COMM	CH 41 LOW
11	CH 42 HIGH	COMM	CH 42 LOW
12	CH 43 HIGH	COMM	CH 43 LOW
13	CH 44 HIGH	COMM	CH 44 LOW
14	CH 45 HIGH	COMM	CH 45 LOW
15	CH 46 HIGH	COMM	CH 46 LOW
16	CH 47 HIGH	COMM	CH 47 LOW
17	CH 48 HIGH	COMM	CH 48 LOW
18	CH 49 HIGH	COMM	CH 49 LOW
19	CH 50 HIGH	COMM	CH 50 LOW
20	CH 51 HIGH	COMM	CH 51 LOW
21	CH 52 HIGH	COMM	CH 52 LOW
22	CH 53 HIGH	COMM	CH 53 LOW
23	CH 54 HIGH	COMM	CH 54 LOW
24	CH 55 HIGH	COMM	CH 55 LOW
25	CH 56 HIGH	COMM	CH 56 LOW
26	CH 57 HIGH	COMM	CH 57 LOW
27	CH 58 HIGH	COMM	CH 58 LOW
28	CH 59 HIGH	COMM	CH 59 LOW
29	CH 60 HIGH	COMM	CH 60 LOW
30	CH 61 HIGH	COMM	CH 61 LOW
31	CH 62 HIGH	COMM	CH 62 LOW
32	CH 63 HIGH	COMM	CH 63 LOW*

* Channel 31 and 63 LOW inputs can be jumpered individually to either COMM or AGND returns.

M3118/T5.5.3-1

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5.6.3 Input Cables

If 96-wire 0.033-inch ribbon cables or discrete wire type cables are used for the analog inputs, the center row COMM bus can provide a ground reference to the analog return (AGND) on the board by installing Jumper J3. If 64-wire 0.050-inch ribbon cables are used, "VARI TWIST" or equivalent twisted-pair cables are recommended to minimize crosstalk and induced noise. Access to AGND is available in 64-wire cables at pin C32 of P3 and P4 by installing J1-1,2 for P4, or J2-1, 2 for P3.

5.6.4 External Synchronization

External TTL-level synchronization triggers are connected to the EXT STRT L input at the P2 connector (refer to Section 5.4.7). The EN EXT STRT H output is a flag to the triggering device that the VMIVME-3118 is ready to accept an external trigger. To synchronize multiple VMIVME-3118 Boards together, connect the TRIG OUT H output from the designated "master" board to the EXT STRT L input of all boards to be synchronized to the master.

5.7 SYSTEM CONSIDERATIONS

5.7.1 Applications with Signal Conditioning Boards

The VMIVME-3118 Board serves as a multiplexer/digitizer for signal conditioning boards such as the VMIVME-3413 32-Channel Low-Level Input Board. The output connectors on the signal conditioning boards are configured to cable directly to either P3 or P4 on the VMIVME-3118.

When used with signal conditioning boards, the VMIVME-3118 is configured with either differential or pseudo-differential inputs, and with a low-input gain of x1 or x10. These applications must utilize the 1.6 kHz input filter option.

5.7.2 Operation with Direct Analog Inputs

When used without signal conditioning input boards, the VMIVME-3118 Board provides direct full-scale input ranges from ±25 mV to ±10 V. The optimum input filter for these applications is the 50 Hz filter, although the 10 Hz filter will provide improved attenuation of power line frequency interference at the expense of decreased common-mode rejection. To minimize the effects of direct input multiplexing, the source impedance of analog inputs should not exceed 1,500 Ω for the ±10 V input range, or 10 Ω for the ±25 mV range. Use the lowest input gain and the largest block size (Section 4.4.3) that are practical for the application.

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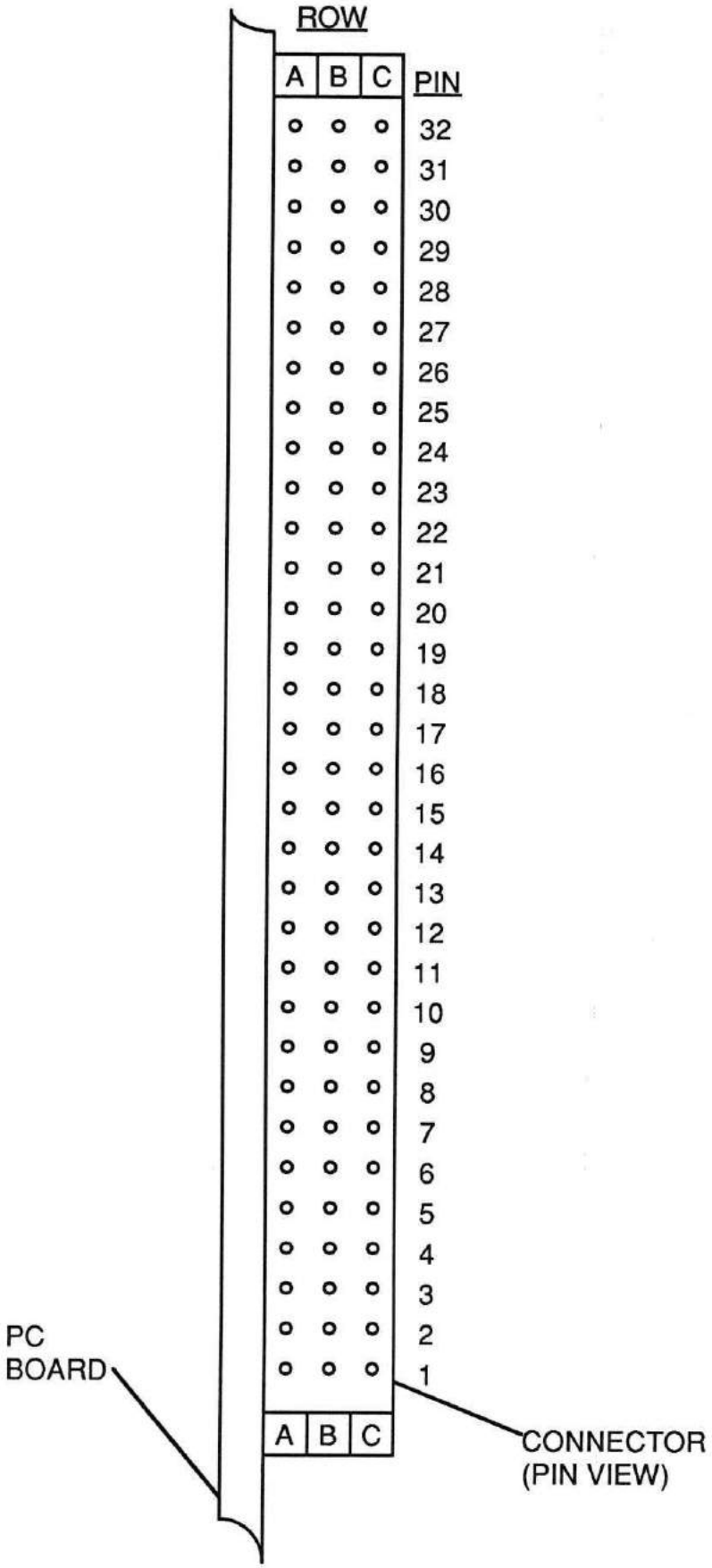


Figure 5.6.1-1. P1 to P4 Connector Pin Configuration

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If inputs are obtained directly from remote sources, the grounding scheme used can have a major effect on system performance. Each system has its own unique interference considerations, but the following general guidelines will apply in most cases.

a. Long Input Lines: Long input lines (greater than 10 feet), or inputs from grounded sources (sources which are not floating), should be connected to ***differential inputs***, and overall shields should be extended from the input sources to as close to the board as possible. ***Single-ended inputs*** are susceptible to ground loop errors, and should be used only with high-level floating sources.

b. Source Impedance: Use signal sources with the lowest available source impedances. Susceptibility to crosstalk and induced interference increases as the source impedance increases.

c. Floating Signal Sources: The shield from a floating signal source (RTD, strain gage, etc.) should be connected to the LOW (negative) terminal at the source. For low impedance sources (less than 10 Ω), or for sources which are protected from interference fields, connect the board end of the shield to analog return (AGND) at the board. For high impedance sources, connect all shield terminals of the sources together, and leave the board ends of the shields open.

d. Grounded Signal Sources: Outputs of grounded sources (sources which are not floating) must be referenced to a common ground which ensures that the input voltage will not exceed the input range (± 10 V) of the board. Shields from grounded sources should be connected to the LOW terminal of the sources, and left open at the board.

e. Unused Inputs: Unused inputs within each group of eight channels (0 through 7, 8 through 15, etc.) should be connected to a common ground to avoid interference with active channels. Grounding of unused 8-channel groups is not essential, but will assist in minimizing susceptibility to system noise.

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SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

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defective product(s) or part(s) must also be properly boxed and weighed. After a VMIC Call Ticket Number and RMA Number have been obtained, the defective product(s) or part(s) may be returned (transportation collect for surface UPS) to VMIC. Any replaced or repaired product(s) or part(s) will be shipped back to the customer's at the expense of VMIC (also UPS surface).

The customer should be aware that the above process can sometimes take up to eight (8) days for the shipment to reach VMIC. The customer has the option to ship the defective product(s) or part(s) at the customer's own expense if the customer cannot afford this possible delay.

There shall be no warranty or liability on any VMIC product(s) or part(s) that is (are) damaged or subjected to accident(s), perils of nature, negligence, overtemperature, overvoltage, misapplication of electrical power, insertion or removal of boards from backplanes and/or I/O connectors with power applied by the customer(s), appointee(s), or any other person(s) without the expressed approval of VMIC.

Final determination of warranty eligibility shall be made by VMIC, and if a warranty claim is considered invalid for any reason, the customer will be charged for services performed and expenses incurred by VMIC in repair, handling and shipping the returned product or part. Determination as to whether the item is within warranty, coverage shall not be unreasonably withheld.

The warranty period of the replacement or repaired product(s) or part(s) shall terminate with the termination of the warranty period with respect to the original product(s) or part(s) for all replacement parts supplied or repairs made during the original warranty period.

THE FOREGOING WARRANTY AND REMEDY ARE EXCLUSIVE AND VMIC SHALL HAVE NO OTHER OR ADDITIONAL LIABILITY TO BUYER OR TO ANYONE CLAIMING UNDER BUYER (THIRD PARTY) UNDER ANY OTHER AGREEMENT OR WARRANTY, EXPRESS OR IMPLIED EITHER IN FACT OR BY OPERATION OF THE LAW, INCLUDING ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS, STATUTORY, OR OTHERWISE. VMIC SHALL HAVE NO LIABILITY FOR SPECIAL OR CONSEQUENTIAL DAMAGES OF ANY KIND OR FROM ANY CAUSE ARISING OUT OF THE INSTALLATION OR USE OF ANY PRODUCT FURNISHED HEREUNDER.

6.4 OUT-OF-WARRANTY REPAIR POLICY

The following sections describe VMIC's policy on repairs and warranties on repaired products.

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6.4.1 Repair Category

VMIC's repair policy of standard products is divided into two categories, depending on the item to be repaired. These categories are:

a. Product Exchange
b. Fixed Price Repair

Category 1 (product exchange) represents the fastest turn around of the two categories. In this case, the customer sends the malfunctioning product to VMIC. VMIC will return an operational product to the customer within 72 hours of receipt provided VMIC has the product in stock.

Provided that the returned product is repairable customers should contact VMIC prior to returning products for repair to determine stocking status.

Category 2 (Fixed Price Repair) applies to products returned to VMIC for repair and subsequent return to the customer.

Return authorizations are required on all product repairs, and all purchase orders should refer to VMIC's RMA Number which is assigned by VMIC's Customer Service Department.

6.4.2 Repair Pricing

Contact your factory representative for repair pricing. Current pricing can be found in the Repair and Replacement Policy in the most current Standard Conditions of Sales Document (F0109-91). Refer to exclusions (Section 6.4.7).

6.4.3 Payment

Payment is due upon delivery or at VMIC's option, net thirty (30) days from the date of delivery. Payment should be made to:

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, Alabama 35803-3308
Attention: Accounts Receivable

VMIC allows a one (1) percent discount for payment made within ten (10) days of invoice date or a two (2) percent discount on payment made prior to shipment of order. This payment discount, however, does not apply to freight.

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6.4.4 Shipping Charges

Shipping charges are the customer's responsibility, with the exception of warranty repairs, whereby VMIC will pay the return to customer shipping charges.

6.4.5 Shipping Instructions

The type of packaging used to ship the product depends on whether the product is shipped singly, in a chassis, or packaged with other boards. The shipper should carefully pack the product(s), using the same precautions listed in the "unpacking procedures". The user should utilize the same (or equivalent) protective packaging container for re-shipment as provided by VMIC. Approved ESD procedures are recommended when handling VMIC's products.

6.4.6 Warranty on Repairs

Products repaired by VMIC are warranted against defects in workmanship and material for a period of ninety (90) days from date of shipment to the customer for all products that were repaired out of warranty. See Standard Conditions of Sale for products repaired within the warranty.

6.4.7 Exclusions

Repair rates may not apply to products which have received unusual physical or electrical damage. In such cases, VMIC will provide an estimated price for product repair or replacement. The customer may then choose to have the product repaired at the estimated price, returned unrepaired at no charge, or replaced at VMIC's current list price.

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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DOCUMENTATION EVALUATION FORM

VMIC welcomes your comments and suggestions.

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DOCUMENT NO.: _____
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READABILITY	_____	ILLUSTRATIONS	_____
ORGANIZATION	_____	PROGRAMMING INFORMATION	_____
ACCURACY	_____	SPECIFICATIONS	_____
COMPLETENESS	_____	MAINTENANCE DIAGRAMS	_____

SPECIFIC PROBLEMS: **PAGE(s)**

( ) CLARIFICATION REQUIRED _____

( ) NOT ENOUGH INFORMATION GIVEN _____

( ) TYPOGRAPHICAL ERRORS _____

( ) TECHNICAL ERRORS (EXPLAIN): _____

DOCUMENT USE: (check all that apply)

( ) HARDWARE	( ) SOFTWARE	( ) PRODUCT EVALUATION
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