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VMIVME-3124
ANALOG INPUT BOARD

PRODUCT MANUAL

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RECORD OF REVISIONS

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VMIC
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DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

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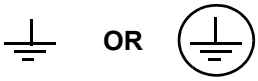
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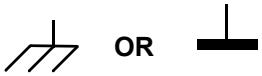
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



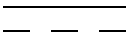
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



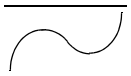
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-3124
ANALOG INPUT BOARD

TABLE OF CONTENTS

Page

SECTION 1. INTRODUCTION

1.1 FEATURES 1-1

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

SECTION 3. THEORY OF OPERATION

3.1 INTRODUCTION 3-1
3.2 FUNCTIONAL ORGANIZATION 3-1
3.3 VMEbus INTERFACE 3-1
3.4 ANALOG-TO-DIGITAL CONTROL AND TIMING 3-3
3.5 BUILT-IN-TEST REFERENCE 3-4
3.6 ANALOG INPUTS 3-4
3.6.1 Low-Pass Filters 3-5
3.6.2 Input Multiplexers 3-5
3.6.3 Current Inputs 3-5
3.7 PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER 3-5
3.8 CHANNEL SEQUENCER AND DUAL-PORTED RAM MEMORY . . . 3-5
3.9 BOARD ID REGISTER 3-6
3.10 BUILT-IN POWER CONVERTER AND ADC POWER SUPPLY 3-6

SECTION 4. PROGRAMMING

4.1 MEMORY MAP 4-1
4.2 REGISTER DESCRIPTIONS 4-4
4.2.1 Board ID Register 4-4
4.2.2 Board Configuration Register 4-4
4.2.3 Control/Status Register 4-5
4.2.4 Channel Pointer Register 4-6
4.2.5 Data Registers 4-6
4.3 BUILT-IN-TEST FUNCTIONS 4-8
4.4 RANGE AND GAIN DETERMINATION 4-9
4.5 ACCESSING DATA AS BYTES 4-9
4.6 CURRENT INPUTS, -2BC AND -3BC OPTIONS 4-10

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 JUMPER INSTALLATIONS 5-2

TABLE OF CONTENTS (Concluded)

SECTION 5. CONFIGURATION AND INSTALLATION (Concluded) Page

5.3.1 Board Address 5-2
5.3.2 Address Modifier 5-3
5.3.3 Input Configuration 5-4
5.4 ANALOG INPUT CONNECTOR DESCRIPTION 5-5
5.5 CALIBRATION PROCEDURES 5-6
5.5.1 Equipment Required 5-6
5.5.2 Instrumentation Amp Offset Calibration 5-6
5.5.3 Unipolar 0-10 V Offset and Gain Calibration 5-6
5.5.4 Bipolar ±5 V Offset and Gain Calibration 5-7
5.5.5 Bipolar ±10 V Offset and Gain Calibration 5-7
5.5.6 Built-In-Test Voltage Calibration 5-8

SECTION 6. MAINTENANCE

6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1

LIST OF FIGURES

Figure Page

3.2-1 VMIVME-3124 Functional Block Diagram 3-2
5.3-1 VMIVME-3124 Configuration Jumper Locations 5-2
5.4-1 P3 Connector 5-5

LIST OF TABLES

Table Page

4.1-1 VMIVME-3124 Memory Map: Differential Inputs, Normal Buffer . . 4-1
4.1-2 VMIVME-3124 Memory Map: Differential Inputs, Maximum Buffer . . 4-2
4.1-3 VMIVME-3124 Memory Map: Single-Ended Inputs 4-3
4.2.1-1 Board Configuration Register Contents 4-4
4.2.3-1 Board Control/Status Register Contents 4-5
4.2.3-2 Board Control/Status Register Modes 4-6
4.2.5-1 LSB Weight 4-7
4.3-1 BIT Values for 0-10 V Range 4-8
4.3-2 BIT Values for ±5 V Range 4-9
4.3-3 BIT Values for ±10 V Range 4-9
4.6-1 Voltage Seen by the ADC 4-10
5.3.1-1 Address Selection Jumpers 5-3
5.3.2-1 Address Modifier Jumper Settings 5-4
5.3.3-1 Input Configuration Jumpers 5-4
5.4-1 P2 Analog Connector Pinout 5-5

APPENDIX

Assembly Drawing, Parts List, and Schematic

SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-3124 Analog Input board provides automatic scanning of 16 differential or 32 single-ended analog input channels. The channels are digitized with a 12-bit resolution Analog-to-Digital Converter (ADC). Each input is over-voltage protected and low-pass filtered. The board is very easy to use, no software setup is required. After power-up or system reset, the VMIVME-3124 automatically starts scanning each of its 16 or 32 input channels. Conversion data is stored automatically in a dual-port memory, making it immediately accessible from the VMEbus. The VMIVME-3124 provides on-board voltage references to perform an on-line or off-line built in self-test. The input voltage range and gain are user programmable with jumpers. The VMEbus base address and the access mode are fully selectable. In short I/O space the board can be ordered to support optional current inputs (0-25 mA) using 32-channel single-ended inputs.

Some of the distinguishing features of the VMIVME-3124 include:

a. VMEbus 3U single height format
b. Sixteen differential or 32 single-ended analog input channels
c. One 12-bit A/D converter with built-in track-and-hold
d. Automatic scanning of all inputs at 40 kHz aggregate rate
e. No software initialization required to begin scanning
f. Input ranges from ±50 mV to ±10 VDC
g. Input over voltage protection
h. Analog inputs are low pass filtered at 50 kHz
i. Optional add on 40 Hz low pass filter card
j. Discrete wire or mass terminated cables
k. Input pull-down resistors prevent floating inputs
l. Supports on-line & off-line Built-In-Test (BIT)
m. Jumper programmable gains of x1, x10, x100
n. Selectable A/D ranges of ±5 VDC, ±10 VDC and 0-10 VDC
o. Data Accesses: D16, D08(EO), D08(O)
p. Front panel LED
q. Optional 0-20, 4-20, and 5-25 mA current input range

The VMIVME-3124 occupies 128 bytes of short I/O VMEbus addressing space. Jumpers are provided to place the board on any 128-byte boundary. The board may also be jumper-programmed to respond to supervisory, nonprivileged, or both accesses.

Conversion data is available from a 16-bit register (12-bit right justified with optional sign extension). This data is stored in on-board dual-ported memory for easy access.

The Built-In-Test (BIT) capability permits the user to verify the on-board ADC using high precision user programmable reference voltages. Software must control the BIT functions.

After a system reset, the board returns to a fixed configuration. All bits in the Control/Status Register are cleared and the front panel FAIL LED is illuminated. The LED must then be extinguished under software control. This LED can then be used to visually locate a faulty board in a system.

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-003124-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

The VMIVME-3124 is a flexible, low-cost analog input board that provides 16 differential or 32 single-ended analog input channels. The channels are scanned continuously at an tartrate rate of 40 kHz using a 12-bit resolution Analog-to-Digital Converter (ADC). Channels are randomly or sequentially read at any time. The current address of the channel being digitized is read from the Channel Pointer Register. Scanning is halted at the current channel using the Stop Auto Scan bit in the Control/Status Register. This disables further channel address increments. The board then locks onto that channel. This allows a single channel to be digitized every 25 μsec. The following sections discuss the functional components of the VMIVME-3124 in detail.

3.2 FUNCTIONAL ORGANIZATION

The VMIVME-3124 is divided into the following functional categories. Each category will be discussed in detail.

a. VMEbus Interface
b. Analog-to-Digital Converter (ADC) and Control Logic
c. Analog Input Multiplexing, Gain and Conversion
d. BIT Voltage Reference and multiplexer
e. Board ID register

Figure 3.2-1 illustrates the functional blocks of the VMIVME-3124.

3.3 VMEbus INTERFACE

The VMIVME-3124 communications registers are memory mapped as 64 16-bit words (128-bytes) in memory. The registers are contiguous and can located on any 128-byte boundary within the short I/O space of the VMEbus. The board can be configured to respond to short supervisory or short nonprivileged data accesses, or both. See Section 5 for address jumper locations and configurations.

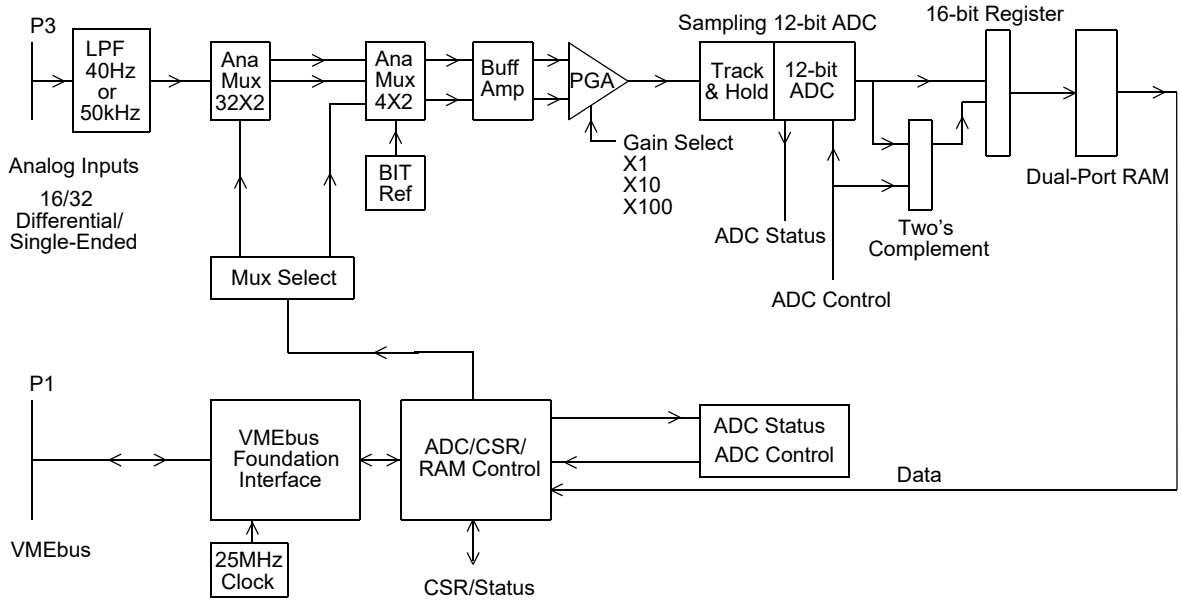


Figure 3.2-1 VMIVME-3124 Functional Block Diagram

During each read or write operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers and the address and address modifier line from the backplane. The appropriate board response occurs if a valid match is detected. The open collector DTACK interface signal is then asserted (driven low). Subsequent completion of the bus master's read or write cycle causes the board-generated DTACK signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communication with the board. They are as follows:

a. Data bus lines D00 to D15
b. Address lines A01, A02, A03, A04, A05, A06, A07
c. Bus Control Signals:
   Write
   DS0*, DS1*
   SYSCLK
   SYSRESET*

Data bus lines are bidirectional and move data to and from the board through a 16-bit data transceiver, responding to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus that interconnects all data devices on the board.

Address lines A01 through A07 map the 64 registers into 128-byte range within the VME address space described in Section 4. The control signals determine whether data is to be moved *to* the board (write) or *from* the board (read). The control signals also provide the necessary data strobes (DS0,DS1). A SYSRESET input resets all CSR bits.

Static controls are latched into the Control Register and are used primarily to establish the operational mode of the board.

3.4 ANALOG-TO-DIGITAL CONTROL AND TIMING

Control commands and status flags associated with controlling the Analog-to-Digital Converter (ADC) are described in Section 4.

There are two modes of operation for this board. The first is to continuously scan all 16 or 32 analog input channels. The second is to halt scanning and lock onto a single channel. In either case, the electrical process of analog-to-digital conversion is similar.

The VMIVME-3124 uses a 12-bit ADC. The ADC has a conversion time of 8.5 μsec. Settling time is required for the multiplexers and the Programmable Gain Amplifier (PGA) before the ADC cycle can begin. The total channel acquisition cycle occurs every 25 μsec. All conversion timing is provided by internal sources. This gives an aggregate scan rate for all channels of 40 kHz. The ADC's built-in track/hold amplifier prevents signals which can vary during a conversion cycle, from giving false ADC readings.

After the multiplexer and gain amp have settled, the ADC is placed into the convert mode. The ADC's BUSY signal then goes active high to indicate the ADC is currently working on a new conversion cycle. The built-in track/hold amp automatically changes from track to hold mode, after which the ADC begins its successive approximation conversion cycle. The conversion digitizes the analog signal from the track and hold amp into a 12-bit data word.

The ADC signals the completion of its cycle by lowering the BUSY signal to a logic "0". If the 2's Complement bit is set in the CSR, the ADC's 12-bit output is modified into this format. At this point the 12-bit word is latched for storage to the Dual-Port RAM.

3.5 BUILT-IN-TEST REFERENCE

The board is equipped with a programmable precision voltage reference which is used as a Built-In-Test (BIT) of the board. When selected, the BIT voltage is transferred through the Programmable Gain Amplifier (PGA) to the Analog-to-Digital Conversion (ADC), bypassing the external analog input on channel zero. Therefore, the channel zero location in the Dual-Port RAM is written with the BIT voltage's equivalent digital value. After enabling the BIT voltage (Mode 0 bit set), the user should allow enough time to elapse (810 μsec max.), to allow sequencing through channel zero before checking its value. The BIT can be used to test the PGA, the ADC, and the Dual-Port RAM memory. The BIT may be enabled at any time during initial board installation or in real time for system self-diagnostics.

The BIT reference is selected from one of three internal precision reference voltages: +4.980 VDC, +0.4928 VDC, +9.915 mVDC or analog ground (0.0 VDC).

The selection is provided by setting the Mode bits 0,1, and 2 in the Control/Status Register (CSR) register. See Section 4.

If mode bit 0 is a logical "0", the board scans all 16 or 32 channels in a normal mode of operation. If the mode bit is set in the CSR, channel 0 will correspond to the selected reference voltage VREF0, VREF1, VREF2, or Analog Ground according to the settings of mode bit 1 and mode bit 2. The digital value received should be within ±10 LSBs of the selected reference voltage. The remaining channels (1-15 or 1-31) digitize their respective external input sources. Thus, channel zero is periodically checked during run time to verify the ADC's operation. Please note that the current gain and unipolar/bipolar modes must be considered when selecting the reference voltage. The BIT voltage precedes the PGA and multiplies the reference voltage selected. Selecting a reference voltage which will exceed the ADC's range when multiplied by the gain amplifier.

3.6 ANALOG VOLTAGE INPUTS

There are 16 differential or 32 single-ended analog inputs available on the front panel connector. It is recommended that the differential mode be used for decreased noise and greater common mode rejection. Unused inputs should be grounded, including the low side of all unused differential inputs. The board has internal 22 MΩ pull-down resistors on the low side of the differential inputs. This prevents the differential input pair from drifting up past the input multiplexers' maximum voltage limit.

3.6.1 Low Pass Filters

The VMIVME-3124 provides passive single-pole low-pass input filters on all inputs. The normal -3 dB cut-off frequency is 50 kHz. This provides some high frequency noise protection for the board. The board may also be configured with an add on daughter board option. The daughter board provides a low-pass filter with a cut-off frequency of 40 Hz. This lower cut-off provides some protection from local 60 Hz AC line noise. This option is normally installed by the factory at the time of the order. It can be removed by the user at a later date if new applications are implemented. If the board is running in single-ended mode, the user must be sure to install the two zero ohm SIP jumpers in locations E1 and E2. This allows the low-pass filter to perform in the single-ended configuration. Adding the 40 Hz daughter board automatically sets the 40 Hz bit in the CSR register.

3.6.2 Input Multiplexers

The board has two-tiers of analog multiplexing. Each of the 32 inputs is selected using one of four 8x1 first-tier analog input multiplexers. The second-tier multiplexer is configured as a 4x2 board. It selects one or two of the first-tier output signals to provide the single-ended or differential mode of operation. The second-tier multiplexer also selects the BIT reference voltage if enabled in the Control/Status Register. The second-tier output is differentially transferred to the Programmable Gain Amplifier (PGA).

3.6.3 Current Inputs

The VMIVME-3124-2BC and -3BC models include current termination resistors using a daughter board installed in the place of the 40 Hz filter. This allows a current signal to be terminated to ground. The voltage developed across a resistor is read by the VMIVME-3124. The optional -2BC board provides resistors value at 250 Ω ±0.01%. The optional -3BC board provides resistors value at 500 Ω ±0.01%. To support this option the 5 kHz low pass filter is not installed at the factory, all other functionality of the board remains the same.

NOTE:

THE OPTIONAL -2BC AND -3BC BOARDS ARE CONFIGURED FOR 32-CHANNEL SINGLE-ENDED MODE ONLY. DIFFERENTIAL INPUTS ARE NOT SUPPORTED.

3.7 PROGRAMMABLE GAIN INSTRUMENTATION AMPLIFIER

Once an input channel has been selected and routed through the input multiplexers, it enters the PGA as a differential input. The differential amplifier rejects common mode noise and delivers a scaled, single-ended output to the ADC. The PGA can be hardware jumpered for gains of 1, 10, and 100. This allows for inputs as low as ±50 mV up to ±10 VDC in range. There is no increase in acquisition time for any change in the gain setting.

3.8 CHANNEL SEQUENCER AND DUAL-PORTED RAM MEMORY

The VMIVME-3124 is normally operated in the scanning mode. When the board is powered up or reset, conversions start immediately. Once the A/D conversion is completed, the Dual-Port control logic takes the converted data and stores it in the channel's appropriate Dual-Port register. The channel counter is incremented by one, which selects the next channel to be multiplexed to the ADC. After selecting the next channel, a new A/D conversion sequence is initiated. When all input channels have been converted and stored (16 or 32), the channel counter is reset and the channel scanning sequence is started again.

The Stop Auto Scan bit in the Control/Status Register may be set to halt the channel sequencer at its current address. This address may be read from the Channel Pointer Register. This feature allows the controlling software to lock onto a channel and digitize it at the maximum rate of 40 kHz. Please note that the desired channel can not be directly set. The software must wait for the desired channel to appear in the Channel Pointer register. It then sets the Stop Auto Scan bit within 25 μsec.

3.9 BOARD ID REGISTER

The first location in the VMIVME-3124 register set is a read-only Board ID Register. It always reads $30. Other VMIC products have similar registers which read different constants. This allows general-purpose system software to automatically determine any installed boards.

3.10 BUILT-IN POWER CONVERTER AND ADC POWER SUPPLY

Electrical power for the VMIVME-3124 analog circuitry is supplied by an on-board DC-to-DC converter. The converter transforms +5 VDC power from the VMEbus into a regulated ±15 VDC power. The VMIVME-3124 does not require any 12 VDC from the VMEbus.

The ADC's +5 VDC logic power is provided by an on-board voltage regulator. Some of the +15 VDC from the DC-to-DC converter’s output is used as the input voltage to this regulator.

SECTION 4

PROGRAMMING

4.1 MEMORY MAP

The VMIVME-3124 occupies 128-bytes of addressing space including four information and control registers plus the conversion data registers. Tables 4.1-1 through 4.1-3 map this addressing space relative to the base address as set by configuration jumpers (see Section 5 for details concerning setting the base address and address modifier jumpers).

The appropriate table is determined by two factors: whether the board is jumpered for single-ended or differential inputs, and whether the user has selected the normal or maximum data buffer for differential inputs. If the board is jumpered for differential inputs and the Max Buffer bit in the Control/Status Register is clear, Table 4.1-1 applies. If the board is jumpered for differential inputs and the Max Buffer bit is set, Table 4.1-2 applies. If the board is jumpered for single-ended inputs, Table 4.1-3 is the only map that applies (see Section 5 for details concerning setting the input configuration jumpers).

Table 4.1-1. VMIVME-3124 Memory Map: Differential Inputs, Normal Buffer

Offset Address	Function	Width	Access
$00	Board ID Register	byte	read-only
$01	Configuration Register	byte	read-only
$02	Control/Status Register	byte	read/write
$03	Channel Pointer Register	byte	read-only
$04-$3F	Reserved		
$40	Channel 0 Data	word	read/(write)
$42	Channel 1 Data	word	read/(write)
$44	Channel 2 Data	word	read/(write)
$46	Channel 3 Data	word	read/(write)
$48	Channel 4 Data	word	read/(write)
$4A	Channel 5 Data	word	read/(write)
$4C	Channel 6 Data	word	read/(write)
$4E	Channel 7 Data	word	read/(write)
$50	Channel 8 Data	word	read/(write)
$52	Channel 9 Data	word	read/(write)
$54	Channel 10 Data	word	read/(write)
$56	Channel 11 Data	word	read/(write)
$58	Channel 12 Data	word	read/(write)
$5A	Channel 13 Data	word	read/(write)
$5C	Channel 14 Data	word	read/(write)
$5E	Channel 15 Data	word	read/(write)
$60-$7E	Reserved		

Table 4.1-2. VMIVME-3124 Memory Map: Differential Inputs, Maximum Buffer

Offset Address	Function	Width	Access
$00	Board ID Register	byte	read-only
$01	Configuration Register	byte	read-only
$02	Control/Status Register	byte	read/write
$03	Channel Pointer Register	byte	read-only
$04-$3F	Reserved		
$40	Channel 0 Data	word	read/(write)
$42	Channel 1 Data	word	read/(write)
$44	Channel 2 Data	word	read/(write)
$46	Channel 3 Data	word	read/(write)
$48	Channel 4 Data	word	read/(write)
$4A	Channel 5 Data	word	read/(write)
$4C	Channel 6 Data	word	read/(write)
$4E	Channel 7 Data	word	read/(write)
$50	Channel 8 Data	word	read/(write)
$52	Channel 9 Data	word	read/(write)
$54	Channel 10 Data	word	read/(write)
$56	Channel 11 Data	word	read/(write)
$58	Channel 12 Data	word	read/(write)
$5A	Channel 13 Data	word	read/(write)
$5C	Channel 14 Data	word	read/(write)
$5E	Channel 15 Data	word	read/(write)
$60	Channel 0 Data	word	read/(write)
$62	Channel 1 Data	word	read/(write)
$64	Channel 2 Data	word	read/(write)
$66	Channel 3 Data	word	read/(write)
$68	Channel 4 Data	word	read/(write)
$6A	Channel 5 Data	word	read/(write)
$6C	Channel 6 Data	word	read/(write)
$6E	Channel 7 Data	word	read/(write)
$70	Channel 8 Data	word	read/(write)
$72	Channel 9 Data	word	read/(write)
$74	Channel 10 Data	word	read/(write)
$76	Channel 11 Data	word	read/(write)
$78	Channel 12 Data	word	read/(write)
$7A	Channel 13 Data	word	read/(write)
$7C	Channel 14 Data	word	read/(write)
$7E	Channel 15 Data	word	read/(write)

Table 4.1-3. VMIVME-3124 Memory Map: Single-Ended Inputs

Offset Address	Function	Width	Access
$00	Board ID Register	byte	read-only
$01	Configuration Register	byte	read-only
$02	Control/Status Register	byte	read/write
$03	Channel Pointer Register	byte	read-only
$04-$3F	Reserved		
$40	Channel 0 Data	word	read/(write)
$42	Channel 1 Data	word	read/(write)
$44	Channel 2 Data	word	read/(write)
$46	Channel 3 Data	word	read/(write)
$48	Channel 4 Data	word	read/(write)
$4A	Channel 5 Data	word	read/(write)
$4C	Channel 6 Data	word	read/(write)
$4E	Channel 7 Data	word	read/(write)
$50	Channel 8 Data	word	read/(write)
$52	Channel 9 Data	word	read/(write)
$54	Channel 10 Data	word	read/(write)
$56	Channel 11 Data	word	read/(write)
$58	Channel 12 Data	word	read/(write)
$5A	Channel 13 Data	word	read/(write)
$5C	Channel 14 Data	word	read/(write)
$5E	Channel 15 Data	word	read/(write)
$60	Channel 16 Data	word	read/(write)
$62	Channel 17 Data	word	read/(write)
$64	Channel 18 Data	word	read/(write)
$66	Channel 19 Data	word	read/(write)
$68	Channel 20 Data	word	read/(write)
$6A	Channel 21 Data	word	read/(write)
$6C	Channel 22 Data	word	read/(write)
$6E	Channel 23 Data	word	read/(write)
$70	Channel 24 Data	word	read/(write)
$72	Channel 25 Data	word	read/(write)
$74	Channel 26 Data	word	read/(write)
$76	Channel 27 Data	word	read/(write)
$78	Channel 28 Data	word	read/(write)
$7A	Channel 29 Data	word	read/(write)
$7C	Channel 30 Data	word	read/(write)
$7E	Channel 31 Data	word	read/(write)

4.2 REGISTER DESCRIPTIONS

The VMIVME-3124 control registers are all byte-wide registers, while the data registers are all 16-bits wide. The control registers are also accessed as 16-bit word, in which case two successive registers are accessed.

NOTE:

All bits documented as "Reserved" will read as zero and, if written, must always be zero.

4.2.1 Board ID Register

The Board ID Register is an 8-bit read only register at offset $00 with a constant value set to $30 for the VMIVME-3124. This ID number uniquely identifies the board from other VMIC products.

4.2.2 Board Configuration Register

The Configuration Register is an 8-bit read-only register at offset $01 that indicates the current configuration of the VMIVME-3124 board. It contains two bits of configuration status information, each determined by the state of jumpers on the board. See Table 4.2.2-1 for the definition of these bits. The Input Mode bit indicating single-ended or differential operation is controlled by a jumper shunt and may be set as desired (see Section 5 for details) Note that the 40 Hz bit indicating analog input filter bandwidth is determined automatically on the VMIVME-3124 by the presence or absence of the 40 Hz optional daughter board.

Table 4.2.2-1. Board Configuration Register Contents

Bit Position	Bit Name	Function
0	Input Mode	0 = 16 Differential Inputs 1 = 32 Single-Ended Inputs
1	40 Hz	0 = 50 kHz Input Filters 1 = 40 Hz Input Filters
2-7		Reserved

NOTE:

FOR THE -2BC AND -3BC CURRENT INPUT OPTIONS, THE BIT POSITIONS ARE SHOWN AS FOLLOWS:

- Bit Position 1 = 0, indicating the current termination resistor board is not installed.
- Bit Position 1 = 1, indicating the termination board is installed.

4.2.3 Control/Status Register

The Board Control/Status register is an 8-bit read/write register at offset $02 that allows software to control the VMIVME-3124 and also indicates its current status. Seven of the eight bits provide control and indication functions. Table 4.2.3-1 defines the contents of this register.

Table 4.2.3-1. Board Control/Status Register Contents

Bit Position	Bit Name	Function
0	Stop Auto Scan	0 = Scan All Channels (Default) 1 = Scan Single Channel
1	Max Buffer	0 = 16 Differential Data Registers (Default) 1 = 32 Differential Data Registers
2	2's Complement	0 = Binary Data (Default) 1 = two's complement Data
3	Mode 0	Channel 0 BIT Mode 0
4	Mode 1	Channel 0 BIT Mode 1
5	Mode 2	Channel 0 BIT Mode 2
6		Reserved
7	LED Off	0 = Board LED On (Default) 1 = Board LED Off

Normally, the VMIVME-3124 automatically scans all input channels, continually converting each successive input. The user may set the Stop Auto Scan bit; however, to cause the VMIVME-3124 to stop on a single channel. If the Stop Auto Scan bit is set, only the Data Register pointed to by the Channel Pointer Register is updated, although it will be updated much faster than usual – approximately every 25 μsec. The best way to stop on a single desired channel is to observe the Channel Pointer Register while auto scanning. Then set the Stop Auto Scan bit within 25 μsec as soon as the desired channel appears. Auto-scanning proceeds from the current channel as soon as this bit is cleared again.

The Max Buffer bit is only significant when the hardware is configured for differential inputs, where it controls whether there are 16 Data Registers (one for each input) or 32 Data Registers (two for each input). The difference between these two scanning modes is discussed in detail in the Data Register description (Section 4.2.5). Tables 4.1-1 (Max Buffer clear) and 4.1-2 (Max Buffer set) detail the differences in the overall VMIVME-3124 memory map.

If the 2's Complement bit is set, all information in the Data Registers is in two's complement format. This data format is only useful when the inputs are configured as byplay. In this case, the two's complement data format causes the Data Registers to contain values already sign-extended. This saves the programmer from having to convert the data in the host code.

The three Mode bits determine the stimulus to channel 0, according to Table 4.2.3-2.

Table 4.2.3-2. Board Control/Status Register Modes

Mode 2	Mode 1	Mode 0	Channel 0 Stimulus
X	X	0	External Input (Default)
1	1	1	Internal 0.000 V Reference
1	0	1	Internal 9.915 mV Reference
0	1	1	Internal 492.8 mV Reference
0	0	1	Internal 4.980 V Reference

The LED Off bit is self-explanatory. Note that the LED is ON by default and should normally be turned off after power-up or reset by the host software. The LED can thus be used to visually verify that the board has been initialized.

4.2.4 Channel Pointer Register

The Channel Pointer Register is an eight-bit read-only register at offset $03. Under most circumstances, the Channel Pointer Register holds the channel number of the current input being sampled and converted by the VMIVME-3124. The only exception occurs when the board is configured for differential input and the Max Buffer bit in the Control/Status Register is set. In this case, two data pages get updated and each input is converted in two separate passes. The Channel Pointer Register can be used to determine which of the two Data Registers has been most recently updated. The address offset of the Data Register being converted is calculated as follows:

(Channel Pointer Register value X 2) + $40 = Offset Address of Current Data Register

Note that the corresponding channel number is the Channel Pointer Register value modulo 16. Also note that the value in this register represents the current channel under conversion. Decrement the value by one (modulo 16 for differential inputs or 32 for single-ended inputs) to determine the location of the most recently completed channel data.

4.2.5 Data Registers

There are either 16 or 32 Data Registers beginning at offset $40, depending on the condition of the Max Buffer bit. Each Data Register contains 12-bits of conversion data for its associated channel. The data is right-justified within each 16-bit Data Register. Each register should generally be treated as read-only, and each should be accessed as a 16-bit word. The hardware does not restrict the user from accessing the Data Registers via two consecutive byte reads, **although this is not**

recommended. When accessing the Data Registers as bytes, it is possible for the value in the Data Register to be updated *between* byte reads, potentially scrambling the data. Section 4.5 provides methods to avoid scrambled byte data reads.

The data is a linear binary representation of the input voltage on the corresponding channel at the time of the most recent conversion. The LSB weight (that is, the voltage value corresponding to a single bit of data) depends on the input voltage range, which in turn depends on the range and gain jumper configuration (see Section 5 for details). Calculate the LSB weight by dividing the full-scale range by 4096. For example, the LSB weight for a VMIVME-3124 configured for ±10 V at unity gain would be 4.883 mV (20/4096). Table 4.2.5-1 lists the LSB weights for all possible VMIVME-3124 configurations.

Table 4.2.5-1 LSB Weight

	LSB Weight		
Voltage Range	**Gain x1**	**Gain x10**	**Gain x100**
±5 V	2.441 mV	.2441 mV	24.41 μV
±10 V	4.883 mV	.4883 mV	48.83 μV
0-10 V	2.441 mV	.2441 mV	24.41 μV

The voltage on any channel can be determined by multiplying the Data Register value by the appropriate LSB Weight from Table 4.2.5-1.

Two other values necessary to determine the meaning of the values in the Data Registers: the Channel Pointer Register and the Max Buffer bit, both previously described. The Channel Pointer Register holds the channel number of the Data Register currently being updated. Therefore, the most recent complete conversion data is for the channel one less than the value of the Channel Pointer Register (modulo 32 or 16, depending upon the number of active Data Registers). The Max Buffer bit in the Control/Status Register determines whether there are 16 or 32 active differential data registers. If the bit is set, all 32 registers are actively updated, but if the bit is clear, only the first 16 registers are updated.

If the board is configured for single-ended inputs (i.e. if the Single-Ended bit in the Configuration Register is set), then the Max Buffer bit is meaningless. In this configuration, the 32 Data Registers contain the data for channels 0-31 consecutively, beginning with channel 0 at offset $40.

If the board is configured for differential inputs (i.e., if the Single-Ended bit in the Configuration Register is clear), then the Max Buffer bit may be either set or cleared. The trade-off is between simplicity of access (Max Buffer bit clear; 16 Data Registers) and relaxed access requirements (Max Buffer bit set; 32 Data Registers).

By clearing the Max Buffer bit, only the first 16 Data Registers are updated. The updates correspond to channels 0-15 consecutively, beginning with channel 0 at offset $40. This is the simplest configuration, but it requires more bus overhead than desired if the user wishes to avoid constantly reading the board but still wants to capture every single data sample.

On the other hand, the user may wish to set the Max Buffer bit to increase the time interval by extending the aggregate sample time from just under 500 μsec to nearly a millisecond. By setting the Max Buffer bit, all 32 Data Registers are updated. Data for channels 0-15 is stored consecutively, first in the lowest 16 Data Registers (channel 0 data at offset $40), then in the higher 16 Data Registers (channel 0 data at offset $60). Using this technique, the two most recent scans are always available in the Data Registers. The Channel Pointer Register must be read to determine which of the two data sets is most recent. In this case, the Channel Pointer Register value does not hold a channel number, but an offset value into the extended data buffer. The code must still be structured such that the previously updated data is read prior to being overwritten by new data.

Note that the Data Registers are actually writable. Since the registers physically consist of RAM, writes are allowed to facilitate testing of the data RAM. Unless auto-scanning is halted, any data written to a Data Register is overwritten with new data the next time that channel is scanned and converted.

4.3 BUILT-IN-TEST FUNCTIONS

The VMIVME-3124 has the ability to test its functionality by applying various internal reference voltages to the channel 0 input. Host software may then read the value for channel 0 and compare it to its predicted quantity. Tables 4.3-1 through 4.3-3 show all possible BIT values.

Table 4.3-1. BIT Values for 0-10V Range

	Gain Setting		
BIT Voltage	**X 1**	**X 10**	**X 100**
0.000 V	$0000	$0000	$0000
9.915 mV	$0004	$0028	$0196
492.8 mV	$00C9	$07E2	$0FFF
4.980 V	$07F8	$0FFF	$0FFF

Table 4.3-2. BIT Values for ±5 V Range

BIT Voltage	Gain Setting X 1	X 10	X 100
0.000 V	$0800	$0800	$0800
9.915 mV	$0804	$0828	$0996
492.8 mV	$08C9	$0FE2	$0FFF
4.980 V	$0FF8	$0FFF	$0FFF

Table 4.3-3. BIT Values for ±10 V Range

BIT Voltage	Gain Setting X 1	X 10	X 100
0.000 V	$0800	$0800	$0800
9.915 mV	$0802	$0814	$08CB
492.8 mV	$0864	$0BF1	$0FFF
4.980 V	$0BFB	$0FFF	$0FFF

Of course, these tables assume precisely calibrated BIT reference voltages. Check the specification for exact tolerances of these voltages. Note also that these tables assume pure binary data. The 2's complement bit in the Control/Status Register must be clear. Any value of $0FFF indicates an over-voltage condition.

4.4 RANGE AND GAIN DETERMINATION

While the VMIVME-3124 analog gain and range may be set by the user, there is no direct way to read these settings in software (see Section 5 for hardware gain and range configuration). Software applies a BIT voltage stimulus and attempt to determine the current gain and range settings by comparing the data to the values in Tables 4.3-1 through 4.3-3. This technique is not recommended; however, since the board must be calibrated to a single gain and range setting.

4.5 ACCESSING DATA AS BYTES

As stated in the Data Register description (Section 4.2.5), the Data Registers should generally be accessed using single 16-bit word transfers. it is possible to access a Data Register using two successive byte transfers, although there are risks involved. The data as interpreted by the host may be completely scrambled if the VMIVME-3124 updates the Data Register in between the two byte accesses. There are two methods to avoid this:

One method uses the Halt bit in the Control/Status Register to temporarily suspend automatic scanning while the two bytes are being read. Valid data can be guaranteed by carefully monitoring the Channel Pointer Register to avoid accessing channel data currently being converted or data about to be converted and by temporarily stopping all conversions with the Halt bit in the Control/Status Register.

Once scanning is halted, any Data Register may be safely read as bytes except for the Data Register pointed to by the Channel Pointer Register. Drawbacks to this method is that it is inherently slow and the programmer loses a regular time reference. The clock is stopped while the Halt bit is set (that is, the data is frozen for all channels except the one pointed to by the Channel Pointer Register, whose input gets converted constantly).

The other method to read the Data Registers as bytes, avoids interrupting the regular automatic scanning process and thus preserves the conversion frequency of all channels. This method requires the programmer to structure the code so the two-byte accesses are guaranteed to be consecutive and uninterrupted. The Channel Pointer Register must still be monitored and interrupts disabled to avoid accessing a Data Register while the data is being updated preferably one should access a channel immediately after it has been updated. Interrupts should always be disabled before accessing a Data Register to avoid the possibility of a long interrupt service routine coming between the two-byte accesses.

Of course, there are no problems if the Data Registers are accessed as a single word, as recommended. For reference, however, the MSB of the data is in the lower byte address while the LSB is in the higher byte address.

4.6 CURRENT INPUT -2BC AND -3BC OPTIONS

The -2BC option provides the current signal a 250 Ω ±0.01%, path to ground. The -3BC option provides the current signal a 500 Ω ±0.01%, path to ground.

Table 4.6-1 shows the voltages seen by the ADC:

Table 4.6-1. Voltages Seen by the ADC

Current Range (mA)	Termination Resistor	ADC Voltage Input (V_{ADC})
0 - 25	250	0 - 6.25 VDC
0 - 25	500	Not Recommended
0 -20	250	0 - 5 VDC
0 - 20	500	0 - 10 VDC
4 - 20	250	1 - 5 VDC
4 - 20	500	2 - 10 VDC
5 - 25	250	1.25 - 6.25 VDC
5 - 25	500	Not Recommended

Use the formula: $I = \frac{V_{ADC}}{R_{TERMINATION}}$

to convert the ADC readings to the actual current signal.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

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**********
*  CAUTION  *
**********
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SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

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**********
*  CAUTION  *
**********
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DO NOT INSTALL OR REMOVE BOARD WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 JUMPER INSTALLATIONS

Figure 5.3-1 identifies the location of configuration jumpers and calibration potentiometers for the VMIVME-3124. Jumpers E1 through E9 are address jumpers which must be set to the desired base address of the board as described in Section 5.3.1. Jumper E10 controls the VMEbus access mode, either supervisory or nonprivileged; refer to Section 5.3.2. The remaining jumpers must be set according to Section 5.3.3 to configure the board's analog inputs.

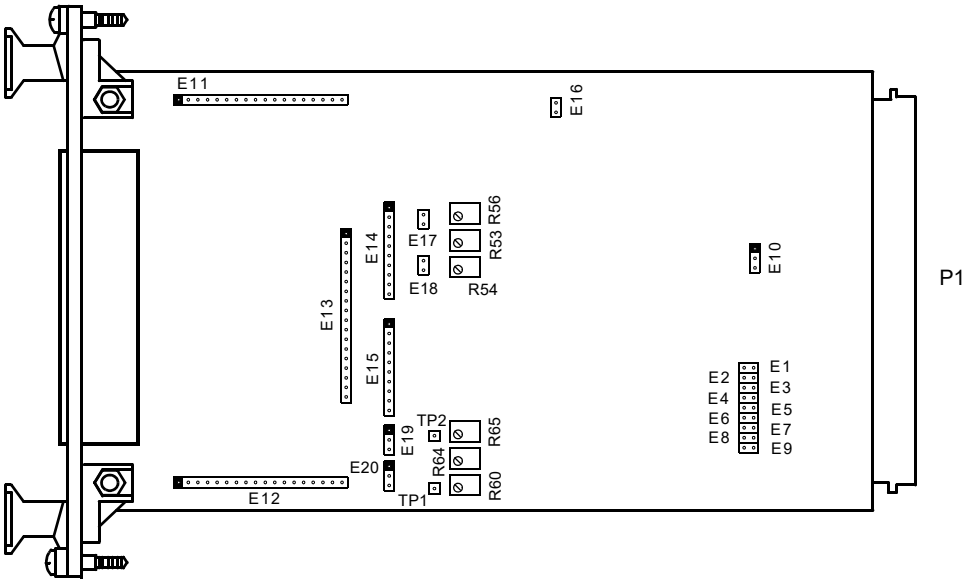


Figure 5.3-1. VMIVME-3124 Configuration Jumper Locations

5.3.1 Board Address

The VMIVME-3124 occupies 128 contiguous bytes of short I/O address space (see Section 4 for register details). The base address is controlled by jumpers E1 through E9 according to Table 5.3.1-1. Each installed jumper corresponds to a binary 0, while each uninstalled jumper corresponds to a binary 1. For base address calculation, note that address bits A0 through A6 are assumed to be zero. The factory default address is at short I/O $0000 (all jumpers installed).

Table 5.3.1-1. Address Selection Jumpers

Short I/O Address Bit	Jumper # (installed=0 removed=1)
A15	E1*
A14	E6*
A13	E7*
A12	E8*
A11	E9*
A10	E2*
A9	E3*
A8	E4*
A7	E5*
* installed for factory default address of $0000	

To change the address, first determine the new address in hexadecimal (note that the address must be an even multiple of 128 decimal, or $80). Convert the address to binary and assign the address bits A0 through A15 to the binary address, starting from the least significant bit. Then check Table 5.3.1-1. All clear bits should have a jumper installed on the corresponding address bit jumper, and all set bits should have a jumper removed.

For example, assume a target address of $3A00 is desired. In binary, that number is %0011 1010 0000 0000. Assigning address bits to these shows that only bits A13, A12, A11, and A9 are set. Check Table 5.3.1-1. All jumpers should be installed (for the clear address bits) except for jumpers E7, E8, E9, and E3 (for the set address bits).

5.3.2 Address Modifier

Jumper E10 determines whether the VMIVME-3124 responds to supervisory or nonprivileged accesses according to Table 5.3.2-1.

Table 5.3.2-1. Address Modifier Jumper Settings

Short I/O Addressing Mode	Jumper E10 Setting
Supervisory	1&2
Nonprivileged	2&3
Both	no jumper

5.3.3 Input Configuration

Three jumpers (E14, E15, and E16) are used to configure the VMIVME-3124 for single-ended or differential inputs. Two jumpers (E19 and E20) control the input voltage range, and two jumpers (E18 and E17) control the amount of gain. The jumpers are shown in Table 5.3.3-1 below. The factory default configuration is single-ended, ±10 V range, and unity gain.

Table 5.3.3-1. Input Configuration Jumpers

Input Configuration Option		Jumper Configuration
MODE	Single-ended inputs*	Install jumpers E14†, E15†; remove E16
	Differential inputs	Remove jumpers E14, E15; install E16
RANGE	±10 V range*	Install jumpers E19 pins 1&2; E20 pins 2&3
	±5 V range	Install jumpers E19 pins 1&2; E20 pins 1&2
	0-10 V range	Install jumpers E19 pins 2&3; E20 pins 1&2
GAIN	unity gain*	Remove jumpers E18 and E17
	X10 gain	Remove jumper E18; install jumper E17
	X100 gain	Install jumper E18; remove jumper E17
* indicates factory default		†note that E14 and E15 must be jumpered with a "zero ohm" SIP pack (included)

Note that the board comes factory configured for either 50 kHz input filters or 40 Hz input filters, depending on the ordering option. If the 40 Hz input filter option is ordered, a daughter board is factory installed into sockets E11, E12, and E13. If the 50 kHz input filter option is ordered, no daughter board is installed and sockets E11, E12, and E13 remain empty.

For the -2BC and -3BC current input options configure the VMIVME-3124 as follows:

- Single-Ended 32 channels
- 0 - 10 VDC range
- Unity Gain

5.4 ANALOG INPUT CONNECTOR DESCRIPTION

The 16 differential or 32 single-ended analog input connections to the VMIVME-3124 board are made using the front panel 37-pin D connector labelled P3. See Figure 5.4-1 and Table 5.4-1 below for connector pin and signal assignments.

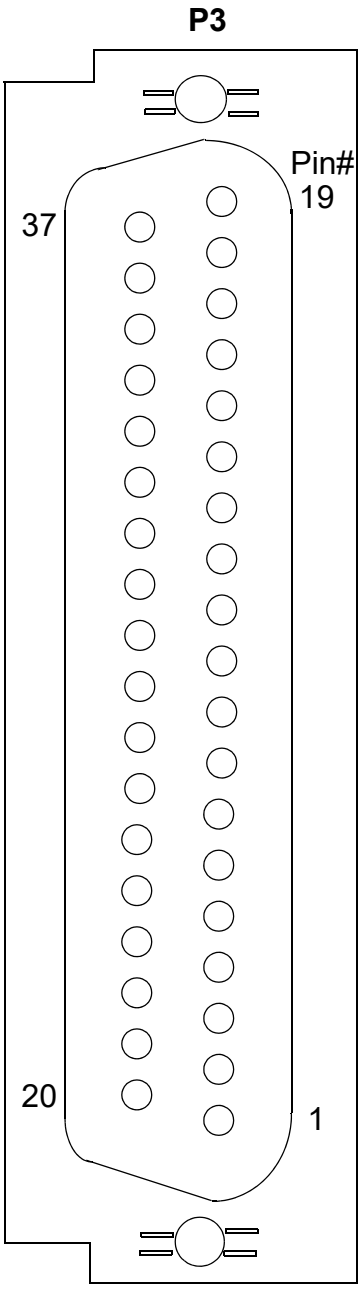


Figure 5.4-1. P3 Connector

Table 5.4-1. P3 Analog Connector Pinout

Pin #	Single-Ended Signal	Differential Signal
1	Analog Ground CH 24-31 LO	Analog Ground
2	CH30-HI	CH15-HI
3	CH28-HI	CH14-HI
4	CH26-HI	CH13-HI
5	CH24-HI	CH12-HI
6	CH23-HI	CH11-LO
7	CH21-HI	CH10-LO
8	CH19-HI	CH09-LO
9	CH17-HI	CH08-LO
10	Analog Ground CH 08-15 LO	Analog Ground
11	CH14-HI	CH07-HI
12	CH12-HI	CH06-HI
13	CH10-HI	CH05-HI
14	CH08-HI	CH04-HI
15	CH07-HI	CH03-LO
16	CH05-HI	CH02-LO
17	CH03-HI	CH01-LO
18	CH01-HI	CH00-LO
19	Analog Ground	Analog Ground
20	CH31-HI	CH15-LO
21	CH29-HI	CH14-LO
22	CH27-HI	CH13-LO
23	CH25-HI	CH12-LO
24	Analog Ground CH 16-23 LO	Analog Ground
25	CH22-HI	CH11-HI
26	CH20-HI	CH10-HI
27	CH18-HI	CH09-HI
28	CH16-HI	CH08-HI
29	CH15-HI	CH07-LO
30	CH13-HI	CH06-LO
31	CH11-HI	CH05-LO
32	CH09-HI	CH04-LO
33	Analog Ground CH 00-07 LO	Analog Ground
34	CH06-HI	CH03-HI
35	CH04-HI	CH02-HI
36	CH02-HI	CH01-HI
37	CH00-HI	CH00-HI

5.5 CALIBRATION PROCEDURES

To obtain the specified accuracy for analog measurements, the VMIVME-3124 must be calibrated for the range used. For greatest possible accuracy, VMIC recommends calibrating the board after it has been installed in its target chassis and after power has been applied for at least a half hour.

Always run the Instrumentation Amp Offset Calibration procedure first. Afterwards, select the offset and gain calibration procedure corresponding to the selected range. The BIT reference voltages should always be calibrated last. See Figure 5.3-1 for the locations of test points and user-adjustable potentiometers.

5.5.1 Equipment Required

a. 4-digit Digital Voltmeter (DVM)
b. Precision Voltage Reference

5.5.2 Instrumentation Amp Offset Calibration

a. Configure the board for differential unipolar 0-10 V range, X100 gain:
   Install jumpers E18, E19 pins 2 and 3, E20 pins 1 and 2, E16
   Remove jumpers E14, E15, E17
b. If this is the first run through the procedure, center potentiometer R53.
c. Attach DVM positive to ADC input at TP1; attach negative to analog ground at TP2.
d. Short the channel 0 input HI and LO inputs.
e. Halt scanning on channel 0.
f. Adjust input offset potentiometer R54 until DVM reads as near 0.000 mVDC as possible (acceptable range is 0.0 mV-0.7 mV).
g. Remove jumper E18 for unity gain.
h. Adjust output offset potentiometer R53 until DVM reads as near 0.000 VDC as possible (acceptable range is 0.0 mV-0.2 mV).
i. Repeat this procedure at least once.

5.5.3 Unipolar 0-10 V Offset and Gain Calibration

NOTE:

Run this calibration procedure only if the board is to remain in the unipolar configuration with 0-10 V range.

a. Configure the board for single-ended unipolar 0-10 V range, unity gain:
   Install jumpers E14, E15, E19 pins 2 and 3, E20 pins 1 and 2
   Remove jumpers E18, E17, E16
b. Connect precision voltage source to channel 0 input.
c. Adjust precision voltage source to +1.221 mVDC.

NOTE:

FOLLOW THE STEPS IN SECTION 5.5.3 FOR THE -2BC AND -3BC CURRENT INPUT OPTIONS. REMOVE THE -0158 TERMINATION BOARD DURING CALIBRATION. REINSTALL WHEN CALIBRATION IS COMPLETE. THE BOARD SHOULD BE IN THE SINGLE-ENDED, 0-10 VDC RANGE, WITH A GAIN OF X1.

d. Halt scanning on channel 0 and monitor channel 0 data.
e. Adjust unipolar offset potentiometer R60 until channel 0 data fluctuates between $000 and $001.
f. Connect precision voltage source to channel 0 input.
g. Adjust precision voltage source to +9.996338 VDC.
h. Adjust gain potentiometer R65 until channel 0 data fluctuates between $FFE and $FFF.
i. Change mode and gain jumpers as necessary for your final configuration.

5.5.4 Bipolar ±5 V Offset and Gain Calibration

NOTE:

Run this calibration procedure only if the board is to remain in the bipolar configuration with ±5 V range.

a. Configure the board for single-ended bipolar ±5 V range, unity gain:
   Install jumpers E14, E15, E19 pins 1 & 2, E20 pins 1 & 2
   Remove jumpers E18, E17, E16
b. Connect precision voltage source to channel 0 input.
c. Adjust precision voltage source to -4.998779 VDC.
d. Halt scanning on channel 0 and monitor channel 0 data.
e. Adjust bipolar offset potentiometer R64 until channel 0 data fluctuates between $000 and $001.
f. Adjust precision voltage source to +4.996338 VDC.
g. Adjust gain potentiometer R65 until channel 0 data fluctuates between $FFE and $FFF.
h. Change mode and gain jumpers as necessary for your final configuration.

5.5.5 Bipolar ±10 V Offset and Gain Calibration

NOTE:

Run this calibration procedure only if the board is to remain in the bipolar configuration with ±10 V range.

a. Configure the board for single-ended bipolar ±10 V range, unity gain:
   Install jumpers E14, E15, E19 pins 1 and 2, E20 pins 2 and 3
   Remove jumpers E18, E17, E16
b. Connect precision voltage source to channel 0 input.
c. Adjust precision voltage source to -9.997559 VDC.
d. Halt scanning on channel 0 and monitor channel 0 data.
e. Adjust bipolar offset potentiometer R64 until channel 0 data fluctuates between $000 and $001.
f. Adjust precision voltage source to +9.992676 VDC.
g. Adjust gain potentiometer R65 until channel 0 data fluctuates between $FFE and $FFF.

h. Change mode and gain jumpers as necessary for your final configuration.

5.5.6 Built In Test Voltage Calibration

NOTE:

Run this calibration procedure only after the instrumentation amp and appropriate offset and gain calibration procedures.

a. Attach DVM positive to ADC input at TP1; attach negative to analog ground at TP2.
b. Halt scanning on channel 0.
c. Apply the 4.980 V BIT voltage to channel 0 by writing the appropriate value to the mode bits in the Control/Status Register.
d. Adjust R56 until DVM reads 4.980 VDC.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

6.2 MAINTENANCE PRINTS

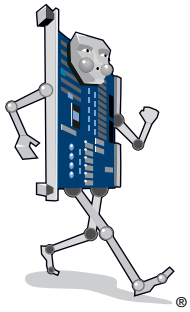
User level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

ACKNOWLEDGEMENTS

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APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

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