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VMIVME-4800

ISOLATED 8-CHANNEL 12-bit ANALOG OUTPUT BOARD WITH VOLTAGE OR CURRENT LOOP OUTPUTS

PRODUCT MANUAL

DOCUMENT NO. 500-004800-000 REV. B

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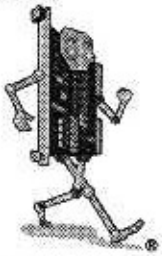
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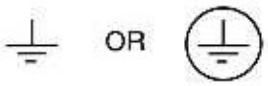
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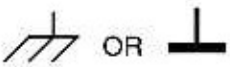
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Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

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The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition, or the like, which is essential to highlight.

VMIVME-4800

ISOLATED 8-CHANNEL 12-bit ANALOG OUTPUT BOARD WITH VOLTAGE OR CURRENT LOOP OUTPUTS

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A Assembly Drawing, Parts List, and Schematic

SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-4800 is a 12-bit Analog Output Board which provides 8 isolated high quality 12-bit analog output channels on a single 6U form factor VMEbus board. Each channel is electrically isolated from all other channels and from the VMEbus.

Listed below are some features of the VMIVME-4800 :

a. Eight fully isolated analog outputs
b. 1,500 Vpk isolation, channel-to-channel and channel-to-bus
c. 12-bit resolution
d. Bipolar voltage output ranges selectable as ±2.5, ±5, or ±10 V
e. Unipolar voltage output ranges selectable as 0 to 2.5 V, 0 to 5 V, or 0 to 10 V
f. 10 mA load capacity for voltage outputs over full ±10 V range
g. Available with 4 to 20, 0 to 20, or 5 to 25 mA current loop outputs
h. 0.05 percent accuracy for voltage outputs, 0.08 percent for current loop outputs
i. Four or eight-channel options
j. Optical data coupling provides full galvanic isolation
k. Static readback data registers simplify program control
l. Front panel access for field connections
m. Program-controlled connect/disconnect operation of voltage outputs facilitates system testing

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-4800 internal organization is illustrated in the functional block diagram shown in Figure 1.2-1 on page 1-2. The board will operate with sustained isolation voltages as high as 1,500 Vpk. Bipolar output voltage ranges are selectable as ±2.5 V, ±5 V, or ±10 V. Unipolar output voltage ranges are selectable as 0 to 2.5 V, 0 to 5 V, or 0 to 10 V, and full 10 mA loading is supported throughout these ranges. Four or 8 channel configurations are available.

Voltage outputs may be disconnected under program control during system testing, and are disconnected automatically during reset. Optional current-mode outputs support applications that require standard 4 to 20 mA, 0 to 20 mA, or 5 to 25 mA analog current loops. Compliance of the current mode outputs is 9 V if the loop supply originates on the board, or 27 V with an external loop power supply. A front panel LED (Fail) is provided. The LED is illuminated during power up or system reset and can be turned OFF under user software control.

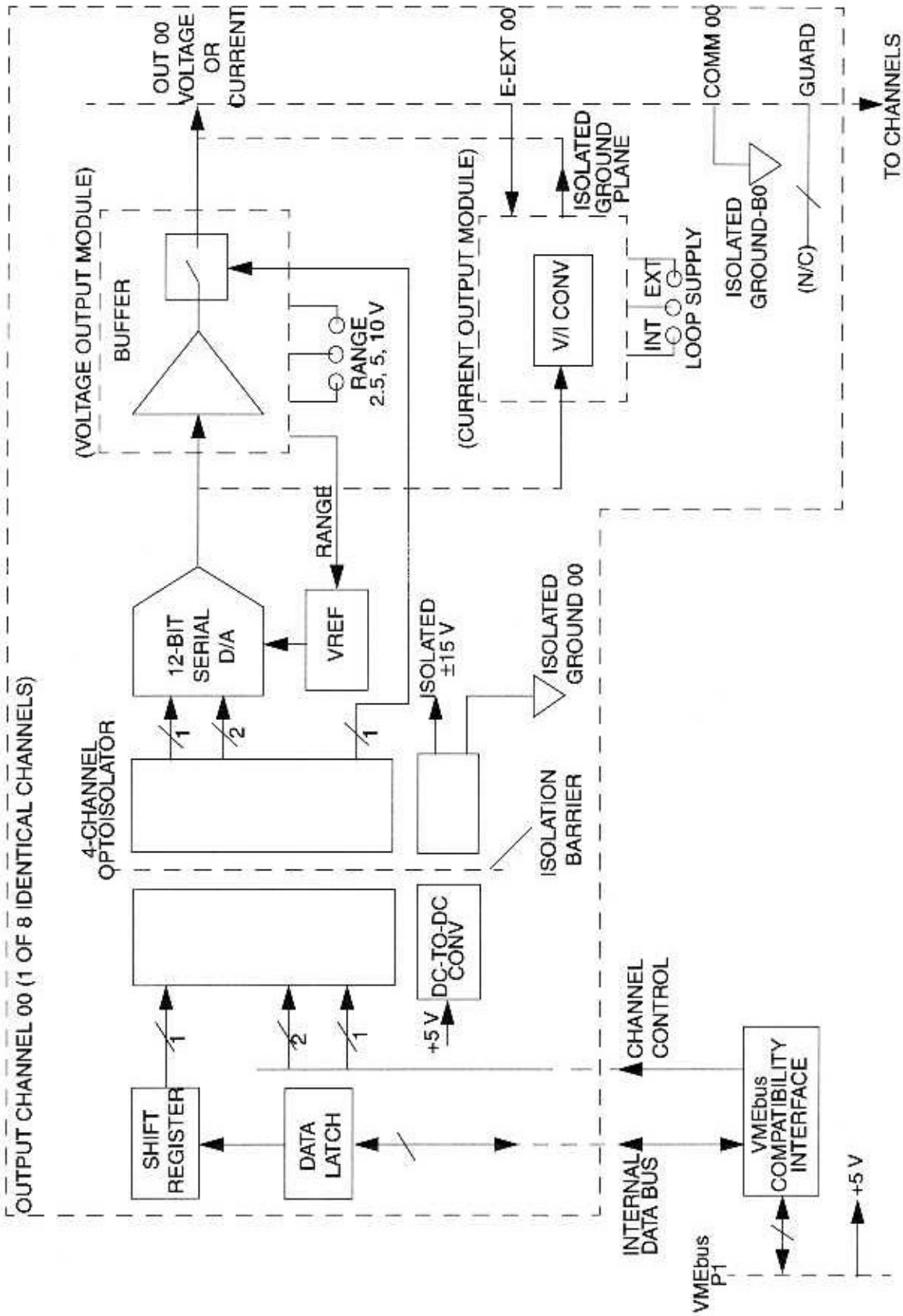


Figure 1.2-1. VMIVME-4800 Functional Block Diagram

1.3 REFERENCE MATERIAL LIST

For a detailed explanation of the VMEbus and its characteristics, the publication "The VMEbus Specification" is available from:

VITA

VFEA International Trade Association

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Scottsdale, AZ 85253

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The following Application and Configuration Guides are available from VMIC to assist in the selection, specification, and implementation of systems based upon VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-In-Test) Product Line Description	825-000000-003
Synchro/Resolver (Built-In-Test) Subsystem Configuration Guide	825-000000-004
Analog I/O Products (with Built-In-Test) Configuration Guide	825-000000-005
Connector and I/O Cable Application Guide	825-000000-006

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-004800-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

Optical data coupling, serial data transfers, and isolated Digital-to-Analog Converters (DACs) are used to produce eight galvanically isolated analog output channels. Each channel contains a serial 12-bit DAC which generates a signal voltage in response to commands from the VMEbus. The DAC voltage then drives an output module which is factory configured for a specific voltage or current output option. Power for each channel is supplied as ±15 VDC by an isolated DC-to-DC converter. A functional block diagram of the VMIVME-4800 board is shown in Figure 1.2-1 on page 1-2.

3.2 INTERNAL FUNCTIONAL ORGANIZATION

The VMIVME-4800 board consists of the following functional elements, all of which are described in the following sections:

a. VMEbus interface
b. Channel control logic
c. Isolated analog outputs
d. DC/DC power converters.

3.3 VMEbus INTERFACE

Communications with the VMEbus is controlled with a single Electrically Programmable Logic Device (EPLD), as shown in Figure 3.3-1 on page 3-2. Data and control registers are distributed among two channel-control EPLD's. The control-logic EPLD responds to data transfer requests from the VMEbus, and directs the flow of data between the bus and the internal data and control registers. Data Transfer Acknowledge (DTACK*) is generated when a transfer from the bus has been completed, or when data is ready to be transferred to the bus. Transfers proceed normally if address pipelining is present, but the board will respond only to the first address in the pipeline sequence. The VMEbus interface logic will not respond to transfer requests in which the BERR*, DTACK*, LWORD*, or IACK* control line is asserted.

3.4 CHANNEL CONTROL LOGIC

Control of data transfer to the output DAC is partitioned into two identical 4 channel groups, with a single EPLD assigned to each group. This method of partitioning permits the board to be populated with only those devices required to support the 4 or 8 channel optional configuration.

As shown in Figure 3.3-1 on page 3-2, the EPLD which controls channels 00 through 03 also contains the Board Identification Register (BIR) and part of the Control/ Status register (CSR). This EPLD detects the presence of one or both of the channel-control EPLD, and adjusts the distribution of the CSR accordingly.

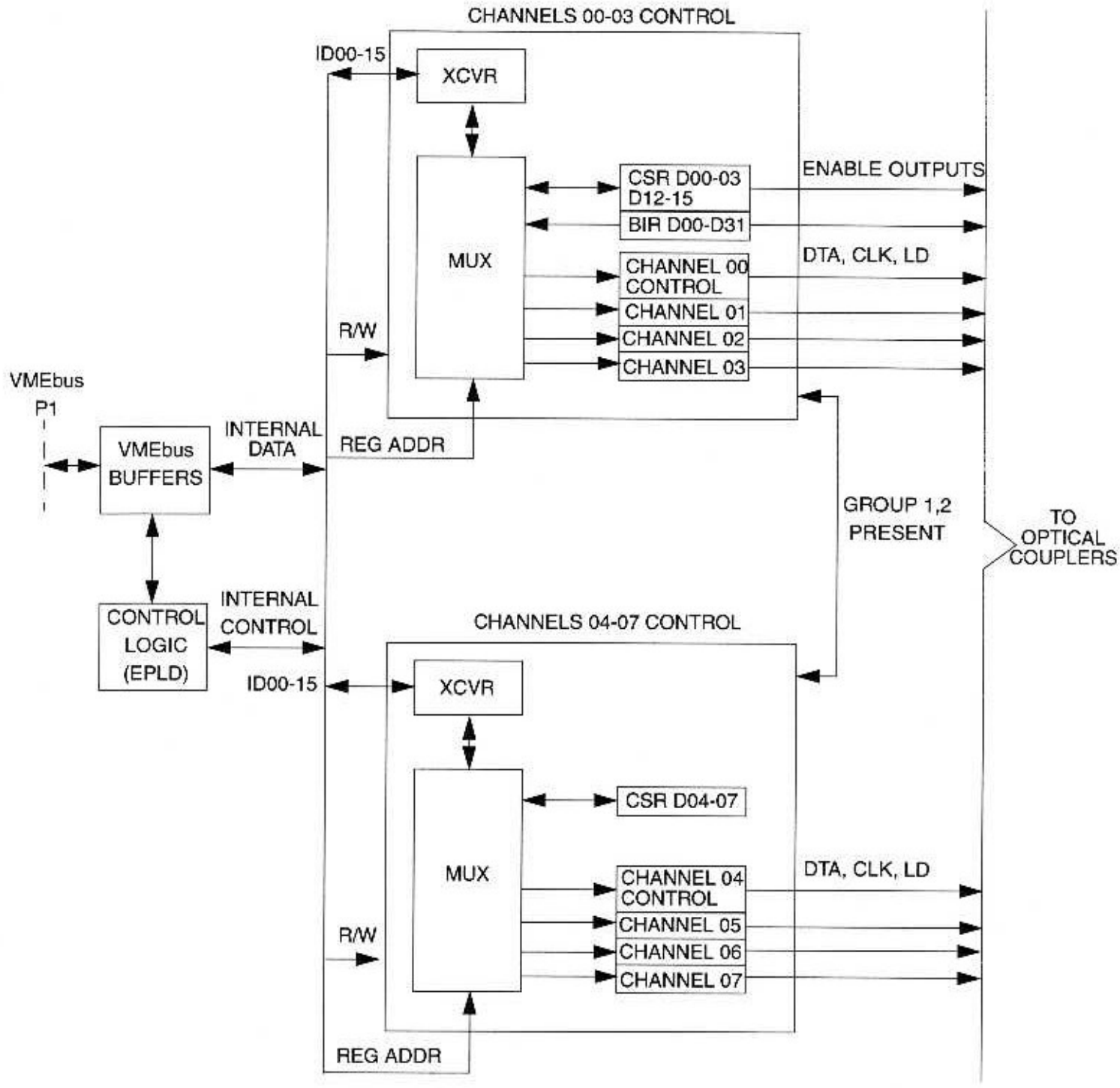


Figure 3.3-1. VMEbus Interface and Control

Each channel-control EPLD contains four data registers which receive the channel data words from the VMEbus, and provides an independent data serializer for each channel. Figure 3.4-1 on page 3-4 illustrates the movement of data within a single control channel. A data transfer to any 16-bit channel data register from the bus initiates the serializing process which moves the data to the serial output D/A converter. Data in each register is right-justified with 12 significant bits.

Only the 12 significant data bits in each channel are serialized for transfer to the associated D/A converter. The four digital signals required to produce the transfer are shown in Figure 3.4-2 on page 3-5. The board selection (BDSEL L) initiates the transfer sequence. The CLOCK line provides the primary timing, and clocks the information present on the DATA line into the serial D/A converter, MSB first through LSB last. The output of the converter does not change during the serial transfer. When the serial transfer has been completed, the LOAD signal performs a parallel transfer of data to an output latch in the converter, and the output voltage responds to the new data.

3.5 ANALOG OUTPUT CHANNELS

3.5.1 Isolation

Each output channel is isolated from the VMEbus and from all other channels by an isolated DC/DC converter and by four optical couplers. The DC/DC converter provides isolated ±15 VDC power for the channel, and the optical couplers isolate the digital control signals IDTA, ICLK, ILD, and IENA from EPLD signals DATA, CLOCK, LOAD, and ENAOUT (Figure 3.5.1-1 on page 3-6). Power for the optical couplers is supplied as +5 VDC, and is series regulated from the isolated +15 V rail.

3.5.2 Digital-to-Analog Conversion

A serial Digital-to-Analog Converter (DAC) receives the 12-bit data word from the channel control EPLD, and produces an output voltage range that is jumper controlled from 0 to 10 V. The D/A buffer converts this range into the output ranges specified in the output ordering option. Channel span is adjusted in the feedback loop of the D/A buffer.

The voltage reference level is selected as +2.5 V, +5 V, or +10 V by the output module. A current output module automatically selects a +10 V reference. A voltage output module passes the state of the module control jumpers directly to the reference, and permits any of the three voltages to be selected.

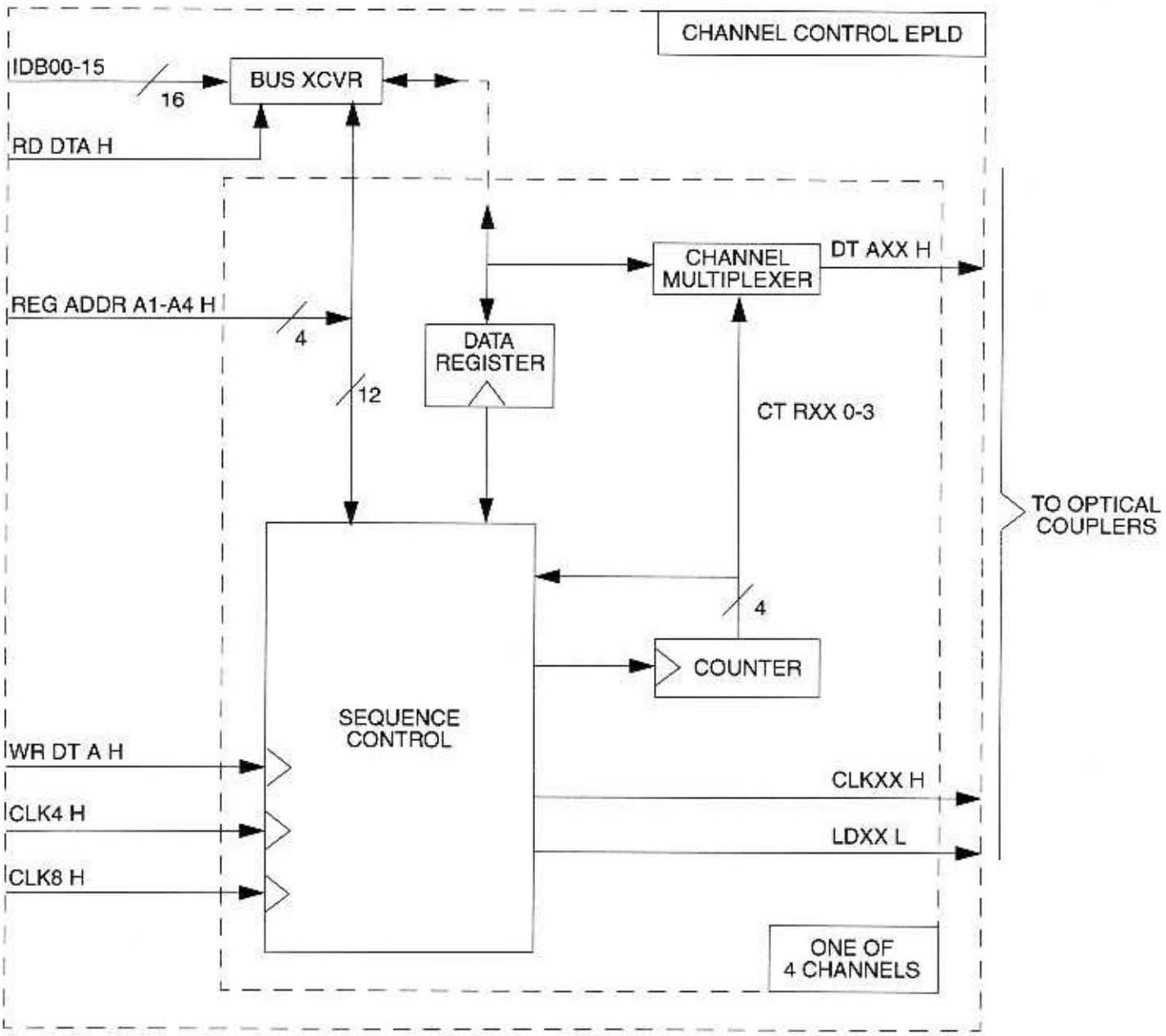


Figure 3.4-1. VMIVME-4800 Channel Control

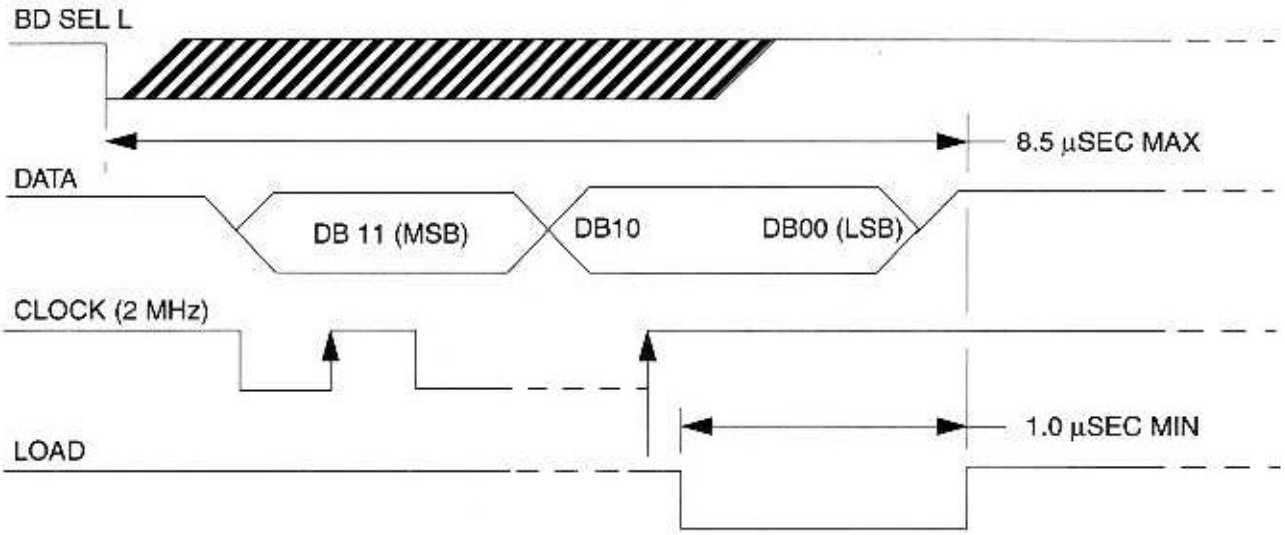


Figure 3.4-2. VMIVME-4800 Output Timing (Typical Channel)

3.5.3 Voltage and Current Outputs

All outputs are factory-configured for either unipolar voltage, bipolar voltage, or constant current. Each module contains an offset potentiometer to permit adjustment of the channel offset error to zero.

A voltage output module consists of a unity gain buffer and an output switch. The buffer provides the output drive capability necessary to support 10 mA loads over the maximum output range of ±10 V. The switch provides the on-line/off-line field disconnect feature, and is controlled by the Output Enable (OUTPUT EN) bit in the Control/Status Register (CSR). The output switch is located in the feedback loop of the buffer, and consequently does not contribute significantly to the final output impedence of 0.5 Ω. The jumpers connected to the voltage module permit selection of any of the three available reference voltages.

The current output module contains a voltage-to-current converter and a pass transistor. The module is factory-jumpered to provide the specified output current range with a voltage range from the D/A converter of 0 to +10 V. The pass transistor boosts the current output capability to the maximum level necessary to support the specified output current range. The jumpers which are connected to the module are used to select the source of loop power either as the internal isolated +15 V rail, or as an external supply which can provide a loop voltage up to +30 V.

3.6 DC/DC POWER CONVERTERS

Each channel contains a single DC/DC converter (Figure 3.5.1-1 on page 3-6) which derives isolated ±15 VDC power from the VMEbus +5 VDC power bus, and is packaged in a 24-pin dual-in-line module. The isolated ±15 VDC outputs from the converter supply all power required for the isolated section of each channel, including the optical isolators, the DAC, and the output module.

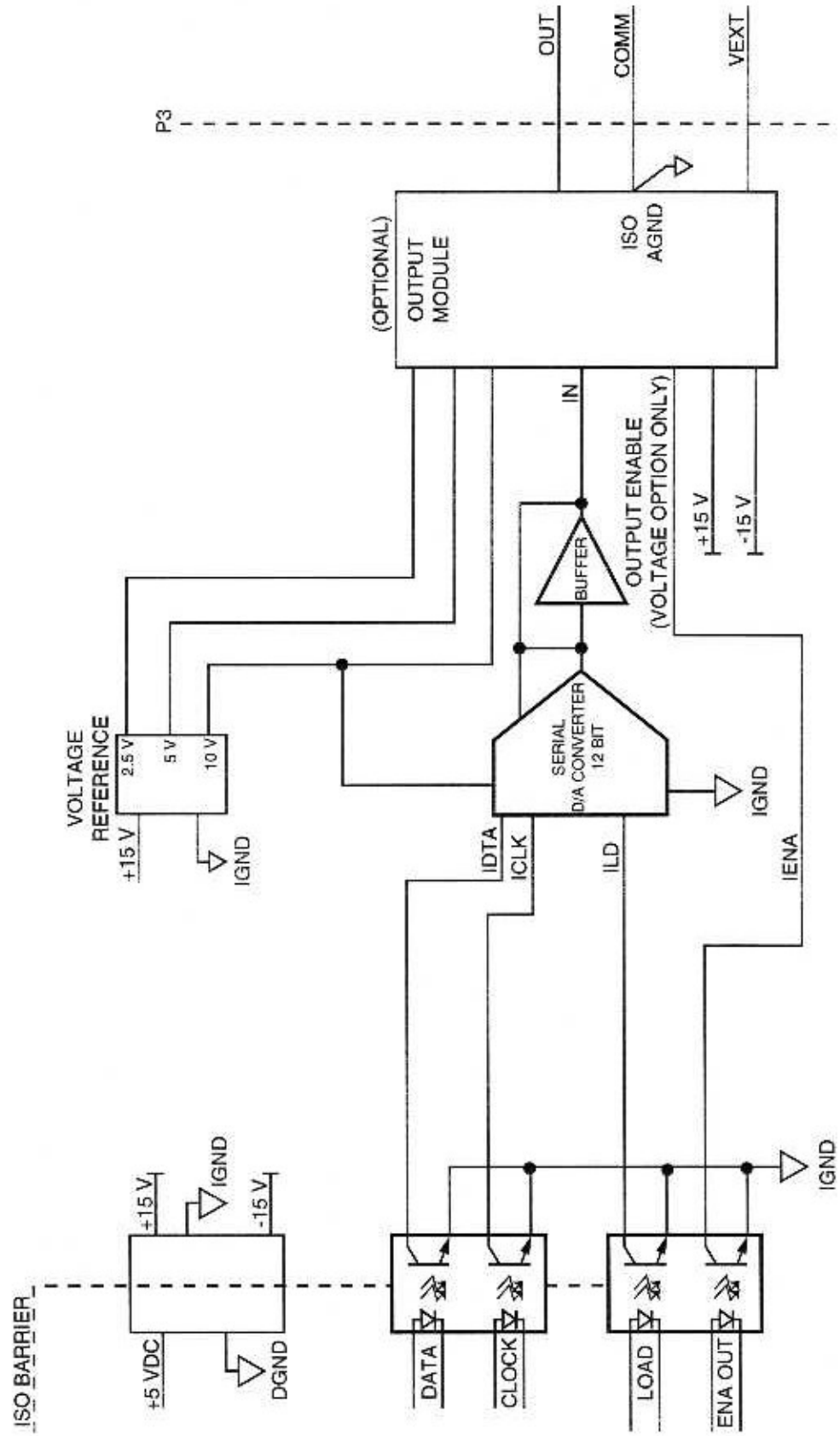


Figure 3.5.1-1. Isolated Output Channel

SECTION 4

PROGRAMMING

4.1 INTRODUCTION TO CONTROLLING THE VMIVME-4800 BOARD

Communication with the VMIVME-4800 is established through control, status, data, and identification registers that are mapped into a 16-word block. On-board configurable address jumpers permit the communication registers to be located in either the A16 short or the A24 standard I/O data space. Access privilege is jumper-selectable as supervisory, nonprivileged, or both. All registers are listed in Table 4.1-1 and described throughout this section.

Each of the eight analog outputs is controlled through a dedicated 12-bit Output Data Register (ODR). Data is serialized and transferred to an output D/A converter when the associated ODR receives a data transfer from the bus. All channels operate independently.

All read/write registers are cleared to ZERO by a system reset or power up operation. The reset operation places the board in the following state:

a. Analog Output Level....Current and voltage outputs are at lowest level.
b. Analog Output State....All voltage channels are disconnected from the output connectors, no effect on current option
c. Data Coding .....Offset binary
d. Front Panel LED .....Illuminated

Table 4.1-1. VMIVME-4800 Board Register Map

Board Address (Hex)	Register Function	Description	Access	Size
00	Board ID	BIR	Read Only	Byte/Word/Longword
04	Control and Status	CSR	Read/Write	Byte/Word
06	Reserved	...	...	
08	CH 00 Output Data	ODR 00	Read/Write	Word
0A	CH 01 Output Data	ODR 01	Read/Write	Word
0C	CH 02 Output Data	ODR 02	Read/Write	Word
0E	CH 03 Output Data	ODR 03	Read/Write	Word
10	CH 04 Output Data	ODR 04	Read/Write	Word
12	CH 05 Output Data	ODR 05	Read/Write	Word
14	CH 06 Output Data	ODR 06	Read/Write	Word
16	CH 07 Output Data	ODR 07	Read/Write	Word
18 to 1E	Reserved	...	...	

4.2 BOARD IDENTIFICATION REGISTER (BIR)

The Board Identification register contains the board identification code ($46000000) for the VMIVME-4800 board, and occupies the first two words at the board base address.

Table 4.2-1. Board ID Register Bit Map

Board ID Register (Offset Address $00) Read-Only, Byte							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	1	0	0	0	1	1	0

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	0

4.3 CONTROL/STATUS REGISTER (CSR)

Control/Status register functions and the bitmap are summarized in Table 4.3-1. Control register bits are mapped directly to the readback STATUS register at the same location. All CSR bits are cleared to zero (LOW) during a power up or reset operation. The CSR provides control and monitoring of the following board functions:

a. Output enabling (voltage outputs)
b. Output load cycle status
c. Data coding
d. Self test LED

Table 4.3-1. VMIVME-4800 Control/Status Register (CSR) Bit Map

CSR (Offset Address $04) Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
LED	Reserved	Output EN	Two's CMPL	Reserved			

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 7 Busy	CH 6 Busy	CH 5 Busy	CH 4 Busy	CH 3 Busy	CH 2 Busy	CH 1 Busy	CH 0 Busy

Control/Status Register Bit Definitions

Bit 15, LED: The "FAIL LED" is OFF if bit 15 is set (logical "1"), or is ON if bit is cleared (logical "0"). Default = logical "0".

Bit 14, Reserved: This bit is reserved and forced to a logical "0".

Bit 13, Output Enable: All outputs are connected to the output connectors if bit 13 is set to a logical "1," or disconnected if bit 13 is cleared to a logical zero.

NOTE:

FOR CURRENT OUTPUT OPTIONS, THE OUTPUTS ARE PLACED IN A MINIMAL CURRENT OUTPUT STATE WHEN THIS BIT IS CLEARED TO A ZERO. THIS BIT MUST BE SET TO A "1" TO ALLOW OPERATION. FOR THE DEFAULT STATE, REFERENCE SECTION 4.5.

Bit 13 has no effect on current outputs. Default = logical "0."

Bit 12, Two's Complement: Channel data is processed in 12-bit offset binary if bit 12 is cleared (reset default) or in two's complement format with extended sign if bit 12 is set a logical "1".

Bits 11 through 8, Reserved: These bits are reserved and forced to a logical "0".

Bit 7 through 0, CH Busy: The Channel Busy flag is set when the associated channel Output Data Register receives a data transfer from the bus, and remains set for approximately 8 µsec while the data word is transferred to the output D/A converter. A channel register should not be updated from the bus while the associated busy flag is set.

NOTE:

LOGIC STATE CONVENTION: TO AVOID AMBIGUITIES IN REFERENCES TO LOGIC LEVELS, THIS DOCUMENT USES THE CONVENTION THAT A DATA BIT OR CONTROL LINE IS "SET" WHEN IT IS IN THE "1", OR HIGH STATE, AND IS "CLEARED" WHEN "0" OR LOW STATE.

4.4 CONTROL OF ANALOG OUTPUTS

4.4.1 Output Registers and Data Format

The eight independent analog outputs are controlled through output data registers ODR 00 through ODR 07. Readback capability is provided, and both D8 (even/odd) and D16 transfers are supported. It is advisable to update data registers in word format. Data is configured in right-justified 12-bit offset binary format or two's complement format, data format is controlled by CSR bit 12.

In the offset binary format (reset default), the upper four bits D12 to D15 are ignored during loading and are returned as zero during readback. In two's complement format, data is received and returned in two's complement with the sign extended through the most significant bit, bit 15 during readback.

Table 4.4.1-1. Bipolar Output Offset Binary Format Bit Map

Bipolar Output Data Register Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	D11	D10	D09	D08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
D07	D06	D05	D04	D03	D02	D01	D00

Table 4.4.1-2. Bipolar Output Data Register Bit Map (Two's Complement)

Bipolar Output Data Register Read/Write, Byte/Word							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	D11	D10	D09	D08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
D07	D06	D05	D04	D03	D02	D01	D00

Table 4.4.1-3. Data Codes for Some Selected Output Voltages

Offset Binary	Two's Comp	Bipolar Output ±10 V	Unipolar Output 0 - 10 V	Scale Factor
000	800	-10 V	+0 V	- FSR
400	C00	-5 V	+2.5 V	1/4 FSR
800	000	+0 V	+5 V	1/2 FSR
C00	400	+5 V	+7.5 V	3/4 FSR
FFF	7FF	+9.9951 V	+9.9951 V	+ FSR - 1 LSB

4.4.2 Scaling and Enabling

Available output ranges are ±2.5 V, ±5 V, or ±10 V for bipolar voltage outputs, 0 to +2.5 V, 0 to +5 V, or 0 to +10 V for unipolar voltage outputs, and 4 to 20 mA, 0 to 20 mA, or 5 to 25 mA for current outputs. The analog output range is determined independently for each output channel by on-board jumpers which are described in Section 5. All voltage outputs are disconnected from the output connectors if bit 13 in the CSR is cleared, or connected to the output connectors if CSR bit 13 is set.

If the CSR bit 12 control bit is cleared, the output data is coded in offset binary. Each output level is scaled linearly from $0000 for negative full scale or lowest output level, to $0FFF for positive full scale, or highest output level.

For two's complement coding (CSR bit 12 set), the output data is scaled from $F800 for negative full scale to $07FF for positive full scale. Two's complement coding normally is used only for bipolar outputs. Various coding examples are summarized in Table 4.4.1-3.

4.4.3 Output Load Cycles

Data from an output data register is transferred serially to the output D/A converter during an internal Output Load Cycle. A data transfer to a data register initiates a load cycle for the associated output channel. The load cycle is completed in approximately 8 µsec, and proceeds automatically after initiation without further intervention from the VMEbus. The level of the associated analog output channel is updated at the end of the load cycle. For D8 transfers, the load cycle is initiated by an odd-byte transfer.

Each Channel Busy Flag (bit 00 through bit 07) is set when the assigned channel output data register receives a data transfer from the bus, and remains set for approximately 8 µsec during the ensuing output load cycle. Data transfers to an output register should not take place while the associated busy flag is set. However, any register can be read at any time without affecting board performance. All output channels are controlled independently, and any output data register can be updated without affecting the other seven channels.

4.5 RESET OPERATIONS

All read/write registers are cleared to ZERO by a system reset operation. The reset operation places the board in the following state:

a. Analog Output Level.... For options "-AB1," current outputs are minimal; For options "-AB0," current outputs are on-line and full-scale voltage outputs are minus full scale.

b. Analog Output State... All voltage channels are disconnected from the output connectors.

c. Data Coding..... Offset binary.

d. Front Panel LED..... Illuminated.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

****
* CAUTION *
****

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice about the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

****
* CAUTION *
****

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 BEFORE APPLYING POWER: CHECKLIST

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

a. Have the sections pertaining to theory and programming, Sections 3 and 4, been reviewed and applied to system requirements?

b. Review Section 5.4 and Table 5.4-1 to verify that all factory-installed jumpers are in place. To change the board address or address modifier response, refer to Section 5.4.

c. Have the I/O cables, with the proper mating connectors, been connected to the input/output connectors? Refer to Section 5.6 for connector descriptions

d. Calibration has been performed at the factory. If recalibration is required, refer to Section 5.5.

After the checklist above has been completed, the board can be installed in a VMEbus system. This board may be installed in any slot position, except slot-one which is usually reserved for the system controller.

****
* CAUTION *
****

DO NOT INSTALL OR REMOVE THIS BOARD WITH POWER APPLIED

5.4 OPERATIONAL CONFIGURATION

Control of the VMIVME-4800 board address and I/O access mode are determined by field replaceable, onboard jumpers. This section describes the use of these jumpers, and their effects on-board performance. The VMIVME-4800 jumpers are summarized in Table 5.4-1 on page 5-3. The locations and functions of all VMIVME-4800 jumpers are shown in Figure 5.4-1 on page 5-4. The function of the output range select jumpers are option dependent and will be discussed in detail in Sections 5.4.1 through 5.4.3.

Table 5.4-1. VMIVME-4800 Jumper Configuration and Functions

Jumper ID	Function	Configurable	Factory Configuration
E11-1,2	Supervisory Only	Yes	Omitted
E11-3,4	Nonprivileged Only	Yes	Installed
E11-5,6	Short I/O	Yes	Installed
E12-1,2	Memory Address Bit A5=0	Yes	Installed
E12-3,4	Memory Address Bit A6=0	Yes	Installed
E12-5,6	Memory Address Bit A7=0	Yes	Installed
E9-1,2	Memory Address Bit A8=0	Yes	Installed
E9-3,4	Memory Address Bit A9=0	Yes	Installed
E9-5,6	Memory Address Bit A10=0	Yes	Installed
E9-7,8	Memory Address Bit A11=0	Yes	Installed
E9-9,10	Memory Address Bit A12=0	Yes	Installed
E9-11,12	Memory Address Bit A13=0	Yes	Installed
E9-13,14	Memory Address Bit A14=0	Yes	Installed
E9-15,16	Memory Address Bit A15=0	Yes	Installed
E10-1,2	Memory Address Bit A16=0	Yes	Installed
E10-3,4	Memory Address Bit A17=0	Yes	Installed
E10-5,6	Memory Address Bit A18=0	Yes	Installed
E10-7,8	Memory Address Bit A19=0	Yes	Installed
E10-9,10	Memory Address Bit A20=0	Yes	Installed
E10-11,12	Memory Address Bit A21=0	Yes	Installed
E10-13,14	Memory Address Bit A22=0	Yes	Installed
E10-15,16	Memory Address Bit A23=0	Yes	Installed
E1-1,2	Channel 0 Output Range Sel	Yes	Installed
E1-2,3	Channel 0 Output Range Sel	Yes	Omitted
E2-1,2	Channel 1 Output Range Sel	Yes	Installed
E2-2,3	Channel 1 Output Range Sel	Yes	Omitted
E3-1,2	Channel 2 Output Range Sel	Yes	Installed
E3-2,3	Channel 2 Output Range Sel	Yes	Omitted
E4-1,2	Channel 3 Output Range Sel	Yes	Installed
E4-2,3	Channel 3 Output Range Sel	Yes	Omitted
E5-1,2	Channel 4 Output Range Sel	Yes	*Installed
E5-2,3	Channel 4 Output Range Sel	Yes	Omitted
E6-1,2	Channel 5 Output Range Sel	Yes	*Installed
E6-2,3	Channel 5 Output Range Sel	Yes	Omitted
E7-1,2	Channel 6 Output Range Sel	Yes	*Installed
E7-2,3	Channel 6 Output Range Sel	Yes	Omitted
E8-1,2	Channel 7 Output Range Sel	Yes	*Installed
E8-2,3	Channel 7 Output Range Sel	Yes	Omitted

* Omitted for 4 Channel Options

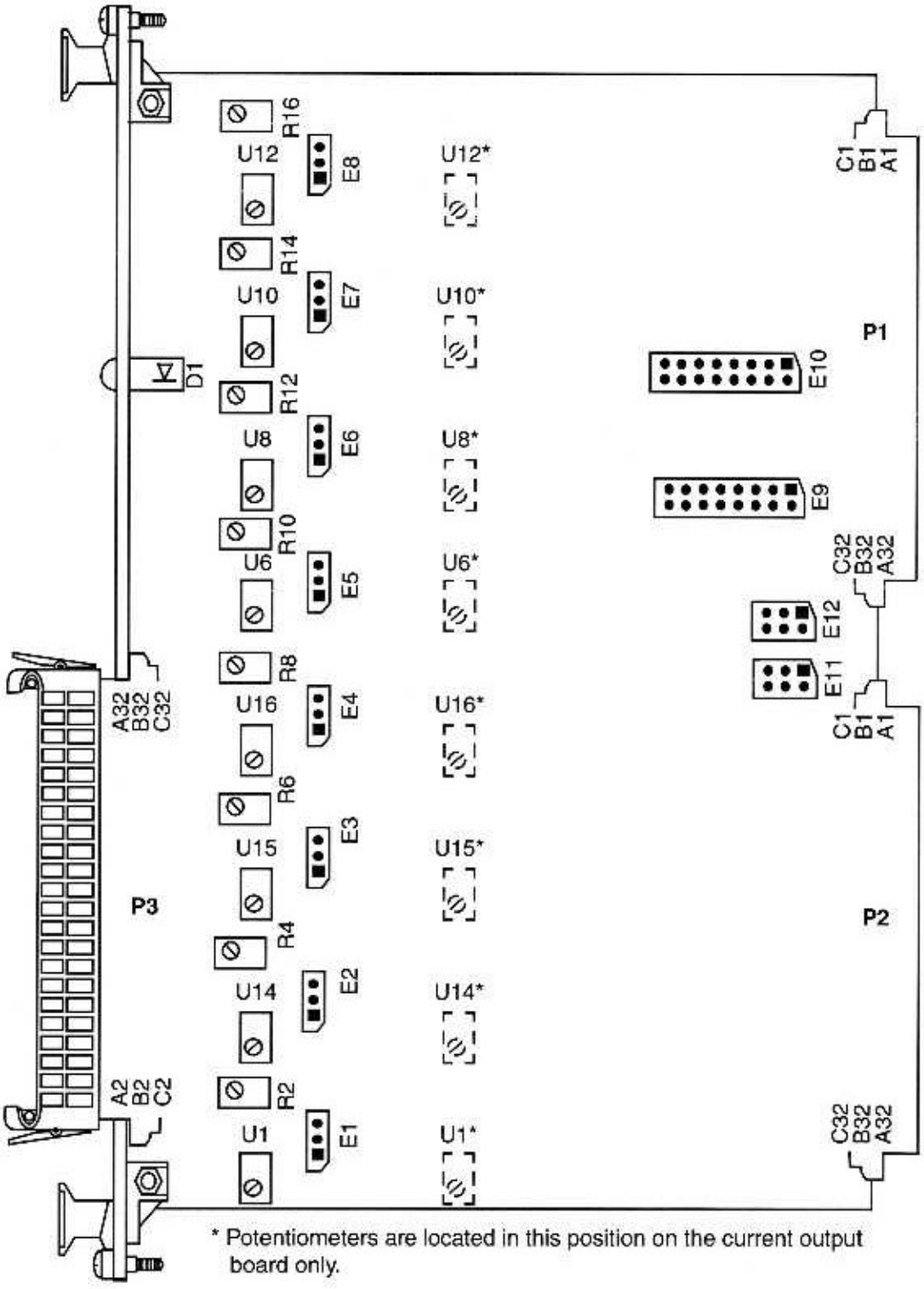


Figure 5.4-1. Location of User-Configurable Jumpers and Potentiometers

5.4.1 Bipolar Voltage Outputs (Optional)

The VMIVME-4800 provides Bipolar Voltage Outputs for 4 or 8 channels. The channel can be configured by user-installed jumpers for ±2.5 V, ±5 V, or ±10 V. The Table below describes the jumper functions for this mode, along with the designators for the adjustment potentiometers (POT) associated with each channel.

Table 5.4.1-1. Bipolar Voltage Jumper Functions

Channel*	Output Range Jumper	Voltage	Gain Adj	Zero Adj
0	E1-1,2	±2.5 V	R2	U1 POT
0	E1-2,3	±5 V	R2	U1 POT
0	E1-OPEN	±10 V	R2	U1 POT
1	E2-1,2	±2.5 V	R4	U14 POT
1	E2-2,3	±5 V	R4	U14 POT
1	E2-OPEN	±10 V	R4	U14 POT
2	E3-1,2	±2.5 V	R6	U15 POT
2	E3-2,3	±5 V	R6	U15 POT
2	E3-OPEN	±10 V	R6	U15 POT
3	E4-1,2	±2.5 V	R8	U16 POT
3	E4-2,3	±5 V	R8	U16 POT
3	E4-OPEN	±10 V	R8	U16 POT
4	E5-1,2	±2.5 V	R10	U6 POT
4	E5-2,3	±5 V	R10	U6 POT
4	E5-OPEN	±10 V	R10	U6 POT
5	E6-1,2	±2.5 V	R12	U8 POT
5	E6-2,3	±5 V	R12	U8 POT
5	E6-OPEN	±10 V	R12	U8 POT
6	E7-1,2	±2.5 V	R14	U10 POT
6	E7-2,3	±5.0 V	R14	U10 POT
6	E7-OPEN	±10 V	R14	U10 POT
7	E8-1,2	±2.5 V	R16	U12 POT
7	E8-2,3	±5 V	R16	U12 POT
7	E8-OPEN	±10 V	R16	U12 POT

* Channels 0 through 3, VMIVME-4800-000
Channels 0 through 7, VMIVME-4800-100

5.4.2 Unipolar Voltage Outputs (Optional)

The VMIVME-4800 provides Unipolar Voltage outputs for 4 or 8 channels. The channel can be configured by way of user-installed jumpers for 0 to 2.5 V, 0 to 5 V, or 0 to 10 V. Table 5.4.2-1 describes the jumper functions for this mode, along with the associated gain and zero adjustment designator for each channel.

Table 5.4.2-1. Unipolar Voltage Jumper Functions

Channel*	Output Range Jumper	Voltage	Gain Adj	Zero Adj
0	E1-1,2	0 to 2.5 V	R2	U1 POT
0	E1-2,3	0 to 5 V	R2	U1 POT
0	E1-OPEN	0 to 10 V	R2	U1 POT
1	E2-1,2	0 to 2.5 V	R4	U14 POT
1	E2-2,3	0 to 5 V	R4	U14 POT
1	E2-OPEN	0 to 10 V	R4	U14 POT
2	E3-1,2	0 to 2.5 V	R6	U15 POT
2	E3-2,3	0 to 5 V	R6	U15 POT
2	E3-OPEN	0 to 10 V	R6	U15 POT
3	E4-1,2	0 to 2.5 V	R8	U16 POT
3	E4-2,3	0 to 5 V	R8	U16 POT
3	E4-OPEN	0 to 10 V	R8	U16 POT
4	E5-1,2	0 to 2.5 V	R10	U6 POT
4	E5-2,3	0 to 5 V	R10	U6 POT
4	E5-OPEN	0 to 10 V	R10	U6 POT
5	E6-1,2	0 to 2.5 V	R12	U8 POT
5	E6-2,3	0 to 5 V	R12	U8 POT
5	E6-OPEN	0 to 10 V	R12	U8 POT
6	E7-1,2	0 to 2.5 V	R14	U10 POT
6	E7-2,3	0 to 5 V	R14	U10 POT
6	E7-OPEN	0 to 10 V	R14	U10 POT
7	E8-1,2	0 to 2.5 V	R16	U12 POT
7	E8-2,3	0 to 5 V	R16	U12 POT
7	E8-OPEN	0 to 10 V	R16	U12 POT

* Channels 0 Through 3, VMIVME-4800-040
Channels 0 Through 7, VMIVME-4800-140

5.4.3 Current Loop Output (Optional)

The VMIVME-4800 provides Current Loop Outputs for 4 or 8 channels. A 15 V loop power supply is provided on the board, or a maximum of 30 V can be supplied with an external loop power supply. A jumper is provided for each channel to configure the internal or external power supply as shown in Table 5.4.3-1. Figure 5.4.3-1 on page 5-8 shows a typical connection for an external loop power supply.

Table 5.4.3-1. Current Loop Output Jumper Functions

Channel*	Jumper	Loop Supply	Gain Adj	Zero Adj
0	E1-1,2	Internal	R2	U1 POT
0	E1-2,3	External	R2	U1 POT
1	E2-1,2	Internal	R4	U14 POT
1	E2-2,3	External	R4	U14 POT
2	E3-1,2	Internal	R6	U15 POT
2	E3-2,3	External	R6	U15 POT
3	E4-1,2	Internal	R8	U16 POT
3	E4-2,3	External	R8	U16 POT
4	E5-1,2	Internal	R10	U6 POT
4	E5-2,3	External	R10	U6 POT
5	E6-1,2	Internal	R12	U8 POT
5	E6-2,3	External	R12	U8 POT
6	E7-1,2	Internal	R14	U10 POT
6	E7-2,3	External	R14	U10 POT
7	E8-1,2	Internal	R16	U12 POT
7	E8-2,3	External	R16	U12 POT

* Channels 0 Through 3, VMIVME-4800-010, 020 or 030
Channels 0 Through 7, VMIVME-4800-110, 120 or 130

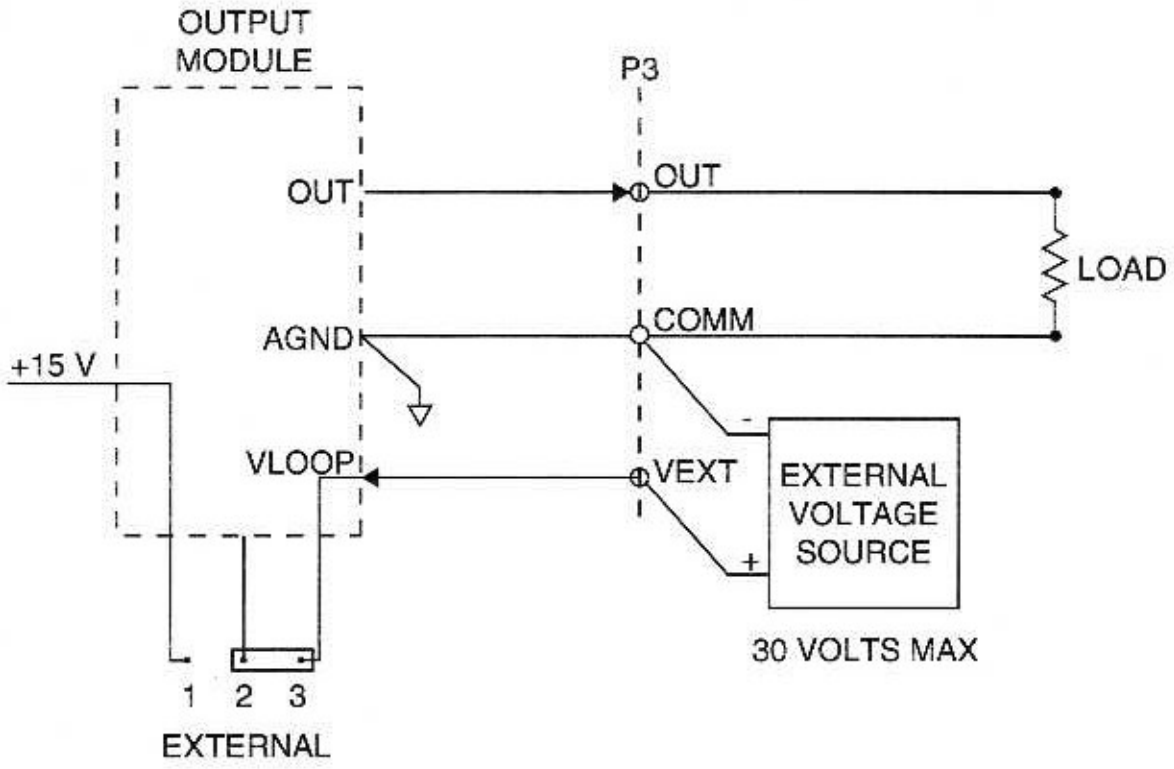
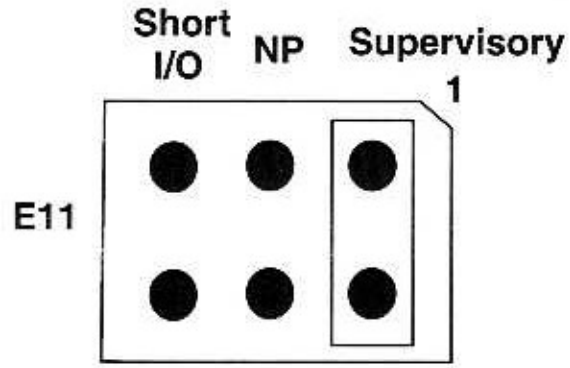


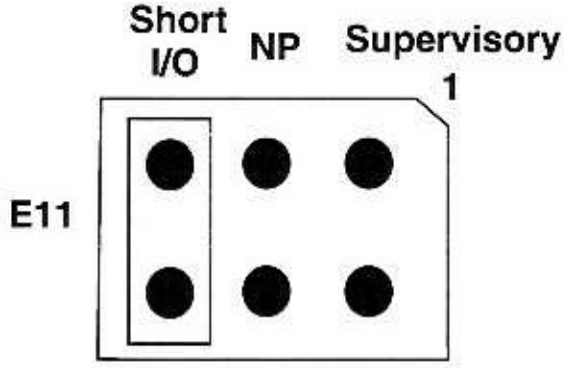
Figure 5.4.3-1. Typical External Voltage Connection

5.4.4 Address Modifiers

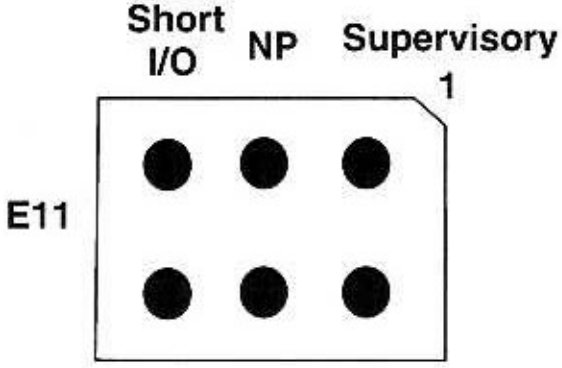
The VMIVME-4800 is factory configured to respond to short nonprivileged access as shown in Figure 5.4.4-1. The configuration can be changed by installing jumpers at the appropriate locations in the header as shown in Figure 5.4.4-1 on pages 5-9 and 5-10.



Jumper Configuration for Standard Supervisory Access

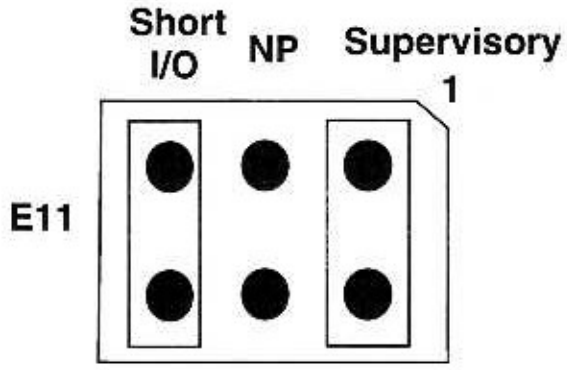


Jumper Configuration for Short Addressing with Supervisory or Nonprivileged Access

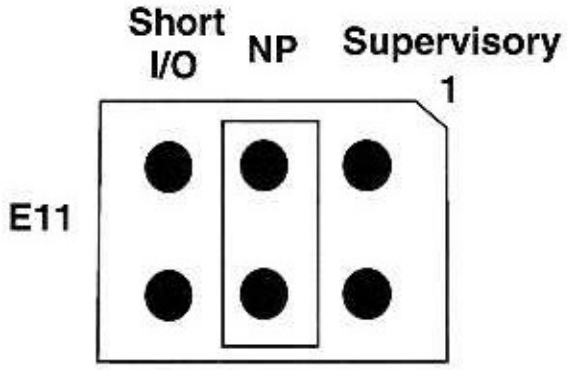


Jumper Configuration for Standard Addressing with Supervisory or Nonprivileged Access

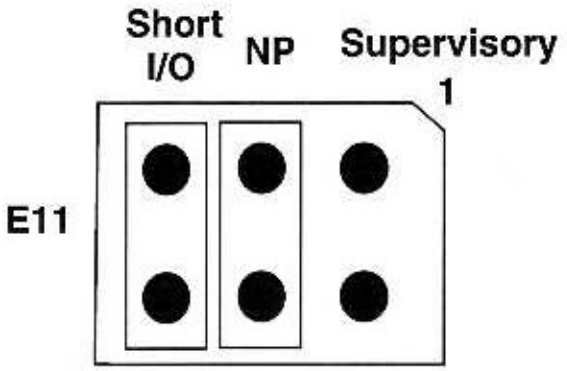
Figure 5.4.4-1. Address Modifier Jumper Configurations (a)



Jumper Configuration for Short Supervisory Access



Jumper Configuration for Standard Nonprivileged Access

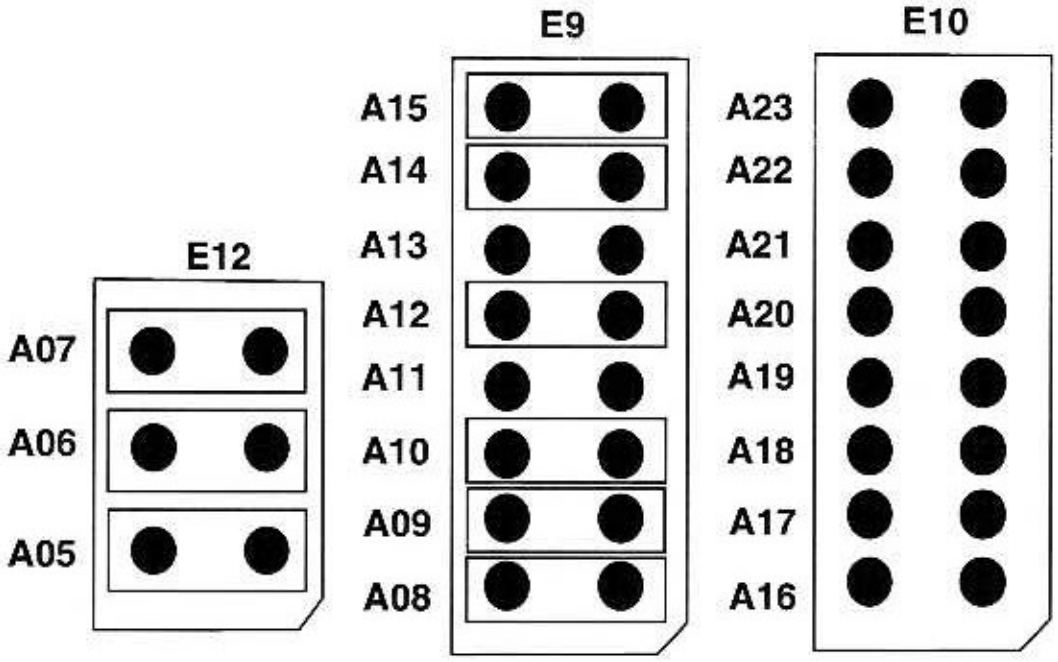


Jumper Configuration for Short Nonprivileged Access

Figure 5.4.4-1. Address Modifier Jumper Configurations (b)

5.4.5 Address Selection

The VMIVME-4800 is designed with banks of Address Select Jumpers that specify the base address of the board. The Address Selection Jumpers are shown in Figure 5.4.5-1. The VMIVME-4800 is factory configured to respond to $0000 short nonprivileged access. An installed jumper causes the board to compare to a low address line, an omitted jumper causes the board to compare to a high address line.



The example shown is for a I/O base address of $2800h (Short I/O Access) or FF2800 (Standard I/O Access)

Figure 5.4.5-1. Base Address Select Jumpers

5.5 CALIBRATION

Before delivery from the factory, the VMIVME-4800 board is fully calibrated. Should recalibration be required, refer to Sections 5.5.1 through 5.5.5 and perform the indicated calibration procedures in the order shown. Location of all adjustments are shown in Figure 5.4-1 on page 5-4. As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration, however, all adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

NOTE:

THE BIPOLAR AND UNIPOLAR VOLTAGE MODULES (OPTION DEPENDENT) WILL BE CALIBRATED AT FULL SCALE VALUE FOR THE MINIMUM RANGE. IF THE USER CONFIGURES THE BOARD FOR ANY OTHER RANGE, CALIBRATION WILL BE REQUIRED.

5.5.1 Equipment Required

a. Digital Multimeter:	Voltage Measurements: ±10 VDC range; 5 or more digits; ±0.005 percent of reading accuracy; 10Ω minimum input resistance. Current Measurements: 0 -100 mADC range; 5 or more digits; ±0.005 percent of reading accuracy; 100 maximum input resistance.
b. Chassis:	VMEbus 6U backplane or equivalent, with J1 and J2 connectors, 680x0 series controller, +5 ±0.2 VDC, 8 Amp (reserved current) power supply. One slot allocated for testing the VMIVME-4800 board.
c. Extender Card:	VMEbus 6U extender card.
d. Resistors:	250Ω ±5%, 1/4 watt (current outputs only)

5.5.2 Analog Outputs Calibration Procedure

a. Refer to Section 5.4 and configure the VMIVME-4800 board for the output configuration that is required for the application. For calibration of current outputs, configure the outputs for operation with the internal loop supply.

b. Install the VMIVME-4800 board on an extender card in the VMEbus chassis. Make provisions for connecting the DMM to each analog output channel, with the (+) common lead at the output pin (OUT*) and the (-) lead at the common pin (COMM*). The channel output pins are defined in Table 5.6-1 on page 5-15.

c. Apply power to the board. Write the value A000 (HEX) to the CSR, this will enable all outputs and extinguish the fail LED (refer to Table 4.1-1 on page 4-1 for the locations of all registers). All data transfers will be D16.

d. Allow a minimum warm-up interval of ten minutes before proceeding.

e. Proceed with paragraph 5.5.3 for bipolar voltage outputs, paragraph 5.5.4 for unipolar voltage outputs or paragraph 5.5.5 for current outputs. The locations of output modules and adjustment potentiometers are illustrated in Figure 5.4-1 on page 5-4.

5.5.3 Bipolar Voltage Output Calibration

a. Connect the DMM to the channel 00 output pins, with the (+) lead connected to the output pin and the (-) lead connected to the common pin.

b. Write the value $0800 to the channel 00 output data register. Adjust the ZERO potentiometer on the channel 00 output module for a DMM indication that conforms to the MIDSCALE value contained in Table 5.5.3-1 for the assigned output range.

c. Write the value $0FFF to the channel 00 output data register. Adjust the Channel-00 gain potentiometer for a DMM indication that conforms to the POSITIVE FULLI SCALE value contained in Table 5.5.3-1 for the assigned output range.

d. Write the value $0000 to the channel 00 output data register. If the DMM indication does not conform to the NEGATIVE FULL SCALE value contained in Table 5.5.3-1 for the assigned output range, repeat steps (b), (c), and (d) until the measurements for all three steps are correct.

e. Repeat steps (a) through (d) for the remaining active output channels.

f. Bipolar calibration is completed. Remove power. Remove all test connections.

Table 5.5.3-1. Bipolar Voltage Output Calibration Values

Output Range (VDC)	Output Value (VDC)		
	Midscale	Positive Full Scale	Negative Full Scale
±2.5	0.0000 ±0.0006	+2.4988 ±0.0006	-2.5000 ±0.008
±5	0.0000 ±0.0010	+4.9975 ±0.0010	-5.0000 ±0.011
±10	0.0000 ±0.0002	+9.9951 ±0.0020	-10.0000 ±0.018

5.5.4 Unipolar Voltage Output Calibration

a. Connect the DMM to the channel 00 output pins, with the (+) lead connected to the output pin and the (-) lead connected to the common pin.

b. Write the value $0000 to the channel 00 output data register. Adjust the channel 00 gain potentiometer for a DMM indication that conforms to the ZERO value contained in Table 5.5.4-1 on page 5-14 for the assigned output range.

c. Write the value $0FFF to the channel 00 output data register. If the DMM indication does not conform to the POSITIVE FULL SCALE value contained in Table 5.5.4-1on page 5-14 for the assigned output range, repeat steps (b), (c), and (d) until the measurements for all three steps are correct.

d. Repeat steps (a) through (c) for the remaining active output channels.

e. Unipolar calibration is completed. Remove power. Remove all test connections.

Table 5.5.4-1. Unipolar Voltage Output Calibration Values

Output Range (VDC)	Output Value (VDC)	
	Zero	Positive Full Scale
0 to +2.5	0.0000 ±0.0006	+2.4988 ±0.0015
0 to +5	0.0000 ±0.0010	+4.9975 ±0.0020
0 to +10	0.0000 ±0.0020	+9.9951 ±0.0040

5.5.5 Current Output Calibration

a. Connect the DMM to the channel 00 output pins (Table 5.6-1 on page 5-15), with the (+) lead connected to the output pin through a series resistance of 250, and the (-) lead connected to the common pin. Leave the external loop supply pins (VEXT) disconnected.

b. Write the value $0000 to the channel 00 output data register. Adjust the ZERO potentiometer on the channel 00 output module for a DMM indication that conforms to the ZERO SCALE value contained in Table 5.5.5-1 for the assigned output range.

c. Write the value $0FFF to the channel 00 output data register. Adjust the channel 00 gain potentiometer for a DMM indication that conforms to the FULL SCALE value contained in Table 5.5.5-1 for the assigned output range.

d. Repeat steps (a) through (d) for the remaining active output channels.

e. Calibration is completed. Remove power, remove all test connections.

Table 5.5.5-1. Current Output Calibration Values

Output Range (mADC)	Output Value (mADC)	
	Zero	Positive Full Scale
4 to 20	4.000 ±0.004	+20.000 ±0.008
0 to 20	0.000 ±0.004	+20.000 ±0.008
5 to 25	5.000 ±0.004	+25.000 ±0.008

5.6 I/O CABLE AND FRONT CONNECTOR CONFIGURATION

The front input connector (P3) on the VMIVME-4800 is a standard 41612 DIN form E screw terminal connector. The P3 connector pin layout is shown in Figure 5.6-1 on page 5-15. The pin assignments for P3 are shown in Table 5.6-1 on page 5-15. The connector is supplied with integral latches. To remove connector depress both latches simultaneously, while gently pulling connector from socket. Install connector by aligning keying and pressing the connector into place.

5.6.1 32-Pin DIN Connector: Connector Specification

Wire should be 14-22 AWG
Insulation stripping length: .315" ±.20"/8mm ±0.5mm
The binding screw terminals are best suited for a .138" x.20"/3.5mm x 0.5mm common flat-blade screwdriver.
Recommended screw tightening torque: 5.22 lb./in. /0.6mN
Contact resistance: ≤10 mΩ

NOTE
DUE TO CHASSIS VIBRATION VMIC RECOMMENDS PERIODIC CHECKS OF SCREW TORQUE.

Front View (Cable Side) of "P3" Connector

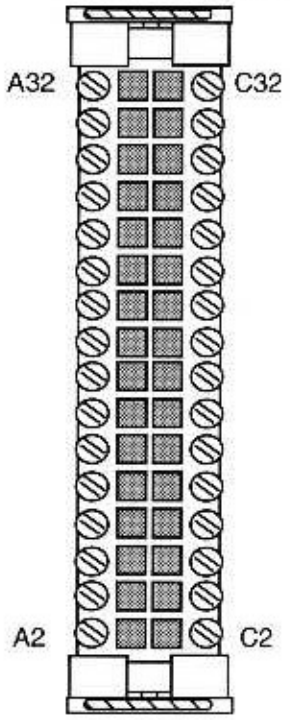


Figure 5.6-1. P3 Connector Pin Layout

Table 5.6-1. P3 Pin Assignments

P3 Pin #	Signal	Pin	Signal
A32	*VEXT 7	C32	N/C
A30	OUT 7	C30	COMM 7
A28	*VEXT 6	C28	N/C
A26	OUT 6	C26	COMM 6
A24	*VEXT 5	C24	N/C
A22	OUT 5	C22	COMM 5
A20	*VEXT 4	C20	N/C
A18	OUT 4	C18	COMM 4
A16	*VEXT 3	C16	N/C
A14	OUT 3	C14	COMM 3
A12	*VEXT 2	C12	N/C
A10	OUT 2	C10	COMM 2
A8	*VEXT 1	C8	N/C
A6	OUT 1	C6	COMM 1
A4	*VEXT 0	C4	N/C
A2	OUT 0	C2	COMM 0

* VEXT Pins have no Effect on Voltage Outputs

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software

b. System configuration

c. Electrical connections

d. Jumper or configuration options

e. Boards are fully inserted into their proper connector location

f. Connector pins are clean and free from contamination

g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis

h. Quality of cables and I/O connections

If the products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**

6.2 MAINTENANCE PRINTS

User-level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

ACKNOWLEDGEMENTS

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