

ARTISAN®
TECHNOLOGY GROUP

Your **definitive** source for quality pre-owned equipment.

Artisan Technology Group
(217) 352-9330 | sales@artisantg.com | artisantg.com

Full-service, independent repair center
with experienced engineers and technicians on staff.

We buy your excess, underutilized, and idle equipment
along with credit for buybacks and trade-ins.

Custom engineering
so your equipment works exactly as you specify.

- Critical and expedited services
- In stock / Ready-to-ship
- Leasing / Rentals / Demos
- ITAR-certified secure asset solutions

Expert team | Trust guarantee | 100% satisfaction

All trademarks, brand names, and brands appearing herein are the property of their respective owners.

Visit our website - *Click HERE*

VMIVME-5588
REFLECTIVE MEMORY BOARD

PRODUCT MANUAL

DOCUMENT NO. 500-005588-000 B

Revised March 18, 1996

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, AL 35803-3308
(205) 880-0444
1-(800)-322-3616
FAX NO. (205) 882-0859

NOTICE

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, VMIC assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contained herein.

VMIC reserves the right to make any changes, without notice, to this or any of VMIC's products to improve reliability, performance, function, or design.

VMIC does not assume any liability arising out of the application or use of any product or circuit described herein; nor does VMIC convey any license under its patent rights or the rights of others.

For warranty and repair policies, refer to VMIC's Standard Conditions of Sale.

AMXbus, BITMODULE, COSMODULE, DMAbus, IOWorks, IOWorks Access, IOWorks Foundation, MAGICWARE, MEGAMODULE, PLC ACCELERATOR, QUICK-R-NET, Soft Logic Link, SRTbus, TESTCAL, "The Next Generation PLC", The PLC Connection, TURBOMODULE, UCLIO, UIOD, UPLC, Visual IOWorks, Visual Soft Logic Control(ler), *VMEaccess, VMEmanager, VMEmonitor,* VMEnet, VMEnet II, *VMEprobe*, and *WinUIOC* are trademarks of VME Microsystems International Corporation. The VMIC logo, I/O man figure, and UIOC are registered trademarks of VME Microsystems International Corporation. Other registered trademarks are the property of their respective owners.

VME Microsystems International Corporation

All Rights Reserved

This document shall not be duplicated, nor its contents used for any purpose, unless granted express written permission from VMIC.

Copyright © February 1995 by
VME Microsystems International Corporation

RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	02/06/95	Release	95-0117
B	03/18/96	Cover, Pages ii and 5-3	96-0192

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

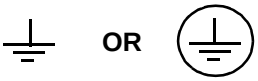
GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL



Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.



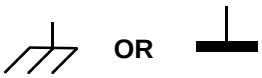
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



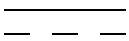
Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



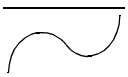
Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).



The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.



The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE:

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-5588
REFLECTIVE MEMORY BOARD

TABLE OF CONTENTS

Page

SECTION 1. INTRODUCTION

1.1 FEATURES 1-1
1.2 FUNCTIONAL DESCRIPTION 1-2
1.2.1 Software Requirements 1-2
1.2.2 Hardware Requirements 1-2

SECTION 2. PHYSICAL DESCRIPTION AND SPECIFICATIONS

SECTION 3. THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW 3-1
3.2 BASE ADDRESS SELECTION 3-1
3.3 LINK SPEED SELECTION AND ERROR DETECTION 3-2
3.4 BUS INTERRUPTER MODULE 3-2
3.5 ADDRESSING FEATURES 3-2
3.6 NODE LATENCY 3-4

SECTION 4. PROGRAMMING

4.1 PROGRAMMING 4-1
4.2 BOARD IDENTIFICATION REGISTER (BID) 4-2
4.3 INT STATUS AND RECEIVER STATUS (IRS) 4-2
4.4 NODE ID REGISTER (NID) 4-3
4.5 BOARD CONTROL AND STATUS REGISTER (CSR) 4-3
4.6 THE COMMAND REGISTER (CMD) 4-4
4.7 COMMAND NODE (CMDN) 4-6
4.8 PROGRAMMING INTERRUPTS 4-7
4.8.1 Control Registers (CR0-CR3) 4-7
4.8.2 Local Status Interrupt (CR0) 4-8
4.8.3 Interrupt Sender ID Registers (SID1-SID3) 4-9
4.8.4 Vector Registers (VR0-VR3) 4-9
4.8.5 Device Reset 4-10

TABLE OF CONTENTS (Continued)

Page

SECTION 5. CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES 5-1
5.2 PHYSICAL INSTALLATION 5-1
5.3 JUMPER INSTALLATIONS 5-2
5.3.1 Extended Address Field (E1, E2) 5-3
5.3.2 Address Modifier Select (E3) 5-3
5.3.3 Standard Address Field (E4) 5-3
5.3.4 Link SYSRESET Enable (E5) 5-4
5.3.5 Fast Field (E6) 5-4
5.3.6 Mask Field (E7) 5-4
5.3.7 Board Node ID Field (E9) 5-4
5.3.8 Loop-Back Enable (E10) 5-5
5.3.9 Optical Relay Bit P2 Disconnect (E8) 5-5
5.4 FIBER-OPTIC LINK CONFIGURATION 5-6

SECTION 6. MAINTENANCE

6.1 MAINTENANCE 6-1
6.2 MAINTENANCE PRINTS 6-1
6.3 TROUBLESHOOTING HINTS 6-1

LIST OF FIGURES

Figure Page

1.2-1 VMIVME-5588 Functional Block Diagram 1-3
3.5-1 Example Memory Configurations for 1 Mbyte or Smaller Options 3-3
4.6-1 Interrupt/Data Receive Path 4-6
5.3-1 VMIVME-5588 Jumper Locations 5-2
5.3.2-1 Address Modifier Jumper Options 5-3
5.3.9-1 Node Bypass Configuration 5-5
5.3.9-2 Optical Relay Jumper Options 5-6

TABLE OF CONTENTS (Concluded)

LIST OF TABLES

Table		Page
4.1-1	VMIVME-5588 Memory Map	4-1
4.2-1	Board Identification Register Bit Map	4-2
4.3-1	INT Status and Receiver Status Register Bit Map	4-2
4.4-1	Node ID Register Bit Map	4-3
4.5-1	Board Control and Status Register Bit Map	4-3
4.6-1	VMIVME-5588 Interrupt Codes	4-5
4.7-1	VMIVME-5588 Node ID	4-7
4.8.1-1	Control Register Bit Map	4-7
4.8.3-1	Interrupt Sender ID Register Bit Map	4-9
4.8.4-1	Vector Register Bit Map	4-9
5.3.3-1	Standard Address Field Jumpers	5-3

APPENDIX

Assembly Drawing, Parts List, and Schematic

SECTION 1

INTRODUCTION

1.1 FEATURES

The VMIVME-5588 is a high-performance, easy-to-use method of linking up to 256 VMEbus systems together using global memory. Any data written to a specific location in memory appears in the same location in each of the other 255 nodes with no programming or other intervention required by the user.

This reflective memory board has several useful features:

a. No software necessary to establish communications

b. On-board interrupt generation ability, i.e., any node may generate interrupts on any one node or all other nodes on the system

c. Facilitates communications over very long link lengths, up to 1,000 feet

d. Can be selected to operate in privileged or nonprivileged modes or in both modes at once

e. Memory can be mapped in either standard (A24) or extended (A32) address space

f. Supports 8-, 16-, 24-, and 32-bit transfers (bi-directional)

g. Attention interrupts are channeled to one of seven programmable interrupt levels

h. Double Eurocard form factor

i. Any board may be jumpered to be any node

j. Selectable 256 Kbyte, 512 Kbyte, 1 Mbyte, 2 Mbyte, 4 Mbyte, 8 Mbyte, or 16 Mbyte of SRAM on-board

k. Options for 512 byte or 4 Kbyte FIFOs

l. A software accessible bit for controlling an external optical bypass switch

m. Software compatible with the VMIVME-5578

1.2 FUNCTIONAL DESCRIPTION

Figure 1.2-1 shows the block diagram of the reflective memory board. Note that the FIFO memory is on the same bus as the SRAM memory. The user sees only the SRAM memory and is not aware of the FIFO memory which does the actual bus transfer to the other boards. The reflective memory board appears to the user as standard SRAM memory and can be used as such. The only effect noticeable to the user due to the presence of the communications bus is that the SRAM takes slightly longer to DTACK when the receive FIFO is writing to RAM.

1.2.1 Software Requirements

The reflective memory board upon power up is able to establish the board-to-board link without any program setup. The Bus Interrupter Module (BIM) which controls the interrupt generation on the reflective memory board is initialized to mask all interrupts upon power up.

If interrupts are desired, the appropriate registers in the BIM chip must be initialized through software control. The Control and Status Register (CSR) controls the Fail LED on the reflective memory board. The user must write to the CSR after any test software is run successfully on the board in order to turn OFF the Fail LED. There is no automatic diagnostic software on the board to perform a self-test. The LED being ON does not indicate a failure on-board unless the VMEbus software has turned it ON. LED ON is a standard power up mode for the Fail LED. If the output FIFO becomes over half-full, the reflective memory board issues an interrupt if the BIM has been programmed and enabled. The user software may choose to ignore this warning.

1.2.2 Hardware Requirements

Aside from the address map decoding required on the reflective memory board, a few jumpering requirements must be followed. The first requirement is that each reflective memory board on the communications bus must have a unique node ID address (jumper-selectable on-board). No two nodes can share the same node number (0,1...255). Nodes may be physically located in any order. Each reflective memory board may be mapped into a different address space. For the 1 Mbyte and smaller option VMIVME-5588s, data appears in the same location in each node relative to the base 1 Mbyte boundary to which each reflective memory is mapped (see Section 3.5). The relative address boundary is 4 Mbytes for the 2 Mbyte and 4 Mbyte options.

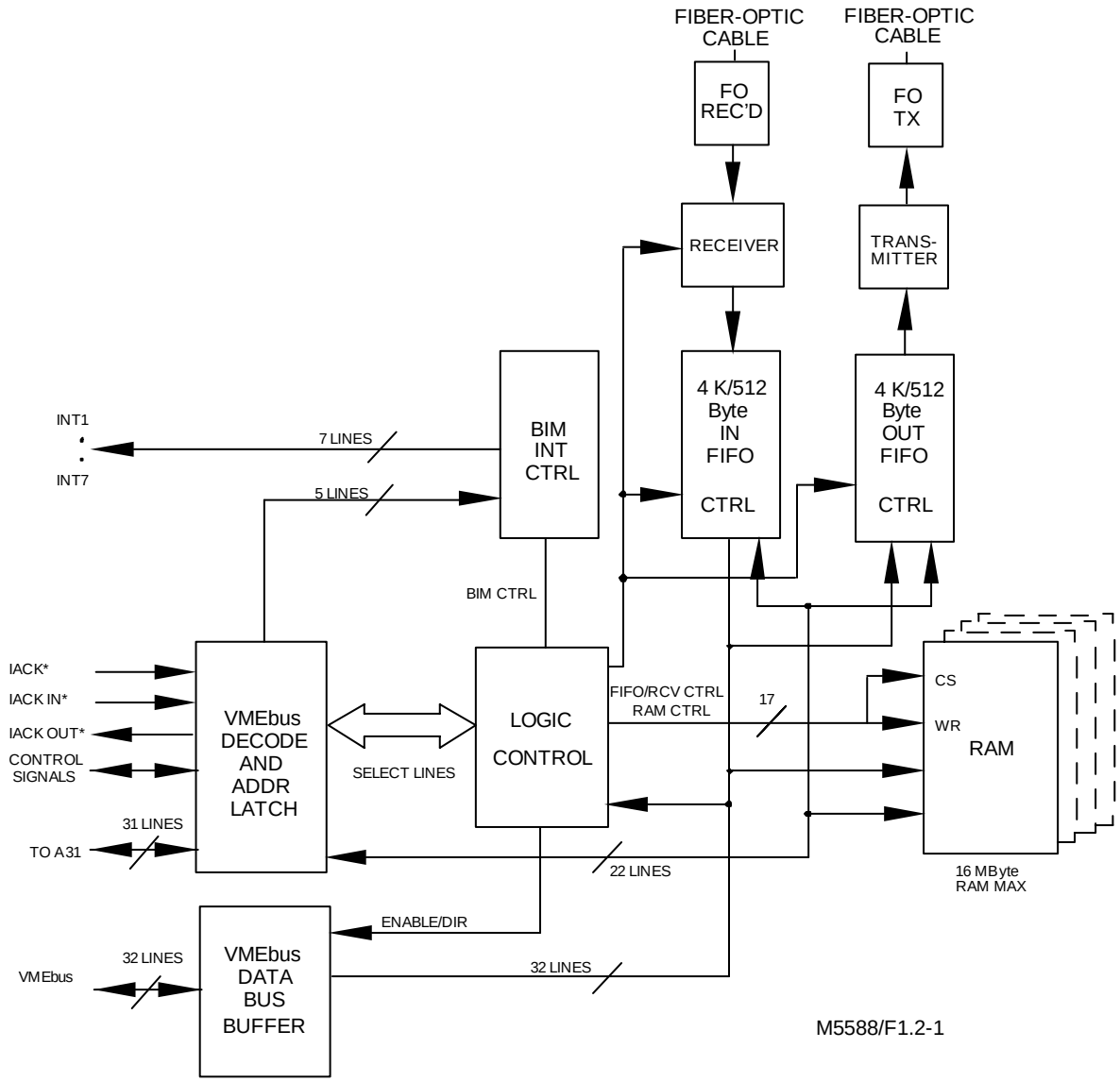


Figure 1.2-1. VMIVME-5588 Functional Block Diagram

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

Refer to 800-005588-000 Specification

SECTION 3

THEORY OF OPERATION

3.1 OPERATIONAL OVERVIEW

The VMIVME-5588 allows up to 256 VMEbus chassis to be linked together sequentially. Data written to any node appears in all other nodes without programming or other intervention by the user. The link between the nodes is two fiber-optic cables which pass address, data, and interrupt information between adjacent boards on the link.

The VMIVME-5588 allows a user to read or write the RAM address space at will. All memory writes are stored in SRAM on the board and also put in a FIFO to be broadcast to all other nodes. An interrupt command may also be written to any or all chassis by writing a data word into a specific location. The data value written dictates which node(s) will receive the interrupt. The interrupt is sent out in the order the data was received from the VMEbus. If a block of data was written to the board before the interrupt command is sent, then the data is broadcast to all boards before the interrupt command is broadcast.

Data not generated by the local node is placed in the receive FIFO. The receive FIFO then places data into RAM and into the transmit FIFO to be sent to the next node on the link. Since a node can receive data from both the local VMEbus and the link, data transfers from the VMEbus may be inserted among those from the link.

If both the local VMEbus and the receive FIFO access the RAM and transmit FIFO simultaneously, priority is given to the local VMEbus. In any other case, the first one to access the RAM and transmit FIFO receives priority.

3.2 BASE ADDRESS SELECTION

The base address of the VMIVME-5588 is jumper selectable. Once the base address is established, all accesses to the VMIVME-5588 are relative to the base address. Each node on the link may have a different base address. Only the relative offset to the base address is passed across the link. Thus, each board on the link may have a different VMEbus address and addressing mode.

3.3 LINK SPEED SELECTION AND ERROR DETECTION

The VMIVME-5588's high-speed serial fiber optics possess a finite bit error rate. For this reason, interlaced parity and other error detection hardware have been implemented. This hardware makes it virtually impossible for a data transfer error to go undetected. If an error is detected, the corrupted data packet is discarded and the user is notified. This process ensures that the receiving node's memory does not become corrupted. If the user wants more assurance that uncorrupted data will be received by all nodes, a redundant transfer mode can be used. Fast mode supports a 29.5 Mbytes/second data transfer rate. Redundant mode slows the throughput to 14.8 Mbytes/second. VMEbus interface response time is not affected by this data slowdown. The slowdown results from sending each data point twice. The probability of data transmission failure of both transmissions is once every three thousand years. Single transmission mode (Fast mode) is preferable in order to maintain high data throughput.

3.4 BUS INTERRUPTER MODULE

To facilitate the handling of interrupts, a Bus Interrupter Module (BIM) is used on the board. The attention interrupts (INT1, INT2, and INT3) are used to signal an interrupt from a remote chassis. An interrupt (INT0) may be generated as a result of an on-board potentially urgent situation. All interrupts are masked off at power up and become enabled under program control.

3.5 ADDRESSING FEATURES

Not all nodes have to be configured with the same memory size. Nodes may be configured to make optimum use of memory. Also, there are a few restrictions relating to address configuration.

For the 512 Kbyte and 256 Kbyte option reflective memory boards, more than one position is available relative to the 1 Mbyte boundary. To communicate with each other, all boards on the link which have the same memory size must be mapped to the same position relative to the 1 Mbyte boundary. No restriction exists concerning which 1 Mbyte boundary each board is on. Exact address matching is not required; only the position relative to the 1 Mbyte boundary must be the same (see Figure 3.5-1).

Likewise, the 2 Mbyte option board is mapped relative to the 4 Mbyte boundary. Because the 2 Mbyte and 4 Mbyte boards pass a 4 Mbyte relative address, they cannot be used on the same link with 1 Mbyte or smaller boards.

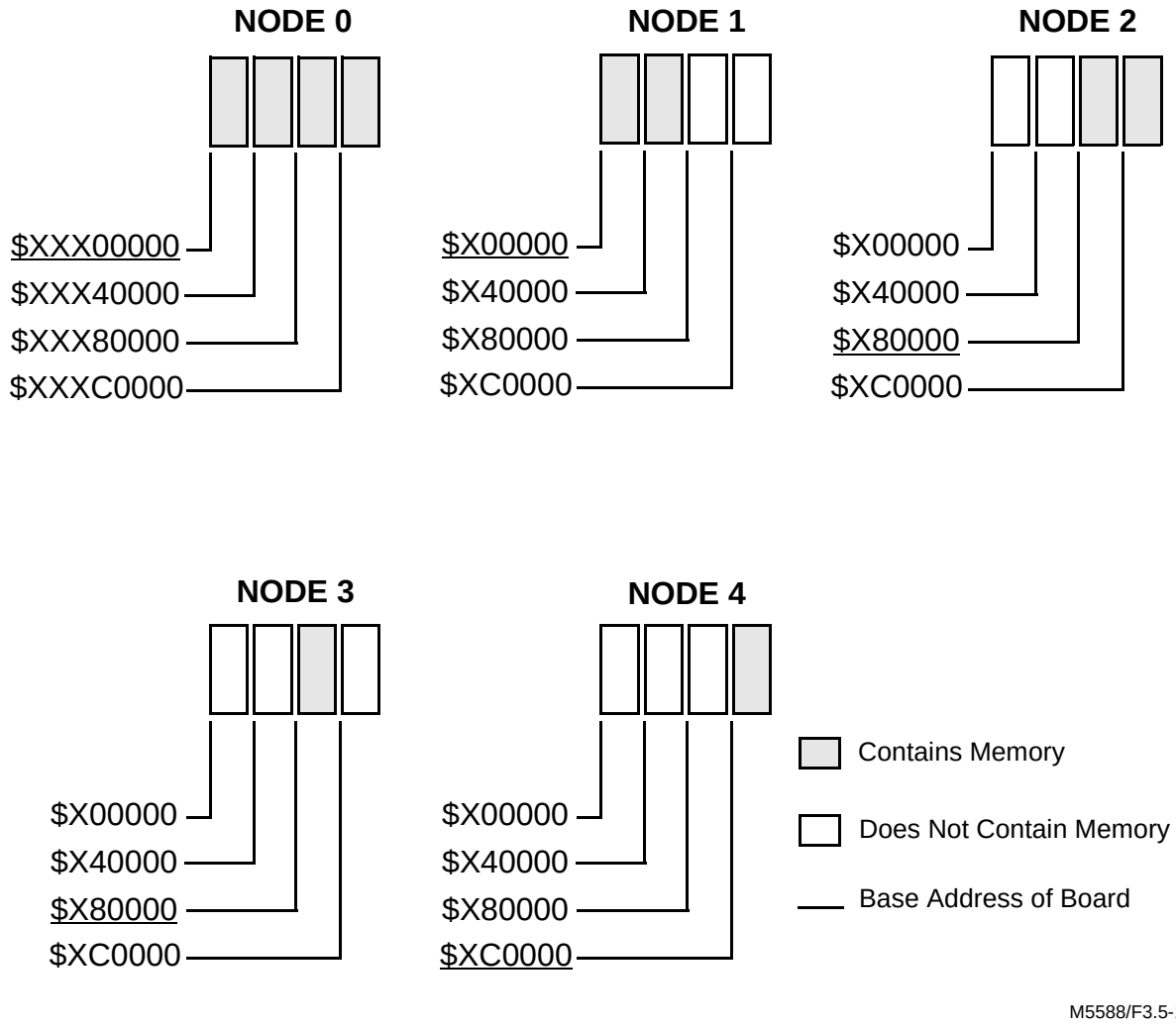


Figure 3.5-1. Example Memory Configurations for 1 Mbyte or Smaller Options

Node 0 is configured with 1 Mbyte of memory, nodes 1 and 2 are configured with 512 Kbytes of memory, and nodes 3 and 4 are configured with 256 Kbytes of memory. Because of the relative location of the memory, data written to address range $X00000 to $X7FFFF by a processor in node 0 is also written into the corresponding address in node 1. However, no data is written into nodes 2, 3, and 4 because there is no memory in that range in those nodes. Similarly, data written into address range $X80000 to $XBFFFF in node 2 is also written into nodes 0 and 3, but not nodes 1 and 4.

3.6 NODE LATENCY

If the fiber-optic data bandwidth has not been exceeded, data latency is typically 0.7 μs/node in single transfer mode. Longer latencies result if data input rates exceed 29.5 Mbytes/second. The transmit FIFOs back up with data until the half-full interrupts are set off. Once the transmit half-full occurs, the VMEbus response rate is automatically slowed down from 200 ns to 3.2 μs in order to allow the transmitter time to empty out. The throttling mode is removed once the transmit half-full flag de-asserts on the transmit FIFO.

SECTION 4

PROGRAMMING

4.1 PROGRAMMING

Although the VMIVME-5588 reflective memory board is software transparent on power up, some registers are present to facilitate user information and interrupt generation. Table 4.1-1 shows the memory-mapped registers used by the VMIVME-5588. This memory map is identical to that of the VMIVME-5578.

Table 4.1-1. VMIVME-5588 Memory Map

Offset	Description	Name	Access Mode
$01	Board ID	BID	Byte (R)
$02	INT & Receiver Status	IRS	Byte (R/W)
$04	Node ID	NID	Byte (R)
$05	Board Control and Status	CSR	Byte (R/W)
$06	Command	CMD	Byte/Word (W)
$07	Command Node	CMDN	Byte/Word (R/W)
$23	INT0 Control	CR0	Byte (R/W)
$26	INT1 Sender ID	SID1	Byte (R/W)
$27	INT1 Control	CR1	Byte (R/W)
$2A	INT2 Sender ID	SID2	Byte (R/W)
$2B	INT2 Control	CR2	Byte (R/W)
$2E	INT3 Sender ID	SID3	Byte (R/W)
$2F	INT3 Control	CR3	Byte (R/W)
$33	INT0 Vector	VR0	Byte (R/W)
$37	INT1 Vector	VR1	Byte (R/W)
$3B	INT2 Vector	VR2	Byte (R/W)
$3F	INT3 Vector	VR3	Byte (R/W)
$40	Start of RAM		All modes (Byte, Word, Lword) R/W
$03FFFF	End of 1/4 Mbyte RAM		All modes (Byte, Word, Lword) R/W
$07FFFF	End of 1/2 Mbyte RAM		All modes (Byte, Word, Lword) R/W
$0FFFFF	End of 1 Mbyte RAM		All modes (Byte, Word, Lword) R/W
$1FFFFF	End of 2 Mbyte RAM		All modes (Byte, Word, Lword) R/W
$3FFFFF	End of 4 Mbyte RAM		All modes (Byte, Word, Lword) R/W
$7FFFFF	End of 8 Mbyte RAM		All modes (Byte, Word, Lword) R/W
$FFFFFF	End of 16 Mbyte RAM		All modes (Byte, Word, Lword) R/W

M5588/T4.1-1

4.2 BOARD IDENTIFICATION REGISTER (BID)

The Board Identification (ID) Register allows the user to verify the presence of the reflective memory board at the correct address. The VMIVME-5588 board ID is $42.

Table 4.2-1. Board Identification Register Bit Map

Relative Offset $01 BID (Read Only)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
0	1	0	0	0	0	1	0

M5588/T4.2-1

4.3 INT STATUS AND RECEIVER STATUS (IRS)

Table 4.3-1. INT Status and Receiver Status Register Bit Map

Relative Offset $02 IRS (Read/Write)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
RCVR RESET	LATCHED SYNC LOSS	RCVR SYNC'D LOW	RX SIG DETECT LOW	NODE BYPASS	INT3 PENDING	INT2 PENDING	INT1 PENDING

M5588/T4.3-1

Bit 07: RCVR RESET (Read/Write) – Writing a one (1), then a zero (0) to this bit initiates a receiver reset. If the receiver comes out of reset while a receive transfer is in progress, a partially received data packet is discarded and a receive error is indicated. This bit is typically not used.

Bit 06: LATCHED SYNC LOSS (Read/Write) – A one (1) in this bit indicates that the receiver has lost synchronization since the last time this register was cleared.

Bit 05: RCVR SYNC'D LOW (Read Only) – A one (1) in this bit indicates the phase lock loop on the receiver is not locked.

NOTE

DUE TO LIMITATIONS IMPOSED BY THE FIBER CHANNEL CHIP SET USED ON THE VMIVME-5588, AFTER POWER UP OR SYSTEM RESET, THE RCVR SYNC'D LOW BIT MAY INDICATE THAT THE RECEIVER IS NOT SYNCHRONIZED WHEN IT ACTUALLY IS. SOMETIMES THE CHIP SET REQUIRES DATA TO BE RECEIVED BEFORE IT INDICATES THAT IT IS SYNCHRONIZED. THEREFORE, AT INITIALIZATION, THE USER SHOULD POLL THE NETWORK UNTIL EACH NODE IS "ALIVE" AND SYNCHRONIZED. TO PERFORM THIS OPERATION, USE THE OWN DATA BIT (BIT 2) OF THE CSR AS DESCRIBED IN SECTION 4.5.

Bit 04: RX SIG DETECT (Read Only) – This bit becomes zero (0) when a good optical signal is detected at the fiber-optic receiver. This does **not** indicate the receiver is phase locked. When this bit is a zero (0), the front panel

"SIGNAL DETECT" LED will be illuminated. See Section 5.4 for a description of the front panel "SIGNAL DETECT" and "OPTICAL STATUS" LEDs.

Bit 03: NODE BYPASS (Read/Write) – Writing a one (1) to this bit causes the node to be removed from the network. An external optical switch is required to implement this function. See Section 5.3.9.

Bit 02*: INT3 PENDING (Read Only) – When this bit is set to one (1), an INT3 has been received intended for the local node. Bit 2 may be cleared by reading INT3 sender ID ($2E).

Bit 01*: INT2 PENDING (Read Only) – When this bit is set to one (1), an INT2 has been received intended for the local node. Bit 1 may be cleared by reading INT2 sender ID ($2A).

Bit 00*: INT1 PENDING (Read Only) – When this bit is set to one (1), an INT1 has been received intended for the local node. Bit 0 may be cleared by reading INT1 sender ID ($26).

*These bits allow interrupts to be sent using polling methods.

4.4 NODE ID REGISTER (NID)

A value from 0 to 255 can be read from this byte. The value read corresponds to the node ID jumper selected for the board (see Section 5.3.3).

Table 4.4-1. Node ID Register Bit Map

Relative Offset $04 NID (Read Only)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
NODE ID							

M5588/T4.4-1

4.5 BOARD CONTROL AND STATUS REGISTER (CSR)

The CSR contains local node state information and is mapped as follows:

Table 4.5-1. Board Control and Status Register Bit Map

Relative Offset $05 CSR (Read/Write)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
LED	RCV HALF-FULL	TX HALF-FULL	TX EMPTY	BAD DATA	OWN DATA	MASK	FAST

M5588/T4.5-1

Bit 07: FAIL LED STATUS (Read/Write) – When this bit is set to one (1), the LED is ON. The LED is ON after power up. The user must write a zero (0) to this bit to turn the Fail LED OFF.

Bit 06: RECEIVE FIFO HALF-FULL (Read Only) – When this bit is zero (0), the receive FIFO is at least half-full. This bit displays the current status of the receive FIFO. This bit should **never** be zero (0). If this bit is zero, local VMEbus access should be suspended or at least curtailed for a period of time or data loss could occur. A zero in this bit indicates a local VMEbus condition (extremely slow release of data strobes after DTACK). In an optimally functioning VMEbus system, this should never occur.

Bit 05: TRANSMIT FIFO HALF-FULL (Read Only) – When this bit is zero (0), the transmit FIFO on the local node is over half-full.

Bit 04: TRANSMIT FIFO EMPTY (Read Only) – When this bit is zero (0), the transmit FIFO on the local node is empty.

Bit 03: BAD-DATA (Read/Write) – When this bit is set to one (1), a transfer error has occurred. It does **not** depend on the removal of the Mask jumper. In redundant transmission mode, this bit indicates only that a transfer error occurred on one of the two transfers.

Bit 02: OWN-DATA (Read/Write) – When this bit is set to one (1), the link is intact. This bit indicates that the local node has received data back that originated on the local node. It may be reset by writing this bit to zero (0). Once set by receiving its own node ID from the fiber-optic receiver, the bit remains set until cleared by the local VMEbus side. To test link latency, write a zero (0) to this bit and poll until it returns to a one (1). Writing to the CSR generates a packet which is sent around the link. This packet does not affect any other node's CSR. See the note in Section 4.3.

Bit 01: MASK TRANSFER ERROR INTERRUPT (Read Only) – When this bit is set to one (1), interrupts are masked. If the Mask jumper E7 is installed and INT0 is enabled by software on the BIM, an interrupt is generated each time a receive error is detected on the fiber-optic link.

Bit 00: FAST MODE (Read Only) – When this bit is set to one (1), Fast mode is enabled. Fast mode transmits each data transfer once on the fiber-optic link. If the jumper E6 is installed, each transfer is sent twice on the fiber-optic link.

4.6 THE COMMAND REGISTER (CMD)

The VMIVME-5588 may generate an interrupt to one or all other chassis through the use of the Command Register. Valid choices for interrupts are 1, 2, and 3. Table 4.6-1 shows all possible combinations. The interrupts are processed just like data so all words sent previous to the interrupt command are present on the receiving board's memory before the interrupt is issued to the receiving board. The Command Register is write only.

Table 4.6-1. VMIVME-5588 Interrupt Codes

D7	D6	D5	D4	D3	D2	D1	D0	Function
						0	0	reset node(s) is sent
						0	1	interrupt 1 is generated
						1	0	interrupt 2 is generated
						1	1	interrupt 3 is generated
X	1	X	X	X	X	X	X	interrupt is generated in all chassis
X	0	X	X	X	X	X	X	interrupt is generated in chassis ID which was written previously at relative address $07. A word or longword write can specify both interrupt type and receiving node ID in one transfer.

M5588/T4.6-1

In the event of an external interrupt (INT1, INT2, INT3), the VMIVME-5588 prevents the loss of any subsequent interrupt of the same type through the use of a dedicated FIFO for each interrupt type. The interrupt handler must read the Sender ID Register before the next interrupt of the same type can be sent to the BIM. For example, an interrupt INT1 has been sent across the link immediately followed by a second INT1. The receiving node must determine that the VMIVME-5588 has issued an INT1 through the use of the resulting VMEbus IRQ level (1 through 7) and its vector. The second interrupt remains in the INT1 FIFO until the receiving node reads the SID Register, then the second interrupt INT1 is issued to the BIM. This method guarantees that all interrupts sent on the link get serviced and that the receiver knows the ID of the node which sent each interrupt. Only one read per interrupt is allowed, otherwise loss of subsequent interrupts may occur.

The three interrupt FIFOs are 512 bytes deep allowing up to 512 interrupts of any type to be received and queued in the FIFO. Since interrupts go through the same receive FIFO as data (see Figure 4.6-1), all data sent before an interrupt is present in the local node’s memory before the interrupt is issued to the local node. Writing to the Sender ID Register resets the associated FIFO and clears any interrupts in that FIFO that have not been serviced. This clear function is especially useful when an interrupt level has been masked off and the corresponding interrupt FIFO contains many global or local interrupts. These interrupts can all be cleared at once without having to service each one individually.

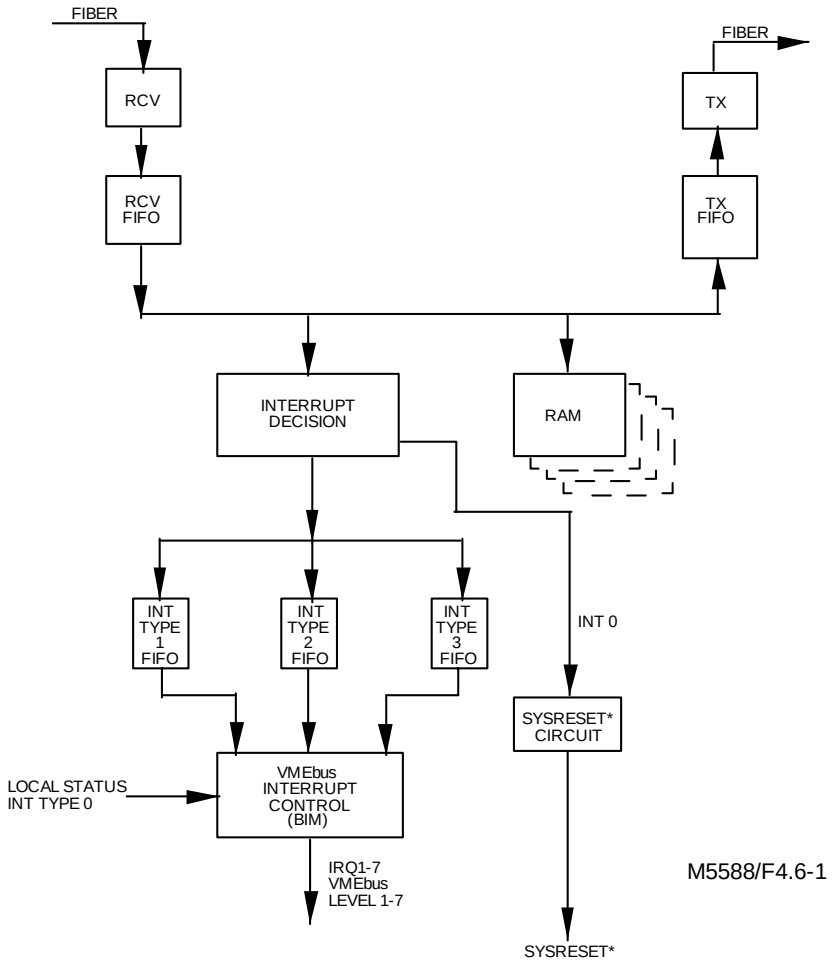


Figure 4.6-1. Interrupt/Data Receive Path

4.7 COMMAND NODE (CMDN)

This register contains the ID of the node to receive the interrupt sent by writing the Command Register. This register must be set by writing a 16-bit word to both the Command Register and the Command Node or writing an 8-bit byte to Command Node prior to writing a byte to the Command Register. Table 4.7-1 shows node ID patterns.

Table 4.7-1. VMIVME-5588 Node ID

D7	D6	D5	D4	D3	D2	D1	D0	Node
0	0	0	0	0	0	0	0	Node 0
0	0	0	0	0	0	0	1	Node 1
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	Node 255

M5588/T4.7-1

4.8 PROGRAMMING INTERRUPTS

The Bus Interrupter Module (BIM) controls interrupt programming. The BIM contains eight programmable read/write registers, one Interrupt Control Register (CR), and one Interrupt Vector Register (VR) for each of the four interrupt sources. The BIM also has three Interrupt Sender ID Registers that contain the ID of the node which originated the current interrupt.

The four identical Control Registers (CR0 through CR3) govern the operation of the board. CR1 through CR3 control interrupts from other nodes while CR0 monitors the status of local FIFOs.

The other four registers (VR0 through VR3) are identical Vector Registers that contain the vector data used during an interrupt acknowledge cycle.

4.8.1 Control Registers (CR0-CR3)

There is a Control Register for each interrupt source (CR0 controls INT0, CR1 controls INT1, and so on). Figure 4.8.1-1 shows the bit map of the Control Registers; all Control Registers have the same bit map.

Table 4.8.1-1. Control Register Bit Map

CR0 ($23), CR1 ($27), CR2 ($2B), and CR3 ($2F) (Read/Write)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FLAG	FLAG AUTO CLEAR	VECTOR SOURCE	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		

M5588/T4.8.1-1

Bit 07: FLAG (F) – This bit can be read from or written to without affecting the interrupt operation of the device. The flag is useful as a status indicator for resource management and as a semaphore in multitasking or multiprocessing systems.

Bit 06: FLAG AUTO-CLEAR (FAC) – When this bit is set to one (1), the Flag bit is automatically cleared during an interrupt acknowledge cycle. This feature is useful in determining the interrupt status and passing messages.

Bit 05: VECTOR SOURCE – External vector not supported. Always set this bit to zero (0) for the VMIVME-5588.

Bit 04: INTERRUPT ENABLE (IRE) – This bit must be set to one (1) to enable the bus interrupt request associated with the Control Register. Thus, if the INTX line is asserted and IRE is cleared, **no** interrupt request (IRQX) is asserted.

Bit 03: INTERRUPT AUTO-CLEAR (IRAC) – When this bit is set to one (1), IRE is cleared during an interrupt acknowledge cycle responding to this request. Clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, write a one (1) to the IRE bit.

Bits 02-00: INTERRUPT LEVEL (L2, L1, L0) – The least significant three bits of the register determines the level at which an interrupt is generated:

L2	L1	L0	IRQ Level
0	0	0	Disabled
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

4.8.2 Local Status Interrupt (CR0)

The fourth interrupt on the BIM (CR0) is dedicated to generate an interrupt in the event that the local FIFOs become half-full or a corrupt transfer has been received. If the interrupt is not disabled, every time the local VMIVME-5588 is written to and the transmit FIFO is over half-full or a transfer error occurs, an INT0 is generated. The half-full information flag is also available by looking at the CSR. The corrupt transfer interrupt may be masked off by removing the Mask jumper. This is done so the user is not bothered by interrupts in redundant transfer mode.

4.8.3 Interrupt Sender ID Registers (SID1-SID3)

The three Interrupt Sender ID Registers contain the ID of the node which originated the interrupt currently being serviced. All data sent across the fiber-optic link is tagged with the ID of the originating node so it may be removed from the link once it has been passed around the link one time. The ID is stored in the appropriate register if the data word received is an interrupt. As part of the interrupt handler software, the user must read the appropriate ID register in order to re-arm the currently used interrupt. This process ensures that all interrupts sent to the node are processed. The user may or may not use the ID, but it must be read as part of the interrupt handler process. Table 4.8.3-1 shows the bit map for the SID Registers; all SID Registers follow the same bit map.

Table 4.8.3-1. Interrupt Sender ID Register Bit Map

SID1 ($26), SID2 ($2A), and SID3 ($2E) (Read/Write)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
SENDER ID							

M5588/T4.8.3-1

In the event that a certain interrupt has been masked off at the BIM, the FIFO for that interrupt may be cleared by writing to the Sender ID register for the specific interrupt source before the BIM is armed. The ID write process is to be done in addition to the BIM arming process. In the interrupt handling sequence, the user should perform only one read per interrupt cycle. Erroneous results are caused by multiple reads.

4.8.4 Vector Registers (VR0-VR3)

Each interrupt input has its own associated Vector Register (see Table 4.8.4-1). Each register is eight bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/IN) Control Register bit is zero (0). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

Table 4.8.4-1. Vector Register Bit Map

VR0 ($33), VR1 ($37), VR2 ($3B), and VR3 ($3F) (Read/Write)							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
VECTOR							

M5588/T4.8.4-1

4.8.5 Device Reset

When the BIM is reset, the registers are set to a known condition. The Control Registers are set to all zeros. The Vector Registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

```
**********
*  CAUTION  *
**********
```

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. WHEN THE BOARD IS PLACED ON A BENCH FOR CONFIGURING, ETC., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL SHOULD BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning the disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

```
**********
*  CAUTION  *
**********
```

DO NOT INSTALL OR REMOVE THE BOARD WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting board guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 JUMPER INSTALLATIONS

Figure 5.3-1 shows the layout of jumpers on the reflective memory board. Jumpers E1 and E4 on the mother board are address jumpers which must be set to the desired base address of the board as described in Sections 5.3.1 and 5.3.3.

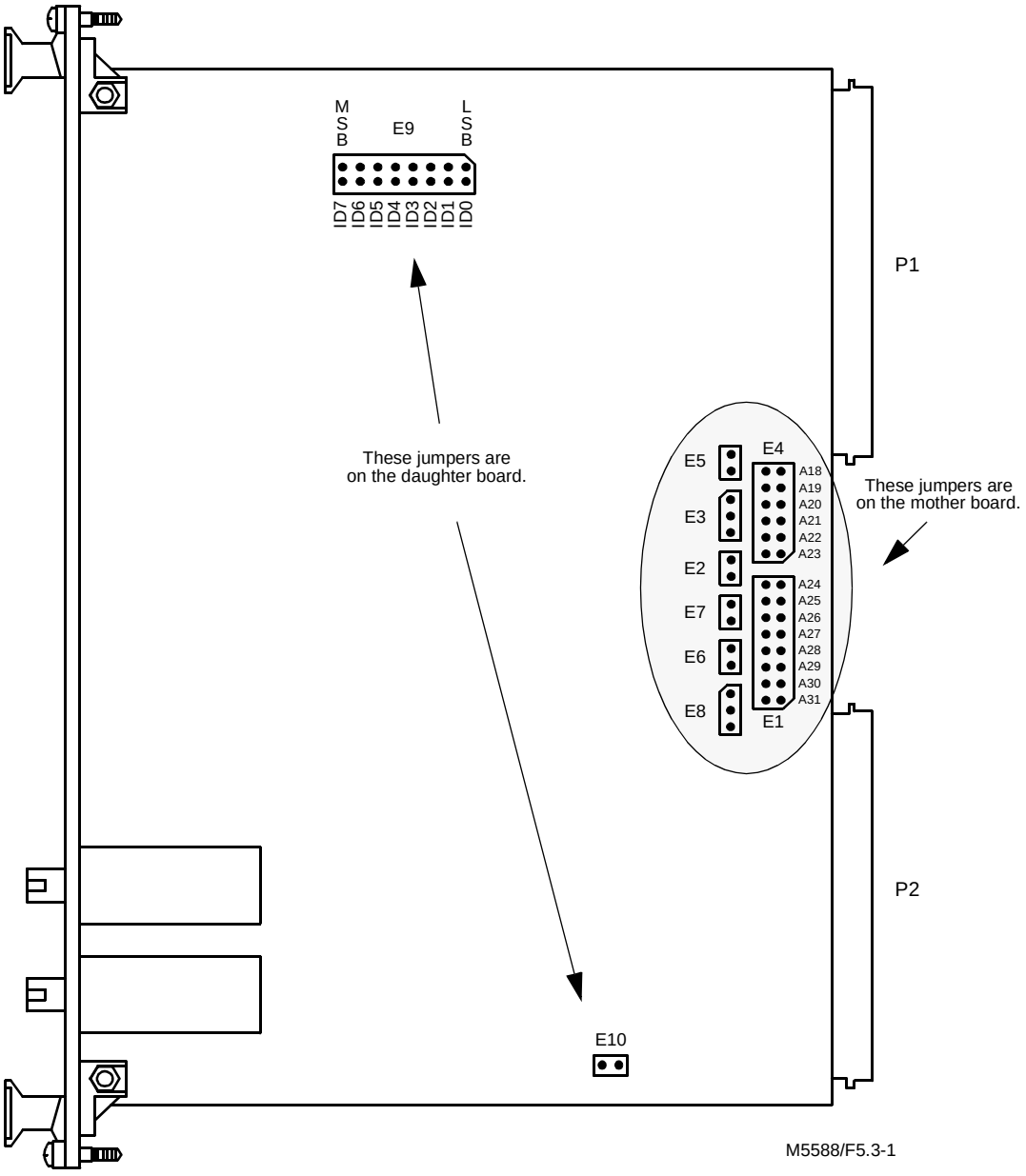


Figure 5.3-1. VMIVME-5588 Jumper Locations

5.3.1 Extended Address Field (E1, E2)

If the Extended Address Jumper, E2 on the mother board, is installed, the Extended Address Field, E1, becomes active. The Extended Address Field selects A31 through A24. An installed jumper is a zero (0) and an omitted jumper is a one (1).

5.3.2 Address Modifier Select (E3)

The reflective memory board may operate in one of three modes, supervisory data access, nonprivileged data access, or both. The different options are shown in Figure 5.3.2-1.

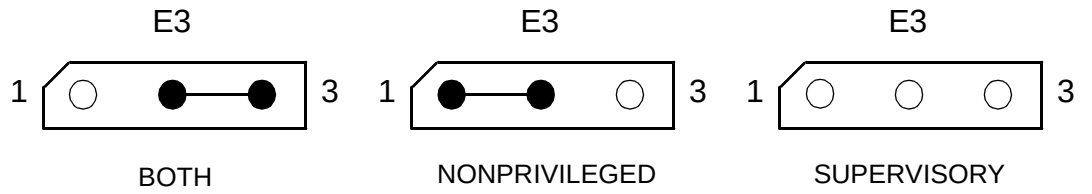


Figure 5.3.2-1. Address Modifier Jumper Options

5.3.3 Standard Address Field (E4)

The Standard Address Field is always active. An installed jumper indicates a zero (0) address. Some jumpers must be left open (no jumper) depending on the board memory options. The active fields are shown in Table 5.3.3-1. An ‘X’ indicates this position may or may not be jumpered (selected by the user). An ‘O’ indicates this position is always left open.

Table 5.3.3-1. Standard Address Field Jumpers

Memory*	A23	A22	A21	A20	A19	A18
16 Mbyte	O	O	O	O	O	O
8 Mbyte	X	O	O	O	O	O
4 Mbyte	X	X	O	O	O	O
2 Mbyte	X	X	X	O	O	O
1 Mbyte	X	X	X	X	O	O
512 Kbyte	X	X	X	X	X	O
256 Kbyte	X	X	X	X	X	X

M5588/T5.3.3-1

* An omitted jumper is a one (1); an installed jumper is a zero (0).

Jumper fields which must be left open due to specified memory options are left unpopulated on the PCB. For example, with the 512 Kbyte SRAM option, A18 is not used for standard address decode; it must be left open.

5.3.4 Link SYSRESET Enable (E5)

If this jumper is installed, the local node responds to the reception of an Attention Interrupt INT0 by issuing SYSRESET on the local VMEbus chassis. No SYSRESET is issued if jumper E5 is omitted.

5.3.5 Fast Field (E6)

If the E6 jumper is omitted, the fiber-optic link rate is 29.5 Mbytes/second. If the jumper is installed, the link rate is 14.8 Mbytes/second. The 14.8 Mbytes/second rate results from transmitting every data point twice. If an error is detected in the first transmission, it is thrown away and the second transmission of data is used. If the first transmission is okay, the second is ignored.

5.3.6 Mask Field (E7)

If the Mask Jumper is installed, the INT0 on the BIM interrupt IC is set when a data error is detected. The CSR can be read to determine if the INT0 was set by the transmitter becoming half-full or by a transfer error. If the Mask Jumper is omitted, then no interrupt is generated due to a transfer error. In redundant transfer mode, the user does not care if a transfer error occurs on a single transfer since the second transfer statistically is certain to be received correctly. The CSR bit 3 is always set if a single transfer error is detected regardless of the state of the Mask Jumper.

5.3.7 Board Node ID Field (E9)

The Board Node ID Field identifies each board on the memory link. No ID may be used more than once on the link. All nodes on the link should be sequentially numbered starting with zero. Jumper field E9 provides 8 bits to define the board node ID. An installed jumper sets the corresponding bit to zero. There is no relation between node number and physical position on the link. Nodes may be physically located in any order.

5.3.8 Loop-Back Enable (E10)

Loop-back mode can be enabled by removing jumper E10. Loop-back mode causes the serialized data to bypass the optics. The receiver circuitry is held in reset any time the optical receiver module is not detecting an optical signal. Therefore, in order for loop-back mode to function correctly, a fiber-optic cable must be connected between the optical receiver module and any VMIVME-5588's optical transmitter module.

5.3.9 Optical Relay Bit P2 Disconnect (E8)

The VMIVME-5588 has provisions which allow the user to use an optical relay (2x2 switch) in order to bypass the local node. An example of how this can be accomplished is shown in Figure 5.3.9-1. The optical relay is not part of the VMIVME-5588 and must be added externally. A relay driver's output (600 mA max) and +5 V are routed to a 6-pin mini-DIN front panel connector (P5).

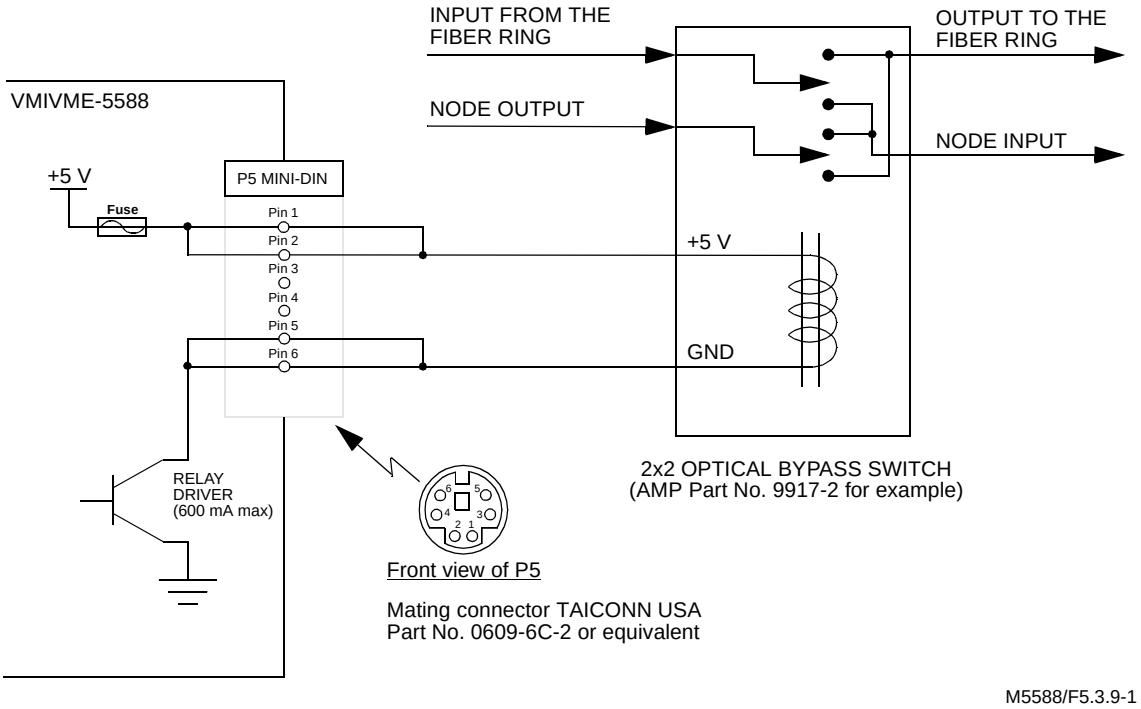


Figure 5.3.9-1. Node Bypass Configuration

A jumper can be used to route the relay driver's output, a TTL signal, or neither to P2 pin A32. The different options are shown in Figure 5.3.9-2.

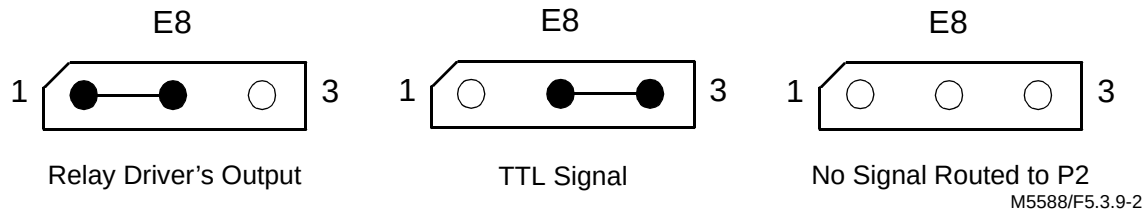


Figure 5.3.9-2. Optical Relay Jumper Options

The TTL signal is provided for use with the VMIVME-5599 Fiber-Optic Bypass Switch VMEbus board. This signal is actually the logical inverse of Bit 3 of the IRS register. For instance, the Node Bypass bit (Bit 3) of the IRS register is reset to zero (0); the TTL output signal on P2 is reset to one (1). If the user writes a one (1) to the Node Bypass bit, the TTL signal on P2 goes to zero (0).

To use the VMIVME-5599, the user must connect J2 pin A32 of the VMEbus slot containing the VMIVME-5588 to the J2 pin A32 of the VMEbus slot containing the VMIVME-5599. One way of doing this is by connecting a 64-conductor flat ribbon cable with DIN insulation displacement connectors onto the J2 connectors on the back side of the backplane. Upon power up or system reset, the VMIVME-5599 will operate in normal (nonbypass) mode. In order to optically bypass the local node, the user must write a one (1) to the Node Bypass bit (bit 3) of the IRS register or power down the local node.

5.4 FIBER-OPTIC LINK CONFIGURATION

A VMIVME-5588 link is formed by connecting the transmitter of board A into the receiver of board B. Board B's transmitter is then connected to the receiver of board C and so on. The last board in the link has its transmitter connected back to board A's receiver to close the link.

When data has been sent around the link and has returned to the originating node, two things happen. First, the data is removed from the link by comparing the data packet's ID to the local node's ID. If they match, the data packet is removed from the link. Second, the OWN DATA bit is set in the CSR. Loop data latency can be measured by writing a zero to the OWN DATA bit in the CSR and polling until it returns to a one state. This test assumes there is no other data originated by the local node on the link before the latency test is initiated. The data write to the CSR is passed around the link as regular traffic but does not affect the status of any other node's CSR.

The VMIVME-5588 front panel provides two LEDs to give a quick indication of the optical status of the board. The "SIGNAL DETECT" LED indicates whether or not the local fiber-optic receiver module is receiving an optical signal. If the receiver detects a signal, the LED will be illuminated.

The "OPTICAL STATUS" LED should flash at a 1 Hz rate under normal circumstances. If this is not occurring, one or both of the fiber-optic modules (transmit or receive) is malfunctioning. This indicator is not foolproof; there is a chance that it could be flashing even though the optics are malfunctioning.

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section provides information relative to the care and maintenance of VMIC's products. If the products malfunction, verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards are fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the chassis
h. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

6.2 MAINTENANCE PRINTS

User level repairs are not recommended. The appendix to this manual contains drawings and diagrams for reference purposes only.

6.3 TROUBLESHOOTING HINTS

The following pages list problems you may have when using the VMIVME-5588. The list also contains the possible causes and solutions for those problems.

SYMPTOM	POSSIBLE CAUSES
Board/Boards bus error when accessed from VMEbus after multiple writes.	1) System throughput has reached maximum, FIFOs have filled up with data to be sent, and the transmit FIFO half-full signal has been ignored.
Communications lost after power down of one or more nodes on the link.	1) The VMIVME-5588 is a ring architecture network and all data must be repeated at each node. If a node is powered down, the ring is opened at that point. The fiber-optic cable may be moved to complete the ring again or a fiber-optic bypass switch may be used to automatically complete the ring.
Node does not answer at expected address.	1) Address modifier incorrectly strapped on board. 2) Address strapped wrong (certain LSB address jumpers must be left off because of memory size options).
Data written to one node does not appear in other nodes.	1) For nodes of memory size 1 Mbyte or smaller, a 1 Mbyte relative address is passed. If two 0.25 Mbyte boards are not mapped in the same relative address in relation to the 1 Mbyte boundary, then they will not appear to communicate since they contain no common space in RAM. The 2 and 4 Mbyte boards pass a 4 Mbyte relative address and thus must be mapped in the same address relative to 4 Mbyte boundaries (note that 4 and 2 Mbyte nodes may not be used on the same link as 1 Mbyte or smaller nodes because they look at different relative address sizes). 2) The sending node ID is the same as another node on the ring. Each node must have a unique node ID, otherwise data originated on one node will be removed by the other node of the same ID.

SYMPTOM	POSSIBLE CAUSES
	3) Open or defective connection to fiber-optic cable.
	4) Defective FIFO module on either receiving node or transmitting node (the bad board may be found by checking memory on other nodes to see if they received data correctly).
	5) Phase lock loop on a node did not lock to incoming data from node transmitting to it. This condition may be checked by monitoring relative address location 2, Bit 5. See Section 4.3 for more details.
	6) Mixed nodes on the link (redundant and single transfer nodes on link). All nodes must be in either redundant or single transmission mode.
Data bits dropped or data appears in wrong address in memory.	1) Damaged or defective FIFO on node.
	2) Damaged cable or connector to link.
Data is wrong in one node and is correct in all other nodes.	1) Possible write to same memory location in two or more boards (in separate nodes) at the same time (this must be prevented in software).
	2) Damaged local node.
Parity errors commonly seen on local node.	1) Defective fiber-optic cable. It may have insufficient length-bandwidth or simply be broken. Light loss error budget has been exceeded.
	2) Damaged fiber-optic transmitter or receiver.
	3) Damaged node on ring (if parity errors are seen on a node, the failing node is either the local node or the node sending data to the local node).

SYMPTOM

When interrupts are being used, a spurious interrupt is issued from the CPU.

POSSIBLE CAUSES

1) IACKIN is not daisy chained from the CPU to the reflective memory board on the backplane. The VMEbus Specification requires all empty VMEbus slots to have IACKIN jumpered to IACKOUT.

APPENDIX A

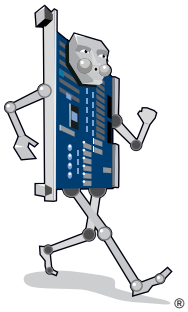
ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

ACKNOWLEDGEMENTS

Trademarks of VME Microsystems International Corporation:

AMXbus	The PLC Connection
BITMODULE	TURBOMODULE
COSMODULE	UCLIO
DMAbus	UIOD
IOWorks	UPLC
IOWorks Access	Visual IOWorks
IOWorks Foundation	Visual Soft Logic Control(ler)
MAGICWARE	*VMEaccess*
MEGAMODULE	*VMEmanager*
PLC ACCELERATOR	*VMEmonitor*
QUICK-R-NET	VMEnet
Soft Logic Link	VMEnet II
SRTbus	*VMEprobe*
TESTCAL	*WinUIOC*
“The Next Generation PLC”	

Registered Trademarks of VME Microsystems International Corporation:



(I/O man figure)

UIOC®

(VMIC logo)

Other registered trademarks are the property of their respective owners.

Artisan Technology Group is an independent supplier of quality pre-owned equipment

Gold-standard solutions

Extend the life of your critical industrial, commercial, and military systems with our superior service and support.

We buy equipment

Planning to upgrade your current equipment? Have surplus equipment taking up shelf space? We'll give it a new home.

Learn more!

Visit us at **artisantg.com** for more info on price quotes, drivers, technical specifications, manuals, and documentation.

Artisan Scientific Corporation dba Artisan Technology Group is not an affiliate, representative, or authorized distributor for any manufacturer listed herein.

We're here to make your life easier. How can we help you today?

(217) 352-9330 | sales@artisantg.com | artisantg.com

ARTISAN® TECHNOLOGY GROUP