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GE
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Hardware Reference

VMIVME-7645*

Intel 400MHz Front-Side Bus Pentium M Processor VMEbus SBC

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Table of Contents

Overview 13

Intel 855GME Chipset 15
Organization of the Manual 17
References 18
Safety Summary 20
Warnings, Cautions and Notes 21
Notation and Terminology 22

Chapter 1 - Installation and Setup 23

Unpacking Procedures 23
Hardware Setup 24
Power Requirements 28
Installation 29
BIOS Setup 30
Front/Rear Panel Connectors 32
LED Definition 33
Battery Mounted in Clip-Style Holder 34
For Battery Removal: 34
For Battery Installation: 34

Chapter 2 - Standard Features 35

CPU Socket 36
Physical Memory 36
Memory and Port Maps 37
Memory Map - Tundra Universe II-Based PCI-to-VMEbus Bridge 37
I/O Port Map 38
Interrupts 40
System Interrupts 40

PCI Interrupts 43
PCI Device Interrupt Map 45
Integrated Peripherals 48
Ethernet Controllers 49
10BaseT 49
100BaseTx 49
1000BaseT 49
Video Graphics Adapter 50
Universal Serial Bus 51
Dual Ultra 160 SCSI 52
PCI Interface 52
Ultra160 SCSI Memory 52
Ultra160 SCSI Processor 52
Ultra160 SCSI Termination 53
Media Connection 53

Chapter 3 - Embedded PC/RTOS Features 54

VMEbus Bridge 55
Embedded PCI Functions 56
Timers 57
General 57
Timer Control Status Register 1 (TCSR1) 57
Timer Control Status Register 2 (TCSR2) 58
Timer 1 & 2 Load Count Register (TMRLCR12) 59
Timer 3 Load Count Register (TMRLCR3) 59
Timer 4 Load Count Register (TMRLCR4) 60
Timer 1 & 2 Current Count Register (TMRCCR12) 60
Timer 3 Current Count Register (TMRCCR3) 60
Timer 4 Current Count Register (TMRCCR4) 61
Timer 1 IRQ Clear (T1IC) 61
Timer 2 IRQ Clear (T2IC) 61
Timer 3 IRQ Clear (T3IC) 61
Timer 4 IRQ Clear (T4IC) 62
VME Control 63
Remote Ethernet Booting 64
BootWare Features: 64

Chapter 4 - Maintenance 65

Maintenance Prints 65

Appendix A - Connector Pinouts 66

VMEbus Connector Pinout 67
Serial Connector P5 69
Keyboard and Mouse Connector and Pinout (J10) 70
PMC Connector Pinout (J11 - J13) 72
PMC (J11) Connector and Pinout 72
PMC (J12) Connector and Pinout 73
PMC (J13) Connector and Pinout 74
Ethernet Connector (J15) 75
USB Connectors (J16 and J17) 76

Appendix B - System Driver Software 77

Microsoft Windows XP Professional Software Driver Installation 78
Hance Rapids Chipset Software Installation 78
USB 2.0 EHCI Host Controller 78
Ethernet Adapter Drivers Installation 79
Status of PCI Devices Listed in Windows Device Manager 80

Appendix C - AMI BIOS 81

System BIOS Setup Utility 81
Help Window 81
Main Menu 82
System Time 82
System Date 82
Advanced Menu 83
CPU Configuration 83
CPU Speed 84
Thermal Monitor 2 84
IDE Configuration 84
IDE Configuration 84
Combined Mode Option 85
Primary/Secondary IDE Master/Slave 85
Type 85
LBA/Large Mode 85
Block (Multi-Sector Transfer) 85
PIO Mode 86
PIO Mode Descriptions 86
DMA Mode 86
S.M.A.R.T. 86
32Bit Data Transfer 86

Hard Disk Write Protect 86
IDE Detect Time Out (Sec) 86
ATA(PI) 80Pin Cable Detection 86
Floppy Configuration 87
Floppy A/B 87
SuperIO Configuration 87
Onboard Floppy Controller 88
Serial Port 1 & 2 Address 88
ICH SIO Serial Port 1 & 2 Address 88
Remote Access Configuration 88
Remote Access 88
Serial Port Number 89
Serial Port Mode 89
Flow Control 89
Redirection After BIOS POST 89
Terminal Type 89
UT-F8 Combo Key Support 89
USB Configuration 90
USB Function 90
Legacy USB Support 90
USB 2.0 Controller 90
USB 2.0 Controller Mode 90
PCIPnP Menu 91
Plug & Play OS 91
PCI Latency Timer 91
Allocate IRQ to PCI VGA 91
Palette Snooping 91
PCI IDE BusMaster 92
Onboard PCI/ISA IDE Card 92
IRQ Availability 92
DMA Channel Availability 92
Reserved Memory Size 92
Boot Menu 93
Boot from LAN OPROM 93
Boot Settings Configuration 93
Quick Boot 94
Quiet Boot 94
AddOn ROM Display Mode 94
Boot-up Num-Lock 94
PS/2 Mouse Support 94
Wait For ‘F1’ If Error 94

Hit ‘DEL’ Message Display 94
Interrupt 19 Capture 94
Boot Device Priority 94
1st, 2nd or 3rd Boot Device 95
Hard Disk Drives 95
Removable Drives 96
Security Menu 97
Security Settings 97
Change Supervisor Password 97
User Access Level 97
Change User Password 97
Clear User Password 98
Password Check 98
Boot Sector Virus Protection 98
Chipset Menu 99
Intel Montara NorthBridge Configuration 99
Primary Video Device 100
Graphics Mode Select 100
SouthBridge Configuration 100
IOAPIC 100
Extended IOAPIC 100
OnBoard AC’97 Audio 101
OnBoard AC’97 Modem 101
Exit Menu 102
Save Changes and Exit 102
Discard Changes and Exit 102
Discard Changes 102
Load Optimal Defaults 102
Main menu: 103
Advanced menu: 103
PCIPnP menu: 104
Boot menu: 105
Security menu: 105
..... 106
..... 106
Chipset menu: 106
Exit menu: 106
Load Failsafe Defaults 106

Appendix D - Argon BIOS 107

Boot Menus 108

First Boot Menu 108
Boot Menu 108
BIOS Features Setup 110
RPL 110
TCP/IP 110
Netware 111
PXE 111

Appendix E - SCSI BIOS 112

Features 113
Boot Initialization with BIOS Boot Specification (BBS) 113
CD-ROM Boot Initialization 113
Starting the SCSI BIOS Configuration Utility 113
Using the Configuration Utility 115
Screen Format 115
Header Area 115
Menu Area 115
Main Area 116
Footer Area 116
User Input 116
Main Menu 116
Field Descriptions 117
Adapter 117
PCI Bus 117
Dev/Func 118
Port Number 118
IRQ 118
NVM 118
Boot Order 118
LSI Logic Control 118
Global 118
Boot Adapter List 119
Field Descriptions 120
Adapter 120
PCI Bus 120
Dev/Func 120
Boot Order 120
Current Status 120
Next Boot 120
Global Properties 121
Field Descriptions 121

Pause When Boot Alert Displayed ... 121
Boot Information Display Mode ... 122
Negotiate With Devices ... 122
Video Mode ... 122
Support Interrupt ... 122
Restore Defaults ... 122
Adapter Properties ... 123
Field Descriptions ... 124
Device Properties ... 124
SCSI Parity ... 124
Host SCSI ID ... 124
SCSI Bus Scan Order ... 124
Removable Media Support ... 124
CHS Mapping ... 125
Spinup Delay (Secs) ... 125
Secondary Cluster Server ... 125
Termination Control ... 125
Restore Defaults ... 126
Device Properties ... 126
Field Descriptions ... 127
SCSI Device Identifier ... 127
Sync Rate (MB/Sec and MT/Sec) ... 127
Data Width ... 128
Scan ID ... 128
Scan LUNs > 0 ... 128
Disconnect ... 128
SCSI Timeout ... 128
Queue Tags ... 128
Boot Choice ... 129
Format ... 129
Verify ... 129
Restore Defaults ... 129
Exiting the SCSI BIOS Configuration Utility ... 130
Cancel Exit ... 130
Save changes then exit this menu ... 130
Discard changes then exit this menu ... 130
Cancel Exit ... 131
Exit the Configuration ... 131

Appendix F - Sample C Software ... 132

Directory \VME ... 132

Directory \fpga 132
Directory \include 133
Directory \max6657 133
Directory \support 133
Directory \vlm 133

List of Figures

Figure 1 VMIVME-7645 Block Diagram 16
Figure 1-1 VMIVME-7645 Board Layout and Jumper Locations 25
Figure 1-2 Installing a PMC Card on the VMIVME-7645 31
Figure 1-3 Front Panel LED Positions 33
Figure 1-4 Battery Removal 34
Figure 2-1 Connections for the PC Interrupt Logic Controller 46
Figure A-1 VMEbus Connector Diagram 67
Figure A-2 Serial Connector Pinouts 69
Figure A-3 Keyboard/Mouse Connector and Pinout 70
Figure A-4 Mouse/Keyboard Splitter Cable (p/n 360-000153-000) 71
Figure A-5 Ethernet Connector and Pinout 75
Figure A-6 USB Connector Pinout 76

List of Tables

Table 1-1	CPU Board Connectors	26
Table 1-2	Battery (Factory Configured) - Jumper (E3)	26
Table 1-3	Password Clear (User Configurable) - Jumper (E4)	26
Table 1-4	Boot Errors (User Configurable) - Jumper (E4)	27
Table 1-5	VME Jumper (User Configurable) - Jumper (E5)	27
Table 1-6	VME Jumper (User Configurable) - Jumper (E6)	27
Table 1-7	VME SYSFAIL (User Configurable) - Jumper (E6)	27
Table 1-8	SCSI Terminator (User Configurable) - Jumper (E8)	27
Table 1-9	Watchdog Timer (User Configurable) - Jumper (E9)	27
Table 2-1	VMIVME-7645, Universe II-Based Interface Memory Address Map	37
Table 2-2	VMIVME-7645 I/O Address Map	38
Table 2-3	PC Hardware Interrupt Line Assignments	40
Table 2-4	PC Interrupt Vector Table	41
Table 2-5	PCI Device Interrupt Mapping by the BIOS	45
Table 2-6	NMI Register Bit Descriptions	47
Table 2-7	Supported Graphics Video Resolutions	50
Table 2-8	PCI Configuration Space Registers	56
Table 2-9	Register Definitions Offset From BAR0	63
Table A-1	VMEbus Connector Pinout (bottom board)	67
Table A-2	Keyboard/Mouse Y Splitter Cable	71
Table A-3	PMC (J11) Connector Pinout	72
Table A-4	PMC (J12) Connector Pinout	73
Table A-5	PMC (J13) Connector Pinout	74

Overview

Introduction

GE Intelligent Platforms' VMIVME-7645 is a full-featured Pentium M computer in a single-slot, passively cooled, Eurocard form factor that utilizes the advanced technology of Intel's 855GME chipset running at a front-side bus rate of 400 MHz. The VMIVME-7645 is compliant with the VME Specification Rev. C.1 and features a transparent PCI-to-VME bridge, allowing the board to function as a system controller or peripheral CPU in multi-CPU systems.

The VMIVME-7645 provides features typically found on desktop systems such as:

- Up to 1GB PC2100 DDR SDRAM
- Built-in SVGA support with selectable size display cache
- Built-in 10/100 Mbit Ethernet
- Built-in dual Gigabit Ethernet
- Floppy drive support
- Four RS232 serial ports
- Three USB ports
- Real-Time clock/calendar
- Front panel reset switch
- Miniature speaker
- Keyboard/Mouse port

The 855GME chipset allows the VMIVME-7645 to provide enhanced features such as 400MHz front-side bus support. The VMIVME-7645 is capable of executing many of today's desktop operating systems such as Microsoft's Windows XP. The standard desktop features of the VMIVME-7645 are described in Chapter 2 of this manual.

The VMIVME-7645 provides features useful to embedded applications such as:

- I^2C bus support
- Remote Ethernet booting
- Up to 1 Gbytes of bootable compact flash (optional)
- Four general-purpose programmable timers (two 16-bit and two 32-bit)
- Software-selectable Watchdog Timer with reset

Additionally, the VMIVME-7645 offers a PMC expansion site with front-panel access. The VMIVME-7645 is capable of executing many of today's embedded operating systems such as VxWorks, QNX, Solaris, LynxOS and Microsoft's embedded Windows XP. The embedded features of the VMIVME-7645 are described in Chapter 3 of this manual.

The VMIVME-7645 is suitable for use in a variety of applications, such as: telecommunications, simulation, instrumentation, industrial control, process control and monitoring, factory automation, automated test systems, data acquisition systems and anywhere that the highest performance processing power in a single VME slot is desired.

Intel 855GME Chipset

The VMIVME-7645 incorporates the latest Intel chipset technology, the 855GME. This chipset departs from previous generation devices by utilizing a new Advanced Hub Architecture (AHA). The AHA allows for increased system performance by separating many high-bandwidth I/O accesses (like IDE or USB devices) from PCI accesses, relieving bottlenecks on the PCI bus. Furthermore, the 855GME chipset brings new levels of integration to motherboard chipsets and provides additional features over other chipsets.

The Hance Rapids I/O Controller Hub (ICH) incorporates much of the hardware for the VMIVME-7645's input/output ports, or drives the interfaces to which the controllers for the remainder of the I/O are connected. It includes support for two external PCI buses (32-bit 33MHz and 64-bit 66MHz), four USB ports, DMA controller, two 16550 serial ports, real-time clock, interrupt controller and Watchdog Timer.

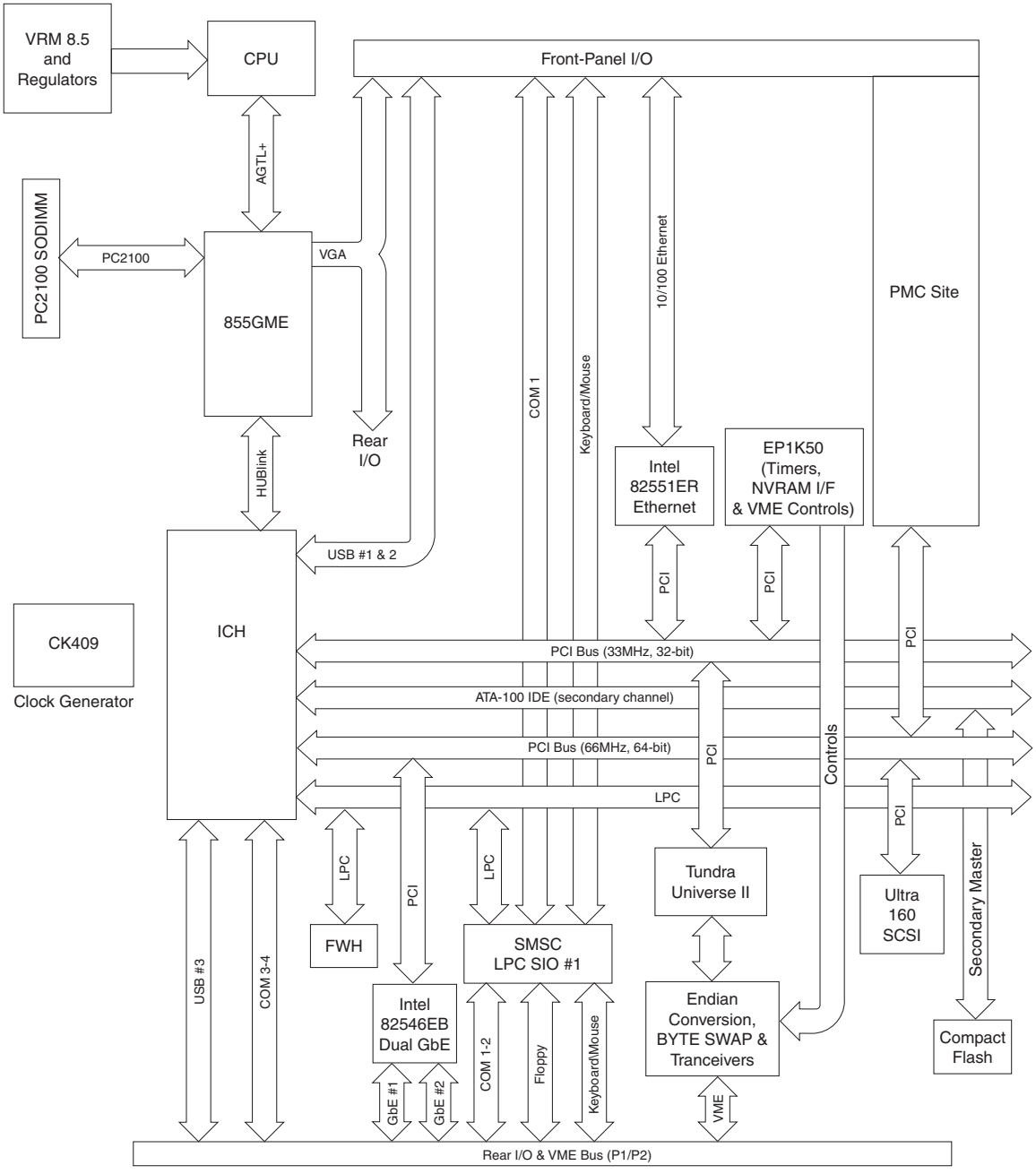


Figure 1 VMIVME-7645 Block Diagram

Organization of the Manual

This manual is composed of the following chapters and appendices:

Chapter 1 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup and operation of the VMIVME-7645.

Chapter 2 - Standard Features describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 3 - Embedded PC/RTOS Features describes the unit features that are beyond standard functions.

Chapter 4 - Maintenance provides information relative to the care and maintenance of the unit.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - System Driver Software provides details for installing drivers under Windows XP.

Appendix C - AMI BIOS describes the menus and options associated with the AMI (system) BIOS.

Appendix D - Argon BIOS describes the menus and options associated with the LAN Boot BIOS.

Appendix E - Sample C Software provides example code to use with the VMIVME-7645.

References

Intel Pentium M Processor
June 2003, Order Number 252612-002

Intel 855GM/GME Chipset Graphics and Memory Controller Hub (GMCH)
September 2003, Order Number 252615-002

Intel 80001 Hance Rapids I/O Controller Hub (ICH)
February 2003, Reference Number 13259

PCI Local Bus Specification, Rev. 2.1
PCI Special Interest Group
P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.)
(503) 797-4207 (International)
(503) 234-6762 (FAX)

LPC47M107S 100-Pin Enhanced Super I/O with LPC Interface

July 2000
SMSC
80 Arkay Dr.
Hauppage, NY 11788-8847
(631) 435-6000
(613) 273-3123 (FAX)

CMC Specification, P1386/Draft 2.0 from:
IEEE Standards Department
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VMISFT-9420 IOWorks Access User's Guide
Doc. No. 520-009420-910
VMIC
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.vmic.com

Tundra Universe II Based VMEbus Interface

Doc. No. 500-000211-000
VMIC
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616
www.vmic.com

For a detailed description and specification of the VME bus, please refer to:

VMEbus Specification Rev. C. and the VMEbus Handbook

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Scottsdale, AZ 85260
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(602) 951-0720 (FAX)
www.vita.com

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

VMIC assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VMIC for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING: Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

STOP informs the operator that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

WARNING denotes a hazard. It calls attention to a procedure, practice or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION denotes a hazard. It calls attention to an operating procedure, practice or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE denotes important information. It calls attention to a procedure, practice or condition which is essential to highlight.

Notation and Terminology

This product bridges the traditionally divergent worlds of Intel-based PC's and Motorola-based VMEbus controllers; therefore, some confusion over "conventional" notation and terminology may exist. Every effort has been made to make this manual consistent by adhering to conventions typical for the Motorola/VMEbus world; nevertheless, users in both camps should review the following notes:

- Hexadecimal numbers are listed Motorola-style, prefixed with a dollar sign: $F79, for example. By contrast, this same number would be signified 0F79H according to the Intel convention, or 0xF79 by many programmers. Less common are forms such as $F79_h$ or the mathematician's $F79_{16}$.
- An 8-bit quantity is termed a "byte," a 16-bit quantity is termed a "word," and a 32-bit quantity is termed a "longword." The Intel convention is similar, although their 32-bit quantity is more often called a "doubleword."
- Motorola programmers should note that Intel processors have an I/O bus that is completely independent from the memory bus. Every effort has been made in the manual to clarify this by referring to registers and logical entities in I/O space by prefixing I/O addresses as such. Thus, a register at "I/O $140" is not the same as a register at "$140," since the latter is on the memory bus while the former is on the I/O bus.
- Intel programmers should note that addresses are listed in this manual using a linear, "flat-memory" model rather than the old segment:offset model associated with Intel Real Mode programming. Thus, a ROM chip at a segment:offset address of C000:0 will be listed in this manual as being at address $C0000. For reference, here are some quick conversion formulas:

Segment:Offset to Linear Address

Linear Address = (Segment × 16) + Offset

Linear Address to Segment:Offset

Segment = ((Linear Address ÷ 65536) − *remainder*) × 4096

Offset = *remainder* × 65536

Where *remainder* = the fractional part of (Linear Address ÷ 65536)

Note that there are many possible segment:offset addresses for a single location. The formula above will provide a unique segment:offset address by forcing the segment to an even 64 Kbyte boundary, for example, $C000, $E000, etc. When using this formula, make sure to round the offset calculation properly!

CHAPTER

1

Installation and Setup

Contents

Unpacking Procedures 23
Hardware Setup 24
Installation 29

Introduction

This chapter describes the hardware jumper settings, connector descriptions, installation, system setup and operation of the VMIVME-7645.

Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC Customer Care along with a request for advice concerning the disposition of the damaged item(s).

CAUTION: Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

Hardware Setup

The VMIVME-7645 is factory populated with user-specified options as part of the VMIVME-7645 ordering information. The CPU speed, RAM size and flash memory size are not user-upgradable. To change CPU speeds or RAM/Flash size, contact Customer Care to receive a Return Material Authorization (RMA).

Technical support is available at: 1-800-240-7782.

Or E-mail us at customer.service@vmic.com

The VMIVME-7645 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the single board CPU are illustrated in Figure 1-1 on page 25. The definitions of the CPU board jumpers and connectors are included in Table 1-1 through Table 1-9.

CAUTION: All jumpers marked *User Configurable* in the following tables may be changed or modified by the user. All jumpers marked factory configured should not be modified by the user.

Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit.

Modifying any jumper not marked "User Configurable" will void the Warranty and may damage the unit. The default jumper condition of the VMIVME-7645 is expressed in Table 1-1 through Table 1-9 with **bold text** in the table cells.

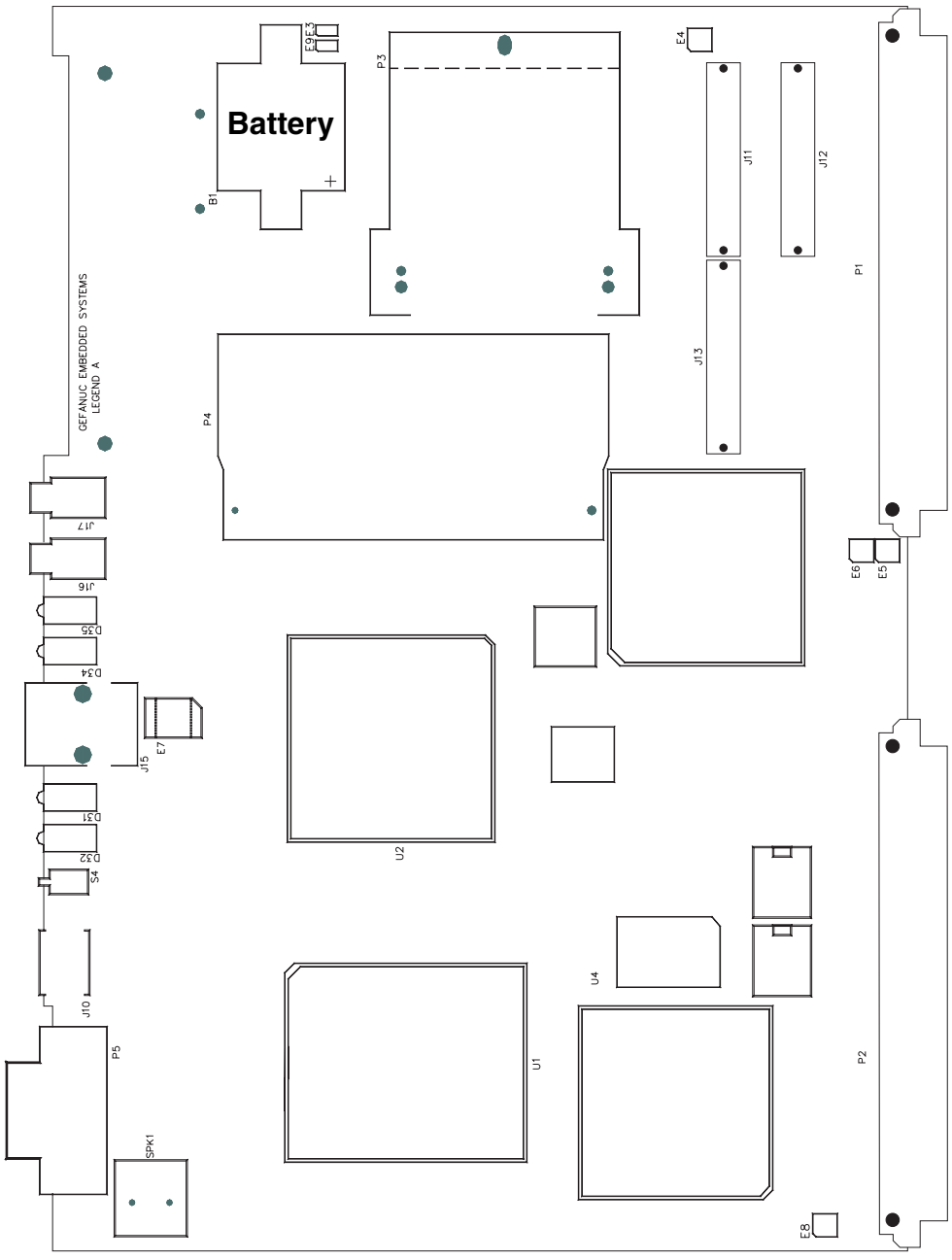


Figure 1-1 VMIVME-7645 Board Layout and Jumper Locations

Table 1-1 CPU Board Connectors

Connector	Function
J9	ITP
J10	Mouse/Keyboard
J11, J12, J13	PMC Slot 1
J15	Ethernet 3 (10/100Mbit)
J16, J17	USB
P1, P2	VME
P3	IDE (Sec)
P5	COM 1

Table 1-2 Battery (**Factory Configured**) - Jumper (E3)

Select	Jumper Position
Connect Battery	**On**
Disconnect Battery	Off

NOTE: The BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper allows the user to clear the password in the case of a forgotten password.

To clear the CMOS password:

1. Turn off power to the unit.
2. Momentarily short pins 1 and 2 of E4 for approximately five seconds.
3. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared.

Table 1-3 Password Clear (**User Configurable**) - Jumper (E4)

Select	Jumper Position
Normal	**Off**
Clear CMOS/Password	1-2

Table 1-4 Boot Errors (**User Configurable**) - Jumper (E4)

Select	Jumper Position
Boot with POST Errors	**3-4**
Halt on Error	Off

Table 1-5 VME Jumper (**User Configurable**) - Jumper (E5)

Select	Jumper Position
Enable VME SYSRESET Driver	**1-3**
Enable SYSRESET Receiver	**2-4**

Table 1-6 VME Jumper (**User Configurable**) - Jumper (E6)

Select	Jumper Position
Map UNIV2 to I/O Space	**1-2**

Table 1-7 VME SYSFAIL (**User Configurable**) - Jumper (E6)

Select	Jumper Position
SYSFAIL during Reset	**Pins 3-4 On**
SYSFAIL under Software Control	Pins 3-4 Off

Table 1-8 SCSI Terminator (**User Configurable**) - Jumper (E8)

Select	Jumper Position
Disable Termination	1-2
Auto Termination	**3-4**

Table 1-9 Watchdog Timer (**User Configurable**) - Jumper (E9)

Select	Jumper Position
Enabled	**On**
Disabled	Off

Power Requirements

The VMIVME-7645 requires +5V, +12V and -12V from the VME backplane. Below are the voltage and current requirements.

Supply	Current (Typical)	Current (Maximum)
+5V	6.4A	12A
+12V	0.00A	750mA*
-12V	0.00A	750mA*

** If a PMC card is installed.*

The VMIVME-7645 provides power to the PMC site in accordance with the PMC specification. The maximum current provided on the +5V supply is 1.5A per PMC site. The maximum current provided on the +3.3V supply is 1.5A.

The +12V and -12V supplies are provided to the PMC site. The total +12V or -12V current provided to the VMIVME-7645 PMC site must not exceed 750mA each, in accordance with the VMEbus Specification.

Installation

The VMIVME-7645 conforms to the VMEbus physical specification for a single slot 6U dual Eurocard (dual height). However, it can not be plugged directly into any standard chassis accepting this type of board. The custom nature of the VME P2 connector prohibit its use in any chassis for which it is not intended.

CAUTION: Do not install or remove the board while power is applied.

The following steps describe the VMIC recommended method for VMIVME-7645 installation and power-up:

1. Make sure power to the equipment is off.
2. The VMIVME-7645 ***must*** be attached to a custom P1/P2 VMEbus backplane, and in the first (left most) slot in the chassis.

   The VMIVME-7645 does not require jumpers for enabling/disabling the system controller function.

NOTE: Air flow requirements as measured at output side of heatsink is to be greater than 350LFM.

3. Connect all needed peripherals to the front and rear panels. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A. Minimally, a keyboard and a monitor are required if the user has not previously configured the system.
4. Apply power to the system. Several messages are displayed on the screen, including names, versions and copyright dates for the various BIOS modules on the VMIVME-7645.
5. If an external drive module is installed, the BIOS Setup program must be run to configure the drive types. See Appendix C to properly configure the system.
6. If a drive module is present, install the operating system according to the manufacturer's instructions.

See Appendix B for instructions on installing VMIVME-7645 peripheral driver software during operating system installation.

BIOS Setup

The VMIVME-7645 has an on-board BIOS Setup program that controls many configuration options. These options are saved in a special non-volatile, battery-backed memory chip and are collectively referred to as the board's 'CMOS Configuration'. The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

Details of the VMIVME-7645 BIOS setup program are included in Appendix C.

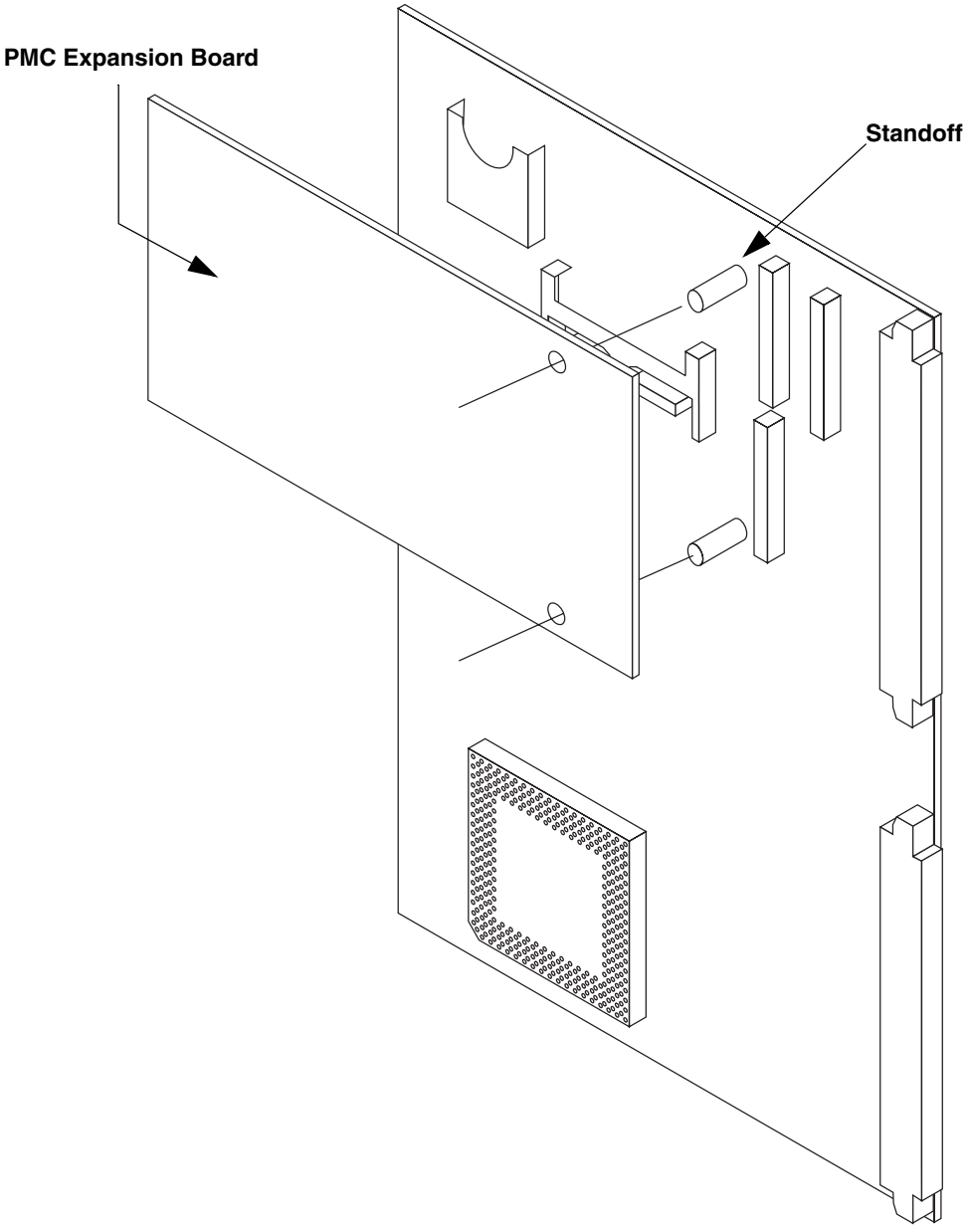


Figure 1-2 Installing a PMC Card on the VMIVME-7645

Front/Rear Panel Connectors

The VMIVME-7645 provides front-panel access to the PMC expansion site, a 10/100 Ethernet connector, the manual reset switch, COM 1, dual USB and the status LEDs. A drawing of the VMIVME-7645 front-panel is shown in Figure 1-3. The front-panel connectors and indicators are labeled as follows:

- 10/100/1000 — 10/100/1000 Mbit Ethernet connector
- RST — Manual reset switch
- COM 1 — COM port 1
- M/K — Dual mouse/keyboard connector
- USB 1 — USB port 1 connector
- USB 2 — USB port 2 connector
- BOOT — Boot status
- POWER — Power status
- SCSI — SCSI activity
- FAIL — VME SYSFAIL status
- GBE 1 — Gigabit Ethernet channel 1 status
- GBE 2 — Gigabit Ethernet channel 2 status

The VMIVME-7645 provides rear I/O support for the following: dual Gigabit Ethernet, Ultra 160 SCSI, USB, keyboard, mouse, COM 1-4, SVGA and floppy drive. These signals are accessed by the use of a rear-panel transition board.

The front panel connectors, including connector pinouts and orientation, for the VMIVME-7645 are defined in Appendix A.

LED Definition

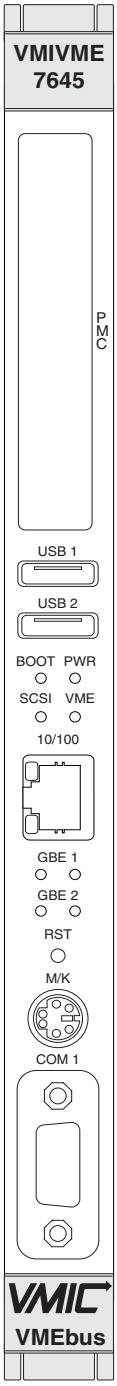


Figure 1-3 Front Panel LED Positions

BOOT	*Booting* - Indicates BIOS Boot is in progress. When LED is off, CPU has finished POST and is ready, (Red LED).
PWR	*Power* - Indicates when power is applied to the board, (Green LED).
SCSI	*SCSI Indicator* - Indicates when SCSI activity is occurring, (Green LED).
VME	*VME failure*- Lights during VME SYSFAIL condition, (Red LED).
10/100 (Top)	Indicates both Ethernet link integrity and activity when flashing, (Green LED).
10/100 (Bottom)	Indicates whether 10BaseT or 100BaseTx mode. Off indicates 10BaseT, Yellow indicates 100BaseTx.
GBE 1/2 (Left)	Indicates both Ethernet link integrity and activity when flashing, (Yellow LED).
GBE 1/2 (Right)	Indicates whether 10BaseT, 100BaseT or 1000BaseTx mode. Off indicates 10BaseT, Yellow LED indicates 100BaseT and Green LED indicates 1000BaseTx.
RST	*Reset* - Allows the system to be reset from the front panel.

Battery Mounted in Clip-Style Holder

For Battery Removal:

1. Locate the battery on the computer. You may need to reference the Product Manual if it is not easily located. See Figure 1-1.

2. Once the battery is located, take a non-conductive tool and gently push on the edges of the battery to slide it from the socket.

The battery should slide forward out of the holder.

a) Pressure can be alternated between the two sides to allow the battery to slide out of the socket.

b) The battery should slide forward enough so that it can be removed from the socket.

For Battery Installation:

1. Observe correct polarity.
2. Press the new battery into the socket until the battery snaps into place.

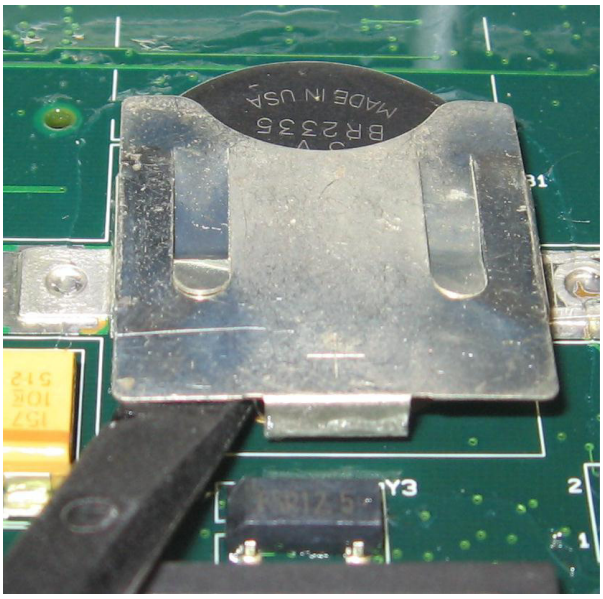


Figure 1-4 Battery Removal

CHAPTER
2

Standard Features

Contents

CPU Socket 36
Physical Memory 36
Memory and Port Maps 37
I/O Port Map 38
Interrupts. 40
Integrated Peripherals. 48
Ethernet Controllers 49
Video Graphics Adapter 50
Universal Serial Bus. 51
Dual Ultra 160 SCSI 52

Introduction

The VMIVME-7645 is an Intel Pentium M processor-based single board computer compatible with modern industry standard desktop systems. The VMIVME-7645 therefore retains industry standard memory and I/O maps along with a standard interrupt architecture. The integrated peripherals described in this section (such as serial ports, USB ports, IDE drive, floppy drive, video controller and Ethernet controllers) are all memory mapped the same as similarly equipped desktop systems, ensuring compatibility with modern operating systems.

The following sections describe the standard features of the VMIVME-7645.

CPU Socket

The VMIVME-7645 CPU socket is factory populated with a high-speed Pentium M processor. The CPU speed and RAM/flash size are user specified as part of the CMOS set-up information.

To change CPU speeds, reboot the CPU and enter CMOS set-up by pressing the “Del” key.

VMIC Customer Care is available at: 1-800-240-7782.

Physical Memory

The VMIVME-7645 provides Dual Data Rate (DDR) Synchronous DRAM (SDRAM) as on-board system memory. Memory can be accessed as bytes, words or longwords.

The VMIVME-7645 accepts one 200-pin SDRAM SODIMM for a maximum capacity of 1 Gbytes. The on-board DRAM is dual-ported to the VME bus through the PCI-to-VME bridge and is addressable by the local processor, as well as the VMEbus slave interface by another VMEbus master. Caution must be used when sharing memory between the local processor and the VMEbus to prevent a VMEbus master from overwriting the local processor’s operating system.

NOTE: Memory capacity may be extended as parts become available.

Memory and Port Maps

Memory Map - Tundra Universe II-Based PCI-to-VMEbus Bridge

The memory map for the Tundra Universe II-based interface VMIVME-7645 is shown in Table 2-1. All systems share this same memory map, although a VMIVME-7645 with less than the full 256 Mbyte of SDRAM does not fill the entire space reserved for On-Board Extended Memory.

Table 2-1 VMIVME-7645, Universe II-Based Interface Memory Address Map

MODE	MEMORY ADDRESS RANGE	SIZE	DESCRIPTION
PROTECTED MODE	$FFFF 0000 - $FFFF FFFF	64 Kbyte	ROM BIOS Image
	$0400 0000 - $FFFE FFFF	3.9 Gbyte	Unused *
	$0010 0000 - $0FFF FFFF	255 Mbyte	Reserved for ** On-Board Extended Memory (not filled on all systems)
REAL MODE	$E0000 - $FFFFF	128 Kbyte	Reserved
	$D8018 - $DFFFF	32 Kbyte	Reserved
	$D8016 - $D8017	2 bytes	Reserved
	$D8014 - $D8015	2 bytes	Reserved
	$D8010 - $D8013	2 bytes	Reserved
	$D800E - $D800F	2 bytes	Reserved
	$D8000 - $D800D	14 bytes	Reserved
	$C8000 - $D7FFF	64 Kbyte	Reserved
	$C0000 - $C7FFF	32 Kbyte	Reserved
	$A0000 - $BFFFF	128 Kbyte	Reserved
	$00000 - $9FFFF	640 Kbyte	Reserved

* This space can be used to set up protected mode PCI-to-VMEbus windows (also referred to as PCI slave images). BIOS will also map on-board PCI based NVRAM, Timers and Watchdog Timers in this area.

** This space can be allocated as shared memory (for example, between the Pentium processor-based CPU and VMEbus Master). Note that if a PMC board is loaded, the expansion BIOS may be placed in this area.

I/O Port Map

Like a desktop system, the VMIVME-7645 includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. Thus, the CPU includes an independent 64 Kbyte I/O address space, which is accessible as bytes, words or longwords.

Standard hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals, such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 2-2.

Table 2-2 VMIVME-7645 I/O Address Map

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$000 - $00F	16	ICH	DMA Controller 1 (Intel 8237A Compatible)
$010 - $01F	16		Reserved
$020 - $021	2	ICH	Master Interrupt Controller (Intel 8259A Compatible)
$022 - $03F	30		Reserved
$040 - $043	4	ICH	Programmable Timer (Intel 8254 Compatible)
$044 - $05F	30		Reserved
$060 - $064	5	Super I/O Chip	Keyboard, Speaker, System Configuration (Intel 8042 Compatible)
$065 - $06F	11		Reserved
$070 - $071	2	ICH	Real-Time Clock
$072 - $07F	14		Reserved
$080 - $08F	16	ICH	DMA Page Registers
$090 - $091	2		Reserved
$092	1	ICH	Alt. Gate A20/Fast Reset Register
$093 - $09F	11		Reserved

Table 2-2 VMIVME-7645 I/O Address Map (Continued)

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$0A0 - $0A1	2	ICH	Slave Interrupt Controller (Intel 8259A Compatible)
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32	ICH	DMA Controller 2 (Intel 8237A Compatible)
$0E0 - $16F	142		Reserved
$170 - $177	8	ICH	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	ICH	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	ICH	COM4 Serial I/O
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	ICH	COM3 Serial I/O
$3F0 - $3F7	8	Super-I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $4FF	256		Reserved
$500 - CFF	2048		Reserved

Interrupts

System Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 2-3 along with their functions. Table 2-4 on page 41 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 2-4 on page 41.

The interrupt hardware implementation on the VMIVME-7645 is standard for computers built around the PC architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 2-1 on page 46.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 2-3 PC Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by VMIVME-7645 PCIbus Interface
0	System Timer	Set by BIOS
1	Keyboard	Set by BIOS
2	Duplexed to IRQ9	
3	COM2	
4	COM1	
5	COM3	Set by BIOS
6	Floppy Controller	
7	COM4	Set by BIOS
8	Real-Time Clock	
9	Old IRQ2	SVGA or Network I/O

Table 2-3 PC Hardware Interrupt Line Assignments (Continued)

IRQ	AT FUNCTION	COMMENTS
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	Not available for use
14	Not assigned	Determined by BIOS
15	Not assigned	Determined by BIOS

Table 2-4 PC Interrupt Vector Table

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VME Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	COM3 Serial I/O	Access Overrun
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	COM4 Serial I/O	Reserved
10	16		BIOS Video I/O	Coprocessor Error
11	17		System Configuration Check	Same as Real Mode

Table 2-4 PC Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26		Time of Day	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode

Table 2-4 PC Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-6F	103-111		Reserved by DOS	Same as Real Mode
70	112	IRQ8	Real Time Clock	
71	113	IRQ9	Redirect to IRQ2	
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	Not assigned	
77	119	IRQ15	Not assigned	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 2-1 on page 46 depicts the VMIVME-7645 interrupt logic pertaining to VME operations and the PMC site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line, or each may have its own (up to a maximum of four functions), or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the VME interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

PCI Device Interrupt Map

The VMIVME-7645 has three PCI buses; two of which are external. Bus 0 is the bus on which devices internal to the Hance Rapids ICH are accessed. Bus 1 is a 32-bit/33MHz bus. Bus 2 is a 64-bit/66MHz bus. The PCI bus-based external devices include the PMC site, Ethernet controllers and the PCI-to-VME bridge. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the ICH. This mapping is illustrated in Figure 2-1 on page 46 and is defined in Table 2-5.

The device PCI interrupt lines (INTA through INTD) that are present on each device cannot be modified.

Table 2-5 PCI Device Interrupt Mapping by the BIOS

Device	Component	PCI Bus No.	Vendor ID	Device ID	CPU Address Map ID Select	PCI IRQ	Request/ Grant Line
Hub to PCI 0 Bridge	Intel 80001 (Hance Rapids ICH)	0	0x8086	0x244E	AD41	N/A	N/A
Hub to PCI 1 Bridge	Intel 80001	0	0x8086	0x25A0		N/A	N/A
LPC Bridge	Intel 80001	0	0x8086	0x25A1	AD42	N/A	N/A
SM Bus Controller	Intel 80001	0	0x8086	0x25A4		N/A	N/A
USB UHCI #1	Intel 80001	0	0x8086	0x25A9	AD40	N/A	N/A
USB UHCI #2	Intel 80001	0	0x8086	0x25AA	AD40	N/A	N/A
Watchdog Timer	Intel 80001	0	0x8086	0x25AB		N/A	N/A
Interrupt Controller	Intel 80001	0	0x8086	0x25AC		N/A	N/A
USB EHCI	Intel 80001	0	0x8086	0x25AD		N/A	N/A
Hub to PCI 2 Bridge	Intel 80001	0	0x8086	0x25AE	AD39	N/A	N/A
Host Bridge	Intel 80001	0	0x8086	0x3580	AD11	N/A	N/A
VGA controller	Intel 80001	0	0x8086	0x3582	AD13	N/A	N/A
Ethernet Controller	Intel 82551ER	1	0x8086	0x1209	AD28	INTF	1
PCI to VME Bridge	Tundra Universe II	1	0x10E3	0x0000	AD29	INTA	0
Timer FPGA	VMIC Proprietary	1	0x114A	0x0004	AD27	INTD	N/A
PMC site	N/A	2	N/A	N/A	AD30	INTC	3
Ultra 160 SCSI	LSI53C1000R	2	0x1000	0x0021	AD19	INTE	2
Gbe LAN #1	Intel 82546EB	2	0x8086	0x1010	AD21	INTA	0
Gbe LAN #2	Intel 82546EB	2	0x8086	0x1010	AD21	INTB	0

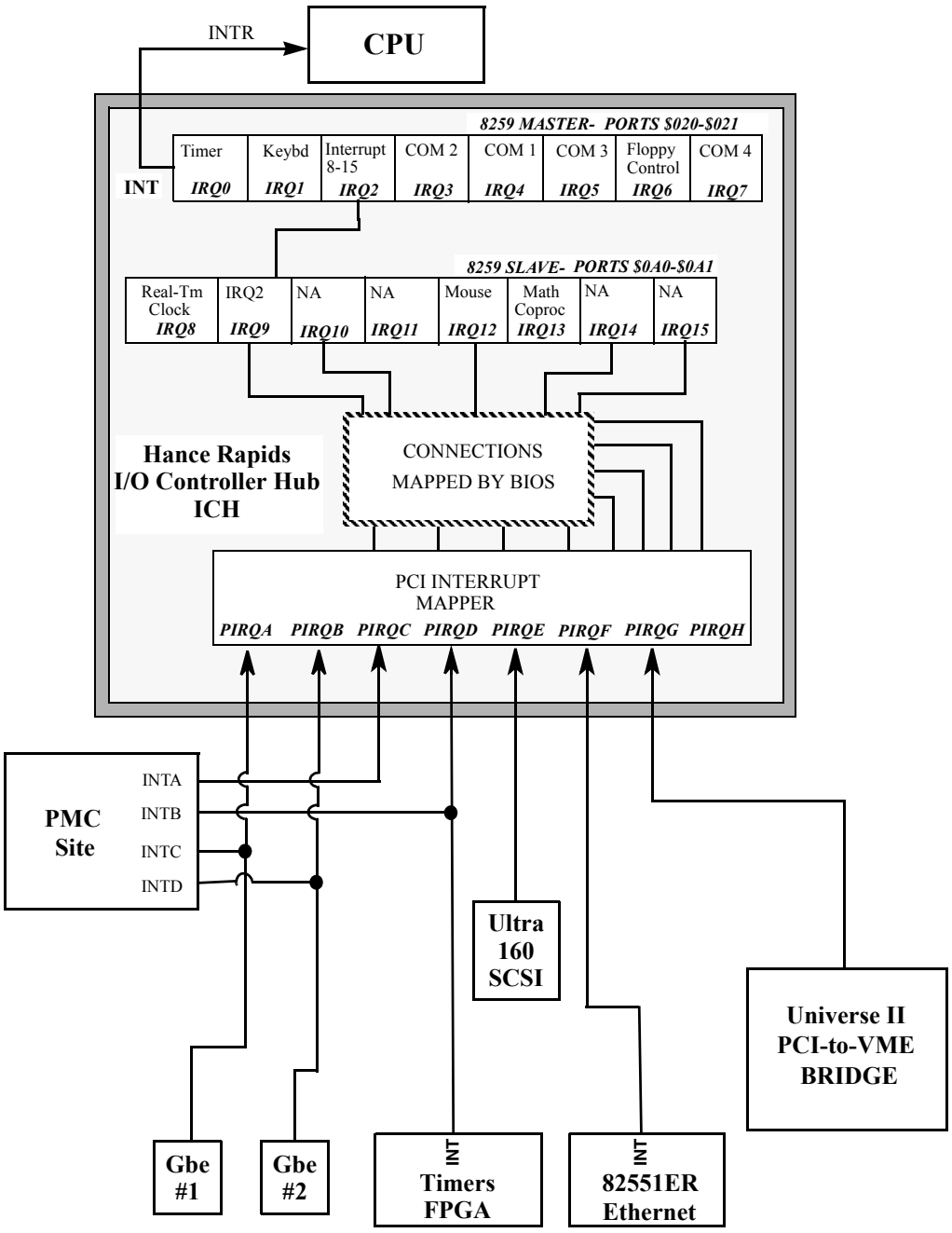


Figure 2-1 Connections for the PC Interrupt Logic Controller

The PCI-to-VME Bridge has the capability of generating a Non-Maskable Interrupt (NMI) via the PCI SERR# line. Table 2-6 describes the register bits that are used by the NMI. The SERR interrupt is routed through logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable/disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable/enable all NMI sources.

Table 2-6 NMI Register Bit Descriptions

Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set Bit 2 to 0 and then set it to 1. When writing to port $061, Bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read/Write) - 1 = Clear and Disable, 0 = Enable
Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

Integrated Peripherals

The VMIVME-7645 incorporates an SMSC Super I/O (SIO) chip. The SIO provides the VMIVME-7645 with a standard floppy drive controller, two 16550 UART-compatible serial ports, keyboard and mouse ports and general purpose I/O for system monitoring functions. Both serial port signals are available from the rear panel. COM 1 is also available on the front panel. The floppy signals are available via the P2 backplane connector.

Ethernet Controllers

The triple network capability is provided by the external Intel 82551ER Ethernet Controller and by the Intel dual Gigabit Ethernet 82546EB chip. Both Ethernet controllers are PCI-based and are software configurable. The 82546EB supports dual 10BaseT, 100BaseTx and 1000BaseT Ethernet.

10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ-45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 meters.

100BaseTx

The VMIVME-7645 also supports the 100BaseTx Ethernet. A network based on a 100BaseTx standard uses unshielded twisted-pair cables and a RJ-45 connector. 100BaseTx has a maximum length of 100 meters.

1000BaseT

The VMIVME-7645 also supports the 1000BaseT Ethernet. A network based on a 1000BaseT standard uses unshielded twisted-pair cables and a RJ-45 connector. 1000BaseT has a maximum length of 100 meters.

Video Graphics Adapter

The SVGA port on the VMIVME-7645 is controlled by the Intel 855GME Graphic and Memory Controller Hub (GMCH) chip. The GMCH is hardware and BIOS compatible with the industry EGA and SVGA standards supporting both VESA high-resolution and extended video modes. Table 3-5 shows the graphics video modes supported by the GMCH video controller.

Table 2-7 Supported Graphics Video Resolutions

Screen Resolution	Maximum Colors	Maximum Refresh Rates (Hz)
800 x 600	32 bit	120
1024 x 768	32 bit	120
1280 x 1024	32 bit	120
1152 x 864	32 bit	85
1400 x 1050	32 bit	85
1600 x 1200	32 bit	85
1856 x 1392	32 bit	75
1920 x 1440	32 bit	75
2048 x 1536	32 bit	75

Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

Universal Serial Bus

The VMIVME-7645 provides a dual Universal Serial Bus (USB) connection on the front panel, and an additional port over the VME connectors at the rear. The on-board USB controllers completely support the standard USB interface.

The USB Host Controller moves data between system memory and the USB by processing and scheduling data structures. The controller executes the scheduled lists, and reports status back to the system.

Dual Ultra 160 SCSI

The VMIVME-7645's dual 160 SCSI interface makes the unit ideal for embedded applications, particularly applications where standard hard drives and floppy disk drives cannot be used.

The VMIVME-7645 Dual-Channel Ultra160 SCSI Host Adapter incorporates the LSI Logic LPC53C1000, a highly integrated PCI Single-Channel Ultra160 SCSI controller. The LPC53C1000 is 100 percent compatible with the Ultra160 SCSI initiative and provides additional features that ensure robust Ultra160 system operation. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the LPC53C1000. Double transition clocking enables throughput of up to 160 Mbytes without increasing the interface clock rate.

The LPC53C1000 uses the same CRC algorithm used by FDDI, Ethernet and Fibre Channel, and detects single bit errors, double bit errors, odd number of errors, and all burst errors up to 32 bits long. To provide complete end-to-end protection of the SCSI I/O, AIP protects all non-data phases, augmenting the CRC feature of Ultra160. SureLINK domain validation technology detects the configuration of the SCSI bus and automatically tests and adjusts the SCSI transfer rate to optimize inter-operability. The LPC53C1000 controller and Ultra160 provide Basic (Level 1) and Enhanced (Level 2) domain validation, while the LPC53C1000 has an added feature of Margining (Level 3) domain validation.

PCI Interface

The Ultra160 SCSI PCI Interface complies with *PCI Local Bus Specification Revision 2.2*, and implements a 64-bit/66 MHz PCI bus. The LPC53C1000 complies with *PCI Power Management Interface Specification Revision 1.1* and *PC 99*, supporting power states D0, D1, D2, D3hot and D3cold, power management capabilities registers, and programmable values for PCI Subsystem Vendor ID and Subsystem ID. Extended access cycles (Memory Read Line, Memory Read Multiple, and Memory Write and Invalidate) are also supported.

Ultra160 SCSI Memory

The BIOS for the LPC53C1000 is located within the system BIOS. A serial 2-wire interface provides a connection to an external serial EEPROM for storing the Subsystem Vendor ID and Subsystem ID.

Ultra160 SCSI Processor

The LPC53C1000 provides an Ultra160 SCSI controller on a single chip. The controller supports wide Ultra160 SCSI synchronous transfer rates up to 160 Mbytes on a LVD SCSI bus. Integrated LVDlink transceivers support both LVD and single-ended signals with no external transceivers required. Fast SCSI, Ultra SCSI, Ultra2 SCSI and Ultra160 SCSI are all supported by the LPC53C1000. An on-chip SCSI clock

quadrupler allows the chip to achieve Ultra160 SCSI transfer rates with an input frequency of 40 MHz. The 8 Kbytes of internal RAM for SCRIPTS instruction storage allow all accesses to remain internal, reducing the time spent on the PCI bus. A 944-byte DMA FIFO on each channel allows the device to efficiently burst up to 512 bytes across the PCI bus. SCSI bus phase mismatches are handled in SCRIPTS, reducing CPU utilization.

Ultra160 SCSI Termination

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI devices are present on the bus. The SCSI Host Adapter uses the UCC5630A termination ICs to automatically sense the SCSI bus and switch the termination to either single ended (SE) or low voltage differential (LVD) SCSI, dependent on which type of devices are connected to the bus. The UCC5630A termination IC is used in multi-mode active termination applications, where SE and LVD devices might coexist. The UCC5630A has both SE and LVD termination networks integrated into a single monolithic component. The correct network is automatically determined by the SCSI bus "DIFSENS" signal. The SCSI bus DIFSENS signal line is used to identify which types of SCSI devices are present on the bus. On power-up, the UCC5630A DIFSENS drivers will attempt to deliver 1.3V to the DIFSENS line.

If only LVD devices are present, the DIFSENS line will be successfully driven to 1.3 V and the terminators will configure for LVD operation. If any single ended devices are present, they will present a short to ground on the DIFSENS line, signaling the UCC5630A(s) to configure into the SE mode, accommodating the SE devices. Or, if any high voltage differential (HVD) devices are present, the DIFSENS line is pulled high and the terminator will enter a high impedance state, effectively disconnecting from the bus.

Media Connection

An external adapter is required to connect the SCSI interface from the VME P2 connector to a standard SCSI connector.

CHAPTER

3

Embedded PC/RTOS Features

Contents

VMEbus Bridge 55
Embedded PCI Functions 56
Timers 57
VME Control 63

Introduction

VMIC's VMIVME-7645 features additional capabilities beyond those of a typical desktop computer system. The unit provides four software-controlled, general-purpose timers for synchronizing and controlling multiple events in embedded applications. Also, the VMIVME-7645 supports an embedded intelligent VME bridge to allow compatibility with the most demanding VME applications.

VMEbus Bridge

In addition to its PC/AT functions, the VMIVME-7645 has the following VMEbus features:

- Complete six-line Address Modifier (AM-Code) programmability
- VME data interface with separate hardware byte/word swapping for master and slave accesses
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VMEbus arbiter (PRI, SGL and RRS modes are supported)
- VMEbus BERR bus error timer (software programmable)
- Slave access from the VMEbus to local RAM and mailbox registers
- Full-featured programmable VMEbus requester (ROR, RWD and BCAP modes are supported)
- System Controller auto detection
- Complete VMEbus master access through five separate Protected-mode memory windows

The VMIVME-7645 supports High Throughput DMA transfers of bytes and words in both Master and Slave configurations.

If Endian conversion is not needed, VMIC offers a special “Bypass” mode that can be used to further enhance throughput (not available for byte transfers).

The VMIVME-7645 VMEbus interface is provided by the PCI-to-VMEbus bridge built around the Tundra Semiconductor Corporation Universe II VMEbus interface chip. The Universe II provides a reliable high-performance 64-bit VMEbus-to-PCI interface in one design. The functions and programming of the Universe-based VMEbus interface are addressed in detail in a companion manual titled: *VMIC’s Tundra Universe II Based VMEbus Interface Product Manual (500-000211-001)*.

Embedded PCI Functions

The VMIVME-7645 provides Timers via the PCI bus. These functions are required for embedded and real time applications. The PCI configuration space of these embedded functions are shown below.

Table 2-8 PCI Configuration Space Registers

31 16	15 00	Register Address
Device ID 0004	Vendor ID 114A	00h
Status	Command	04h
Class Code	Revision ID	08h
BIST / Header Type	Latency Timer / Cache Line Size	0Ch
PCI Base Address 0 for Memory-Mapped VME Control registers (BAR0)		10h
PCI Base Address 1 for memory-mapped timers (BAR1)		14h
Reserved		18h
Reserved		1Ch
Reserved		20h
Reserved		24h
Reserved		28h
Subsystem ID 7645	Subsystem Vendor ID 114A	2Ch
Reserved		30h
Reserved		34h
Reserved		38h
Max_Lat / Min_gnt	Interrupt Pin / Interrupt Line	3Ch

The “Device ID” field indicates that the device is for VME products (00) and indicates the supported embedded feature set.

The “Vender ID” and “Subsystem Vendor ID” fields indicate VMIC’s PICMG assigned Vender ID (114A).

The “Subsystem ID” field indicates the model number of the product (7645).

Timers

General

The VMIVME-7645 provides four user-programmable timers (two 16-bit and two 32-bit) which are completely dedicated to user applications and are not required for any standard system function. Each timer is clocked by independent generators with selectable rates of 2MHz, 1MHz, 500kHz and 250kHz. Each timer may be independently enabled and each is capable of generating a system interrupt on timeout.

Events can be timed by either polling the timers or enabling the interrupt capability of the timer. A status register allows for application software to determine which timer is the cause of any interrupt.

Timer Control Status Register 1 (TCSR1)

The timers are controlled and monitored via the Timer Control Status Register 1 (TCSR1) located at offset 0x00 from the address in BAR2. The mapping of the bits in this register are as follows:

Field	Bits	Read or Write
Timer 1 Caused IRQ	TCSR1[0]	R/W
Timer 1 Enable	TCSR1[1]	R/W
Timer 1 IRQ Enable	TCSR1[2]	R/W
Timer 1 Clock Select	TCSR1[4..3]	R/W
Timer 2 Caused IRQ	TCSR1[8]	R/W
Timer 2 Enable	TCSR1[9]	R/W
Timer 2 IRQ Enable	TCSR1[10]	R/W
Timer 2 Clock Select	TCSR1[12..11]	R/W
Timer 3 Caused IRQ	TCSR1[16]	R/W
Timer 3 Enable	TCSR1[17]	R/W
Timer 3 IRQ Enable	TCSR1[18]	R/W
Timer 3 Clock Select	TCSR1[20..19]	R/W
Timer 4 Caused IRQ	TCSR1[24]	R/W
Timer 4 Enable	TCSR1[25]	R/W
Timer 4 IRQ Enable	TCSR1[26]	R/W
Timer 4 Clock Select	TCSR1[28..27]	R/W
Reserved	All Other Bits	R/W

All of these bits default to "0" after system reset.

Each timer has an independently selectable clock source which is selected by the bit pattern in the “Timer x Clock Select” field as follows:

Clock Rate	MSb	LSb
2MHz	0	0
1MHz	0	1
500kHz	1	0
250kHz	1	1

Each timer can be independently enabled by writing a “1” to the appropriate “Timer x Enable” field. Similarly, the generation of interrupts by each timer can be independently enabled by writing a “1” to the appropriate “Timer x IRQ Enable” field.

If an interrupt is generated by a timer, the source of the interrupt may be determined by reading the “Timer x Caused IRQ” fields. If the field is set to “1”, then the respective timer caused the interrupt. Note that multiple timers can cause a single interrupt. Therefore, the status of all timers must be read to ensure that all interrupt sources are recognized.

A particular timer interrupt can be cleared by writing a “0” to the appropriate “Timer x Caused IRQ” field. Alternately, a write to the appropriate Timer x IRQ Clear (TxIC) register will also clear the interrupt. When clearing the interrupt using the “Timer x Caused IRQ” fields, note that it is very important to ensure that a proper bit mask is used so that other register settings are not affected. The preferred method for clearing interrupts is to use the “Timer x IRQ Clear” registers described below.

Timer Control Status Register 2 (TCSR2)

The timers are also controlled by bits in the Timer Control Status Register 2 (TCSR2) located at offset 0x04 from the address in BAR2. The mapping of the bits in this register are as follows:

Field	Bits	Read or Write
Read Latch Select	TCSR2[0]	R/W
Reserved	All Other Bits	R/W

All of these bits default to “0” after system reset.

The “Read Latch Select” bit is used to select the latching mode of the programmable timers (See “Timers” section above). If this bit is set to “0”, then each timer output is latched upon a read of any one of its address. For example, a read to the TMRCCR12 register latches the count of timers 1 and 2. A read to the TMRCCR3 register latches the count of timer 3. This continues for every read to any one of these registers. As a

result, it is not possible to capture the values of all four timers at a given instance in time. However, by setting this bit to "1", all four timer outputs will be latched only on reads to the Timer 1 & 2 Current Count Register (TMRCCR12). Therefore, to capture the current count of all four timers at the same time, perform a read to the TMRCCR12 first (with a 32-bit read), followed by a read to TMRCCR3 and TMRCCR4. The first read (to the TMRCCR12 register) causes all four timer values to be latched at the same time. The subsequent reads to the TMRCCR3 and TMRCCR4 registers do not latch new count values, allowing the count of all timers at the same instance in time to be obtained.

Timer 1 & 2 Load Count Register (TMRLCR12)

Timers 1 & 2 are 16-bits wide and obtain their load count from the Timer 1 & 2 Load Count Register (TMRLCR12), located at offset 0x10 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 2 Load Count	TMRLCR12[31..16]	R/W
Timer 1 Load Count	TMRLCR12[15..0]	R/W

When either of these fields are written (either by a single 32-bit write or separate 16-bit writes), the respective timer is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 3 Load Count Register (TMRLCR3)

Timer 3 is 32-bits wide and obtains its load count from the Timer 3 Load Count Register (TMRLCR3), located at offset 0x14 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 3 Load Count	TMRLCR3[31..0]	R/W

When this field is written, Timer 3 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 4 Load Count Register (TMRLCR4)

Timer 4 is 32-bits wide and obtains its load count from the Timer 4 Load Count Register (TMRLCR4), located at offset 0x18 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 4 Load Count	TMRLCR4[31..0]	R/W

When this field is written, Timer 4 is loaded with the written value on the next rising edge of the timer clock, regardless of whether the timer is enabled or disabled. The value stored in this register is also automatically reloaded on terminal count (or timeout) of the timer.

Timer 1 & 2 Current Count Register (TMRCCR12)

The current count of timers 1 & 2 may be read via the Timer 1 & 2 Current Count Register (TMRCCR12), located at offset 0x20 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 2 Count	TMRCCR12[31..16]	R.O.
Timer 1 Count	TMRCCR12[15..0]	R.O.

When either field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 3 Current Count Register (TMRCCR3)

The current count of Timer 3 may be read via the Timer 3 Current Count Register (TMRCCR3), located at offset 0x24 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 3 Count	TMRCCR3[31..0]	R.O.

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 4 Current Count Register (TMRCCR4)

The current count of Timer 4 may be read via the Timer 4 Current Count Register (TMRCCR4), located at offset 0x28 from the address in BAR2. The mapping of bits in this register are as follows:

Field	Bits	Read or Write
Timer 4 Count	TMRCCR4[31..0]	R.O.

When this field is read, the current count value is latched and returned. There are two modes that determine how the count is latched depending on the setting of the "Read Latch Select" bit in the WDT Control Status Register (CSR2). See the CSR2 register description for more information on these two modes.

Timer 1 IRQ Clear (T1IC)

The Timer 1 IRQ Clear (T1IC) register is used to clear an interrupt caused by Timer 1. Writing to this register, located at offset 0x30 from the address in BAR2, causes the interrupt from Timer 1 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 2 IRQ Clear (T2IC)

The Timer 2 IRQ Clear (T2IC) register is used to clear an interrupt caused by Timer 2. Writing to this register, located at offset 0x34 from the address in BAR2, causes the interrupt from Timer 2 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 3 IRQ Clear (T3IC)

The Timer 3 IRQ Clear (T3IC) register is used to clear an interrupt caused by Timer 3. Writing to this register, located at offset 0x38 from the address in BAR2, causes the interrupt from Timer 3 to be cleared. This can also be done by writing a "0" to the appropriate "Timer x Caused IRQ" field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

Timer 4 IRQ Clear (T4IC)

The Timer 4 IRQ Clear (T4IC) register is used to clear an interrupt caused by Timer 4. Writing to this register, located at offset 0x3C from the address in BAR2, causes the interrupt from Timer 4 to be cleared. This can also be done by writing a “0” to the appropriate “Timer x Caused IRQ” field of the timer Control Status Register (CSR1). This register is write only and the data written is irrelevant.

VME Control

The following table shows the register definitions for the VMIVME-7645 (offset from BAR0).

Table 2-9 Register Definitions Offset From BAR0

Register Name	Offset	
VMECOMM	0x00	
Bit Name	**Bit**	**Definition**
MEC_SEL	0	Master big-endian enable bit 1=Big Endian 0=Little Endian bit
SEC_SEL	1	Slave Big-Endian enable bit 1=Big Endian 0=Little Endian
ABLE	2	Auxiliary BERR logic enable bit 1=Aux. BERR enabled 0=Aux. BERR disabled
BTO	3	Bus error timer enabled 1=enabled 0=disabled
BTOV [1:0]	5:4	Timeout value
		00 - 16uS
		01 - 64uS
		10 -256uS
		11 - 1.00mS
BERRI	6	BERR interrupt enable 1=Interrupt enabled 0=Interrupt disabled
BERRST	7	BERR status read/clear bit 1=Clear BERR status 0=Do nothing
SFENA	8	Enables generation of VME SYSFAIL upon WDT timeout 1= Enable SYSFAIL generation 0=Disable
Unused	9	Not Used
BPENA	10	Endian conversion bypass bit 1=Bypass 0=Not bypassed
VBENA	11	VMEbus enable bit 1= Enabled 0=Disabled
Unused	31:12	Not Used
VBAM	**0x04**	
VME_ADDR	All	Latched VME Address
VBAR	**0x08**	
VME_ADDR	5:0	Latched VME Address Modifier
Unused	31:6	Not Used
SEC_SEL	0x001	

Please refer to Table 2-8, “PCI Configuration Space Registers,” on page 56 for more information concerning BAR0.

Remote Ethernet Booting

The VMIVME-7645 is capable of booting from a server using the 10/100/1000 Ethernet over a network utilizing Argon BIOS. The BIOS provides the ability to remotely boot the VMIVME-7645 using a variety of network protocols. The Ethernet must be connected through either the GbE#1 port or the GbE#2 port available out the P2 VMEbus connector and the "Boot From Lan OPROM" option, found under the Boot Menu of the BIOS Setup utility, must be enabled to boot remotely. This feature allows users to create systems without the worry of disk drive reliability, or the extra cost of adding Flash drives.

BootWare Features:

- Netware (802.1, 802.3 or EthII), TCP/IP (DHCP or BootP), RPL and PXE boot support
- Unparalleled boot sector virus protection
- Detailed boot configuration screens
- Comprehensive diagnostics
- Optional disabling of local boots
- Dual-boot option lets users select network or local booting

CHAPTER
4

Maintenance

If a VMIC product malfunctions, please verify the following:

1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

Technical support for VMIC products is available at: 1-800-240-7782.
Or E-mail us at customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

Appendix

A

Connector Pinouts

Contents

VMEbus Connector Pinout 67
Serial Connector P5 69
Keyboard and Mouse Connector and Pinout (J10) 70
PMC Connector Pinout (J11 - J13) 72
Ethernet Connector (J15) 75
USB Connectors (J16 and J17) 76

Introduction

The VMIVME-7645 VMEbus SBC has several connectors for its I/O ports. Wherever possible, the VMIVME-7645 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a variety of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in its chassis.

VMEbus Connector Pinout

Figure A-1 shows the location of the VMEbus and P2 connector and its orientation on the VMIVME-7645. Table A-1 shows the pin assignments for the VMEbus connector.

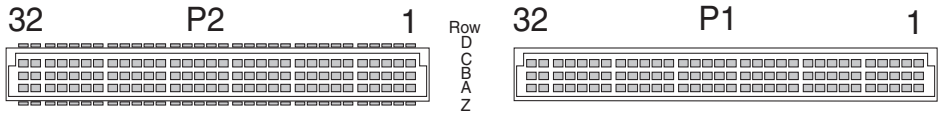


Figure A-1 VMEbus Connector Diagram

Table A-1 VMEbus Connector Pinout (bottom board)

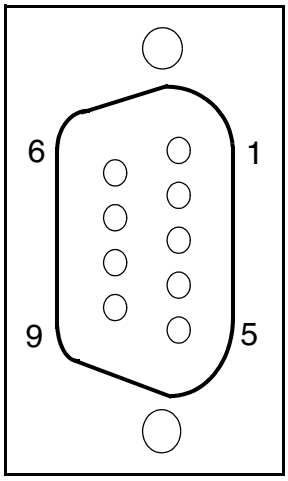
Pin #	P1 Row A Signal	P1 Row B Signal	P1 Row C Signal	P2 Row Z Signal	P2 Row A Signal	P2 Row B Signal	P2 Row C Signal	P2 Row D Signal
1	VME: D0	VME: BBSY#	VME: D8	GbE #1 C+	GbE #1 A+	+5 V	SCSI D8-	SCSI D8+
2	VME: D1	VME: BCLR#	VME: D9	GbE #1 C-	GbE #1 A-	GND	SCSI D9-	SCSI D9+
3	VME: D2	VME: ACFAIL#	VME: D10	GbE #1 D+	GbE #1 B+	SCSI D10+	SCSI D10-	SCSI D11+
4	VME: D3	VME: BG0IN#	VME: D11	GbE #1 D-	GbE #1 B-	SCSI D0+	SCSI D11-	GND
5	VME: D4	VME: BG0OUT#	VME: D12	GND	SCSI D0-	FD INDEX#	SCSI D12-	SCSI D12+
6	VME: D5	VME: BG1IN#	VME: D13	SCSI D1+	SCSI D1-	GND	SCSI D13-	SCSI D13+
7	VME: D6	VME: BG1OUT#	VME: D14	SCSI D2+	SCSI D2-	FD DS0#	SCSI D14-	SCSI D14+
8	VME: D7	VME: BG2IN#	VME: D15	SCSI D3+	SCSI D3-	GND	SCSI D15-	GND
9	GND	VME: BG2OUT#	GND	SCSI D4+	SCSI D4-	FD MTR0#	SCSI DP1-	SCSI D15+
10	VME: SYSCLK	VME: BG3IN#	VME: SYSFAIL#	SCSI D5+	SCSI D5-	GND	SCSI DIFFSEN	SCSI DP1+
11	GND	VME: BG3OUT#	VME: BERR#	SCSI D6+	SCSI D6-	FD DIR#	SCSI TERMPWR	
12	VME: DS1#	VME: BR0#	VME: SYSRST#	SCSI D7+	SCSI D7-	GND	MOUSE DATA	GND
13	VME: DS0#	VME: BR1#	VME: LWORD#	SCSI DP0+	SCSI DP0-	+5 V	MOUSE CLK	
14	VME: WRITE#	VME: BR2#	VME: AM5	SCSI ATN+	SCSI ATN-	GND	COM4 RX	GND
15	GND	VME: BR3#	VME: A23	SCSI BSY+	SCSI BSY-	FD STEP#	COM4 TX	
16	VME: DTACK#	VME: AM0	VME: A22	SCSI ACK+	SCSI ACK-	GND	COM4 RTS#	GND
17	GND	VME: AM1	VME: A21	SCSI RST+	SCSI RST-	FD WDATA#	COM4 CTS#	
18	VME:AS#	VME: AM2	VME: A20	SCSI MSG+	SCSI MSG-	GND	COM3 RX	GND
19	GND	VME: AM3	VME: A19	SCSI SEL+	SCSI SEL-	FD WGATE#	COM3 TX	

Table A-1 VMEbus Connector Pinout (bottom board) (Continued)

Pin #	P1 Row A Signal	P1 Row B Signal	P1 Row C Signal	P2 Row Z Signal	P2 Row A Signal	P2 Row B Signal	P2 Row C Signal	P2 Row D Signal
20	VME: IACK#	GND	VME: A18	SCSI C/D+	SCSI C/D-	GND	COM3 RTS#	GND
21	VME: IACKIN#		VME: A17	SCSI REQ+	SCSI REQ-	FD TRK0#	COM3 CTS#	
22	VME: IACKOUT#		VME: A16	SCSI I/O+	SCSI I/O-	GND	COM2 RX	GND
23	VME: AM4	GND	VME: A15	GND	GbE #2 A+	FD WP#	COM2 TX	
24	VME: A7	VME: IRQ7#	VME: A14	GbE #2 C+	GbE #2 A-	FD RDATA#	COM2 RTS#	GND
25	VME: A6	VME: IRQ6#	VME: A13	GbE #2 C-	GbE #2 B+	FD HDSEL#	COM2 CTS#	
26	VME: A5	VME: IRQ5#	VME: A12	GbE #2 D+	GbE #2 B-	USB P3+	COM1 RX	GND
27	VME: A4	VME: IRQ4#	VME: A11	GbE #2 D-	USB #3 PWR	FD DSKCHG#	COM1 TX	
28	VME: A3	VME: IRQ3#	VME: A10	GND	VIDEO RED	GND	COM1 RTS#	GND
29	VME: A2	VME: IRQ2#	VME: A9	NC	VIDEO GREEN	GND	COM1 CTS#	
30	VME: A1	VME: IRQ1#	VME: A8	GND	VIDEO BLUE	GND	KEYBD DATA	GND
31	-12V		+12V		VIDEO HSYNC	GND	KEYBD CLK	
32	+5V	+5V	+5V	GND	VIDEO VSYNC	+5 V	USB P3-	GND

Serial Connector P5

The standard RS-232 serial port connector is a DB9 male as shown in Figure A-2.

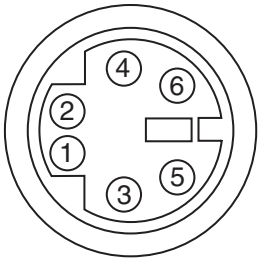


COM 1 and COM 2 SERIAL PORT CONNECTORS			
D9 PIN	**DIR**	**RS-232 SIGNAL**	**FUNCTION**
1	In	DCD	Data Carrier Detect
2	In	RX	Receive Data
3	Out	TX	Transmit Data
4	Out	DTR	Data Terminal Ready
5		GND	Signal Ground
6	In	DSR	Data Set Ready
7	Out	RTS	Request to Send
8	In	CTS	Clear to Send
9	In	RI	Ring Indicator
Shield			Chassis Ground

Figure A-2 Serial Connector Pinouts

Keyboard and Mouse Connector and Pinout (J10)

The keyboard and mouse connector is a standard 6-pin female mini-DIN PS/2 connectors as shown in Figure A-3. Figure A-4 and Table A-2 show the pinouts for the optional splitter cable provided by VMIC (p/n 360-000153-000). Cables supplied by other vendors may vary.



Mouse/Keyboard Connector on the SBC Front Panel

Keyboard/Mouse Connector*		
Pin	**Dir**	**Function**
1	In/Out	Mouse Data
2	In/Out	Keyboard Data
3		Ground
4		+5 V
5	Out	Mouse Clock
6	Out	Keyboard Clock
Shield		Chassis Ground
*An adapter cable is included with the VMIVME-7645 to separate the keyboard and mouse connector.		

Figure A-3 Keyboard/Mouse Connector and Pinout

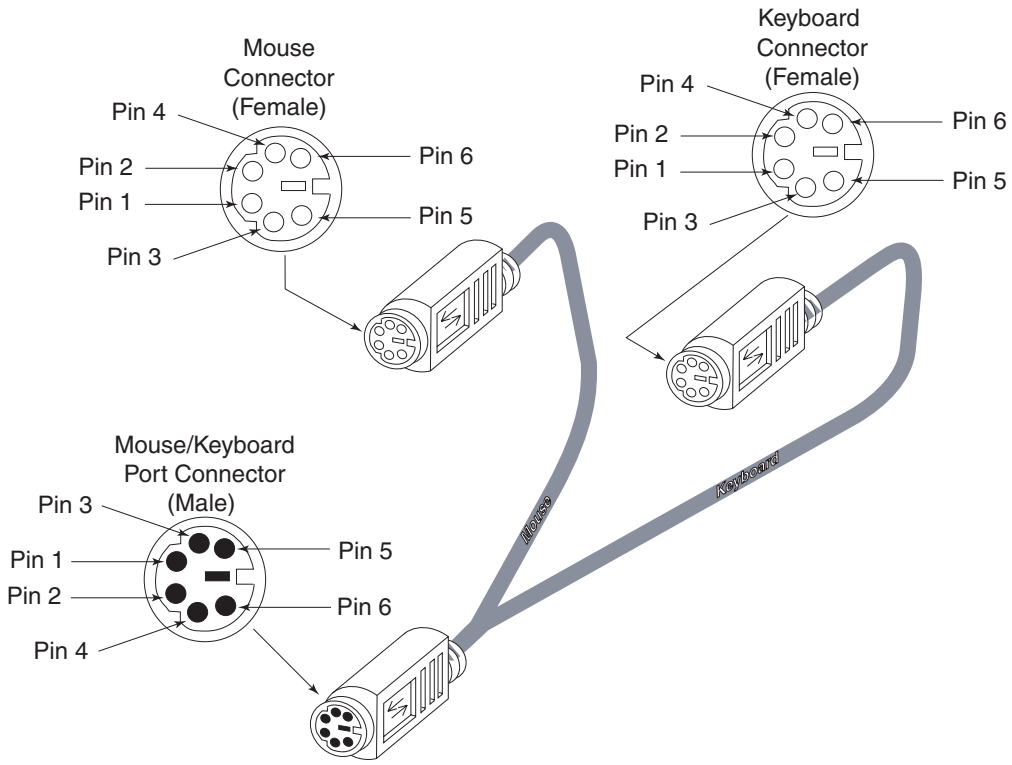


Figure A-4 Mouse/Keyboard Splitter Cable (p/n 360-000153-000)

Table A-2 Keyboard/Mouse Y Splitter Cable

Keyboard			Mouse		
Pin	**Dir**	**Function**	**Pin**	**Dir**	**Function**
1	In/Out	Keyboard Data	1	In/Out	Mouse Data
2		Unused	2		Keyboard Data
3		Ground	3		Ground
4		+5 V	4		+5 V
5	Out	Keyboard Clock	5	Out	Mouse Clock
6		Unused	6		Keyboard Clock
Shield		Chassis Ground	Shield		Chassis Ground

PMC Connector Pinout (J11 - J13)

PMC (J11) Connector and Pinout

The PCI Mezzanine Card (PMC) carries the same signals as the PCI standard; however, the PMC standard uses a completely different form factor. Tables A-3 through A-5 are the pinouts for the PMC connectors (J11 - J13).

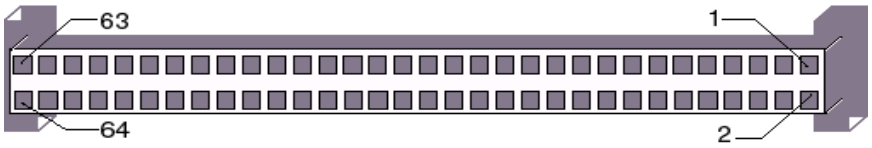


Table A-3 PMC (J11) Connector Pinout

PMC Connector (J11)				PMC Connector (J11)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	GND	2	-12	33	FRAME#	34	GND
3	GND	4	INTA#	35	GND	36	IRDY#
5	INTB#	6	INTC#	37	DEVSEL#	38	+5 V
7	BMODE1A	8	+5 V	39	GND	40	LOCK#
9	INTD#	10	NC	41	SDONE#	42	NC
11	GND	12	NC	43	PAR	44	GND
13	CLK	14	GND	45	+5 V	46	AD[15]
15	GND	16	GNT#	47	AD[12]	48	AD[11]
17	REQ#	18	+5 V	49	AD[9]	50	+5 V
19	+5 V	20	AD[31]	51	GND	52	C/BE0#
21	AD[28]	22	AD[27]	53	AD[6]	54	AD[5]
23	AD[25]	24	GND	55	AD[4]	56	GND
25	GND	26	C/BE3#	57	+5 V	58	AD[3]
27	AD[22]	28	AD[21]	59	AD[2]	60	AD[1]
29	AD[19]	30	+5 V	61	AD[0]	62	+5 V
31	+5 V	32	AD[17]	63	GND	64	REQ64#

PMC (J12) Connector and Pinout

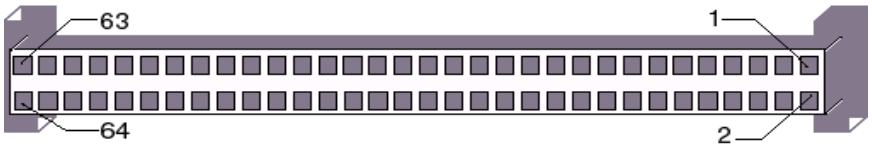


Table A-4 PMC (J12) Connector Pinout

PMC Connector (J12)				PMC Connector (J12)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	+12 V	2	+5 V	33	GND	34	NC
3	GND	4	NC	35	TRDY	36	+3.3 V
5	+5 V	6	GND	37	GND	38	STOP#
7	GND	8	NC	39	PERR#	40	GND
9	NC	10	NC	41	+3.3 V	42	SERR#
11	PRSNT2	12	+3.3 V	43	C/BE1#	44	GND
13	RST#	14	GND	45	AD[14]	46	AD[13]
15	+3.3 V	16	GND	47	MGGEN	48	AD[10]
17	NC	18	GND	49	AD[8]	50	+3.3 V
19	AD[30]	20	AD[29]	51	AD[7]	52	NC
21	GND	22	AD[26]	53	+3.3 V	54	NC
23	AD[24]	24	+3.3 V	55	NC	56	GND
25	IDSEL	26	AD[23]	57	NC	58	NC
27	+3.3 V	28	AD[20]	59	GND	60	NC
29	AD[18]	30	GND	61	ACK64#	62	+3.3 V
31	AD[16]	32	C/BE2#	63	GND	64	NC

PMC (J13) Connector and Pinout

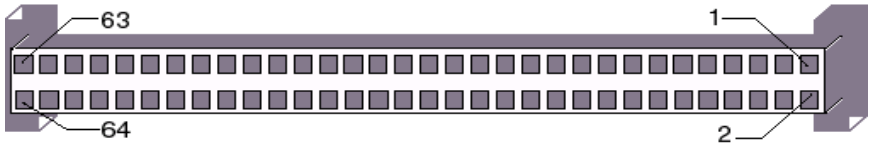
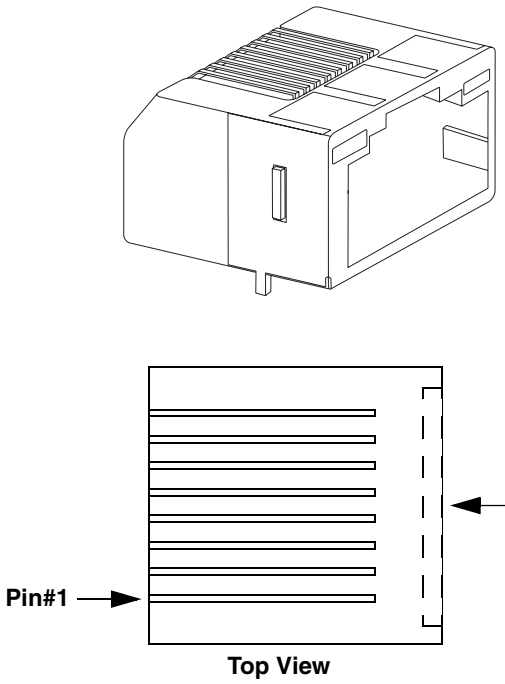


Table A-5 PMC (J13) Connector Pinout

PMC Connector (J13)				PMC Connector (J13)			
Left Side		Right Side		Left Side		Right Side	
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1		2	GND	33	GND	34	AD48
3	GND	4	C/BE#7	35	AD47	36	AD46
5	C/BE#6	6	C/BE#5	37	AD45	38	GND
7	C/BE#4	8	GND	39	+3.3 V	40	AD44
9	+3.3 V	10		41	AD43	42	AD42
11	AD63	12	AD62	43	AD41	44	GND
13	AD61	14	GND	45	GND	46	AD40
15	GND	16	AD60	47	AD39	48	AD38
17	AD59	18	AD58	49	AD37	50	GND
19	AD57	20	GND	51	GND	52	AD36
21	+3.3 V	22	AD56	53	AD35	54	AD34
23	AD55	24	AD54	55	AD33	56	GND
25	AD53	26	GND	57	+3.3 V	58	AD32
27	GND	28	AD52	59		60	
29	AD51	30	AD50	61		62	GND
31	AD49	32	GND	63	GND	64	

Ethernet Connector (J15)

The pinout diagram for the Ethernet 10BaseT/100BaseTx/1000BaseT connector is shown in Figure A-5.

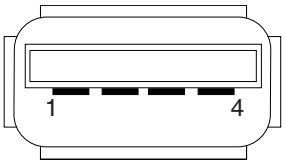


ETHERNET CONNECTOR (10BaseT, 100BaseTx and 1000T)		
PIN	**Signal Name**	
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	TX_CT_OUT	Transmit Center Tap Out
5	TX_CT_OUT	Transmit Center Tap Out
6	RD-	Receive Data
7	RX_CT_OUT	Receive Center Tap Out
8	RX_CT_OUT	Receive Center Tap Out

Figure A-5 Ethernet Connector and Pinout

USB Connectors (J16 and J17)

The USB port uses an industry standard dual 4 position shielded connector. Figure A-6 shows the pinout of the USB connector.



USB1 & 2 CONNECTOR		
PIN	**SIGNAL**	**FUNCTION**
1	USBV	USB Power
2	USB-	USB Data -
3	USB+	USB Data +
4	USBG	USB Ground

Figure A-6 USB Connector Pinout

Appendix

B

System Driver Software

Contents

Microsoft Windows XP Professional Software Driver Installation 78

Introduction

The VMIVME-7645 provides high-performance video, Local Area Network (LAN) access, and Ultra 160 SCSI by means of on-board PCI-based adapters and associated software drivers. High-performance video is provided by the embedded Intel 855GME chipset. High-performance LAN operation is provided by a dual-port Intel FW82546EB Gigabit Ethernet adapter and an Intel 82551ER Fast Ethernet adapter. The three LAN adapters can be configured to allow access to three separate, physical networks. Each LAN adapter is capable of running 10BaseT and 100BaseTx. The two Gigabit adapters are additionally capable of running 1000BaseT. Ultra 160 SCSI is provided by an LSI Logic (Symbios) 53C1000 SCSI controller chip.

To optimize performance of each of these PCI-based subsystems, the user must install the driver software located on the distribution CD-ROM provided with the unit. Detailed instructions for the installation of the drivers under Microsoft Windows XP Professional are provided in the following section.

Microsoft Windows XP Professional Software Driver Installation

NOTE: Prior to installing device drivers, Windows XP should be updated to the latest Service Pack. Visit http://support.microsoft.com and reference Microsoft Knowledge Base Article 322389, ***How to Obtain the Latest Windows XP Service Pack***.

Video Driver Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', 'Run', 'Browse'. In the 'Look in' pull-down selection menu, select the CD-ROM drive. Double-click on the 'Video' folder. Double-click on 'win2k_xp1332'. Click 'OK'.
3. At the 'Intel(R) Extreme Chipset Graphics Driver Software' window, click 'Next'.
4. At the 'Intel(R) Extreme Graphics 2' window, click 'Next'.
5. Click 'Yes' to agree to the software license agreement.
6. Ensure 'Yes, I want to restart my computer now' is selected and click 'Finish'. The computer will restart. The video resolution settings may be changed as desired.

Hance Rapids Chipset Software Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', 'Run', 'Browse'. In the 'Look in' pull-down selection menu, select the CD-ROM drive. Double-click on the 'Hance Rapids' folder. Double-click on the 'Applications' folder. Double-click on 'infinst_enu'. Click 'OK'.
3. At the 'Intel Chipset Software Installation Utility' window, click 'Next'. Click 'Yes' to agree to the software license agreement. Click 'Next'. At each of the following 'Hardware Installation' windows, click 'Continue Anyway'.
4. Ensure 'Yes, I want to restart my computer now' is selected and click 'Finish'. The computer will restart.

USB 2.0 EHCI Host Controller

Depending on how the operating system and the latest service pack were installed, the USB 2.0 controller driver may or may not be running. Visit http://support.microsoft.com and reference Microsoft Knowledge Base Article 329632, ***INFO: Availability of USB 2.0 Support in Windows XP SP1***, for more information on this topic.

To determine whether the driver for the USB 2.0 controller is running, click 'Start', right-click on 'My Computer', and select 'Manage'. In the left pane of the 'Computer Management' window, click on 'Device Manager'. In the right pane, click on the '+' next to 'Universal Serial Bus controllers' to expand the group. If there is a 'Standard Enhanced PCI to USB Host Controller' listed in the group, the USB 2.0 EHCI Host Controller driver is already running, and no further configuration is necessary for the device.

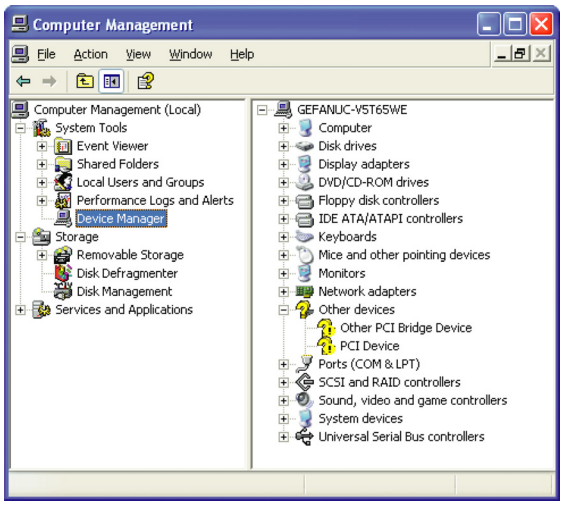
If there is a device labeled 'Universal Serial Bus (USB) controller' under the 'Other devices' section in the right pane of the 'Computer Management' window, the driver has not been installed. To install the driver, right-click on the 'Universal Serial Bus (USB) controller' and select 'Update Driver'. Ensure 'Install the software automatically' is selected and click 'Next'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. Click 'Finish'. Device Manager will relocate the device to the 'Universal Serial Bus controllers' section in the right pane.

Ethernet Adapter Drivers Installation

1. If not already present, insert the Windows Drivers CD-ROM.
2. Click 'Start', right-click on 'My Computer', and select 'Manage'. In the left pane of the 'Computer Management' window, click on 'Device Manager'.
3. **Intel(R) 8255xER PCI Adapter.** Under the 'Other devices' section in the right pane of the 'Computer Management' window , right-click on the third (bottom) 'Ethernet Controller' and select 'Update Driver'. Ensure 'Install the software automatically' is selected and click 'Next'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. At the 'Hardware Installation' window, click 'Continue Anyway'. Click 'Finish'. Device Manager will relocate the device to the 'Network adapters' section in the right pane.
4. **Intel(R) PRO/1000 MT Dual Port Server Adapter.** Perform this step for each of the two remaining Ethernet controllers under the 'Other devices' section in the right pane of the 'Computer Management' window. Right-click on the 'Ethernet Controller' and select 'Update Driver'. Ensure 'Install the software automatically' is selected and click 'Next'. The Hardware Update Wizard will find the appropriate driver and begin installation automatically. Click 'Finish'. Device Manager will relocate the devices to the 'Network adapters' section in the right pane.
5. Click 'X' to close the 'Computer Management' window.
6. Changes may be made to the network configuration as desired.

Status of PCI Devices Listed in Windows Device Manager

After installing all of the drivers provided on the Windows Drivers CD-ROM, Device Manger will still indicate that several PCI devices do not have drivers loaded. In the sample screenshot below, the two devices listed under “Other devices” are the Tundra Universe PCI-to-VMEbus bridge and the VMIC proprietary FPGA. Although these devices are listed as non-functioning by Windows, the hardware is functioning as designed.



Appendix

C

AMI BIOS

Contents

Main Menu 82
Advanced Menu 83
PCIPnP Menu 91
Boot Menu 93
Security Menu 97
Chipset Menu 99
Exit Menu 102

Introduction

The VMIVME-7645 utilizes the BIOS (Basic Input/Output System) in the same manner as other PC/AT compatible computers. This appendix describes the menus and options associated with the VMIVME-7645 BIOS.

System BIOS Setup Utility

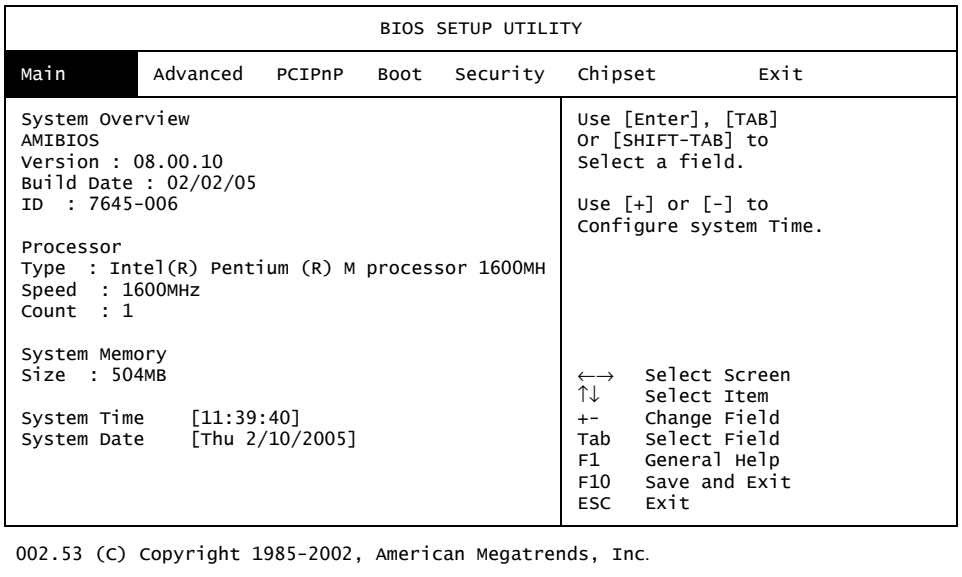
During system bootup, press the Del key to access the AMI BIOS Main screen. From this screen the user can select any selection of the AMI BIOS for configuration, such as floppy drive configuration or system memory. The parameters shown throughout this section are the default values.

Help Window

The help window on the right side of each menu displays the help text for currently selected field. It updates as you move the cursor to each field. Pressing F1 on any menu brings up the General Help window that describes the legend keys and their alternates. The scroll bar on the right of any window indicates that there is more than one page of information in the window. Use PGUP and PGDN to display each page. Pressing HOME and END displays the first and last page. Press ESC to exit the current window.

Main Menu

The Main menu reports the BIOS revision, processor type and clock speed, and allows the user to set the system's clock and calendar. Use the left and right arrow keys to select other screens.



System Time

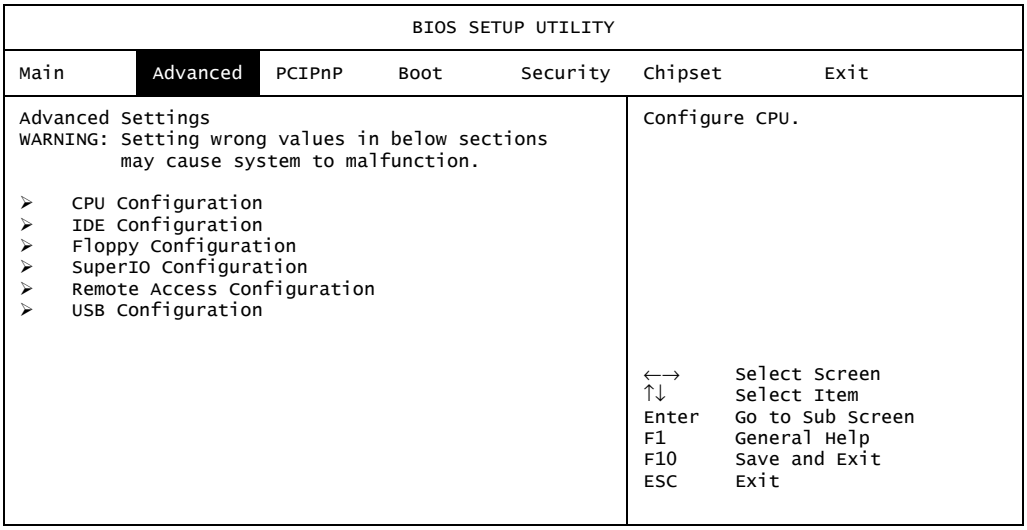
The time format is based on the 24-hour military time clock. For example, 1 PM is 13:00:00. Press the Tab and Shift-Tab to move the cursor to the desired field (hour, minute, second). Press the + or – keys to step through the available choices, or type in the information.

System Date

Press the Tab or Shift-Tab key to move the cursor to the desired field (month, day, year). Press the + or – key to step through the available choices, or type in the information.

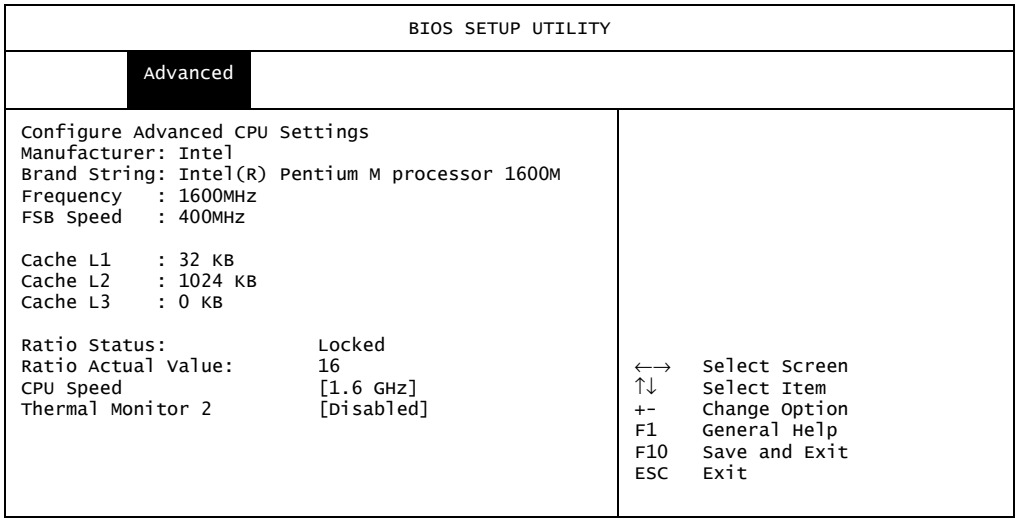
Advanced Menu

Selecting Advanced form the Main menu will display the screen shown below.



CPU Configuration

Selecting CPU Configuration displays the screen shown below. This option provides the user with additional details on the CPU's operation, and allows the user to enable the L3 cache and set the CPU clock speed.



CPU Speed

The value in the field represents the frequency at which the CPU is operating. A lower frequency results in a slower, yet cooler operating CPU. Select from 600MHz, 800MHz, 1GHz, 1.2GHz, 1.4GHz, or 1.6GHz.

Thermal Monitor 2

Enabled allows the processor to throttle the internal frequency if temperatures reach the upper limit.

IDE Configuration

Selecting the IDE Configuration displays the screen shown below. This option allows the user to enable the Compact Flash socket that is on-board. While the Compact Flash drive is not used for normal operation, it may be enabled by the user for test or debugging use, but at the expense using the interrupts IRQ14 and 15, which causes more PCI devices to share the remaining interrupts.

```
BIOS SETUP UTILITY
        Advanced
IDE Configuration                                  |
IDE Configuration                  [P-ATA only]    |
                                                   |
➢   S-ATA Running enhanced mode :  [Yes]           |
➢   P-ATA Channel Selection :      [Both]          |
➢   S-ATA Ports Definition :       [P0-3rd./P1-4th]|
➢   Configure S-ATA as RAID :      [No]            |
                                                   |
➢   Primary IDE Master :           [Not Detected]  |
➢   Primary IDE Slave :            [Not Detected]  |
➢   Secondary IDE Master :         [Not Detected]  |
➢   Secondary IDE Slave :          [Not Detected]  |  ←→     Select Screen
➢   Third IDE Master :             [Not Detected]  |  ↑↓     Select Item
➢   Third IDE Slave :              [Not Detected]  |  Enter  Go to Sub Screen
➢   Fourth IDE Master :            [Not Detected]  |  F1     General Help
➢   Fourth IDE Slave :             [Not Detected]  |  F10    Save and Exit
                                                   |  ESC    Exit
Hard Disk Write Protect            [Disabled]      |
IDE Detect Time Out (Sec)          [35]            |
ATA(PI) 80Pin Cable Detection      [Host & Device] |
```

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IDE Configuration

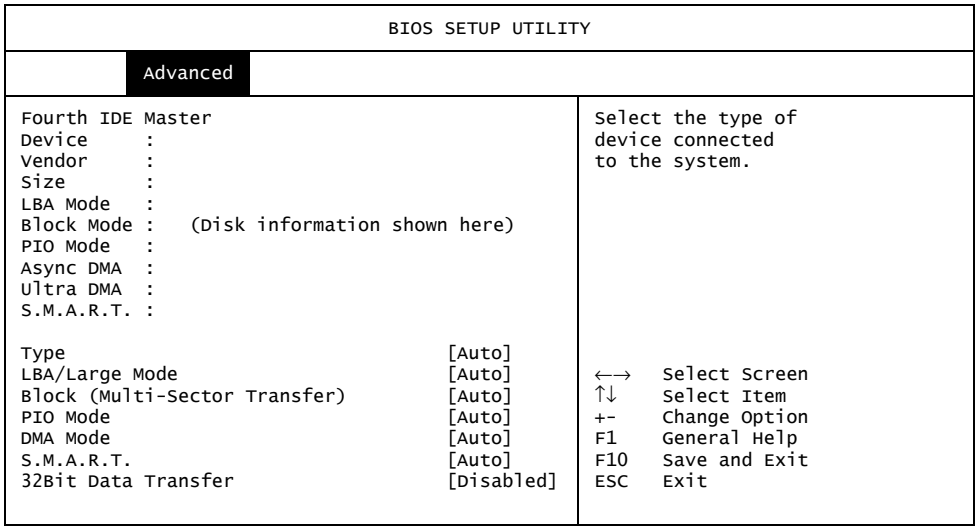
This item allows the user to either disable the IDE bus, or configure it as a parallel or serial interface. Depending upon the selection, additional fields will appear. These fields are:

- S-ATA Running Enhanced Mode
- P-ATA Channel Selection
- S-ATA Ports Definition
- Configure S-ATA as RAID

Combined Mode Option

Primary/Secondary IDE Master/Slave

There are four IDE buses, each capable of supporting a primary and a secondary device. Each device must then be configured as a master or slave device. Selecting the menu for a detected device displays the screen shown below.



Whenever a device is undetected, the same option fields appear but without the preceding disk information.

Type

The user can specify what type of device is attached to the IDE bus. Select from Auto, which automatically detects the device type, CDROM, or ARMD (ATAPI Removable Media Drive).

LBA/Large Mode

This option is used to either disable LBA (Logical Block Addressing) mode or allow the system to automatically determine whether it is required for the selected device.

Block (Multi-Sector Transfer)

This field allows a user to disable block transfers, or enable the system to automatically detect if the hardware is capable of block transfers.

PIO Mode

This field allows the user to select which PIO (Programmed Input Output) mode the drive should operate in. Select from mode 0 to mode 4, or allow the system to automatically determine the appropriate mode.

PIO Mode	Max. Data Rate	Specified In
0	3.3 MB/s	ATA
1	5.2 MB/s	ATA
2	8.3 MB/s	ATA
3	11.1 MB/s	ATA-2
4	16.6 MB/s	ATA-2

PIO Mode Descriptions

DMA Mode

The DMA mode is automatically detected. This field has only one option, and as such, cannot be changed.

S.M.A.R.T.

Hard disks equipped with S.M.A.R.T (Self Monitoring Analysis and Reporting Technology) determine their own status independently as well as any possible functionality restrictions. Use this field to enable, disable, or allow the system to automatically detect S.M.A.R.T. drives.

32Bit Data Transfer

This field is used for enabling or disabling 32-bit data transfers to and from the selected IDE device.

Hard Disk Write Protect

This option allows the user to either enable or disable write protection for hard drives connected to the system. This selection will only be effective for drives that are accessed through the BIOS.

IDE Detect Time Out (Sec)

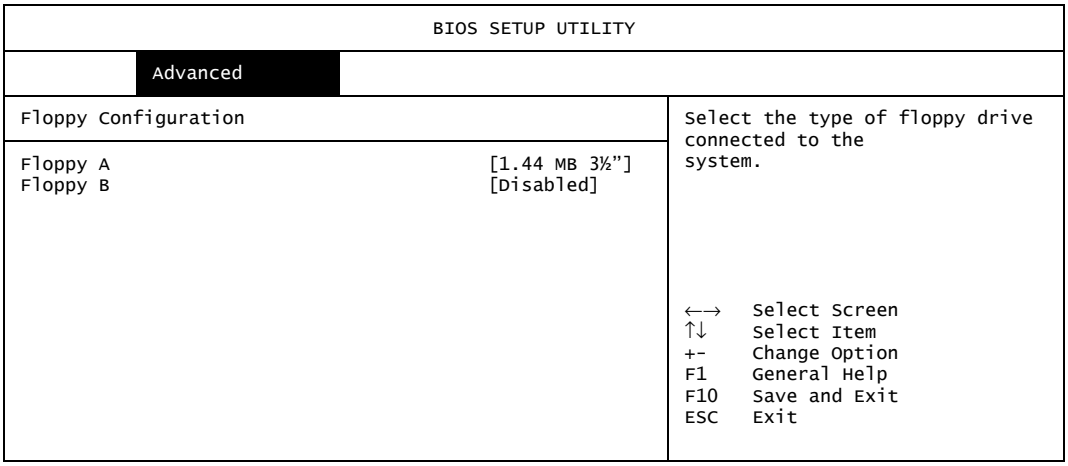
This item allows the user to specify the amount of time that the system has to detect ATA/ATAPI devices. Select a timeout period from zero to 35 seconds.

ATA(PI) 80Pin Cable Detection

This option allows the user to determine the mechanism by which an 80 pin ATA cable is to be detected. Choose from Host, Device, or Host & Device.

Floppy Configuration

Selecting the Floppy Configuration displays the screen shown below. This option allows the user to disable or enable the floppy drive, and to select the drive's format.

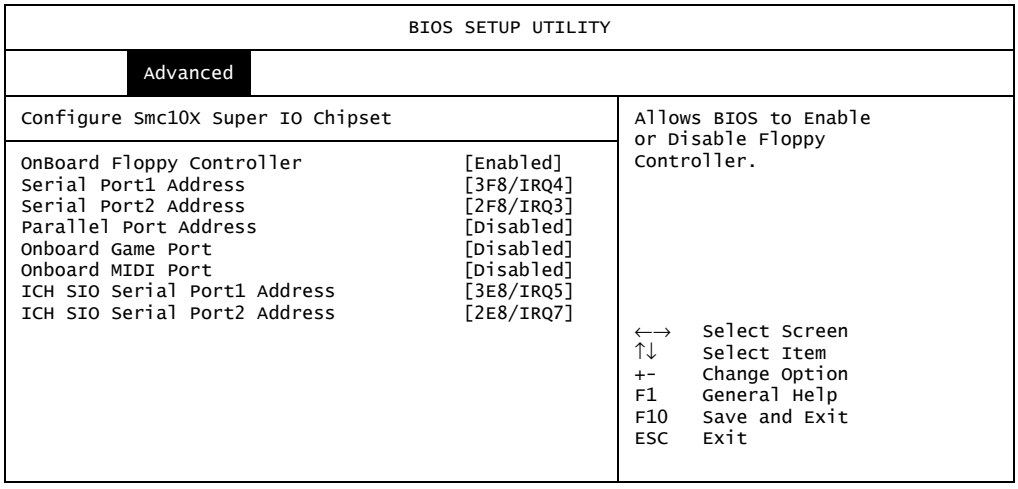


Floppy A/B

Select the format/size of the floppy drive. Choose from 360 KB 5¼", 1.2 MB 5¼", 720 KB 3½", 1.44 MB 3½", or 2.88 MB 3½".

SuperIO Configuration

Selecting the SuperIO Configuration displays the screen shown below. This option allows the user to enable or disable the floppy controller and serial ports, and to set the IO address and interrupt associated with each port.



Onboard Floppy Controller

Use this feature to enable or disable the floppy controller. This controller must be enabled in this field and must have a defined format in order to access the floppy drive.

Serial Port 1 & 2 Address

Use this feature to select the I/O address block and interrupt that will be used to interface with COM ports 1 and 2. The selections are in the form of "address/interrupt (IRQ)". Select from 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ4, and 2E8/IRQ3. These ports physically reside in the on-board Super IO device.

ICH SIO Serial Port 1 & 2 Address

Use this feature to select the I/O address block and interrupt that will be used to interface with COM ports 3 and 4. The selections are in the form of "address/interrupt (IRQ)". Select from 3F8/IRQ4, 2F8/IRQ3, 3E8/IRQ5, and 2E8/IRQ7. These ports physically reside in the Hance Rapids ICH device. For normal operation, set one port address to 3E8/IRQ5, and set the other to 2E8/IRQ7.

Remote Access Configuration

Selecting the Remote Access Configuration displays the screen shown below. This option allows the user to use one of the COM ports for serial redirection; sending ASCII text, as through a terminal, without using the SVGA port.

```
                              BIOS SETUP UTILITY
        Advanced
Configure Remote Access type and parameters     Select Remote Access
                                                type.
Remote Access                    [Disabled]

                                                ←→   Select Screen
                                                ↑↓   Select Item
                                                +-   Change Option
                                                F1   General Help
                                                F10  Save and Exit
                                                ESC  Exit
```

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Remote Access

This field enables or disables the remote access feature.

Serial Port Number

This field allows the user to select which COM port will be used for remote access. Choose between COM1 and COM2.

Serial Port Mode

Select the communication parameters for the COM to be used. The number of bits, parity and number of Stop bits are fixed at 8, None and 1 respectively. Choose a baud rate of 19,200bps, 57,600bps or 115,200bps.

Flow Control

Select the method of flow control used for serial redirection communication. Select None, Hardware or Software.

Redirection After BIOS POST

Serial redirection can only be enabled for certain portions of the bootup process: only during POST, during POST and Boot Loader or Always, by selecting Disabled, Boot Loader or Always respectively.

Terminal Type

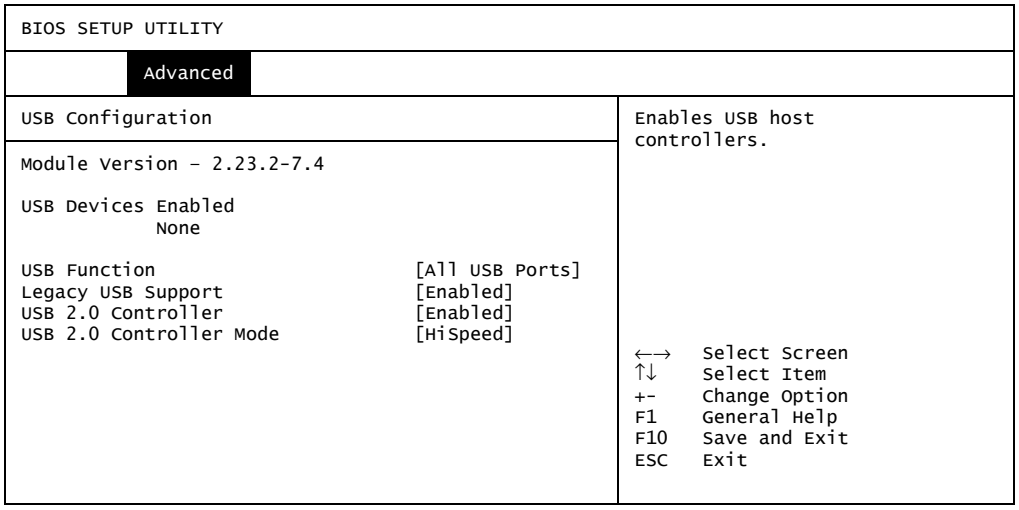
Select the terminal type that the remote access port is to emulate. Choose from ANSI, VT100 or VT-UTF8.

UT-F8 Combo Key Support

Combination Key support for ANSI and VT100 terminals can be enabled or disabled.

USB Configuration

Selecting the USB Configuration displays the screen shown below. This option allows the user to enable none, some or all of the USB ports and to set the data rate.



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USB Function

This field can disable all of the USB ports, enable only two, or enable all controllers.

Legacy USB Support

The USB ports can be configured to support legacy hardware. Use this field to disable or enable support. Select 'Auto' to disable legacy support if no legacy devices are connected.

USB 2.0 Controller

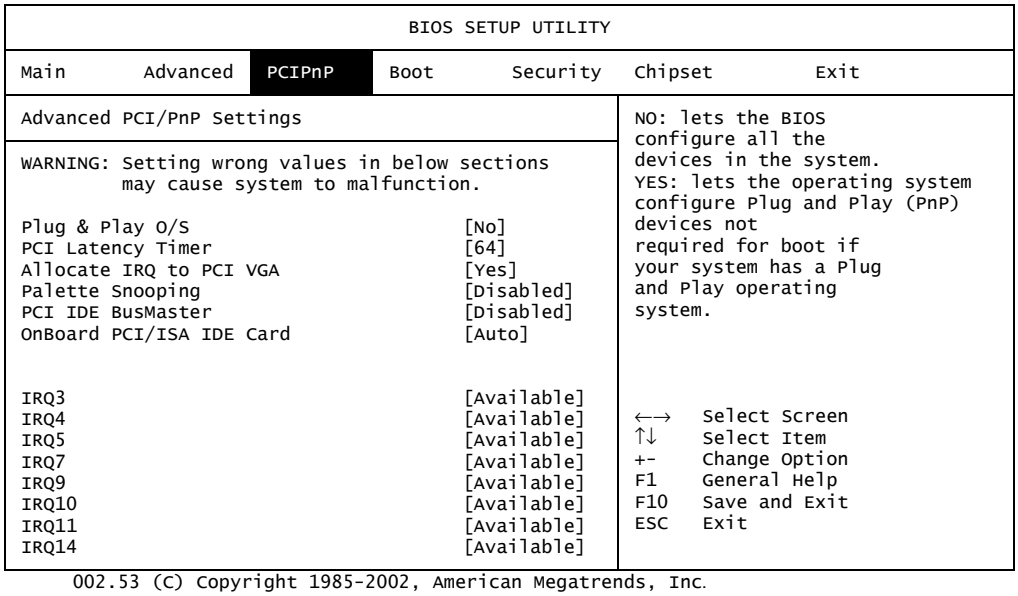
When the USB 2.0 Controller is disabled, the controller defaults to USB 1.1 support.

USB 2.0 Controller Mode

When the USB 2.0 Controller is enabled, the user can select the data rate. Choose either Full Speed (12 Mbsp) or High Speed (480 Mbps). All enabled ports are set to the same speed.

PCIPnP Menu

Selecting the PCIPnP menu will display the screen shown below.



Plug & Play OS

The user must specify whether the operating system used is a “Plug and Play (PnP)” system. If ‘No’ is selected, then the BIOS will configure all the devices in the system. If ‘Yes’, then the BIOS will allow the operating systems to configure the PnP devices not required for booting.

PCI Latency Timer

The latency timer is a mechanism for ensuring that a bus master does not extend the access latency of other masters beyond a specified value. Select the number of PCI clocks for each device’s latency timer register. The user can choose from eight values from 32 to 248 clocks.

Allocate IRQ to PCI VGA

The user can decide whether to allocate an IRQ to the VGA device regardless of whether it requests an IRQ or not.

Palette Snooping

By enabling Palette Snooping, an ISA graphics interface will function properly by informing PCI devices of its presence.

PCI IDE BusMaster

When enabled, the BIOS uses mastership of the PCI bus to read and write to IDE drives.

Onboard PCI/ISA IDE Card

Some PCI IDE cards may require that this field specify the PCI slot number that the device resides in. There are six slots from which to choose. Select 'Auto' if such a specification is unnecessary.

IRQ Availability

The user can specify an individual interrupt request (IRQ) is available to be used by PCI PnP devices. An IRQ can be marked as 'Reserved' when it is used by legacy ISA devices.

DMA Channel Availability

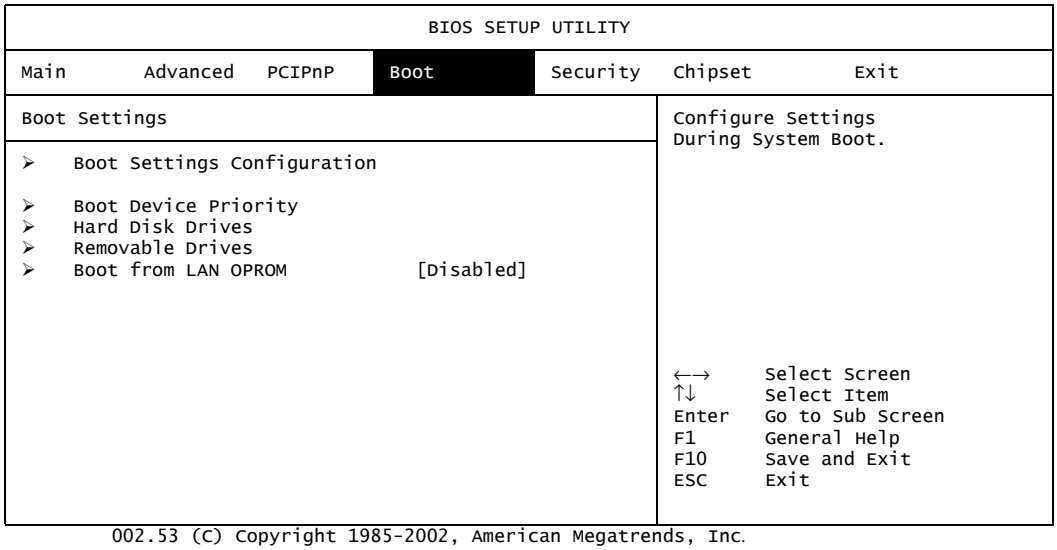
The user can specify a direct memory access (DMA) channel is available to be used by PCI PnP devices. A DMA channel can be marked as 'Reserved' when it is used by legacy ISA devices.

Reserved Memory Size

If desired, the user can specify an amount of memory to be reserved for legacy ISA devices up to 64Kbytes.

Boot Menu

Selecting the Boot Menu displays the screen shown below.

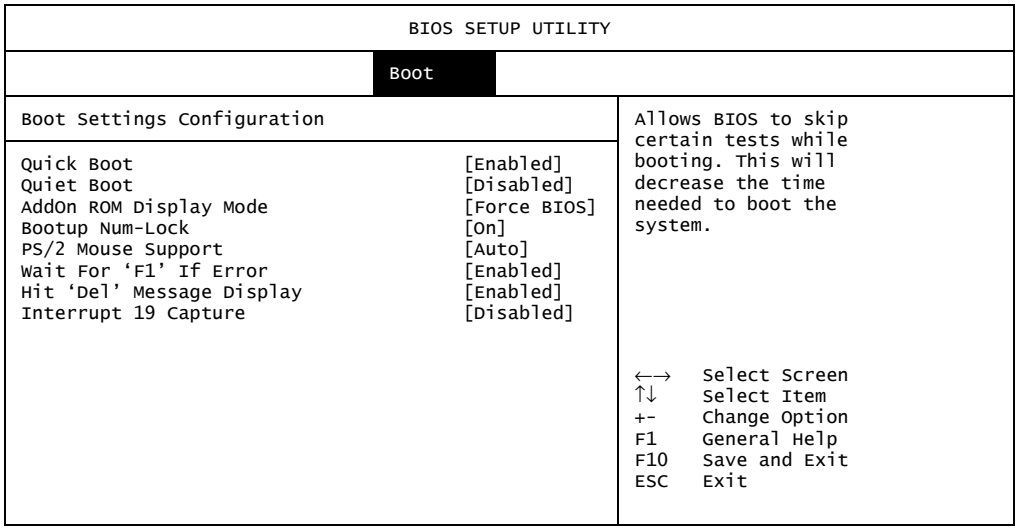


Boot from LAN OPROM

Enable or Disable the Argon Boot from LAN Option ROM.

Boot Settings Configuration

Selecting Boot Settings Configuration displays the screen shown below.



```
002.53 (C) Copyright 1985-2002, American Megatrends, Inc.
```

Quick Boot

When the Quick Boot feature is enabled, the BIOS will skip certain tests while booting. This will decrease the time needed to boot the system.

Quiet Boot

When booting in the Quiet Mode, the BIOS will display the GE Intelligent Platforms' logo instead of post messages. Otherwise the BIOS will display normal POST messages.

AddOn ROM Display Mode

The user can select the display mode for the SCSI BIOS as either 'Force BIOS' or as 'Keep Current'.

Boot-up Num-Lock

The keyboard's Num-Lock key can either be on after boot-up or off.

PS/2 Mouse Support

This field can enable or disable support for a front or rear PS/2 mouse. With the 'Auto' mode selected, support is provided if a PS/2 mouse is present. Otherwise, support is disabled.

Wait For 'F1' If Error

When enabled, the BIOS will halt on an error during boot-up and only proceed after the F1 key has been pressed.

Hit 'DEL' Message Display

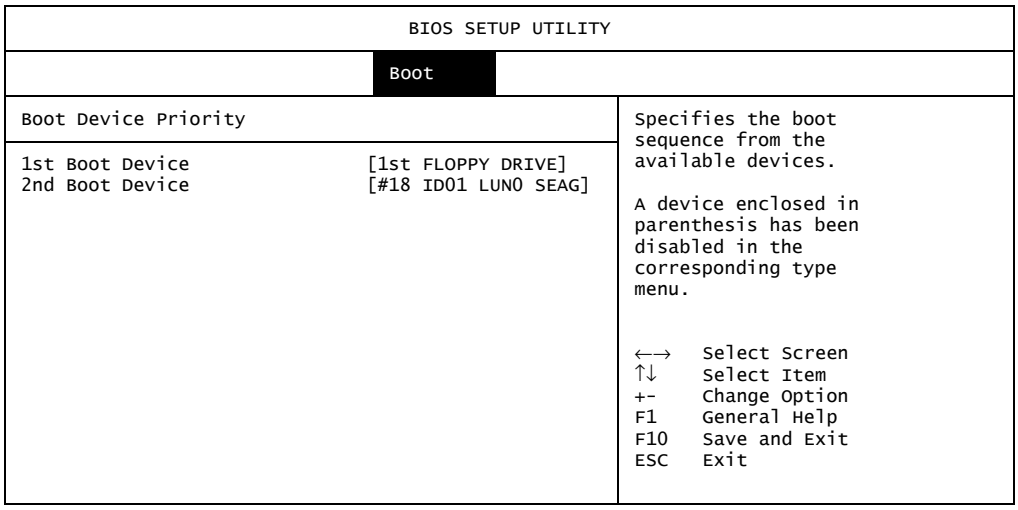
The message "Press DEL to run Setup" will be displayed during POST if this feature is enabled.

Interrupt 19 Capture

Interrupt 19 is the software interrupt that handles the boot function. When this feature is enabled, the SCSI BIOS can trap interrupt 19.

Boot Device Priority

This menu allows the user to select the order in which bootable hardware devices are polled in order to determine the boot device for the current boot-up sequence. Selecting this menu displays the screen shown below.



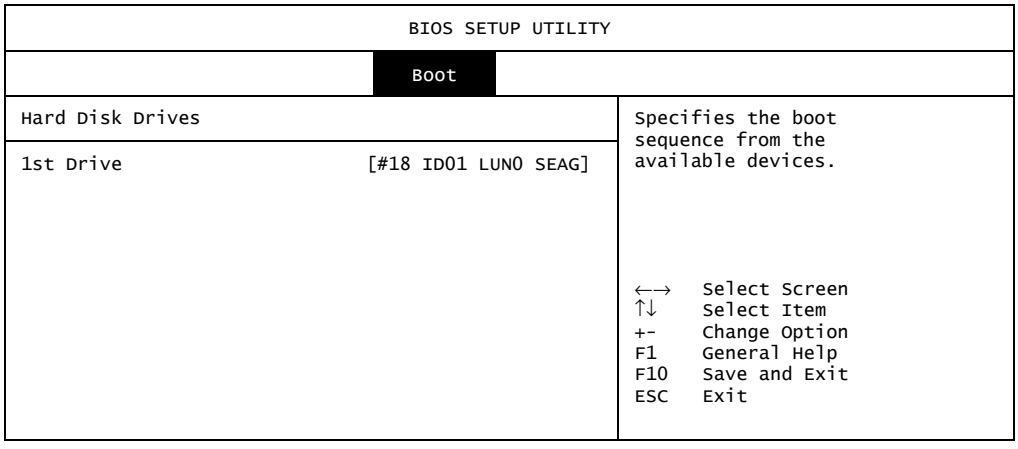
1st, 2nd or 3rd Boot Device

These fields can be altered by pressing the + or – key in order to select the priority of the enabled and detected boot devices available to the system.

The number of boot devices listed in the menu depends on how many boot devices are detected in the system. A maximum of three boot devices may be placed in the boot sequence.

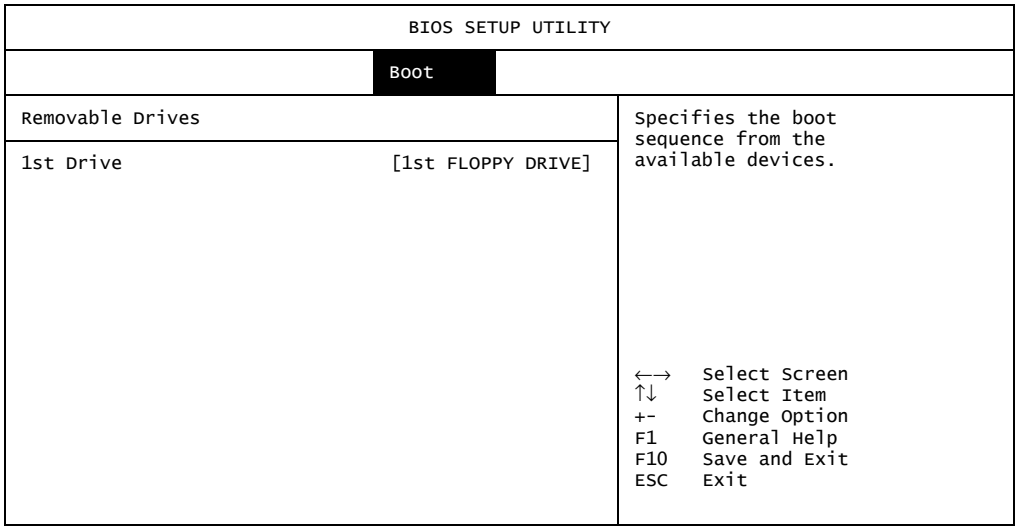
Hard Disk Drives

This menu allows the user to enable or disable system hard drives and specify their boot priority among the hard drives. When this menu is selected, the screen shown below is displayed.



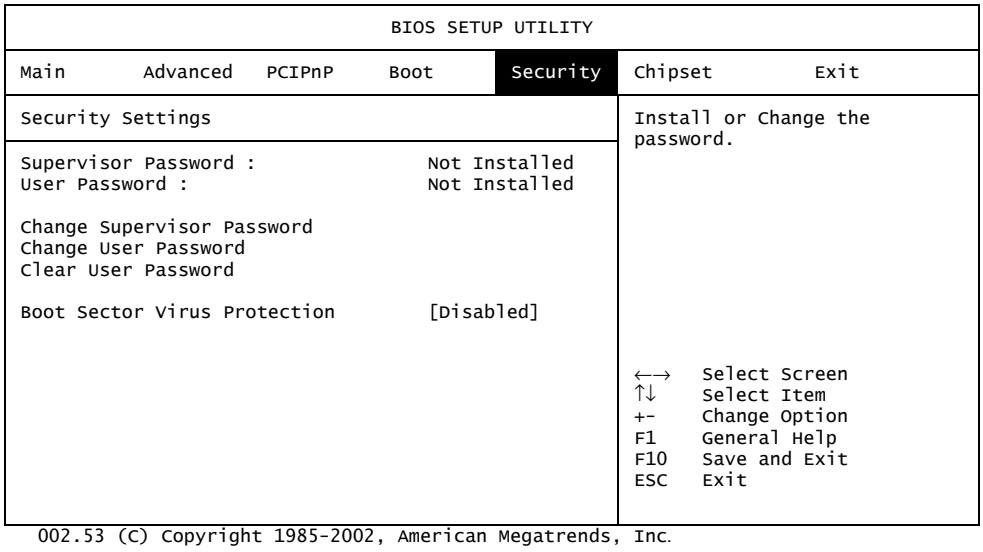
Removable Drives

This menu allows the user to enable or disable removable drives, like Compact Flash or Floppy drives. Selecting this menu displays the screen shown below is displayed.



Security Menu

Selecting the Security Menu displays the screen shown below.



Security Settings

The Security Menu displays the status of the Supervisor and User passwords, and allows appropriate users to make changes to the passwords.

Change Supervisor Password

The Supervisor's password can be changed only by the supervisor. When selected, a prompt will appear for the new password, followed by a confirmation of the new password. Passwords are limited to six characters.

User Access Level

This field specifies the amount of access that a user has to the setup utility. Choose from Full, Limited, View, or No access rights. Full Access allows a user to alter any fields in the setup menu. Limited Access only allows a user to changed fields in the setup such as the date and time. View Only allows a read-only access to the setup utility. No Access prevents a user from accessing the setup utility.

Change User Password

The User password can be changed by a User with Full Access. When selected, a prompt will appear for the new password, followed by a confirmation of the new password. Passwords are limited to six characters.

Clear User Password

The User Password can be cleared by a User with Full Access. Selecting this option will clear the User Password after a confirmation asking “Clear User Password?” is responded to in the affirmative.

Password Check

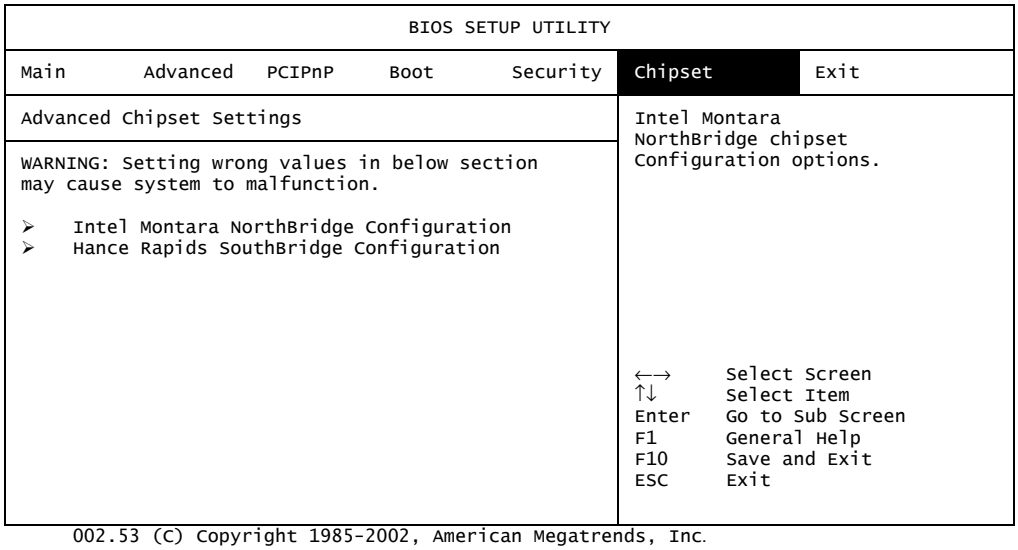
Selecting ‘Setup’ will require a user to enter a password only when invoking the setup utility. Selecting ‘Always’ will ask the user for a password at each bootup.

Boot Sector Virus Protection

Built-in virus protection for the boot sector of bootable devices can be enabled or disabled.

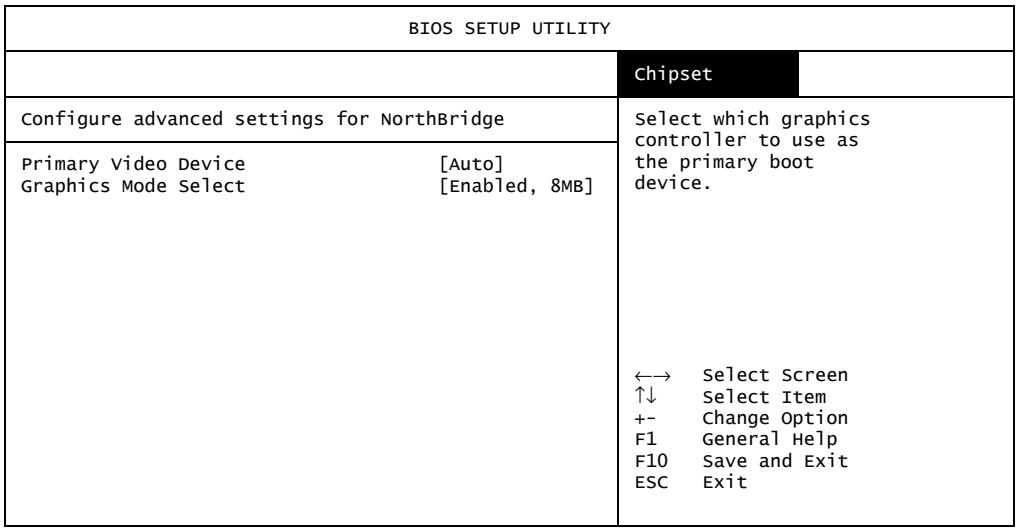
Chipset Menu

Selecting the Chipset Menu displays the screen shown below.



Intel Montara NorthBridge Configuration

The NorthBridge Configuration Menu allows the user to configure the video device. Selecting this menu will display the screen shown below.



Primary Video Device

This field specifies which graphics controller to use as the primary boot device. Choose from Internal, External PCI, External AGP, or Auto, which automatically determines the type of video device that is in use.

Graphics Mode Select

The user can specify the amount, if any, of system memory to be used by the internal graphics device. Values range from 1Mbytes to 32Mbytes.

SouthBridge Configuration

The SouthBridge menu allows users to enable or disable the Hance Rapids South Bridge's IOAPIC, and on-board audio and modem. Selecting this menu will display the screen shown below.

```
                              BIOS SETUP UTILITY
                                                  Chipset
IOAPIC                                    [Enabled]
Extended IOAPIC                           [Enabled]
OnBoard AC'97 Audio                       [Auto]
OnBoard AC'97 Modem                       [Auto]

                                          ←→   Select Screen
                                          ↑↓   Select Item
                                          +-   Change Option
                                          F1   General Help
                                          F10  Save and Exit
                                          ESC  Exit

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```

IOAPIC

The user can either enable or disable the IOAPIC (I/O Advance Programmable Interrupt Controller) with this field.

Extended IOAPIC

This field can be used to enable or disable the extended mode of the ICH4 IOAPIC. This AMI BIOS can be used in systems in which an ICH4 device is present. However, that device is not part of the on-board chipset.

OnBoard AC'97 Audio

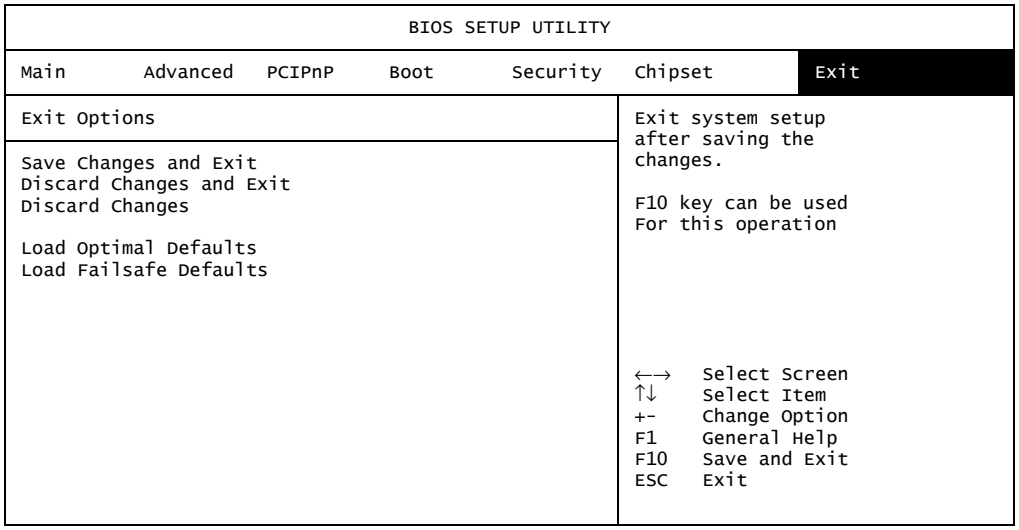
AC'97 refers to the Audio Codec '97 Component Specification, Version 2.2. This field is used to enable or disable the audio function.

OnBoard AC'97 Modem

AC'97 refers to the Audio Codec '97 Component Specification, Version 2.2. This field is used to enable or disable the modem function.

Exit Menu

The Exit menu allows the user to exit the BIOS program, while either saving or discarding any changes. This menus also allows the user to restore the BIOS defaults if desired.



Save Changes and Exit

Selecting this option will exit the system setup after saving changes made during the current session.

Discard Changes and Exit

This option causes the system to exit the setup function without saving any changes made during the current session.

Discard Changes

All changes made during the current session are discarded. Any fields that were changed revert to their previous state. However, the system setup function is not exited.

Load Optimal Defaults

When selected, the setup function automatically selects all of the optimal default values for all setup questions. These defaults are:

Main menu:

None

Advanced menu:

CPU Configuration:

CPU Speed	1.0 GHz
Thermal Monitor 2	Disabled

IDE Configuration:

IDE Configuration	P-ATA Only
S-ATA Running Enhanced Mode	Yes
P-ATA Channel Selection	Both
S-ATA Ports Definition	P0-3rd./P1-4th.
Configure S-ATA as RAID	No

Primary/Secondary IDE Master/Slave

Type	Auto
LBA/Large Mode	Auto
Block (Multi-Sector Transfer)	Auto
PIO Mode	Auto
S.M.A.R.T.	Auto
32Bit Data Transfer	Disabled
Hard Disk Write Protect	Disabled
IDE Detect Time Out (Sec)	35
ATA(PI) 80Pin Cable Detection	Host & Device

Floppy Configuration:

Floppy A	1.44 MB 3½″
Floppy B	Disabled

SuperIO Configuration:

OnBoard Floppy Controller	Enabled
Serial Port1 Address	3F8/IRQ4
Serial Port2 Address	2F8/IRQ3
Parallel Port Address	Disabled
OnBoard Game Port	Disabled
OnBoard MIDI Port	Disabled
ICH SIO Serial Port1 Address	3E8/IRQ5
ICH SIO Serial Port2 Address	2E8/IRQ7

Remote Access Configuration:

Remote Access	Disabled

USB Configuration:

USB Function	All USB Ports
Legacy USB Support	Enabled
USB 2.0 Controller	Enabled
USB 2.0 Controller Mode	HiSpeed

PCIPnP menu:

Plug & Play O/S	No
PCI Latency Timer	64
Allocate IRQ to PCI VGA	Yes
Palette Snooping	Disabled
PCI IDE BusMaster	Disabled
OnBoard PCI/ISA IDE Card	Auto
IRQ3-15	Available
DMA Channel 0-7	Available
Reserved Memory Size	Disabled

Boot menu:

Boot Settings Configuration:

Quick Boot	Enabled
Quiet Boot	Disabled
Add On ROM Display Mode	Force BIOS
Bootup Num-Lock	On
PS/2 Mouse Support	Auto
Wait for 'F1' If Error	Enabled
Hit 'DEL' Message Display	Enabled
Interrupt 19 Capture	Disabled

Boot Device Priority:

The BIOS places the floppy drive, any Compact Flash drive, and the SCSI drive as 1st, 2nd, and 3rd priority respectively.

Hard Disk Drives:

The BIOS places any Compact Flash drive that might be present before the SCSI drive(s) in the boot sequence.

Removable Drives:

The BIOS lists the floppy drive as the only removable drive boot sequence.

Boot from LAN OPROM:

Disabled

Security menu:

User Access Level	Full Access
Password Check	Setup
Boot Sector Virus Protection	Disabled

Chipset menu:

NorthBridge:

Primary Video Device	Auto
Graphics Mode Select	Enabled, 8MB

SouthBridge:

IOAPIC	Enabled
Extended IOAPIC	Enabled
OnBoard AC'97 Audio	Auto
OnBoard AC'97 Modem	Auto

Exit menu:

None

Load Failsafe Defaults

Presently, this command sets the same defaults as the Load Optimal Defaults command.

Appendix

D

Argon BIOS

Contents

Boot Menus 108
BIOS Features Setup 110

Introduction

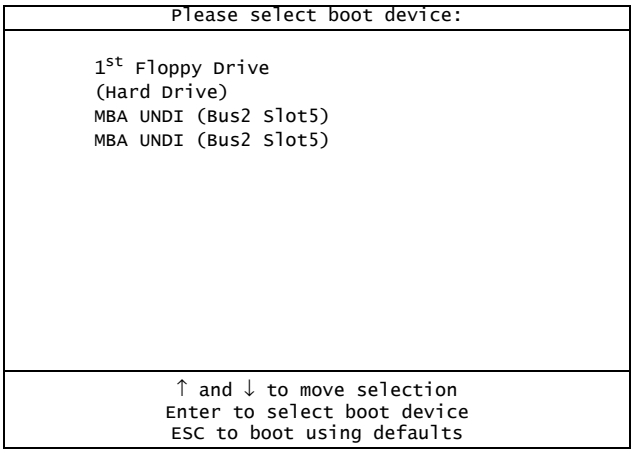
The VMIVME-7645 includes an Argon BIOS option which allows the VMIVME-7645 to be booted from a network. This appendix describes the procedures to enable this option and the Argon BIOS Setup screens.

Boot Menus

There are two methods of enabling the Argon BIOS option. The first method is the *First Boot* menu. The second is the *Boot* menu from the BIOS Setup Utility.

First Boot Menu

Press F11 at the very beginning of the boot cycle, which will access the *First Boot* menu. Selecting "Managed PC Boot Agent (MBA)" to boot from the LAN in this screen applies to the current boot only, at the next reboot the VMIVME-7645 will revert back to the setting in the Boot menu.



Using the arrow keys, highlight *Managed PC Boot Agent (MBA)*, and press the ENTER key to continue with the system boot.

Boot Menu

The second method of enabling the Argon BIOS option is to press the DEL key during system boot. This will access the BIOS Setup Utility. Advance to the Boot menu, and to the Boot Device Priority sub-menu. Use the arrow keys to highlight the Managed PC Boot Agent (MBA) option. Repeat entering <+> until the desired MBA is at the top of the list.

Advance to the Exit menu, select "Exit Saving Changes" and press ENTER. When the system prompts for confirmation, press "Yes". The computer will then restart the system boot-up.

.

BIOS SETUP UTILITY		
Boot		
Boot Device Priority		Specifies the boot sequence from the available devices.
1st Boot Device 2nd Boot Device 3rd Boot Device	[MBA UNDI (Bus2 Slot5)] [1st Floppy Drive] [Hard Drive]	←→ Select Screen ↑↓ Select Item +- Go to Sub Screen F1 General Help F10 Save and Exit ESC Exit

BIOS Features Setup

After the Managed PC Boot Agent has been enabled, there are several boot options available to the user. These options are RPL (default), TCP/IP, Netware and PXE. The screens below show the defaults for each boot method.

RPL

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
All rights reserved
```

```
                                Configuration

     Boot Method:               RPL

     Config Message:            Enabled
     Message Timeout:           3 Seconds
     Boot failure Prompt:       Wait for timeout
     Boot Failure:              Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

TCP/IP

```
Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
(c) Copyright 2002 Argon Technology Corporation
All rights reserved
```

```
                                Configuration

     Boot Method:               TCP/IP

     Protocol                   DHCP
     Config Message:            Enabled
     Message Timeout:           3 Seconds
     Boot failure Prompt:       Wait for timeout
     Boot Failure:              Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

Netware

```
  Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
  (c) Copyright 2002 Argon Technology Corporation
  All rights reserved
```

```
                                Configuration

      Boot Method:              Netware

      Protocol                  802.3
      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot failure Prompt:      Wait for timeout
      Boot Failure:             Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

PXE

```
  Argon Managed PC Boot Agent (MBA) v4.00 (BIOS Integrated)
  (c) Copyright 2002 Argon Technology Corporation
  All rights reserved
```

```
                                Configuration

      Boot Method:              PXE

      Config Message:           Enabled
      Message Timeout:          3 Seconds
      Boot Failure Prompt:      Wait for timeout
      Boot Failure:             Next boot device
```

```
Use cursor keys to edit: Up/Down change field, Left/Right change value
ESC to quit, F9 restore previous settings, F10 to save
```

Appendix

E

SCSI BIOS

Contents

Features 113
Boot Initialization with BIOS Boot Specification (BBS) 113

Introduction

This section presents general information about the SDMS SCSI BIOS and Configuration Utility Version 4.19.00.

A SCSI BIOS is the bootable ROM code that manages SCSI hardware resources. It is specific to a family of LSI Logic SCSI controllers or processors. An SDMS SCSI BIOS integrates with a standard system BIOS, extending the standard disk service routine provided through INT13h.

During the boot time initialization, the SCSI BIOS determines if there are other hard disks, such as an IDE drive, already installed by the system BIOS.

If there are, the SCSI BIOS maps any SCSI drives it finds behind the drive(s) already installed. Otherwise, the SCSI BIOS installs drives starting with the system boot drive. In this case, the system boots from a drive controlled by the SCSI BIOS. For 4.05 versions and higher, LSI Logic supports the BIOS Boot Specification (BBS). The section, "*Boot Initialization with BIOS Boot Specification (BBS)*," page 113 discusses selecting boot and drive order.

Features

The SDMS SCSI BIOS features include:

- Configuration for up to 256 adapters - any four can be chosen for INT13 (bootrom) support
- All LSI53C8xx devices including LSI53C895A
- LSI53C1510 device
- LSI53C1000 device
- SPI-3 Parallel Protocol Request (PPR)
- Basic Domain Validation

Boot Initialization with BIOS Boot Specification (BBS)

The SDMS SCSI BIOS provides support for the BIOS Boot Specification (BBS), which allows you to choose which device to boot from by selecting the priority.

To use this feature, the system BIOS must also be compatible with the BBS. If your system supports the BBS, then you will use the system BIOS setup menu to select the boot and drive order. In the system BIOS setup, the Boot Connection Devices menu appears with a list of available boot options. Use this menu to select the device and rearrange the order, then exit to continue the boot process.

CD-ROM Boot Initialization

The SDMS SCSI BIOS supports boot initialization from a CD-ROM drive. The five types of emulation are:

- No emulation disk
- Floppy 1.2 Mbyte emulation disk
- Floppy 1.44 Mbyte emulation disk
- Floppy 2.88 Mbyte emulation disk
- Hard disk emulation

The type of emulation assigns the drive letter for the CD-ROM. For example, if a 1.44 Mbyte floppy emulation CD-ROM was loaded, then the CD-ROM drive would become the designated A drive, and the existing floppy would become drive B.

Starting the SCSI BIOS Configuration Utility

If you have SCSI BIOS version 4.XX, and it includes the SDMS SCSI BIOS Configuration Utility, you can change the default configuration of your SCSI host adapters. You may decide to alter these default values if there is a conflict between device settings or if you need to optimize system performance.

You can see the version number of the SCSI BIOS in a banner displayed on your computer monitor during boot. If the utility is available, this message also appears on your monitor:

Press Ctrl-C to start LSI Logic Configuration Utility...

This message remains on your screen for about five seconds, giving you time to start the utility. If you decide to press "Ctrl-C", the message changes to:

Please wait, invoking LSI Logic Configuration Utility...

After a brief pause, your computer monitor displays the Main menu of the SDMS PCI SCSI BIOS Configuration Utility.

To make changes with this menu driven utility, one or more SDMS SCSI host adapters must have Non-Volatile Random Access Memory (NVRAM) to store the changes.

These messages may appear during the boot process:

"**Adapter removed from boot order, parameters will be updated accordingly**" appears when an adapter is removed from the system or relocated behind a PCI bridge.

"**Configuration data invalid, saving default configuration!**" appears if information in the NVRAM is invalid.

"**Found SCSI Controller not in following Boot Order List, to Add: Press Ctrl-C to start LSI Logic Configuration Utility...**" or "**Adapter configuration may have changed, reconfiguration is suggested!**" could appear when fewer than four adapters are in the boot order and adapters exist in the system which are not in the boot order.

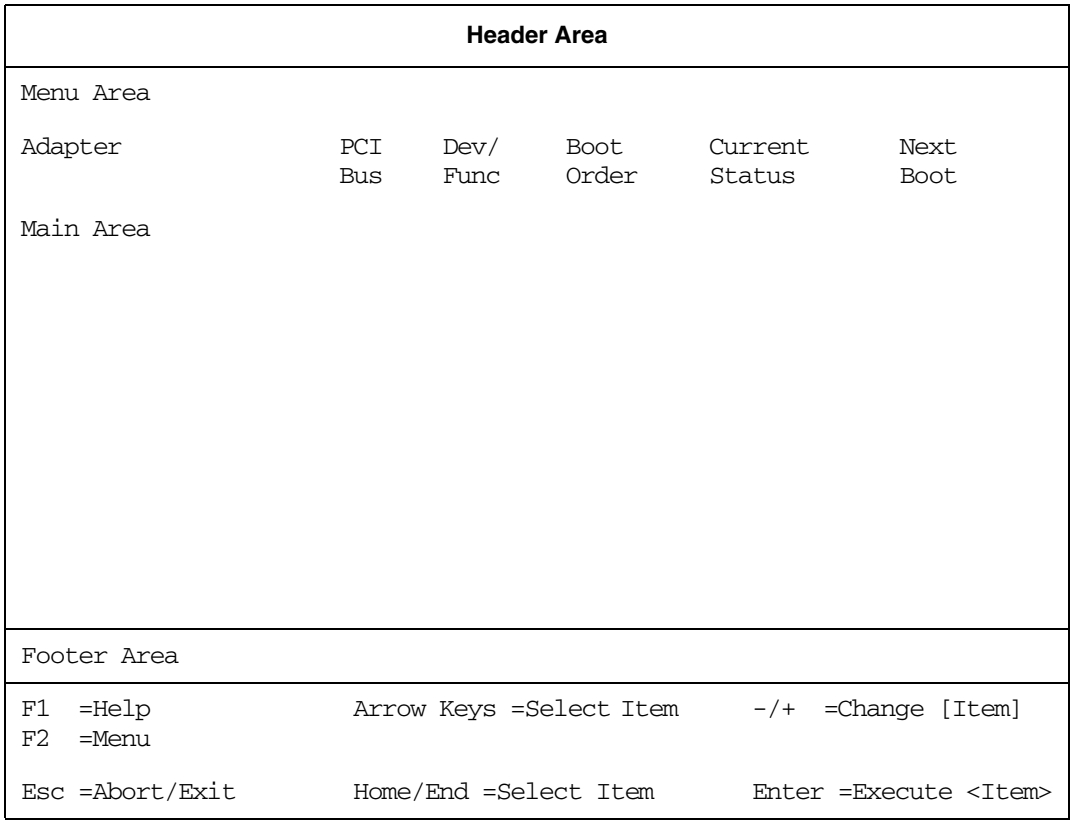
NOTE: The SCSI BIOS Configuration Utility is a powerful tool. If, while using it, you disable all of your controllers, pressing `Ctrl-A` (or `Ctrl-E` on version 4.04 or later) after memory initialization during reboot allows you to re-enable and reconfigure. Also, if the system locks up due to Non-Volatile Storage (NVS), press `Ctrl-N` to bypass the BIOS in order to reflash the card.

Not all devices detected by the SCSI BIOS Configuration Utility can be controlled by the BIOS. Devices such as tape drives and scanners require that a device driver specific to that peripheral be loaded. The SCSI BIOS Configuration Utility does allow parameters to be modified for these devices.

Using the Configuration Utility

Screen Format

All SCSI BIOS Configuration Utility screens are partitioned into fixed areas as shown below.



Header Area

This area provides static information text, which is typically the product title and version.

Menu Area

This area provides the current Main Area's menu, if any. This area has a cursor for menu item selection.

Main Area

This is the main area for presenting data. This area has a cursor for item selection, horizontal scrolling and vertical scrolling. The horizontal and vertical scroll bars appear here.

Footer Area

This area provides general help information text.

User Input

Throughout these screens, selections that are not permissible are grayed out.

F1 = Help	Context sensitive help for the cursor-resident field.
F2 = Menu	Sets cursor context to the menu selection area. Select a menu item and press `Enter`.
Arrow Keys =	Select Item
Home/End =	Select Item Up, down, left, right movement to position the cursor.
+/- = Change [Item]	Items with values in [] brackets are modifiable. Use the '+' or '-' keys in the top row of the main keyboard or use the numeric keypad '+' and '-' keys to change a modifiable field. When pressed, they toggle a modifiable field to its next relative value. For example, '+' toggles the value up and '-' toggles the value down.
Esc = Abort/Exit	Escape aborts the current context operation and/or exits the current screen. User confirmation is requested as required.
Enter = Execute <Item>	Items with values in <> brackets are executable. Press `Enter` to execute the field's associated function.

Main Menu

When you invoke the SDMS SCSI BIOS Configuration Utility, the Main menu appears. This menu displays a scrolling list of up to 256 LSI Logic PCI to SCSI host adapters in the system and information about each of them.

Use the arrow keys to select an adapter, then press `Enter` to view and modify the selected adapter's properties (and to gain access to the attached devices).

Only adapters with LSI Logic Control enabled can be accessed. Adapters with no NVM will show default settings and cannot be changed. After selecting an adapter and pressing `Enter`, the adapter's SCSI bus is scanned and the Adapter Properties menu appears. An example is shown after the descriptions about the Boot Adapter List and Global Properties menus.

On the Main menu, two selections are: Boot Adapter List and Global Properties. Press F2 to access these menus, use the arrow keys to select the desired menu, and press Enter.

"Boot Adapter List" allows selection and ordering of boot adapters.

"Global Properties" allows changes to global scope settings.

To execute an item, select it and press Enter. Here is an example of the Main menu:

LSI Logic SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

<Boot Adapter List> <Global Properties>

LSI Logic Host Bus Adapters

Adapter	PCI Bus	Dev/ Func	Port Number	IRQ	NVM	Boot Order	LSI Logic Control
<53C1010-66	1	68>	1400	11	Yes	0	Enabled

F1 =Help Arrow Keys =Select Item -/+ =Change [Item]
F2 =Menu

Esc =Abort/Exit Home/End =Select Item Enter =Execute <Item>

Field Descriptions

Adapter

Indicates the specific family of LSI Logic Host Adapters.

PCI Bus

Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

Dev/Func

Indicates the PCI Device/Function assigned by the system BIOS to an adapter.

This is an 8-bit value mapped as follows:

Bit # 7 6 5 4 3 2 1 0
> Bits 2-0: Function (range 0 - 7)

> Bits 7-3: Device (range 0x00 - 0x1F, 0 - 31 decimal).

Port Number

Indicates the I/O Port Number that communicates with an adapter. The system BIOS assigns this number.

IRQ

Indicates the Interrupt Request Line used by an adapter. The system BIOS also assigns this value.

NVM

Indicates whether an adapter has non-volatile memory (NVM) associated with it. An adapter's configuration is stored in its associated NVM. NVM can refer to NVRAM that is resident on a host adapter or to the system NVM.

Boot Order

Indicates the relative boot order (0 to 3) of an adapter. The SDMS SCSI BIOS traverses up to four adapters in the specified order in search of bootable media. Access the “Boot Adapter List” Menu to modify this item.

LSI Logic Control

Indicates whether an adapter is eligible for LSI Logic software control, or is reserved for control by non-LSI Logic software.

Global

Indicates global properties that are not associated with a Properties specific adapter or device.

Boot Adapter List

The Boot Adapter List menu specifies the order in which adapters will boot when more than one LSI Logic adapter is in a system. Up to four of the total adapters in a system can be selected as bootable. Adapters can be added or deleted using this menu.

To add an adapter to the boot list, press the `Insert` key while on the Boot Adapter List. This puts the cursor on the adapter select list. Use the arrow keys to select the desired adapter and press `Enter` to add it to the end of Boot Adapter List.

To remove an adapter from the boot list, press the `Delete` key while on the desired adapter in the Boot Adapter List. You can also change the boot order by using the '+' or '-' keys. For example, place the cursor on the adapter that you want to change, and use the '+' or '-' key to raise or lower the boot order.

Here is an example of the Boot Adapter List menu:

LSI Logic SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Boot Adapter List

Insert=Add an adapter Delete=Remove an adapter

Adapter	PCI Bus	Dev/ Func	Boot Order	Current Status	Next Boot
<53C1010-66	1	68>	[0]	On	[On]

F1 =Help Arrow Keys =Select Item -/+ =Change [Item]
F2 =Menu

Esc =Abort/Exit Home/End =Select Item Enter =Execute <Item>

Field Descriptions

Adapter

Indicates the specific family of LSI Logic Host Bus Adapters.

PCI Bus

Indicates the PCI Bus number (range 0x00 - 0xFF, 0 - 255 decimal) assigned by the system BIOS to an adapter.

Dev/Func

Indicates the PCI Device/Function assigned by the system BIOS to an adapter.

This is an 8-bit value mapped as follows:

Bit # 7 6 5 4 3 2 1 0
> Bits 2-0: Function (range 0 - 7)

> Bits 7-3: Device (range 0x00 - 0x1F, 0 - 31 decimal).

Boot Order

Specifies the relative boot order (0 to 3) of an adapter.

- \- : decreases an adapter's relative boot order.
- \+ : increases an adapter's relative boot order.

Current Status

Indicates whether an adapter in the boot list was enabled during the most recent boot. Disabled adapters and their attached devices are ignored by the SDMS SCSI BIOS; they are still visible to the configuration utility.

Next Boot

Specifies whether to enable an adapter upon the next boot. The SDMS SCSI BIOS ignores disabled adapters and their attached devices although they are still visible to the configuration utility.

Global Properties

The Global Properties option on the Main menu allows you to view boot information, set display and video modes, pause if an alert message has been displayed, and other options. Here is an example of the Global Properties menu:

LSI Logic SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Global Properties

Pause When Boot Alert Displayed	[No]
Boot Information Display Mode	[Verbose]
Negotiate With Devices	[Supported]
Video Mode	[Color]
Support Interrupt	[Hook interrupt, the Default]

<Restore Defaults>

```
F1  =Help            Arrow Keys =Select Item        -/+   =Change  [Item]
F2  =Menu

Esc =Abort/Exit      Home/End =Select Item          Enter =Execute <Item>
```

Field Descriptions

Pause When Boot Alert Displayed

This option specifies whether to pause for user acknowledgment after displaying an alert message during boot. The Boot Alert setting can be either No or Yes. To continue after displaying a message, specify No. To wait for any key after displaying a message, specify Yes.

Boot Information Display Mode

This option specifies the information display mode of the BIOS during boot. It controls how much information about adapters and devices are displayed during boot. The Display Mode setting can be either Terse or Verbose. To display minimum information, specify Terse mode. To display detailed information, specify Verbose mode.

Negotiate With Devices

This option sets the default value for synchronous and wide negotiations with specified devices. Options are: All, None or Supported.

Video Mode

This option specifies the default video mode for the SCSI BIOS Configuration Utility. The Video Mode setting can be either Color or Monochrome. The monochrome setting enhances readability on a monochrome monitor.

Support Interrupt

This option allows the ability to prevent a hook on INT40h, if required. The two settings are: Hook Interrupt, the default, and Bypass Interrupt Hook. Hook Interrupt is the normal operation that supports booting CD-ROMs in floppy emulation mode on most machines.

On certain platforms, the system BIOS uses the INT40h interrupt chain in a non-standard way. On these platforms, you should use the “Bypass Interrupt Hook” setting. This setting prevents a hook into the INT40h chain. If the “Bypass Interrupt Hook” setting is used on systems that do not require it, the CD-ROM may fail to boot and an error message may appear and indicate it is unable to read the boot device.

NOTE: Try toggling this value if your machine fails to boot a CD-ROM in floppy emulation mode.

Restore Defaults

Press `Enter` to obtain default settings.

Adapter Properties

The Adapter Properties menu allows you to view and modify adapter settings and SCSI devices connected to it. It also provides access to an adapter's device settings. To display this menu, select a device under the Adapter field on the Main menu and press Enter. Here is an example of the Adapter Properties menu:

LSI Logic SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00

Adapter Properties

Adapter	PCI Bus	Dev/ Func
<53C1010-66	1	68

<Device Properties>	
SCSI Parity	[Yes]
Host SCSI ID	[7]
SCSI Bus Scan Order	[Low to High (0..Max)]
Removable Media Support	[None]
CHS Mapping	[SCSI Plug and Play Mapping]
Spinup Delay (Secs)	[2]
Secondary Cluster Server	[No]
Termination Control	[Auto]
<Restore Defaults>	

```
F1  =Help              Arrow Keys =Select Item          -/+   =Change  [Item]
F2  =Menu

Esc =Abort/Exit        Home/End =Select Item            Enter =Execute <Item>
```

Field Descriptions

If the field displays in grey or yellow text, it is available for changes. If it displays in white text, it is not available.

Device Properties

This option allows you to view and modify device properties. The Device Properties menu appears. Refer to *Device Properties* on page 126 for information about this menu.

SCSI Parity

This field indicates whether SCSI parity is enabled for an adapter. When disabled, it is also necessary to disable disconnects for all devices, as parity checking for the reselection phase is NOT disabled. If a non-parity generating device disconnects, its operation will never complete because the reselection fails due to parity error.

Host SCSI ID

This field indicates the SCSI identifier of an adapter [0-7] or [0-15]. It is recommended that this field be set to the highest priority SCSI identifier, which is 7.

NOTE: 8-bit SCSI devices cannot see identifiers greater than 7.

SCSI Bus Scan Order

This field indicates the order in which to scan SCSI identifiers on an adapter. Changing this item will affect drive letter assignment(s) if more than one device is attached to an adapter.

NOTE: Changing this item may conflict with an operating system that automatically assigns drive order.

Removable Media Support

This field specifies the removable media support option for an adapter. Three settings are allowed:

None indicates no removable media support whether the drive is selected as first (BBS), or is first in the scan order (non-BBS).

Boot Drive Only provides removable media support for a removable hard drive if it is first in the scan order.

With Media Installed provides removable media regardless of the drive number assignment.

CHS Mapping

This field defines how the Cylinder Head Sector values are mapped onto a disk without pre-existing partition information. CHS Mapping allows two settings:

SCSI Plug and Play Mapping (default value) automatically determines the most efficient and compatible mapping.

Alternate CHS Mapping utilizes an alternate, possibly less efficient mapping that may be required if a device is moved between adapters from different vendors.

CAUTION: Neither of these options has any effect after a disk has been partitioned using the FDISK command. The FDISK utility is a tool that you can use to delete partition entries, one or all of them.

If all partition entries are deleted, it is necessary to reboot to clear memory or the old partitioning data will be reused, thus nullifying the previous operation. Use care to ensure that the correct disk is the target of an FDISK command.

Spinup Delay (Secs)

This field indicates the delay in seconds between spinups of devices attached to an adapter. Staggered spinups will balance the total electrical current load on the system during boot. The default value is 2 seconds, with choices between 1 and 10 seconds.

Secondary Cluster Server

This field indicates whether an adapter has one or more devices attached that are shared with one or more other adapters. If so, the SDMS SCSI BIOS should avoid SCSI Bus resets as much as possible.

This option allows you to enable an adapter to join a cluster of adapters without performing any SCSI bus resets. This is a requirement for Microsoft Cluster Server. The default value is No.

Termination Control

This field indicates whether an adapter has automatic termination control. If not available, its current status is either Auto or Off.

Auto means that the adapter automatically determines whether it should enable or disable its termination.

Off means termination at the adapter is off, and the devices at the ends of the SCSI bus must terminate the bus.

NOTE: If Auto is grayed out, it means that termination is automatic, not programmable.

Restore Defaults

To obtain default settings, press `Enter`.

Device Properties

The Device Properties menu allows you to view and update individual device settings for an adapter. Changing a setting for the host device (for example, SCSI ID 7) changes the setting for all devices.

The number of fields displayed requires the menu to scroll left/right in order to display the information. When accessing this menu on-line, use the Home/End keys to scroll to columns currently not displayed. The scroll indicator on the bottom of the menu shows where the cursor is relative to the first and last columns.

Here is an example of the Device Properties menu:

LSI Logic SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00						
Device Properties						
SCSI Device Identifier	MB/Sec	MT/Sec	Data Width	Scan ID	Scan LUNs>0	Disconnect
0	[160]	[80]	[16]	[Yes]	[Yes]	[On]
1	[160]	[80]	[16]	[Yes]	[Yes]	[On]
2	[160]	[80]	[16]	[Yes]	[Yes]	[On]
3 SEAGATE ST31055N	[160]	[80]	[16]	[Yes]	[Yes]	[On]
4	[160]	[80]	[16]	[Yes]	[Yes]	[On]
5	[160]	[80]	[16]	[Yes]	[Yes]	[On]
6	[160]	[80]	[16]	[Yes]	[Yes]	[On]
7 53C1010-33	[160]	[80]	[16]	[Yes]	[Yes]	[On]
8	[160]	[80]	[16]	[Yes]	[Yes]	[On]
9	[160]	[80]	[16]	[Yes]	[Yes]	[On]
10	[160]	[80]	[16]	[Yes]	[Yes]	[On]
11	[160]	[80]	[16]	[Yes]	[Yes]	[On]
12	[160]	[80]	[16]	[Yes]	[Yes]	[On]
13	[160]	[80]	[16]	[Yes]	[Yes]	[On]
14	[160]	[80]	[16]	[Yes]	[Yes]	[On]
15	[160]	[80]	[16]	[Yes]	[Yes]	[On]

SCSI Device Identifier	SCSI Timeout	Queue Tags	Boot Choice	Format	Verify	Restore Defaults
0	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
1	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
2	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
3 SEAGATE ST31055N	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
4	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
5	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
6	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
7	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
8	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
9	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
10	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
11	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
12	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
13	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
14	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>
15	< 10>	[On]	[No]	<Format>	<Verify>	<Defaults>

F1 =Help F2 =Menu	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit	Home/End =Select Item	Enter =Execute <Item>

Field Descriptions

SCSI Device Identifier

This field indicates the device's SCSI Identifier.

Sync Rate (MB/Sec and MT/Sec)

MB/Sec displays the maximum synchronous data transfer rate [0/ 5/ 10/ 20/ 40/ or 160] of the adapter in mega bytes per second corresponding to the width and transfer rate settings that follow.

MT/Sec is a configuration field where these values [0/ 5/ 10/ 20/ 40/ or 80] can be changed. This field indicates the maximum synchronous data transfer rate of the adapter in mega transfers per second. It can be changed to a lower transfer rate.

Data Width

This field indicates the maximum data width in bits.

Scan ID

This field indicates whether to scan for this SCSI identifier at boot time. This item can be used to ignore a device and to decrease boot time by disabling the inquiry of unused SCSI identifiers.

Set this option to “No” if there is a device that you do not want to be available to the system. Also, on a bus with only a few devices attached, the user can speed up boot time by changing this setting to “No” for all unused SCSI IDs.

Scan LUNs > 0

This field indicates whether to scan for LUNs greater than zero for a device. LUN zero is always queried. This option should be used if a multi-LUN device responds to unoccupied LUNs or if it is desired to reduce the visibility of a multi-LUN device to LUN zero only.

Set this option to “No” if you have problems with a device that responds to all LUNs whether they are occupied or not. Also, if a SCSI device with multiple LUNs exists on your system but you do not want all of those LUNs to be available to the system, then set this option to “No.” This will limit the scan to LUN 0 only.

Disconnect

This field indicates whether to allow a device to disconnect during SCSI operations. Some (mostly newer) devices run faster with disconnect enabled, while some (mostly older) devices run faster with disconnect disabled.

SCSI Timeout

This field indicates the maximum amount of time [0 to 9999] in seconds to wait for a SCSI operation to complete.

Since timeouts provide a safeguard that allows the system to recover should an operation fail, it is recommended that a value greater than zero be used. A value of zero allows unlimited time for an operation to complete and could result in the system hanging (waiting forever) should an operation fail.

Press `Enter`, type in a value, and then press `Enter` again to specify a new timeout value.

Queue Tags

This field indicates whether to allow the use of queue tags for a device. Currently the BIOS does not use queue tags. This item specifies queue tag control to higher level device drivers.

Boot Choice

This field indicates whether this device may possibly be selected as the boot device. This option is only applicable to devices attached to adapter number zero (in the boot list) on non-BBS systems. It provides primitive BBS flexibility to non-BBS systems.

Format

Press `Enter` to low-level format the device. If enabled, this option allows low-level formatting on a disk drive. Low-level formatting will completely and irreversibly erase all data on the drive.

NOTE: Formatting will default the drive to a 512-byte sector size even if the drive had previously been formatted to another sector size.

Verify

Press `Enter` to verify all sectors on the device and to reassign defective Logical Block Addresses (LBAs).

Restore Defaults

Press `Enter` to obtain default settings.

Exiting the SCSI BIOS Configuration Utility

The Exit menu for the SCSI BIOS Configuration Utility is used for all five of the configuration menus. However, the available functionality is different for the Main menu and the four subordinate menus. Below is an example of the Exit menu:

LSI Logic SDMS (TM) PCI SCSI Configuration Utility Version PCI-4.19.00		
Adapter and/or device property changes have been made <Cancel exit> Exit the Configuration Utility <Save changes then exit this menu> <Discard changes then exit this menu>		
F1 =Help F2 =Menu	Arrow Keys =Select Item	-/+ =Change [Item]
Esc =Abort/Exit	Home/End =Select Item	Enter =Execute <Item>

To exit from the Adapter Properties, Device Properties, Boot Adapter List or Global Properties menus, use these exit options:

Cancel Exit

This option returns you to the previous menu.

Save changes then exit this menu

This option implements any changes you made on the previous menu and returns you to the Main menu.

Discard changes then exit this menu

This option restores the default settings and returns you to the Main menu.

To exit from the Main menu, use these exit options:

Cancel Exit

This returns you to the Main menu.

Exit the Configuration

This option exits the configuration utility and automatically reboots your system.

NOTE: If you reboot the system without properly exiting from this utility, some changes may not take effect.

Appendix

F

Sample C Software

Contents

Directory \VME 132
Directory \fpga 132
Directory \include 133
Directory \max6657 133
Directory \support 133
Directory \vlm 133

Introduction

This appendix provides listings of a library of sample code that the programmer may utilize to build applications. These files are provided in the directory "\sample code" on CD 320-500077-000, labeled "Windows Drivers", included with the VMIVME-7645.

These files are provided without warranty. All source code is ©2001, VMIC Corporation.

Directory \VME

This directory contains code used to setup the Universe II chip with one PCI-to-VME window and enable Universe II registers to be accessed from the VMEbus to allow mailbox access.

Directory \fpga

This directory contains code used to test the functions of the VMIC-designed FPGA such as timers, SRAM controller and Watchdog Timer.

Directory \include

This directory contains common files required to compile several of the sample code applications.

Directory \max6657

This directory contains code that demonstrates how to read the temperatures from the max6657 device on the VMIVME-7645.

Directory \support

This directory contains memory and PCI access routines used by many of the sample code applications.

Directory \vlm

This directory contains code that demonstrates how to read the voltages from the analog inputs of the super I/O component on the VMIVME-7645.

Index

Numerics

1000BaseT 49, 75
100BaseTx 49, 75
10BaseT 49, 75

B

BIOS 30, 44

C

CMOS configuration 30
connectors 24, 26
CPU board diagram 25
customer service 24, 65

D

DMA controller 38
DMA page registers 38

H

hexadecimal 22

I

I/O
  address space 38
  port map 38
installation 29
Intel 82551ER Ethernet Controller 49
Intel programmers 22
interrupt line assignment 40

J

jumper locations 25

M

master interrupt controller 38
memory address map 37
Motorola programmers 22

N

Non-Maskable Interrupt (NMI) 40, 47

O

offset address conversions 22

P

PCI
  interrupt lines 43
  local bus 43
PCI Configuration Space Registers 56
programmable timer 38
protected mode 37, 41

R

real mode 37, 41
real-time clock 38
Return Material Authorization (RMA) number 65

S

Serial I/O (COM1,2,3 & 4) 39
serial port connector, D9 or RS-232 69
SERR interrupt 47
SIZE 37

T

technical support 24, 65

U

unpacking procedures 23
USB port connector 76

V

vector interrupt table 40
VMEbus connectors 67

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