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Find the *Abaco Systems / VMIC VMIVME-7663-100* at our website: ***Click HERE***

VMIVME-7663

Ultra Low Voltage Intel® Celeron® VMEbus Single Board Computer

This product is no longer available.

- ***Intel® ultra low voltage Celeron® 650 MHz processor***
- ***128 Mbyte PC-100 SDRAM***
- ***100 MHz system bus via Intel 815E chipset***
- ***Dual Ethernet controllers supporting 10BaseT and 100BaseTX interfaces***
- ***Ultra DMA/100 hard drive and floppy drive controllers***
- ***Two high performance 16550-compatible serial ports***
- ***Remote Ethernet booting***
- ***PMC expansion site***
- ***Operating system support for Windows® 2000, Windows XP, QNX®, Linux® and VxWorks®***

Functional Characteristics

Microprocessor: The VMIVME-7663 is based on the Intel ultra low voltage Celeron processor. The enhanced Celeron processor has 256 Kbyte of on-die L2 cache. The µFCBGA package processors offer thermal characteristics that are well suited for embedded systems operating over a wide range of temperatures.

DRAM Memory: The VMIVME-7663 accepts one 144-pin SODIMM
PC-100 module for a maximum memory configuration of 128 Mbyte.

BIOS: The VMIVME-7663 System BIOS and video BIOS are provided in reprogrammable memory.

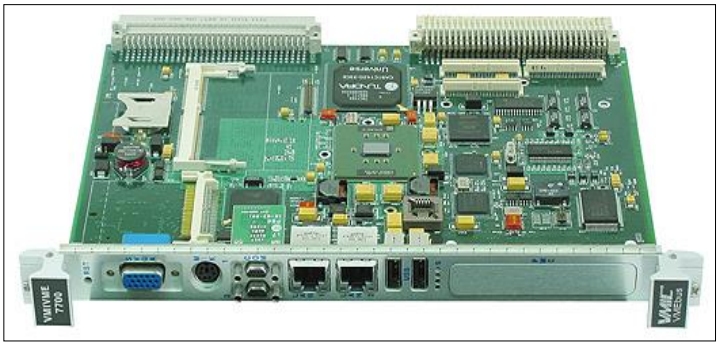
Video Graphic Controller: High-resolution graphics and multimedia-quality video are supported on the VMIVME-7663 by an internal 815E AGP graphics controller. A fully functional, integrated 2D/3D graphics accelerator provides pixel processing and rendering, with display resolutions of up to 1600 x 1200 supported. The video output is provided through the front panel.

IDE Interface: The VMIVME-7663 provides an IDE interface for hard disk drive support. The IDE interface allows support of several types of data transfers: Programmed I/O (PIO), 8237 style DMA, Ultra ATA/33, Ultra ATA/66 and Ultra ATA/100.

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Ethernet Controller: The VMIVME-7663 provides two front panel connections to either 10BaseT or 100BaseTX LAN using two Intel 82551ER Ethernet controllers. Standard RJ45 connectors are provided on the front panel with two network status indicators.

Ordering Options							
Oct. 20, 2004 814-007663-000 A		A	B	C	D	E	F
VMIVME-7663	–			0	0	0	

A = Processor
0 = Reserved
1 = 650 MHz Ultra Low Voltage Celeron Processor
B = SDRAM Memory
1 = 128 Mbyte
2 = Reserved
C = 0 (Reserved for future use.)
D = 0 (Reserved for future use.)
E = 0 (Reserved for future use.)
F = Special Sales Order
0 = VME standard
1 = 1101.10 front panel

Connector Adapter

Abaco Systems Part Number 360-010050-001. The connector adapter is a 9-pin Micro-D to standard D serial adapter. The 360-010050-001 connector adapter is sold separately.

Note

All VME single board computer products come standard with a VME specification compliant front panel.

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Remote Ethernet Booting: The VMIVME-7663 utilizes an Expansion ROM BIOS which enables processor booting from a network server. The facility supports PXE and a variety of network boot protocols including BOOTP and DHCP (TCP/IP).

Universal Serial Bus (USB): The VMIVME-7663 provides front panel dual connection hub host controllers for the USB. Supported USB features include: isochronous data transfers, asynchronous messaging, self-identification and configuration of peripherals, and dynamic (hot) attachment.

Serial Ports: The VMIVME-7663 provides two 16550-compatible serial ports. Each serial port has an independent 16-byte FIFO supporting baud rates up to 115 kbaud. Connection for both serial ports is provided by two micro DB-9 connectors located on the front panel. The micro DB-9 connectors require two micro DB-9 to standard DB-9 adapters, Abaco Systems P/N 360-010050-001.

PMC Expansion Site: The VMIVME-7663 provides one IEEE 1386.1, 5 V PCI mezzanine card (PMC) expansion site. This expansion capability allows the addition of peripherals offered for PMC applications. The PMC site provides for standard I/O out the VMEbus front panel.

Keyboard and Mouse Ports: The VMIVME-7663 supports a PS/2 keyboard and mouse through the front panel.

Hardware Reset: A hardware reset switch is accessible from the front panel.

Programmable Timer: The VMIVME-7663 provides the user with two 16-bit timers and two 32-bit timers. These timers are mapped in PCI memory space, are completely software programmable and can generate PCI bus interrupts.

Watchdog Timer: The VMIVME-7663 provides a software-programmable watchdog timer. The watchdog timer is enabled under software control. Once the timer is enabled, software must access the timer within the specified time period, or the output of the watchdog timer will reset the unit.

Nonvolatile SRAM: The VMIVME-7663 provides 32 Kbyte of nonvolatile SRAM. The contents of the SRAM are preserved when +5 V power is interrupted or removed from the unit.

CMOS Battery: The VMIVME-7663 uses a holder that permits field replacement of the CMOS battery. A header and jumper allows the battery to be disconnected from the circuitry for long-term storage.

Annunciators: Indicators for the board status, +5 V power good, are provided on the front panel. In addition, two indicators for the Ethernet adapter activity are located on each RJ45 network connector.

Thermal Management: The VMIVME-7663 utilizes a passive heat sink that relies on forced air cooling within the equipment rack at the specified flow rate. Please refer to the environmental specifications for more information.

VMEbus Interface: The VMIVME-7663 VMEbus interface is based on the Universe IID high performance PCI-to-VMEbus interface from Newbridge/Tundra.

System Controller: The VMEbus system controller capabilities allow the board to operate as a slot 1 controller, or it can be disabled when another board is acting as the system controller. The system controller may be programmed to provide the following modes of arbitration:

Round Robin (RRS)
Single Level (SGL)
Priority (PRI)

The system controller provides a SYSCLK driver, IACK* daisy-chain driver, and a VMEbus access timeout timer. The system controller also provides an arbitration timeout if BBSY* is not seen within a specified period after a BGOUT* signal is issued. This period is programmable for 16 or 256 µs.

VMEbus Requester: The microprocessor can request and gain control of the bus using any of the VMEbus request lines (BR3* to BR0*) under software control. The requester can be programmed to operate in any of the following modes:

Release-On-Request (ROR)
Release-When-Done (RWD)
VMEbus Capture and Hold (VCAP)

Mailboxes: The VMEbus interface provides four 32-bit mailboxes, which are accessible from both the microprocessor and the VMEbus providing interprocessor communication. The mailboxes have the ability to interrupt the microprocessor when accessed by the VMEbus.

Interrupt Handler: The interrupt handler monitors, and can be programmed to respond to any or all VMEbus IRQ* lines. All normal-process VMEbus-related interrupts can be mapped to PCI INTA# or SERR# interrupts. These include:

Mailbox interrupts
VMEbus interrupts
VMEbus interrupter IACK cycle (acknowledgment of VMIVME-7663 VMEbus-issued interrupts)

All error processing VMEbus-related interrupts can be mapped to PCI INTA# or SERR#. Note: PCI SERR# initiates an SBC NMI. These include:

ACFAIL* interrupt
BERR* interrupt
SYSFAIL* interrupt

The interrupt handler has a corresponding STATUS/ID register for each IRQ* interrupt. Once the handler receives an IRQ*, it requests the VMEbus and, once granted, it performs an IACK cycle for that level. Once the IACK cycle is complete and the STATUS/ID is stored in the corresponding ID register, an appropriate interrupt status bit is set in an internal status register, and a PCI interrupt is generated. The PCI interrupt can be mapped to PCI INTA# or SERR#.

Interrupter: Interrupts can be issued under software control on any or all of the seven VMEbus interrupt lines (IRQ7* to IRQ1*). A common ID register is associated with all interrupt lines. During the interrupt acknowledge cycle, the interrupter issues the ID to the interrupt handler. The interrupter can be programmed to generate a PCI INTA# or SERR# interrupt when a VMEbus interrupt handler acknowledges a software-generated VMEbus interrupt.

Byte Swapping: The Intel 80x86 family of processors uses little-endian format. To accommodate VMEbus modules that transfer data in big-endian format, such as the 680x0 processor family, the VMIVME-7663 incorporates byte-swapping hardware. This provides independent byte swapping for both the master and slave interfaces. Both master and slave interface byte swapping are under software control. The VMIVME-7663 supports high throughput DMA transfers of bytes, words and longwords in both master and slave configurations. If endian conversion is not needed, we offer a special "bypass" mode that can be used to further enhance throughput. (Not available for byte transfers.)

Master Interface: MA32:MBLT32:MBLT64 (A32:A24:A16:D32:D16:D8 (EO):BLT32)

The VMEbus master interface provides nine separate memory windows into VMEbus resources. Each window has separate configuration registers for mapping PCI bus transfers to the VMEbus (that is, PCI bus base address, window size, VMEbus base address, VMEbus access type, VMEbus address/data size, etc.). The maximum/minimum window sizes for the nine windows are as follows:

Window	Minimum Size	Maximum Size
0, 4	4 Kbyte	4 Gbyte
1 to 3, 5 to 7	64 Kbyte	4 Gbyte
Special Cycle	64 Mbyte	64 Mbyte

Slave Interface: Memory Access SAD032:SD32:SBLT32:SBLT64 (A32:A24:A16:D32:D16:D8 (EO): BLT32)

The VMEbus slave interface provides eight separate memory windows into PCI resources. Each window has separate configuration registers for mapping VMEbus transfers to the PCI bus (that is, VMEbus base address, window size, PCI base address, VMEbus access type, VMEbus address/data size, etc.). The maximum/minimum window sizes for the eight windows are as follows:

Window	Minimum Size	Maximum Size
0, 4	4 Kbyte	4 Gbyte
1 to 3, 5 to 7	64 Kbyte	4 Gbyte

In addition, each window can be programmed to operate in coupled or decoupled mode. In decoupled mode, the window utilizes a write-posting FIFO and/or a read prefetching FIFO for increased system performance. In coupled mode, the FIFOs are bypassed and VMEbus transactions are directly coupled to the PCI bus (that is, transfers on VMEbus are not completed until they are completed on the PCI bus).

Enhanced Bus Error Handling: Enhancements over the Universe chip's bus error handling features are provided. A latch and register are provided to allow the SBC to read the VMEbus address that caused the bus error in all modes. The Universe chip's support is limited to decoupled mode. Support for bus cycle timeout and assertion of bus error is provided. The board may be configured to assert bus error upon timeout regardless of its status as system controller. The Universe chip asserts bus error only if it is the system controller. In addition, this board may be configured to assert an interrupt upon bus cycle timeout.

Back Panel Configuration: The VMIVME-7663 provides support for external IDE disk drive and floppy drive through the VMEbus P2 backplane connector and the VMIACC-0562 backplane adapter.

Operating System and Software Support

The VMIVME-7663 provides embedded features beyond PC/AT functionality. These features are supported by Abaco Systems software products aimed at developers who are incorporating Abaco Systems SBCs, I/O boards and workstations into systems. The VMIVME-7663 supports a variety of operating systems including Microsoft® Windows 2000, Windows XP, QNX, Linux and VxWorks.

Physical/Environmental Specifications

Dimensions: 6U (4HP) single slot Eurocard form factor

Height	9.2 in. (233.4 mm)
Depth	6.3 in. (160 mm)
Thickness	0.8 in. (20.3 mm)

Power Requirements:
+5 VDC (±5 percent), 4.0 A (typical), 5.4 A maximum
+12 VDC (±5 percent), Less than 1 mA
-12 VDC (±5 percent), Less than 1 mA

Airflow: Forced air cooling required: 350 LFM minimum, measured at the top (outlet) of the unit

Temperature:
Operating: 0 to +70 °C
Storage: -40 to +80 °C

Altitude:
Operating: 0 – 10,000 ft (3,000 m)
Storage: 0 – 40,000 ft (12,000 m)

Humidity:
Operating: relative humidity 5% to 95%, noncondensing
Storage: relative humidity 5% to 95%, noncondensing

VMEbus Interface:

DTB Master: BLT32/BLT64, A32/D32, A24/D32, A16/D32
DTB Slave: BLT32/BLT64, A32/D32, A24/D32, A16/D32
Requester: Programmable, BR(3 to 0), ROR, RWD, BCAP
Interrupt Handler: IH(1 to 7) D8(O)
Interrupter:Programmable, IRQ7* to IRQ1*
Arbiter: SGL, PRI, RRS
BTO: Programmable (4 to 1,024 µs)
Compliance: ANSI/VITA 1-1994

PMC Expansion Site Connector: 5 V signaling, types 1 and 2
32-bit PCI bus, 33 MHz maximum

MTBF: TBD

Regulatory: CE Mark

The VMIVME-7663 has been designed to meet the following CE Standards where applicable:

EN55022/55024-1
EN55022 Radiated Emissions Class A
EN55022 Conducted Emissions Class A
EN61000-3-2 (Harmonic Current Emissions)
EN61000-3-3 (Voltage Fluctuations and Flicker)
EN61000-4-2 (ESD)
EN61000-4-3 (Radiated Immunity)
EN61000-4-4 (EFT)
EN61000-4-5 (Surge)
EN61000-4-6 (Conducted RF)
EN61000-4-8 (Power Frequency Magnetic Fields)
EN61000-4-11 (Voltage Dips and Interruption)

Safety:

The VMIVME-7663 has been designed to meet the following UL Standards where applicable:

UL60950/EN60950 (LVD)

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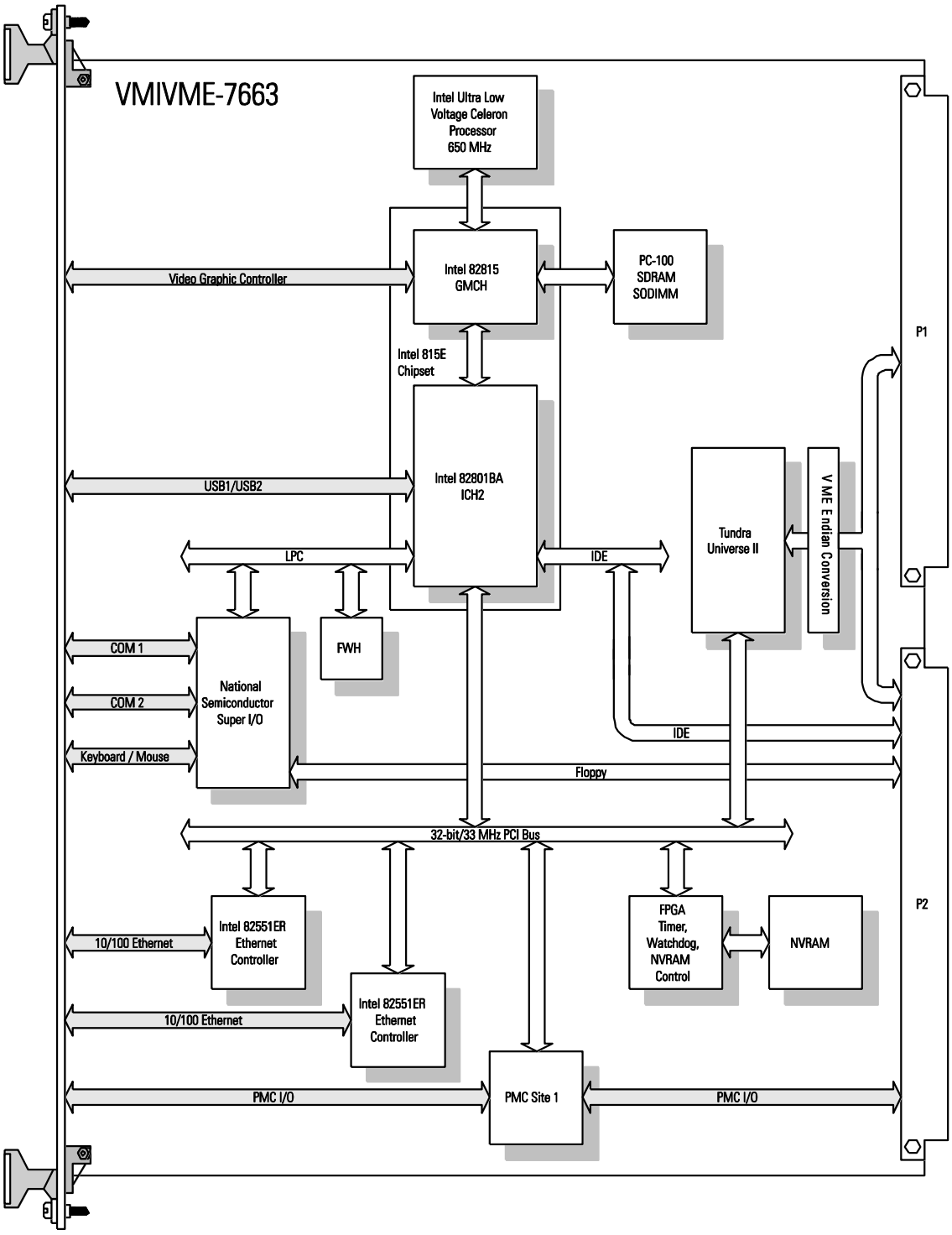


Figure 1. VMIVME-7663 Block Diagram

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