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VMIVME-DMA

VMEbus DMA INTERFACE

INSTRUCTION MANUAL

SECOND EDITION

DOCUMENT NO. 500-000DMA-000

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RECORD OF REVISIONS

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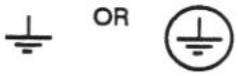
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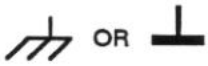
Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.



Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.



Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

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The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-DMA
VMEbus DMA Interface

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A Assembly Drawing, Parts List, and Schematic
B Integrated Circuit Technical Specifications
C DMA Test Software Listing

SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIVME-DMA VMEbus DMA Interface is a general-purpose DMA interface that is compatible with the VMEbus. It can be interfaced with a user's device or connected back-to-back with another VMIVME-DMA to form a high performance VMEbus-to-VMEbus link. Features of the VMIVME-DMA include the following:

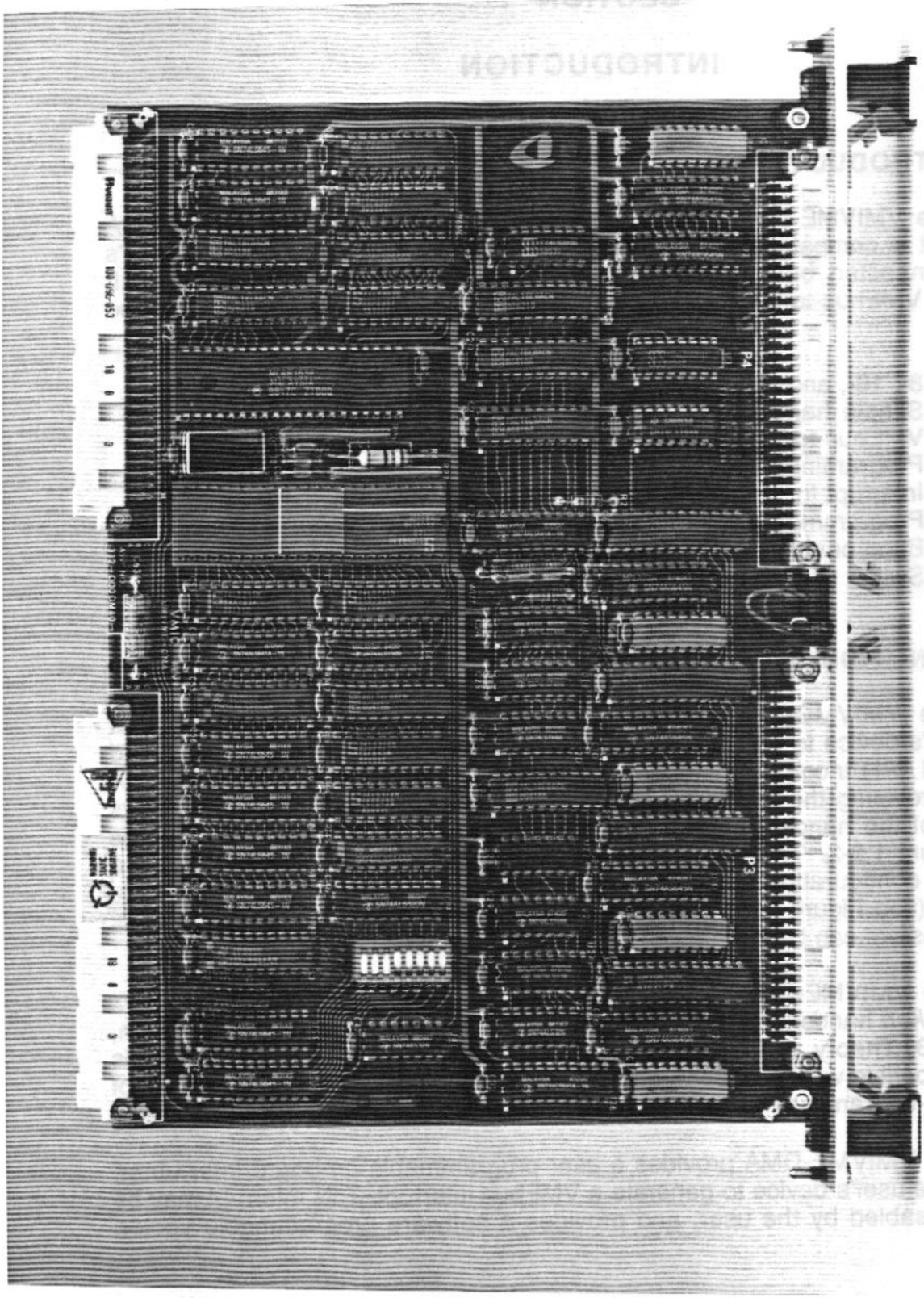
a. 8-, 16-, and 32-bit parallel DMA data transfers
b. Simple handshake
c. VMEbus-to-VMEbus link using two VMIVME-DMAs
d. Programmable address modifiers
e. Interrupt for user's device
f. Programmable interrupt vectors and levels
g. Burst or single-cycle transfers
h. Switch selectable module address

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-DMA provides a general purpose DMA interface that allows a user's device to be connected to the VMEbus. The VMIVME-DMA Board (see Figure 1.2-1) incorporates a 68430 DMA integrated circuit to control DMA transfer by providing the logic necessary to control the VMEbus during transfers and to control the handshake with the user's device. A typical configuration is shown in Figure 1.2-2. The VMIVME-DMA also has the capability of operating in a back-to-back configuration with another VMIVME-DMA to provide a VMEbus-to-VMEbus link (see Figure 1.2-3). If both VMEbuses implement a 32-bit data path, the 32-bit transfers can be performed.

The VMIVME-DMA provides a simple request/acknowledge and *data ready/data taken* handshake to the user's device. For more detailed information, see Section 3, Theory of Operation. The 68430 used in the VMIVME-DMA is software compatible with the 68440 and the 68450, and it also has the capability of performing 32-bit transfers in a single cycle.

The VMIVME-DMA provides a user programmable on-board interrupter. This allows the user's device to generate a VMEbus interrupt. This interrupt may be enabled or disabled by the user, and provides a software programmable vector.



MDMA/F1.2-1

Figure 1.2-1. VMIVME-DMA Photograph

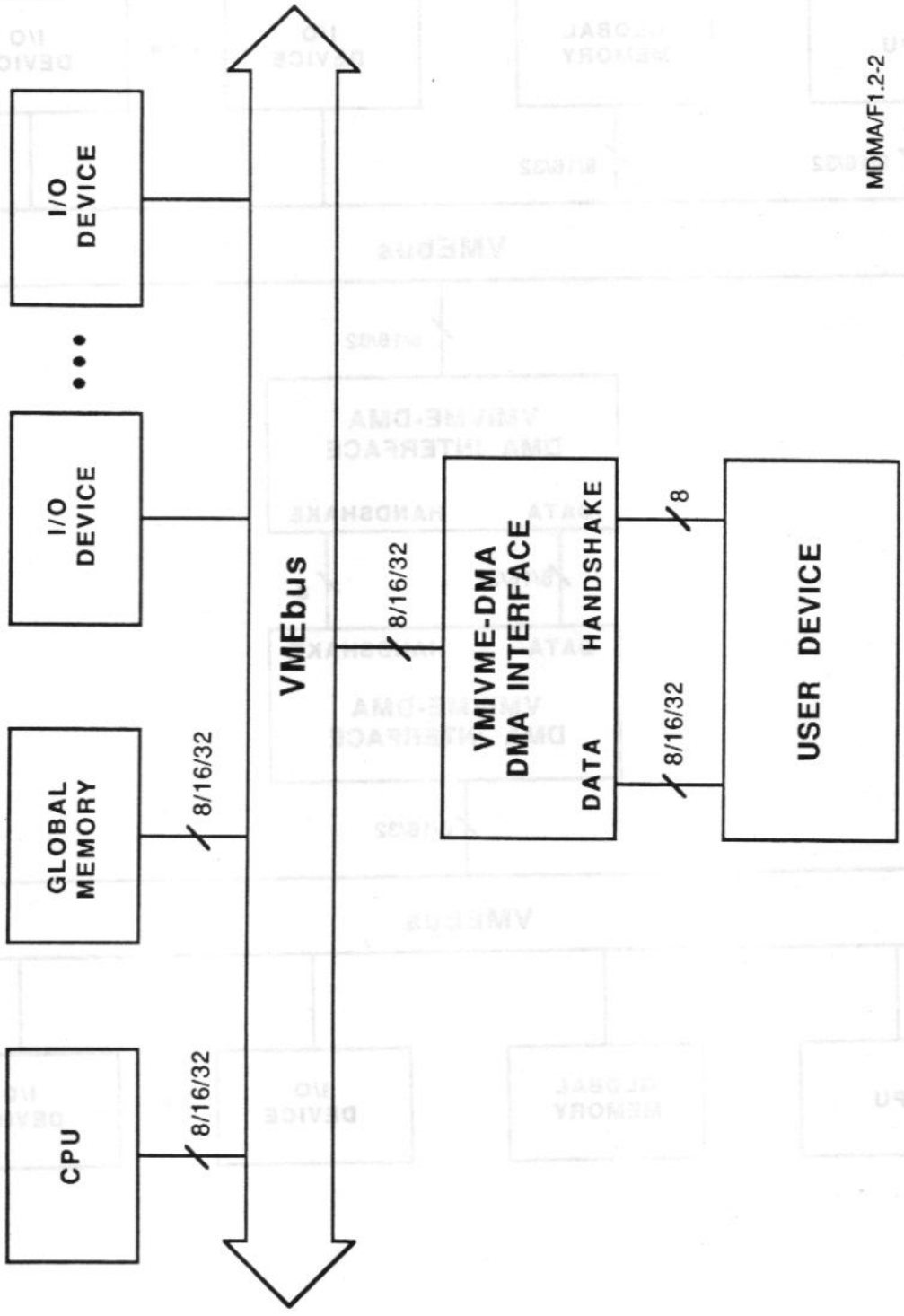


Figure 1.2-2. Typical VMIVME-DMA Configuration with User Device

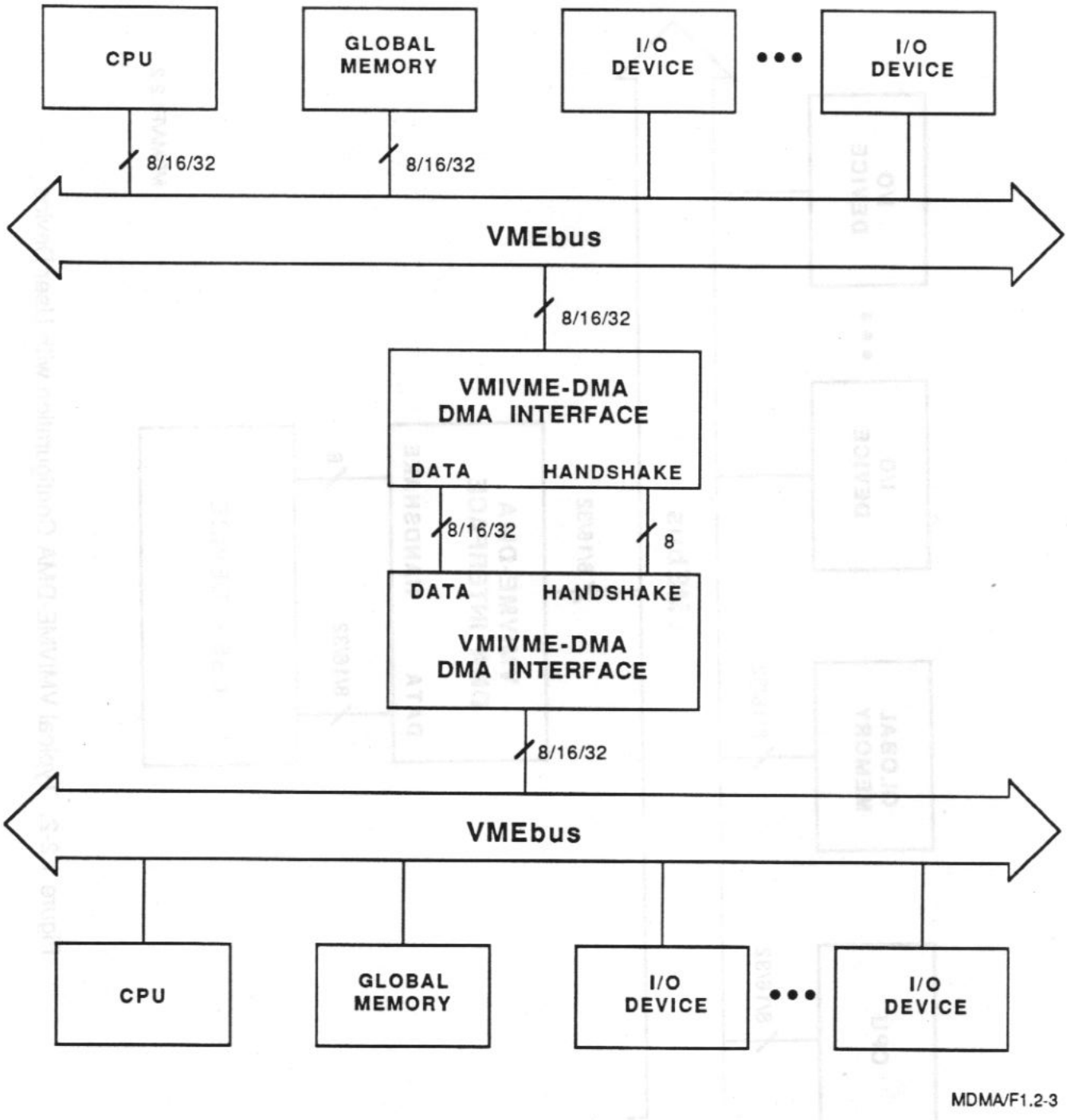


Figure 1.2-3. Typical VMIVME-DMA Back-to-Back Configuration

The VMIVME-DMA also provides a user-programmable output that may be used to interrupt and alert the user's device.

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

2.1 PHYSICAL DESCRIPTION

The VMIVME-DMA interface is implemented on a double Eurocard form factor printed circuit board. Connection to a user's device, or to another VMIVME-DMA, is accomplished via two 64-conductor flat-ribbon cables accessible from the front panel. The VMIVME-DMA has two male DIN connectors (Panduit No. 100-964-053) which mate with DIN connectors designed for flat-ribbon cables (Panduit No. 120-964-455).

2.2 DETAILED SPECIFICATIONS

Detailed specifications are shown in Section 2.3. Transfer rates listed are a function of the speed of global memories and interconnecting cable length. Specifications listed were measured using two DMA boards connected back-to-back as a VMEbus communication link.

The user should refer to Section 5 of this manual for additional information concerning the configuration and installation of this product.

2.3 SPECIFICATIONS

VMEbus MASTER/SLAVE

As a master:	A16:A24:D8:D16:D32 Bus request levels 0, 1, 2, or 3 (jumper selectable)
As a slave:	A16:D8:D16 Addressable on 256-byte boundaries

TRANSFER SPECIFICATIONS

Maximum Transfer Rate	
Burst:	4.65 Megabytes/sec (0.86 µs/transfer)*
Single Cycle:	2.3 Megabytes/sec (1.74 µs/transfer)*
Transfer Mode:	Bidirectional half duplex

*Transfer rates degrade as function of cable length and memory access time. Rates specified are for 125 ns memory and 25-foot cables. Add 4 nanoseconds per foot per transfer.

Transfer Size:	8, 16, 32 bits**
Maximum Block Size:	256 K-4 bytes
Word Counter Range:	16 bits
Address Counter Range:	24 bits

I/O CABLES (not included)

Connection Cables:	Two 64-conductor flat-ribbon cables
Maximum Cable Length:*	50 feet

POWER REQUIREMENTS 3.0 A typical at +5 VDC

ENVIRONMENTAL REQUIREMENTS

Temperature Range:	0° to 55 °C, Operating -20° to 85 °C, Storage
Relative Humidity Range:	20% to 80%, non-condensing

PHYSICAL DIMENSIONS Double Eurocard 160 mm x 233.4 mm x 12 mm EXP

*Transfer rates degrade as function of cable length and memory access time. Rates specified are for 125 ns memory and 25-foot cables. Add 4 nanoseconds per foot per transfer.

**32-bit global memory required.

SECTION 3

THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

As shown in the functional block diagram (see Figure 3.1-1), the VMIVME-DMA interface provides for the exchange of program controlled interrupts and status, as well as a 32-bit data bus with handshake signals. The functions of these interface signals are described in Section 3.9. The handshake sequencing of the signals is depicted in Figures 3.1-2 and 3.1-3. Although the VMIVME-DMA interface was developed for high-speed, 32-bit, VMEbus link communications, it may also be used as a general purpose DMA controller.

3.2 OPERATIONAL OVERVIEW

The VMIVME-DMA may be utilized in a VME-to-VME link (back-to-back configuration) or linked to an external device. In a VME-to-VME link, the VMIVME-DMA communicates with another DMA board in a separate VMEbus chassis. The VMIVME-DMA may communicate with a user's device provided, however, that custom logic is added to a compatibility board.

To operate in any application, a transfer protocol (see Section 3.3) must be established. Once this is determined, the VMIVME-DMA may be programmed, as detailed in Section 4.1. The operation of this device requires that the bus transfer type (word/byte and direction) is set before the start of any data transfers, and not on a cycle-by-cycle basis. Detailed functional block diagrams of all major logic sections of the DMA board are shown in the figures throughout this section of the manual.

3.3 TRANSFER PROTOCOL

In order for DMA transfers to take place, the DMA interfaces must be set up at both ends of the link. Therefore, if a CPU on one bus is to set up a data transfer, a second CPU on the second bus must set up the DMA interface on that bus to the correct memory address, word count, and direction of transfer.

The manner in which CPUs in two separate buses determine the proper setup sequences is referred to as the transfer protocol. There are several types of protocols that may be used with the DMA.

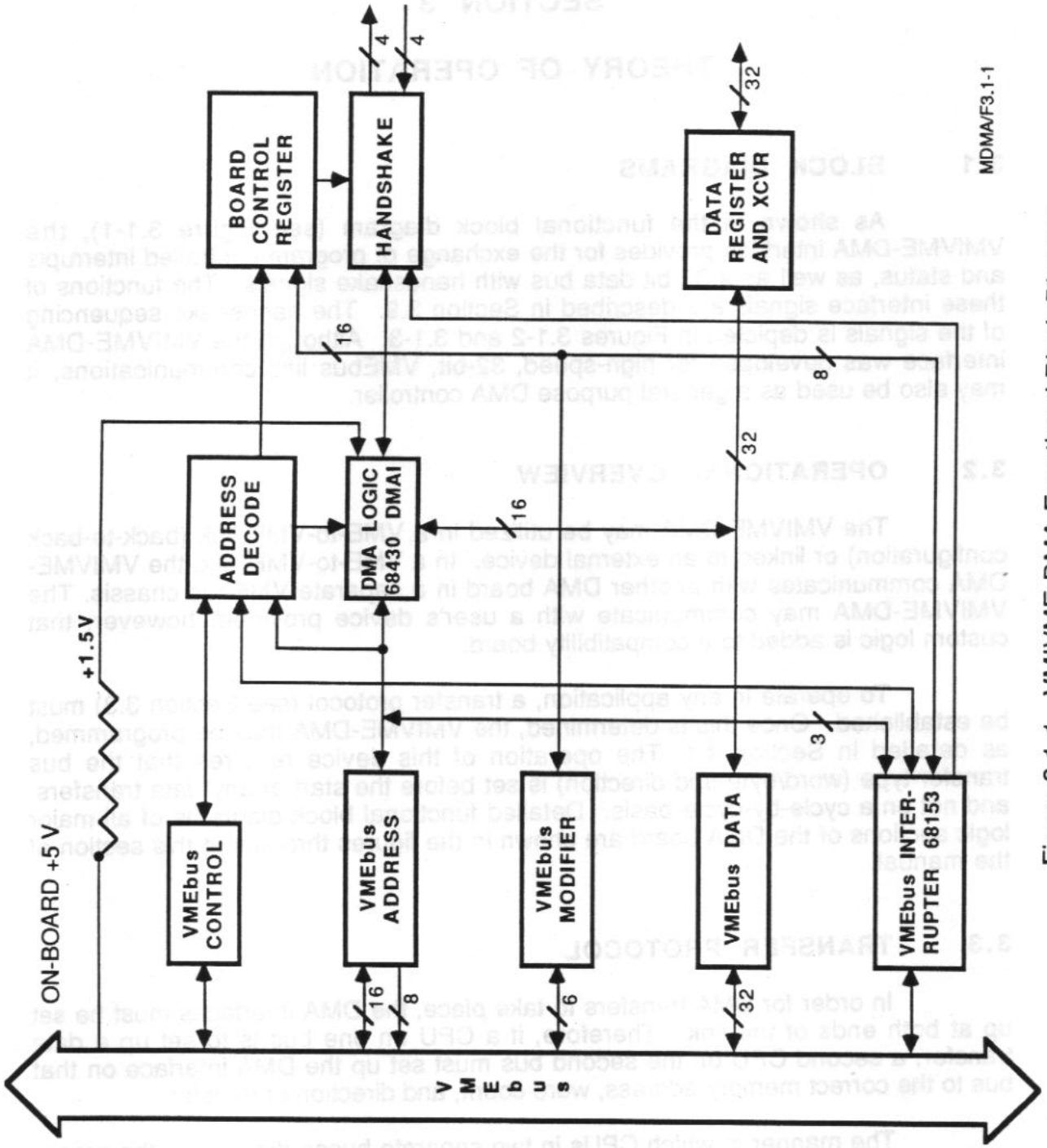
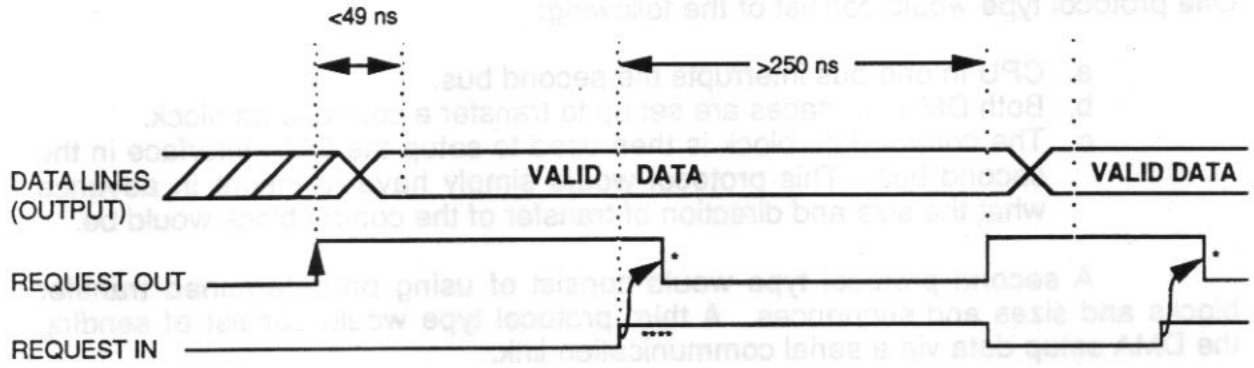


Figure 3.1-1. VMIVME-DMA Functional Block Diagram

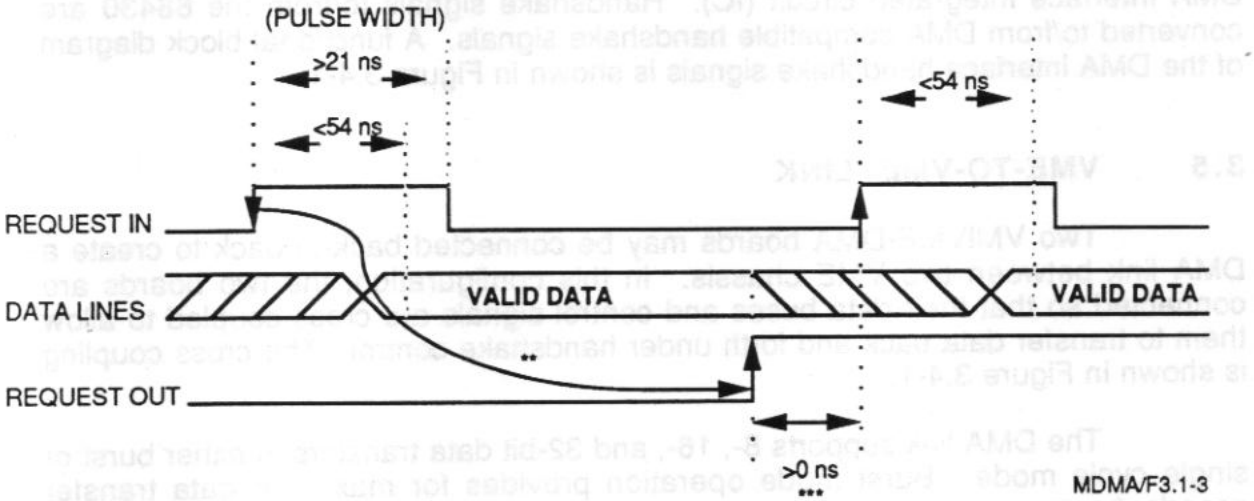


*The rising edge of REQUEST IN clears REQUEST OUT.

MDMA/F3.1-2

**** Do Not Assert REQUEST IN until >250ns after TRANSMIT CMD goes LOW.

Figure 3.1-2. Timing for Output Data Transfers



MDMA/F3.1-3

**Rising edge of REQUEST IN initiates the rising edge of REQUEST OUT.

***Do not assert REQUEST IN until the prior data word has been acknowledged by a positive edge on the REQUEST OUT line.

Figure 3.1-3. Timing for Input Data Transfers

One protocol type would consist of the following:

a. CPU in one bus interrupts the second bus.
b. Both DMA interfaces are set up to transfer a control data block.
c. The control data block is then used to setup the DMA interface in the second bus. This protocol would simply have to insure in advance what the size and direction of transfer of the control block would be.

A second protocol type would consist of using predetermined transfer blocks and sizes and sequences. A third protocol type would consist of sending the DMA setup data via a serial communication link.

3.4 DATA TRANSFER DESCRIPTION

When the VMIVME-DMA transfers individual data works to or from an external device, it becomes the VMEbus master and transfers the data via DMA transfers to or from memory. It asserts the VMEbus address, control lines, address modifier, and sends or receives data. The data transfers are controlled by a 68430 DMA interface integrated circuit (IC). Handshake signals to/from the 68430 are converted to/from DMA compatible handshake signals. A functional block diagram of the DMA interface handshake signals is shown in Figure 3.4-1.

3.5 VME-TO-VME LINK

Two VMIVME-DMA boards may be connected back-to-back to create a DMA link between two VME chassis. In this configuration, the two boards are connected so that their data buses and control signals are cross coupled to allow them to transfer data back and forth under handshake control. The cross coupling is shown in Figure 3.4-1.

The DMA link supports 8-, 16-, and 32-bit data transfers in either burst or single cycle mode. Burst mode operation provides for maximum data transfer speeds; however, other bus masters are prohibited from bus access for the entire data transfer block. Single cycle mode relinquishes the bus after each data cycle, allowing other master devices use of the bus during data transfer blocks.

3.6 POWER CIRCUITS

The SBC 68430 DMA Controller integrated circuit utilizes a 1.5 V (VBB) power source which is derived from the VMEbus +5 V logic supply, as shown in Figure 3.6-1.

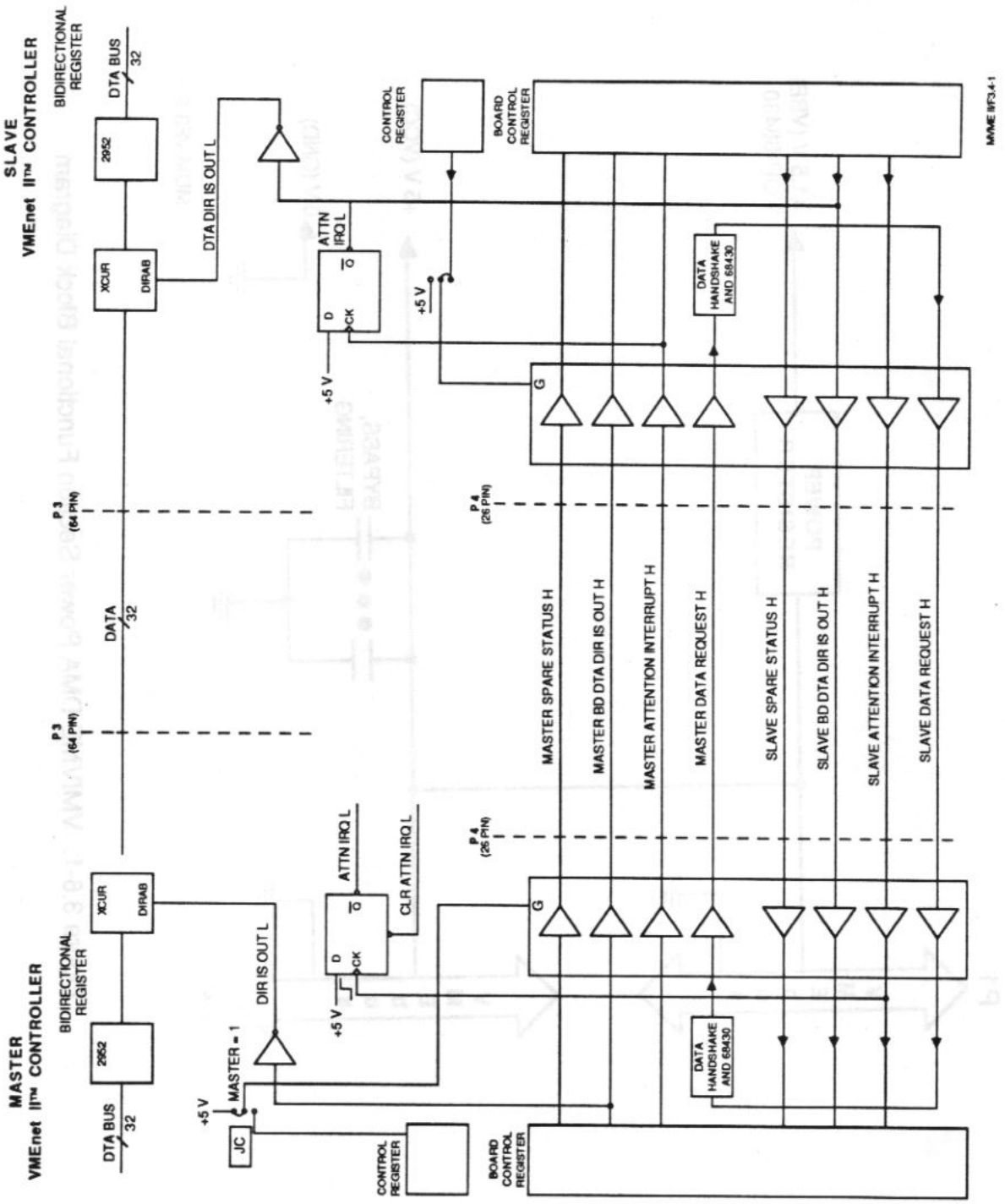


Figure 3.4-1. Functional Block Diagram of DMA Interface Signals

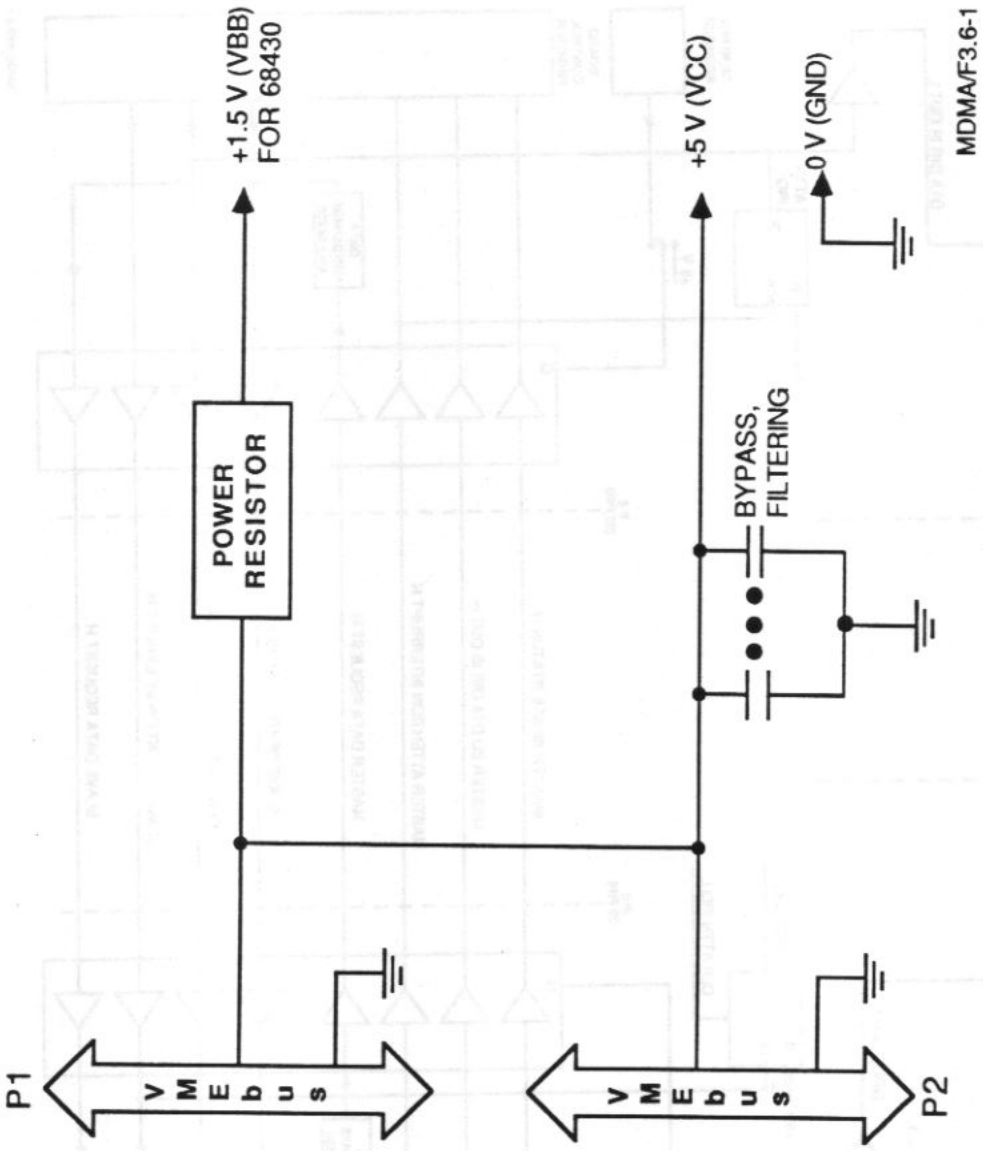


Figure 3.6-1. VMIVME-DMA Power Section Functional Block Diagram

3.7 VMEbus COMPATIBILITY LOGIC

Typical VMEbus compatible signals, buffers, and receivers are shown in Figures 3.7-1, 3.7-2, 3.7-3, and 3.7-4 for VMEbus controls, addresses, and data.

3.8 INTERRUPT LOGIC

The DMA interrupt logic consists of an interrupt vector used for a DMA complete signal that is resident inside the 68430 integrated circuit. Although the 68430 DMA controller supplies the interrupt vector, the 68153 bus interrupter interface provides the interrupt handshake logic. A functional block diagram of the 68430 control logic is shown in Figure 3.7-2.

3.9 SIGNAL FUNCTIONAL DESCRIPTIONS

This section describes the cable interface signals used by the VMIVME-DMA.

3.9.1 ED00-ED31 - Data Bus

These 32 lines make up the data bus. Data is transferred bidirectionally (half duplex) over these lines. The data is TTL compatible, terminated by 120 ohms.

3.9.2 I/O Cable Handshake Signals

When a VMIVME-DMA is selected as the A (i.e., Master) board, the *Master Signals* are driven and the *Slave Signals* are received. Whereas, when a board is selected as the B (i.e., Slave) board, then the transceivers are reversed and the *Slave Signals* are driven and the *Master Signals* are received.

3.9.2.1 Cable Handshake "Master Signals"

The following four signals are driven by the VMIVME-DMA selected as the A (Master) board:

Master Spare Status H. This signal is a user-defined output from the Master (A) board.

Master Transmit CMD. This signal indicates the transfer direction of the VMIVME-DMA. It may be read by the Board Control Register (BCR) of the other VMIVME-DMA or user device.

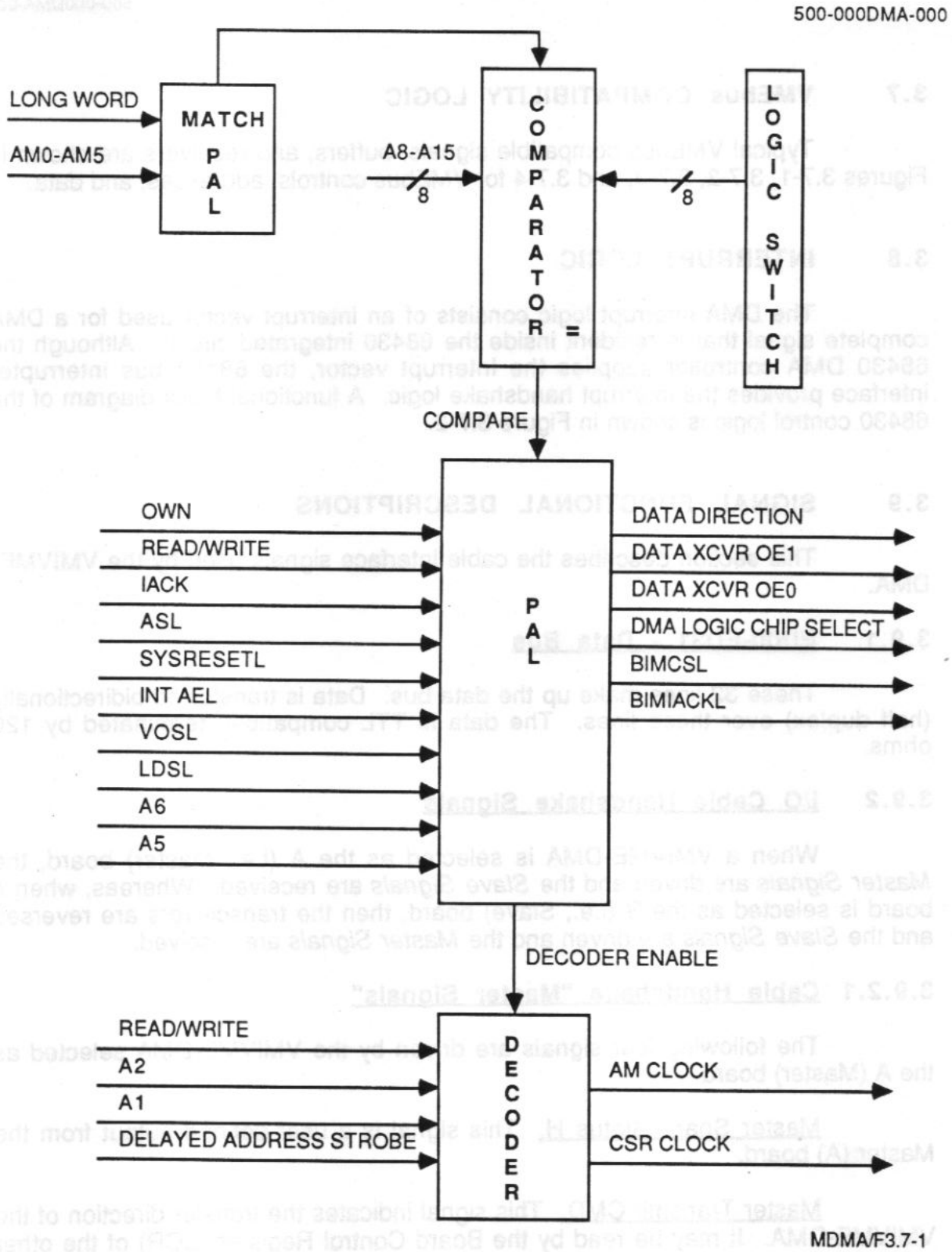


Figure 3.7-1. VMIVME-DMA Address Decode Section Detailed Block Diagram

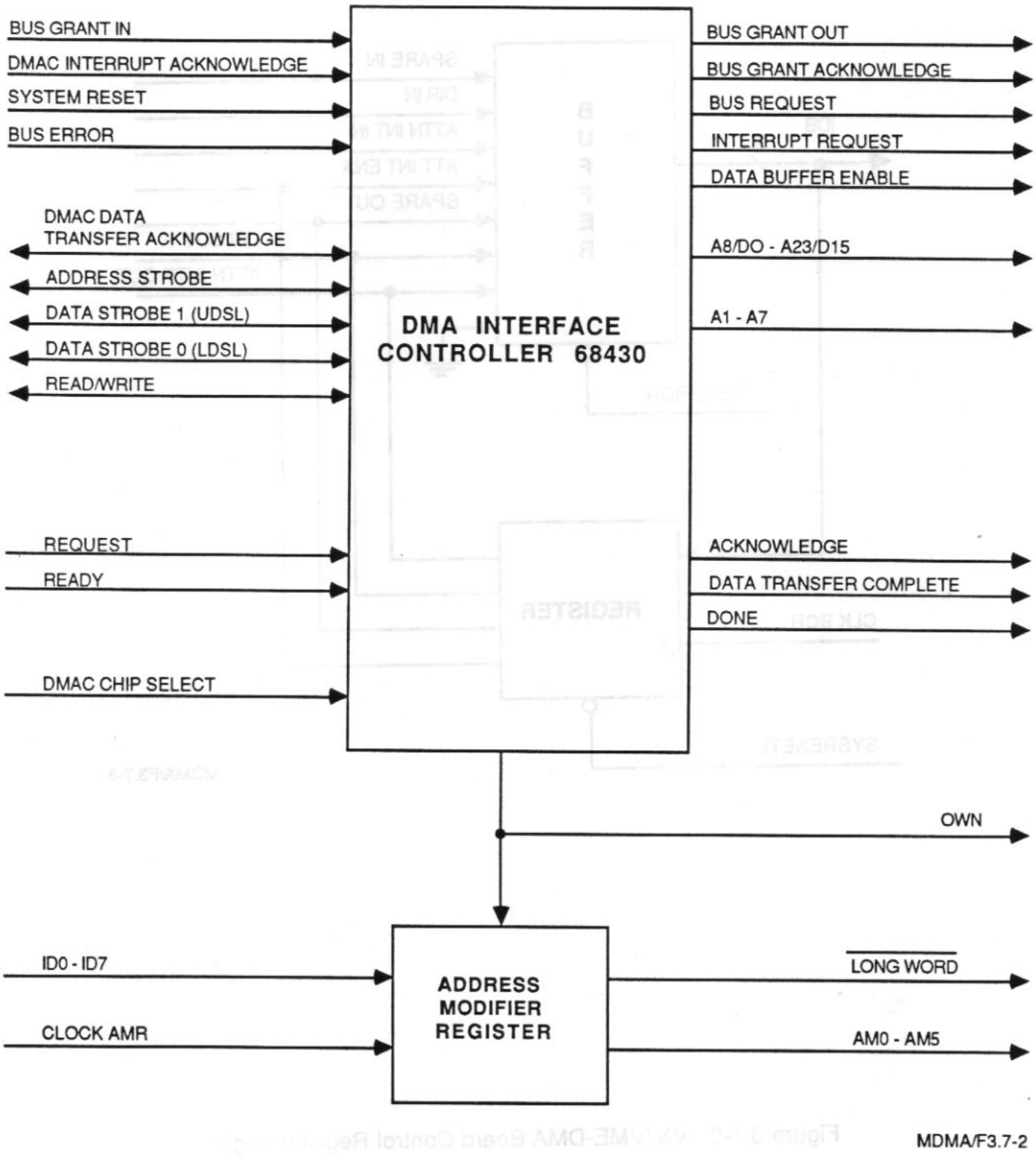


Figure 3.7-2. VMIVME-DMA Functional Block Diagram

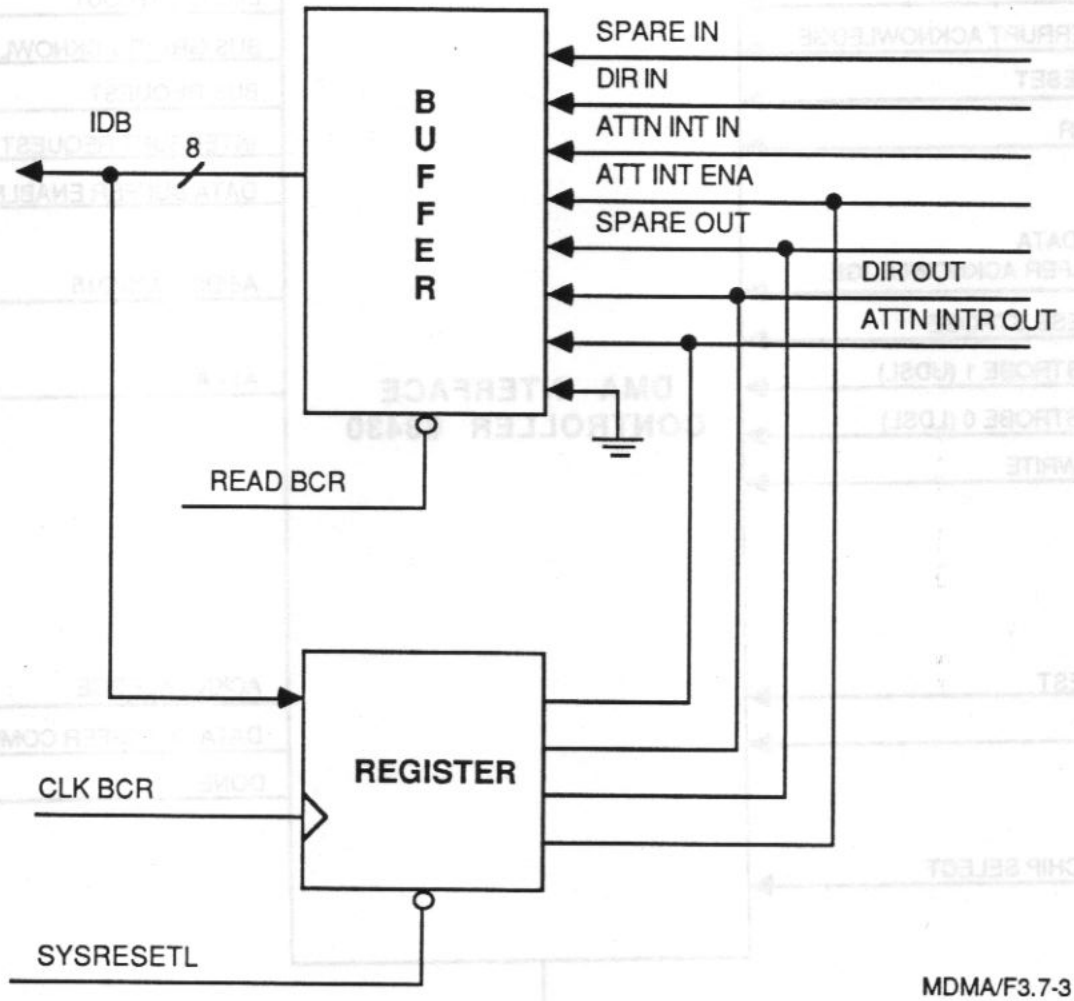


Figure 3.7-3. VMIVME-DMA Board Control Register Logic

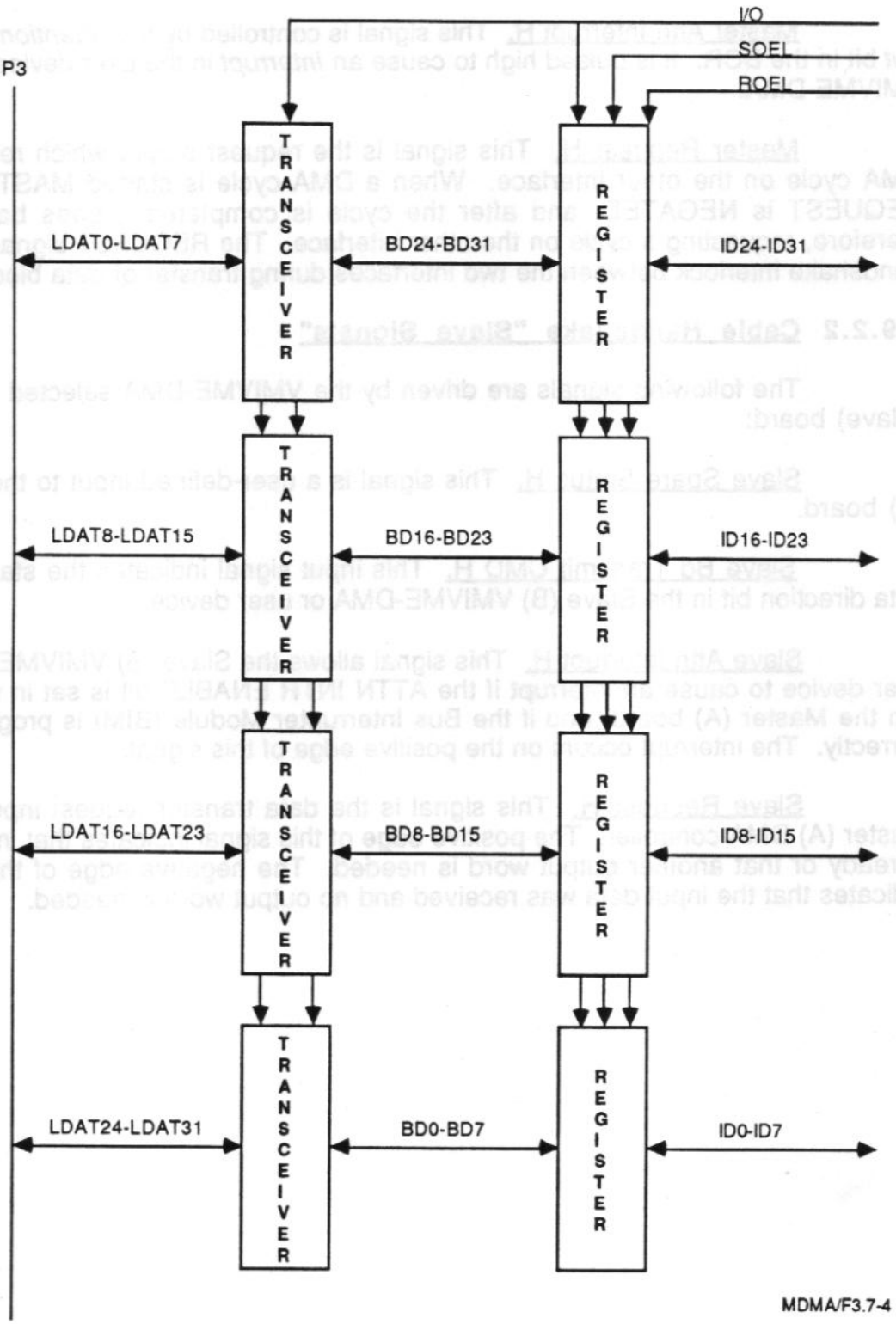


Figure 3.7-4. VMIVME-DMA Data Section Detailed Block Diagram

Master Attn Interrupt H. This signal is controlled by the *attention interrupt out* bit in the BCR. It is pulsed high to cause an *interrupt* in the user device or other VMIVME-DMA.

Master Request H. This signal is the request output which requests a DMA cycle on the other interface. When a DMA cycle is started MASTER DTA REQUEST is NEGATED, and after the cycle is completed it goes back high, therefore, requesting a cycle on the other interface. The REQUEST signals form a handshake interlock between the two interfaces during transfer of data blocks.

3.9.2.2 Cable Handshake "Slave Signals"

The following signals are driven by the VMIVME-DMA selected as the B (Slave) board:

Slave Spare Status H. This signal is a user-defined input to the Master (A) board.

Slave Bd Transmit CMD H. This input signal indicates the state of the data direction bit in the Slave (B) VMIVME-DMA or user device.

Slave Attn Interrupt H. This signal allows the Slave (B) VMIVME-DMA or user device to cause an interrupt if the ATTN INTR ENABLE bit is set in the BCR (on the Master (A) board) and if the Bus Interrupter Module (BIM) is programmed correctly. The interrupt occurs on the positive edge of this signal.

Slave Request H. This signal is the data transfer request input to the Master (A) DMA controller. The positive edge of this signal indicates that input data is ready or that another output word is needed. The negative edge of this signal indicates that the input data was received and no output word is needed.

SECTION 4

PROGRAMMING

4.1 PROGRAMMING OVERVIEW

The VMIVME-DMA has three types of devices that must be programmed for proper operation. These are the SCB68430 DMA Controller, the MC68153 Bus Interrupter Module (BIM), and the on-board registers. The on-board registers are used to provide the address modifiers, which allows the user control of the DMA controller and the Bus Interrupter Module, and to communicate with the external DMA devices or another DMA board connected back-to-back for VMEbus-to-VMEbus communications. Other programming aspects of the DMA include executing the transfer protocol (see Section 4.1.2), handling interrupts, and error processing. See Table 4.1-1 for names and addresses of registers utilized by the DMA. Technical specifications for the MC68153 are included in Appendix B.

4.1.2 Transfer Protocol

In order for DMA transfers to take place, the interfaces must be set up at both ends of the link. Therefore, if a CPU on one bus wants to transfer data, a second CPU on the second bus must set up the DMA interface on that second bus to the correct memory address, word count, and direction of transfer.

The manner in which CPUs in two separate buses determine the proper setup sequences is referred to as the transfer protocol. There are several types of protocols that may be used. One protocol type consists of the following:

a. CPU in one bus interrupts the second bus.
b. Both DMA interfaces are set up to transfer a control data block.
c. The control data block is then used to set up the DMA interface in the second bus. This protocol would simply have to insure in advance what the size and direction of transfer of the control block would be.

A second protocol type consists of using predetermined transfer blocks, sizes, and sequences. A third protocol type consists of sending the DMA setup data via a serial communication link.

4.2 REGISTER BIT DEFINITIONS

Register Bit definitions are shown in Tables 4.2-1, 4.2-2, and 4,2-3.

Table 4.1-1. VMIVME-DMA Register Address Map

ADDRESS	ACRONYM	REGISTER NAME	PHYSICAL LOCATION
00	CSR	Channel Status Register (CSR)	SCB68430 DMAI
01	CER	Channel Error Register (CER)	SCB68430 DMAI
04	DCR	Device Control Register (DCR)	SCB68430 DMAI
05	OCR	Operation Control Register (OCR)	SCB68430 DMAI
06	SCR*	Sequence Control Register (SCR)	SCB68430 DMAI
07	CCR	Channel Control Register (CCR)	SCB68430 DMAI
0A	MTCH	Memory Transfer Count High	SCB68430 DMAI
0B	MTCL	Memory Transfer Count Low	SCB68430 DMAI
0C	MACH**	Memory Address Count High	SCB68430 DMAI
0D	MACMH	Memory Transfer Count Mid-High	SCB68430 DMAI
0E	MACML	Memory Address Count Mid-Low	SCB68430 DMAI
0F	MACL	Memory Address Count Low	SCB68430 DMAI
25	IVR	Interrupt Vector Register	SCB68430 DMAI
27	IVR***	Interrupt Vector Register	SCB68430 DMAI
2D	CPR*	Channel Priority Register	SCB68430 DMAI
41	CRO**	Control Register 0	MC68153 BIM
43	CR1**	Control Register 1	MC68153 BIM
45	AICR (CR2)	Attention Interrupt Control Register	MC68153 BIM
47	DICR (CR3)	DMA Interrupt Control Register	MC68153 BIM
49	VRO**	Vector Register 0	MC68153 BIM
4B	VR1**	Vector Register 1	MC68153 BIM
4D	AIVR (VR2)	Attention Interrupt Vector Register	MC68153 BIM
4F	VR3**	Vector Register 3	MC68153 BIM
61	BCR	Board Control Register	
63	DSR	Device Status Register	(On Board)
65	AMR	Address Modifier Register	

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* Included for software compatibility.
** Register is not used.
*** The IVR has two addresses for software compatibility (see specification sheet).

Table 4.2-1. DMA Interface Register Bit Formats

CHANNEL STATUS REGISTER (ADDRESS: $XX00)

CSR

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
CHANNEL OPERATION COMPLETE	NOT USED	NORMAL DEVICE TERMINATE	ERROR	CHANNEL ACTIVE	NOT USED	NOT USED	READY INPUT STATE
0 = NO 1 = YES	(0)	0 = NO 1 = YES	0 = NO 1 = YES	0 = NO 1 = YES	(0)	(0)	0 = LOW 1 = HIGH

CHANNEL ERROR REGISTER ($XX01)

CER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NOT USED	NOT USED	NOT USED	ERROR CODE				
(0)	(0)	(0)	0000 = NO ERROR 01001 = BUS ERROR 10001 = SOFTWARE ABORT				

DEVICE CONTROL REGISTER ($XX04)

DCR

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11*	BIT 10	BIT 9	BIT 8
EXTERNAL REQUEST MODE	NOT USED	NOT USED	NOT USED	OCR (5:4) = 00 → 0	NOT USED	NOT USED	NOT USED
0 = BURST 1 = CYCLE STEAL	(0)	(1)	(1)	OCR (5:4) 01 10 11 } → 1	(0)	(0)	(0)

*Should be programmed as a logical "zero" if the operand size (see Operation Control Register bits 4 and 5) is BYTE, otherwise it should be programmed as a logic "one".

OPERATION CONTROL REGISTER ($XX05)

OCR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIRECTION	NOT USED	OPERAND SIZE		NOT USED	NOT USED	NOT USED	NOT USED
0 = MEM TO DEV 1 = DEV TO MEM	(0)	00 = BYTE 01 = WORD 10 = LONG WORD* 11 = 32-BIT WORD		(0)	(0)	(1)	(0)

*Do not select Longword transfers for this board.

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Table 4.2-1. DMA Interface Register Bit Formats (Continued)

SEQUENCE CONTROL REGISTER ($XX06)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
SCR**	NOT USED**							
	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy register.

CHANNEL CONTROL REGISTER ($XX07)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CCR	START	NOT USED	NOT USED	SOFTWARE ABORT	INTERRUPT ENABLE	NOT USED	NOT USED	NOT USED
	0 = NO 1 = YES	(0)	(0)	0 = NO 1 = YES	0 = NO 1 = YES	(0)	(0)	(0)

MEMORY TRANSFER COUNT HIGH ($XX0A)

	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MTCH	MEMORY TRANSFER COUNT MSB							
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY TRANSFER COUNT LOW ($XX0B)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MTCL	MEMORY TRANSFER COUNT LSB							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-1/2

Table 4.2-1. DMA Interface Register Bit Formats (Continued)

MEMORY ADDRESS COUNTER HIGH ($XX0C)

MACH

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
NOT USED**							
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy register.

MEMORY ADDRESS COUNTER MID-HIGH ($XX0D)

MACMH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEMORY ADDRESS COUNTER							
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

MEMORY ADDRESS COUNTER MID-LOW ($XX0E)

MACML

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MEMORY ADDRESS COUNTER							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY ADDRESS COUNTER LOW ($XX0F)

MACL

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEMORY ADDRESS COUNTER							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-1/3

Table 4.2-1. DMA Interface Register Bit Formats (Concluded)

DMA INTERRUPT VECTOR REGISTER ($XX25. $XX27)

DIVR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONE INTERRUPT VECTOR							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	NOTE 1

NOTE 1: This bit is automatically set if an error occurred. This register is mapped to two locations to provide compatibility with other controllers.

CHANNEL PRIORITY REGISTER ($XX2D)

CPR

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NOT USED**							
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy registers.

MSIU/T4.2-1/4

Table 4.2-1. DMA Interface Register Bit Formats (Continued)

MEMORY ADDRESS COUNTER HIGH ($XX0C)

MACH

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
NOT USED**							
(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

**Dummy register.

MEMORY ADDRESS COUNTER MID-HIGH ($XX0D)

MACMH

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEMORY ADDRESS COUNTER							
BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

MEMORY ADDRESS COUNTER MID-LOW ($XX0E)

MACML

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MEMORY ADDRESS COUNTER							
BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

MEMORY ADDRESS COUNTER LOW ($XX0F)

MACL

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEMORY ADDRESS COUNTER							
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-1/3

Table 4.2-2. Interrupt Module (68153) Register Bit Definitions

ATTENTION INTERRUPT CONTROL REGISTER ($XX45)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0 = INT 1 = EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

DMA INTERRUPT CONTROL REGISTER ($XX47)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DICR	FLAG BIT	FLAG BIT AUTO CLEAR	VECTOR 0 = INT 1 = EXT	INTER-RUPT ENABLE	INTER-RUPT AUTO CLEAR	IRQ LEVEL 2	IRQ LEVEL 1	IRQ LEVEL 0

ATTENTION INTERRUPT VECTOR REGISTER ($XX4D)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AIVR	ATTENTION INTERRUPT VECTOR							
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

MSIU/T4.2-2

Table 4.2-3. Registers Located External to DMAI and BIM ICs (On Board)

BOARD CONTROL REGISTER ($XX61)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
BCR	SPARE IN	DIR IN	ATTN INTR IN	ATTN INTR ENABLE	SPARE OUT	DIR OUT 0 = Rx 1 = Tx	ATTN INTR OUT	GO
READ/ WRITE	R	R	R	R/W	R/W	R/W	R/W	W

DEVICE STATUS REGISTER ($XX63)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DSR	FAIL LED 1 = OFF 0 = ON	NOT USED	ENABLE WATCH DOG TIMER 1 = ENA	LINK MASTER HIGH "1"	NOT USED	NOT USED	NOT USED	NOT USED
READ/ WRITE	R/W	R/W	R/W	R/W	R	R	R	R

ADDRESS MODIFIER REGISTER ($XX65)

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
AMR	NOT USED	$\overline{\text{LONGWORD}}$	ADDRESS MODIFIER					
			AM5	AM4	AM3	AM2	AM1	AM0

MSIU/T4.2-3

4.3 SEQUENCE OF REGISTER LOADING

The DMA interface at the receiving end must be set up first to avoid missing the first cycle request, furthermore, the overall setup sequence of the VMIVME-DMA should be as follows:

a. Load the registers in the 68153 and 68430.
b. The CCR should be the last register loaded in the 68430.
c. Load the address modifier register (on-board).
d. Load the board control register (on-board) with the GO bit (bit 0) set to 0.
e. Reload the board control register with the GO bit set.

Note that the start bit (CCR bit 7) must be set inside the 68430 before the GO bit is set in the BCR. The start bit in the 68430 is independent of the GO bit in the BCR.

An example of a register re-initialization sequence for transmitting data (from memory) is shown in Table 4.3-1. After the first DMA transfer is done, the VMIVME-DMA can be re-initialized with only eight steps to transmit a second block of data (see Table 4.3-2).

An example of a register initialization sequence for receiving data (transfer to memory) is shown in Table 4.3-3. After the first DMA transfer is done the VMIVME-DMA can be initialized with only eight steps to receive a second block of data (see Table 4.3-4).

4.4 PROGRAMMING THE SCB68430 DMAI

The following paragraphs describe the functions of the internal registers to the DMAI chip.

4.4.1 Channel Status Register/Channel Error Register

These two registers are used together to determine status and error conditions related to the DMA controller.

4.4.1.1 Channel Status Register (CSR)

BIT 15 - CHANNEL OPERATION COMPLETE. This bit will be set when the DMA operation is complete. If interrupts are enabled, an interrupt will be generated at this time.

BITS 14, 13 - NOT USED.

Table 4.3-1. Register Initialization Sequence for Transmitting a 4K Word Block Starting Data Address $40000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	DCR	04	B8	CYCLE STEAL
2	68430	OCR	05	12	WORD FROM MEMORY
3	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
4	68430	MACMH	0D	04	UPPER 8-BITS OF MEMORY ADDRESS
5	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
6	68430	DIVR	25	42	DONE INTERRUPT VECTOR
7	68153	AIVR	4D	40	ATTENTION INTERRUPT VECTOR
8	68153	AICR	45	1F	ENABLE INTERNAL VECTOR WITH AUTO CLEAR
9	68153	DICR	47	3F	ENABLE EXTERNAL VECTOR WITH AUTO CLEAR
10	ON-BOARD	AMR	65	39	LONGWORD, ADDR MOD=39
11	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
12	68430	CCR	07	88	START DMA CHIP
13	ON-BOARD	DSR	63	80	FAIL LED OFF
14	ON-BOARD	BCR	61	15	GO, ENABLE ATTN, TRANSMIT OUT

MSIU/T4.3-1

Table 4.3-2. Register Initialization Sequence for Transmitting a Second 4K Word Block Starting Data Address $20000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
2	68430	MACMH	0D	02	UPPER 8-BITS OF MEMORY ADDRESS
3	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
4	68153	DICR	47	3F	ENABLE INTERRUPTS WITH AUTO CLEAR
5	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
6	68430	CCR	07	88	START DMA CHIP
7	ON-BOARD	DSR	63	80	FAIL LED OFF
8	ON-BOARD	BCR	61	15	GO, ENABLE ATTN, TRANSMIT OUT

MSIU/T4.3-2

Table 4.3-3. Register Initialization Sequence for Receiving a 4K Word Block
Starting Data Address $40000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	DCR	04	B8	CYCLE STEAL
2	68430	OCR	05	92	WORD TO MEMORY
3	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
4	68430	MACMH	0D	04	UPPER 8-BITS OF MEMORY ADDRESS
5	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
6	68430	DIVR	25	42	DONE INTERRUPT VECTOR
7	68153	AIVR	4D	40	ATTENTION INTERRUPT VECTOR
8	68153	AICR	45	17	ENABLE INTERNAL VECTOR WITH AUTO CLEAR
9	68153	DICR	47	3F	ENABLE EXTERNAL VECTOR WITH AUTO CLEAR
10	ON-BOARD	AMR	65	39	LONGWORD, ADDR MODE = 39
11	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
12	68430	CCR	07	88	START DMA CHIP
13	ON-BOARD	BCR	61	10	GO = 0, ENABLE ATTN, RECEIVE
14	ON-BOARD	DSR	63	80	FAIL LED OFF
15	ON-BOARD	BCR	61	11	GO, ENABLE ATTN, RECEIVE

MSIU/T4.3-3

Table 4.3-4. Register Initialization Sequence for Receiving a Second 4K Word Block
Starting Data Address $20000

STEP	REGISTER LOCATION	REGISTER NAME	REGISTER ADDRESS OFFSET	DATA LOADED (HEXADECIMAL)	COMMENT
1	68430	MTCH	0A	1000	16-BIT TRANSFER COUNT
2	68430	MACMH	0D	02	UPPER 8-BITS OF MEMORY ADDRESS
3	68430	MACML	0E	0000	LOWER 16-BITS OF MEMORY ADDRESS
4	68153	DICR	47	3F	ENABLE INTERRUPTS WITH AUTO CLEAR
5	68430	CSR	00	B9	CLEAR CHANNEL STATUS REGISTER
6	68430	CCR	07	88	START DMA CHIP
7	ON-BOARD	DSR	63	80	FAIL LED OFF
8	ON-BOARD	BCR	61	15	GO, ENABLE ATTN, RECEIVE

MSIU/T4.3-4

BIT 12 - ERROR.* This bit will be set if the DMA operation was terminated due to an error condition.

BIT 11 - CHANNEL ACTIVE. This bit indicates that a DMA operation is in progress and is automatically cleared upon termination of the operation.

BITS 10, 9 - NOT USED.

BIT 8- READY INPUT. Indicates the state of the RDY input signal, i.e., a logic "zero" indicates 0 Volts and that data is ready.

4.4.1.2 Channel Error Register (CER)

BITS 7, 6, 5 - NOT USED.

BIT 4, 3, 2, 1, 0 ERROR CODE. These five bits indicate the error type when an error occurs. This register is cleared when the error bit (CSR-BIT 12) is cleared.

ERROR CODE	FUNCTION
00000	No Error
01001	Bus Error
10001	Software Abort

4.4.2 Device Control Register/Operation Control Register

These two registers control the data direction, data size, and request mode of the DMA transfers.

4.4.2.1 Device Control Register (DCR)

BIT 15 - EXTERNAL REQUEST MODE. This bit is set to perform single-cycle transfers and cleared to perform burst transfers.

*CSR-BIT 15 and CSR-BIT 12 must be cleared if set before another DMA operation can be started. These bits may be cleared by writing a "one" to each bit that is set. The following 68000 instruction will do this without testing each of the bits.

MOVE.B CSR, CSR

The other bits in the CSR are unaffected by a write.

BITS 14, 13, 12 - NOT USED.

BIT 11 - SIZE. This bit is read and written as the "LOGICAL OR" of bits 4 and 5 in the OCR, i.e., set it to "zero" if both bits 4 and 5 are zero (otherwise, set it to "one").

BITS 10, 9, 8 - NOT USED.

4.4.2.2 Operation Control Register (OCR)

BIT 7 - DIRECTION. This bit contains the DMA transfer direction.

0=Read from Memory
Write to External Device
1=Write to Memory
Read from External Device

BIT 6 - NOT USED.

BITS 5, 4 OPERAND SIZE. These bits control the operand size.

BIT 5	BIT 4	OPERAND SIZE
0	0	BYTE
0	1	WORD (16-bit)
1	0	LONGWORD* (32-bit, 16 bits at a time)
1	1	DOUBLEWORD (32-bit, 32 bits at a time)

*For maximum bus efficiency, select the doubleword size. Do not use LONGWORD with this board.

BITS 3, 2, 1, 0 - NOT USED.

4.4.3 Sequence Control Register (SCR)

The SCR is a dummy register provided for compatibility with other DMA controllers.

4.4.4 Channel Control Register (CCR)

BIT 7 - START. This bit causes the DMA controller to start its operation.

BITS 6, 5 - NOT USED.

BIT 4 - SOFTWARE ABORT. This bit allows current DMA operation to be aborted under software control.

BIT 3 - INTERRUPT ENABLE. This bit enables the DMA interrupt request when a DMA operation is completed.

BIT 2, 1, 0 - NOT USED.

4.4.5 Memory Transfer Count Register

These registers hold the number of desired transfers for the current operation. The transfer count can be set to FFFF (64k-1) if the VMIVME-DMA is in the slave mode. The Last Word Flag (LWF) signal is used to terminate the transfers in this case. However, setting the transfer counter to FFFF does cause an extra memory cycle to be requested beyond the actual word count (only if a *read* from memory). This should not be a problem unless it happens to be at the end of memory, in that case it will generate a bus error trap.

4.4.6 Memory Address Counter Registers

These four registers hold the memory address for the DMA operation. The MACH register is a dummy register and is provided for compatibility with other DMA controllers. The three real registers provide a 24 bit memory address for the DMA transfers. These registers should be loaded with the starting memory address before an operation is started. The registers are incremented during operation and may be read while an operation is in progress.

4.4.7 DMA Interrupt Vector Register (DIVR)

This register is used to store the interrupt vector used for the DMA complete interrupt. This register is resident inside the SCB68430. It is mapped to two locations to provide compatibility with other DMA controllers. Note: Bit 0 is automatically set when an error occurs and cannot be written. Thus, a DMA interrupt vector for normal conditions must be an even number, and the error vector is automatically the next higher odd vector. Note, that although the 68430 supplies the interrupt vector, the 68153 handles the interrupt handshake, therefore, the 68153 must be programmed to handle the external vector from the 68430.

4.4.8 Channel Priority Register (CPR)

This register is a dummy register provided for compatibility with other DMA controllers.

4.5 PROGRAMMING THE MC68153 BIM

Data sheets for the MC68153 are included in Appendix B. The MC68153 contains eight registers, but only three are used in the VMIVME-DMA. Two of these registers are control registers and one is a vector register.

4.5.1 Attention Interrupt Control Register (AICR) and DMA Interrupt Control Register (DICR)

BITS 7, 6 - FLAG CONTROL - NOT USED.

BIT 5 - VECTOR LOCATION. This bit should be cleared to cause the MC68153 to use its internal vector register for an interrupt acknowledge and set to use an external interrupt vector. For the VMIVME-DMA, this bit should be cleared in the a AICR and set in the DICR since an external vector is obtained from the 68430 DMA controller vector register (DIVR).

BIT 4 - INTERRUPT ENABLE. This bit should be set to enable the corresponding interrupt.

BIT 3 - INTERRUPT AUTO CLEAR. This bit automatically clears the interrupt enable bit and the interrupt request output whenever the interrupt is acknowledged. This bit ***MUST*** be set in both registers to provide VMEbus compatible timing. This requires that the interrupt enable bit be set after each interrupt.

BITS 2,1,0 - IRQ LEVEL BITS. Interrupt level (L2,L1,L0) - The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED*
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

*A value of zero in the field disables the interrupt.

4.5.2 Attention Interrupt Vector Register (AIVR)

This register holds the vector used for the attention interrupt. Any 8-bit integer may be used as determined by the system vector address configuration.

4.6 PROGRAMMING THE ON-BOARD REGISTERS

4.6.1 Board Control Register (BCR)

BIT 7 - SPARE IN (READ ONLY). This bit provides the state of the SPARE IN line. Its function is user defined.

BIT 6 - DIR IN (DIRECTION INPUT; READ ONLY). This bit simply indicates the state of the SPARE IN line. When communicating with another VMIVME-DMA, it should be the complement of DIR OUT.

DIR IN	OTHER VMIVME-DMA FUNCTION
0	Other Interface is a Receiver
1	Other Interface is a Transmitter

BIT 5 - ATT INTR IN (ATTENTION INTERRUPT INPUT; READ ONLY). This bit provides the state of the ATTN INTR IN line. It allows polling or user definition of the ATT INTR line.

BIT 4 - ATT INT ENA (ATTENTION INTERRUPT ENABLE; READ/WRITE). This bit, when set, enables the attention interrupt flip-flop. This bit must be set in addition to the AICR-BIT 4 to allow attention interrupts.

BIT 3 - SPARE OUT (WRITE/READ). This bit drives the SPARE OUT line. Its function is user defined.

BIT 2 - DIR OUT (DIRECTION OUTPUT; WRITE/READ). This bit indicates the transfer direction to the other interface via the DIR OUT line. It also controls the transfer direction of the data transceivers.

DIR OUT	FUNCTION
0	Receive Data From Other Interface
1	Transmit Data to Other Interface

BIT 1 - ATT INT OUT (ATTENTION INTERRUPT OUTPUT). This bit controls the ATT INT OUT line. It should be toggled high and then low to interrupt the other VMIVME-DMA.

BIT 0 - GO (WRITE ONLY). This bit "primes" the handshake logic to start a transfer block. If transmitting, it also initiates the first DMA cycle.

4.6.2 Device Status Register (DSR)

BIT 7 - Fail LED. This bit controls the Fail LED. Settling this bit to a "one" turns the Fail LED OFF.

BIT 6 - NOT USED.

BIT 5 - WATCHDOG TIMER ENABLE. This bit must be set to a "one" in conjunction with the removal of the WDT jumper to enable the watchdog timer (see Section 5.3.3). Writing a "zero" disables the watchdog timer.

BIT 4 - LINK MASTER HIGH. Setting this bit to a logic "one" sets the board as Link Master A. The board may also be jumpered as Link Master A as shown in Table 5.3.2-1. This bit set to a "zero" at power-up and at reset (Link Slave B). See Table 5.3.2-1.

BITS 3, 2, 1, 0 - NOT USED.

4.6.3 Address Modifier Register (AMR)

This register contains the address modifier and longword bits which are asserted when the VMIVME-DMA is bus master. This register is write only.

BIT 7 - NOT USED.

BIT 6 - $\overline{\text{LONGWORD}}$. This bit controls the assertion of the VMEbus LWORDL signal and selects either 16 or 32-bit transfers.

$\overline{\text{LONGWORD}}$	TRANSFER SIZE
0	32-Bit
1	8 or 16-Bit

BITS 5, 4, 3, 2, 1, 0 ADDRESS MODIFIER BITS. See "The VMEbus Specification" for VMEbus address modifier codes.

4.7 SAMPLE SOFTWARE LISTINGS

To assist the user in programming this board, a detailed sample assembly code listing for a 68000 VMEbus CPU is provided in Appendix C.

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