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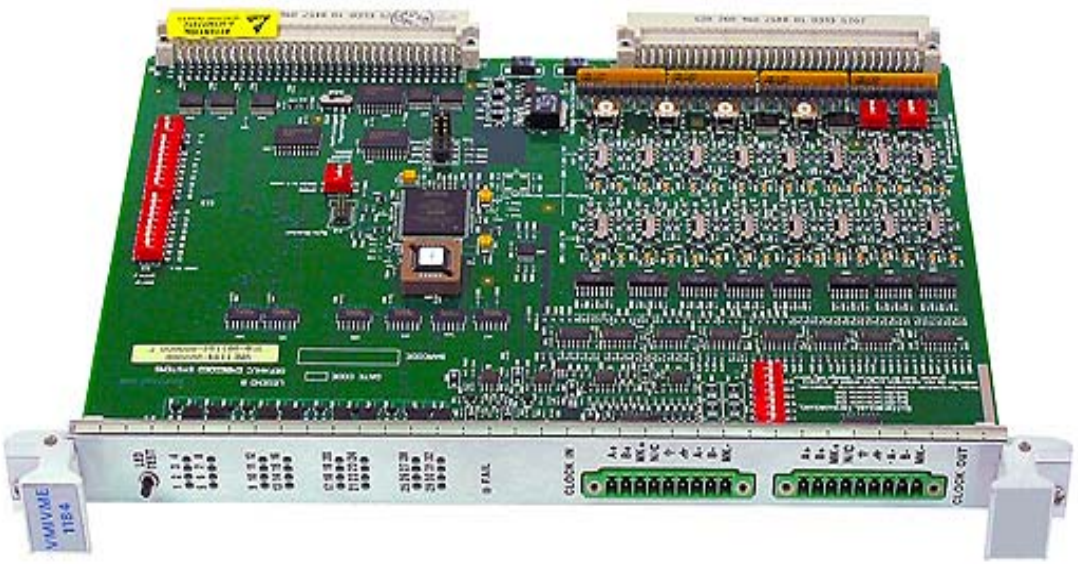
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Hardware Reference Manual

VMIVME-1184* 32-bit Optically Isolated Change-of-State (COS) Input Board with Sequence-of-Events (SOE)

Publication No. 500-001184-000 Rev. B.0



abaco SYSTEMS

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Document History

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Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a "D" subscript and binary numbers have a "b" subscript. The prefix "0x" shows a hexadecimal number, following the 'C' programming language convention. Thus:

$$\text{One dozen} = 12_D = 0x0C = 1100_b$$

The multipliers "k", "M" and "G" have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when "k", "M" and "G" mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.


NOTE
When describing transfer rates, "k", "M" and "G" mean $x10^3$, $x10^6$ and $x10^9$ *not* $x2^{10}$, $x2^{20}$ and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde ("~") denote active low signals; all other signals are active high. "N" and "P" denote the low and high components of a differential signal respectively.

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For a detailed explanation of the VMEbus and its characteristics, refer to "The VMEbus Specification" available from:

VITA
VMEbus International Trade Association
7825 East Gelding Dr., No. 104
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NOTE
Technical literature describing components used on the VME-1184 is available from the manufacturers' websites.

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Additional Notes

The VMIVME-1184* is a 32-channel P2 input board with Change-of-State (COS) and interrupt capabilities. The interrupt control logic can be programmed to issue an interrupt for specific state changes. The user selects the state changes to detect by programming the Control and Status Register (CSR1) and the COS Select register. This board stores up to 512 state changes when the COS logic is enabled. This prevents the board from losing a state change during interrupt servicing. For SOE operation, a maximum of 256 state changes are stored. The board also supports byte, word and longword data transfers during basic input data operations.

Features

The following is a list of some of the features of the VMIVME-1184:

- 32 channels of optically-isolated digital inputs with transient voltage suppression
- Eight inputs are grouped together and called an input port. Each port can be configured by the user to monitor one of the following output circuits:
- — Current sinking (Contact Closure)
- — Voltage sourcing (Voltage Sensing)
- User-configurable input voltage thresholds on a two channel basis
- Each channel has over-voltage and reverse voltage protection
- Reverse voltage is indicated by surface mounted SOT23 LEDs
- Incoming data is available for direct VMEbus read cycles

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- Data can be read using 8-, 16-, or 32-bit data transfers
- Each channel can be independently set by the user to perform the following functions:
  - Per channel COS event storage configuration
  - Ignore all changes (no events stored due to this channel changing)
  - Rising edge (causes 32 channel event storage into FIFO)
  - Falling edge (causes 32 channel event storage into FIFO)
  - Any edge (causes 32 channel event storage into FIFO)
- Each channel can be set to generate an interrupt for each event
- Sequence of Events logging with optional counter stamping
- Differential or Single-Ended inputs and outputs for Quadrature Counter (A, B and Marker/Index) with daisy-chaining capability
- This board complies with the VMEbus Specification Rev. C.1
- The board can be set to respond to short I/O (16-bit) accesses or to standard data I/O (24-bit) accesses
- AM2 setting for supervisor, non-privileged or both VMEbus accesses

Functional Description

The VMIVME-1184 is an optically isolated digital input board with 32 user-configurable channels. The inputs can be set up to monitor either voltage sensing or contact closure. Once the hardware has been configured and installed in the system, you can start monitoring the circuits. The data ports are always available for VMEbus data transfers. Simply read the address of the specific port, and record the state of the external circuits. This data is available in byte, word or longword accesses.

The board can be programmed to interrupt the system based on a change in the inputs. Change-of-State (COS) circuitry monitors the logical state of the inputs. When an input channel changes its state (for example, from a logic one to a logic zero), and the COS logic is set to trigger on that event, an interrupt can be issued to the host CPU. The COS logic is programmed via the Control and Status Register to store an event for certain conditions, such as the falling edge described above, and is channel specific.

The board is also capable of recording Sequence of Events (SOE). In this mode, when a specified change of state occurs on any of the channels, the previous state of all 32 channels is stored in the FIFO, followed by the current state. Additionally, a counter value incremented/decremented from the front panel counter input is stored in a separate FIFO to give the SOE an optional time stamp. The counter feature is also available in COS mode.

The VMIVME-1184 stores state changes in an on-board FIFO. The board can be configured to clear an interrupt request when the FIFO is empty (ROFE), or when an interrupt has been acknowledged (ROAK). If a COS occurs while a previous COS is waiting for service, or during the interrupt service routine, the event will be saved.



NOTE

COS mode only stores the events which have been triggered by certain changes on certain channels (user configured).

SOE mode additionally stores the latched state of the 32 channels just prior to each event which triggers a data storage into the FIFO (only one time stamp per pair).

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

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Table of Contents

1 • Theory of Operation 12
1.1 Introduction. 12
1.2 VMEbus Interface. 13
1.2.1 Data Transfer Cycles 14
1.2.2 Interrupt Acknowledge Cycles 14
1.3 Register Decoder. 15
1.4 Debounce. 15
1.5 Change-of-State Logic. 16
1.5.1 Previous State Data Algorithm 16
1.5.2 “Simultaneous” Data Changes, and the Debounce “Stretching” Effect 16
1.6 Inputs. 18
1.6.1 Voltage Sensing 18
1.6.2 Contact Closure 19
2 • Configuration and Installation 21
2.1 Introduction. 21
2.2 Unpacking Procedures. 21
2.3 Physical Installation. 21
2.3.1 Before Applying Power: Checklist 21
2.4 Operational Configuration. 22
2.4.1 Factory Installed Switches/Jumpers 22
2.4.2 Board Address and Address Modifier Selection 22
2.4.3 Debounce Timing 24
2.5 Input Configurations. 24
2.6 Connector Description. 25
2.6.1 Barrier Terminal Transition Panels 25
3 • Programming 29
3.1 Introduction. 29
3.1.1 Board ID (BD ID) Register 30
3.2 Control and Status Registers. 30
3.2.1 CSR1 Bit Definitions 30
3.2.2 CSR2 Bit Definitions 31
3.2.3 Counter Connectivity 32
3.2.4 Quadrature Counter Decoder Bits (Bits 16, 17 and 18) 32
3.2.5 Encoder Markers 33
3.3 Data FIFO Register. 34
3.4 Interrupt Processor Control Register. 34
3.4.1 Interrupt Levels 35
3.5 Interrupt Processor COS Vector Register (Offset: $XXXX0D). 35
3.6 Interrupt Processor Marker Vector Register (Offset: $XXXX0E). 35
3.7 Counter FIFO Register (Offset: $XXXX10). 35
3.7.1 Counter Register (Offset: $XXXX14) 36
3.7.2 COS SEL B/A 36
3.7.3 COS Select Register 0 37
3.7.4 COS Select Register 1 37
3.7.5 COS Select Register 2 37
3.7.6 COS Select Register 3 37

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3.7.7 FIFO Count Register (FIFO_CNT) 37
3.7.8 Counter FIFO Count Register (CTR_FIFO_CNT) 38
3.8 Channel Interrupt Enable Register (CH_INT_ENA). 38
3.9 Firmware Revision Register (FREV). 38
3.10 Counter Feature. 39
3.11 Counter Operation. 39
3.11.1 CSR1_[5, 4] Definitions 39
3.11.2 2X Quadrature Mode 40
3.11.3 4X Quadrature Mode 41
3.12 Initialization. 41
3.13 VMIVME-1184 Inputs. 42
3.14 Marker Gating. 43

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List of Figures

Figure 1-1 VMIVME-1184 Block Diagram 13
Figure 1-2 AM2 Line (Switch S29) 14
Figure 1-3 Channels 1-30 Input Circuitry 19
Figure 1-4 Channel 31 Input Circuitry (Channel 32 uses Vext #2) 20
Figure 2-1 Switch and Jumper Locations 23
Figure 2-2 P1/P2 Connector Pin Layout 26
Figure 3-1 COS and SOE Registers 36
Figure 3-2 Leading Edge Example 40
Figure 3-3 1x Counter Mode 40
Figure 3-4 2x Counter Mode 40
Figure 3-5 2X Quadrature 40
Figure 3-6 4X Quadrature 41
Figure 3-7 Marker Gating Diagram 43

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List of Tables

Table 1-1 COS Logic 16
Table 1-2 Walking Ones Test 16
Table 1-3 Contact Closure SIP Resistors and Switch Assignments 19
Table 2-1 Voltage Thresholds 24
Table 2-2 Jumper E3 (Extended Debounce Timing) 24
Table 2-3 P1 Pin Assignments 26
Table 2-4 P2 Pin Assignments 27
Table 3-1 VMIVME-1184 Address Map 29
Table 3-2 Board ID Register Bit Map 30
Table 3-3 Control and Status Register 1 Bit Map 30
Table 3-4 Correlating Debounce Times 31
Table 3-5 Control and Status Register 2 Bit Map 31
Table 3-6 Data FIFO Register Bit Map 34
Table 3-7 Interrupt Processor Control Register Bit Map 34
Table 3-8 Interrupt Level Bits 35
Table 3-9 COS SEL B/A 36
Table 3-10 COS Select Register 0 Bit Map 37
Table 3-11 COS Select Register 1 Bit Map 37
Table 3-12 COS Select Register 2 Bit Map 37
Table 3-13 COS Select Register 3 Bit Map 37
Table 3-14 FIFO Count Register Bit Map 38
Table 3-15 Counter FIFO Count Register Bit Map 38
Table 3-16 Channel Interrupt Enable Register Bit Map 38
Table 3-17 Differential Termination (S28) 39
Table 3-18 Example Setup of the VMIVME-1184 42
Table 3-19 Input Connectivity 42

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1 • Theory of Operation

1.1 Introduction

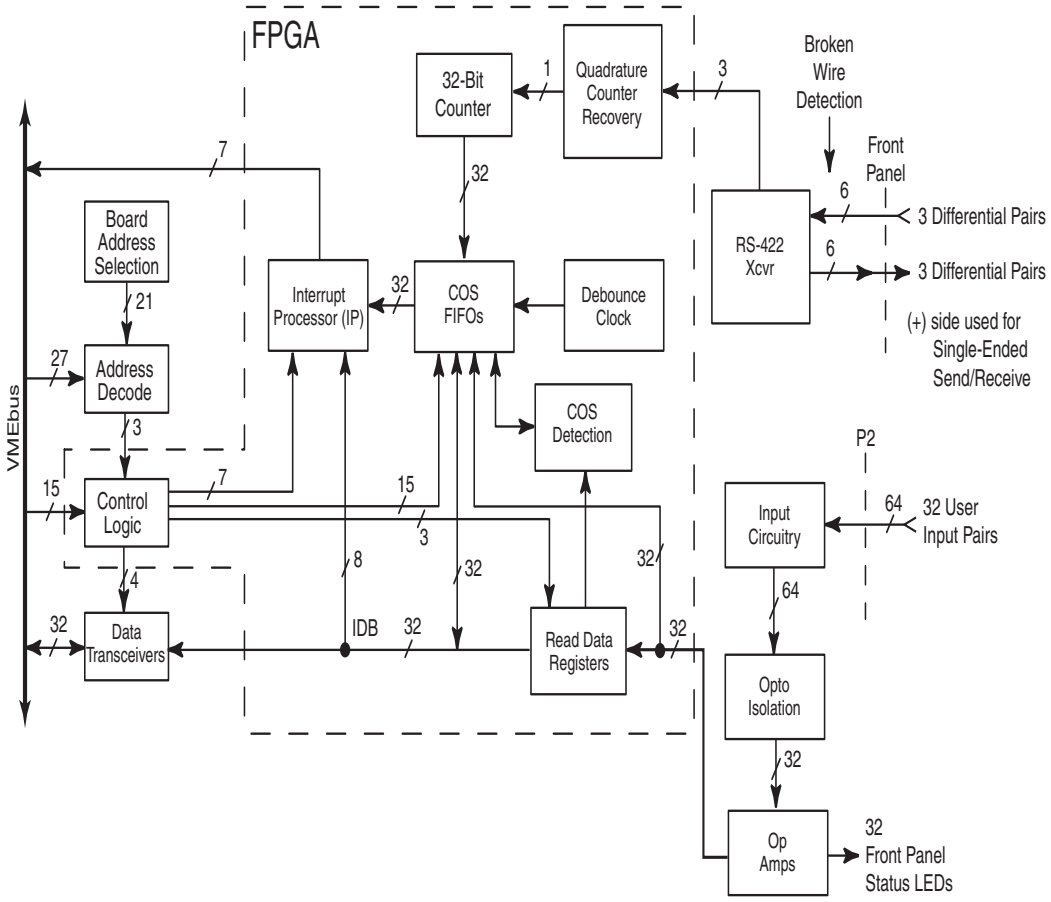
The board functions are broken down into six major blocks. These blocks are:

- Bus interface
- Register decoder
- Interrupt Processor (IP)
- Change-of-State (COS) logic
- Input circuits
- Counter

The bus interface contains the VMEbus interface logic, the board's address decoding logic and the data steering logic. The register decoder selects which data register (BD ID, CSR, IP or input) is used during a data transfer. The IP interface contains the logic to control the IP, interfaces with the VMEbus and issues the interrupt request. The COS logic controls the FIFO's data flow, determines if a change-of-state has occurred and whether it is deemed an event and stored. The input circuits contain the hardware to configure the topology (the shape or type of circuit), and their trigger thresholds.

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Figure 1-1 VMIVME-1184 Block Diagram



During Data-Only operations, the board monitors the external circuitry. When the board's address decoder determines the board is being accessed, it clocks the inputs into the data registers, effectively taking a snapshot of the external world. The data is steered to the correct VMEbus data lines, DTACK* is asserted, and the board re-arms its address decoder for another cycle. These types of transfers are always available to the user and do not effect the COS or SOE logic.

During Interrupt Cycles, the Interrupt Processor (IP) handles the board's functionality. When the COS logic issues an interrupt request to the IP, it also stores the incoming data in the associated FIFOs. The IP issues an interrupt request to the host CPU and waits for the proper Interrupt Acknowledge cycle. When the IP responds to the Acknowledge cycle, it places the user-programmed vector for the Interrupt Service Routine (ISR) on the VMEbus.

1.2 VMEbus Interface

The bus interface logic consists of bus signal buffers and transceivers that meet the VMEbus specification loading requirements. The address decoder (or board-select logic) can respond to standard (24-bit) or short (16-bit) data I/O accesses. The steering logic selects which VMEbus data lines to connect to the board's Internal Data Bus (IDB) and which direction the data will flow. The Board Identification (BD ID) register, the Control and Status Register (CSR) and the COS Select registers are considered part of the bus interface logic.

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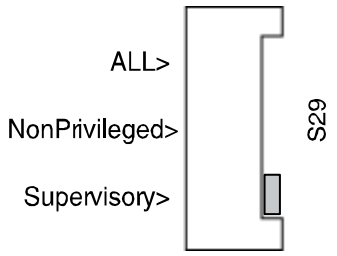
1.2.1 Data Transfer Cycles

The Address switch (S12-1) establishes the upper address line decoding. If the switch is On, the board will respond to standard accesses. If the switch is Off, the board will respond to short accesses. The default configuration is standard accesses.

The address decoder compares the 18 address lines (A06 through A23) and the six address modifier lines (AM0 through AM5) with preset conditions. The address lines, the STD(A24)/SHT(A16) CSR line and the AM2 line have switches that are used to establish the base address of the board. When a switch is On, the corresponding address line is compared to a logic zero (0). When the bus address and the address modifier matches the preset address, the board will respond to the bus cycle.

The AM2 line can be set to respond to a specific state (logic high or low) or to either logic state. With the switch in the ALL position, the board will respond to either Supervisory or Nonprivileged accesses. When set to the middle position, the board will respond to Nonprivileged data accesses only. When set to Supervisory, the board will respond to Supervisory accesses only. Refer to ***Figure 1-2***.

Figure 1-2 AM2 Line (Switch S29)



When the decoder determines that the board is being accessed, the VMEbus state is stored in a register and the BD_SEL lines are activated. The board-select line clocks the input registers and records the state of the external circuits. The register decoder uses the bus state information to put the proper data on the IDB, and to energize the VMEbus interface data transceivers. The bus interface then issues DTACK* and watches the Data Strobes (DS0* and DS1*). When both Data Strobes are asserted high the decoder resets itself and waits for the next matching address. The cycle then restarts.

1.2.2 Interrupt Acknowledge Cycles

During Interrupt Acknowledge (IACK*) cycles, only the three lowest address lines are valid. They carry the interrupt level being acknowledged by the host CPU, bypassing the address decoder and activating the IP. If the IP has an interrupt pending, it places its vector on the bus and issues a DTACK*. If not, the IP passes the IACKIN* signal to the IACKOUT* line.

If the interrupting FIFO is not empty after the interrupt service routine is read, and ROFE is selected, the IP will not release the interrupt until the FIFO is empty. When more than one longword of data is in the FIFO, multiple events may have occurred before or after the event that generated the interrupt. If the FIFO gets full, the state changes are occurring too fast for the system to handle. If COS

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interrupts are enabled, a full FIFO will generate an interrupt with the same level and vector as COS.



NOTE

If COS events come faster than the CPU can service, interrupt starvation will occur, keeping regular programs from executing. Please keep this in mind when configuring your system. Be especially mindful of completely emptying the FIFO(s) and limiting the capture of events to those which are actually necessary for operation. You could easily setup a condition in which too many events are being stored before an interrupt-generating event occurs..

1.3 Register Decoder

The register decoder uses the five lowest address lines and data strobes to select which register is placed on the IDB. The decoder is used during any board access. It uses a simple demultiplexer scheme. The address lines are decoded when the board select lines are asserted. Based upon the address lines and the data strobes, the proper register or registers are activated or clocked. A memory map showing the relative addresses for each register is listed in *Chapter 3, Programming* of this manual.

1.4 Debounce

The debounce clock is derived from the 16 MHz VMEbus system clock and is not intended as a synchronizing clock. The debounce clock is started when a COS condition is detected. This approach yields a lower latency with glitch-reduction capability.

Debounce is used on inputs to reduce 'glitches', false data transitions or noise. Typically, a state machine is used to transition with a clock of a particular rate or frequency. If the data's new state changes back, before two clock cycles, then that transition is thrown away (the data is considered not to have changed) and the input channel is resampled for any new changes.

All 32 data input channels are debounced (the debounce time is user-configurable from 1µs to 10ms). None of the counter inputs are debounced in order to more accurately track high-speed precision encoders, and to better handle an encoder stopping on a transition when machine vibration causes small but high speed movement back and forth across the same transition. The counter should never accumulate, or lose counts when the encoder is simply vibrating.



NOTE

Although the counter inputs are not debounced, they do have a maximum input change rate of 100nsec. If changes occur faster than 100nsec, then missed changes or counting errors may occur.

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1.5 Change-of-State Logic

The COS logic bases its actions on the state of its select lines A and B. These lines are controlled by the COS register values. The states are listed in ***Table 1-1*** below:

Table 1-1 COS Logic

SEL B	SEL A	COS Logic's Action
0	0	COS, event not flagged
0	1	COS event flagged on rising edges only
1	0	COS event flagged on falling edges only
1	1	COS event flagged on any edge

The COS logic writes data into a FIFO based on the board's configuration. The COS logic decides when to load data into the FIFO. If either select lines A or B are set to '1' and the corresponding event occurs on that channel, 32 channels of data will be stored in the data FIFO. When select lines A or B are set to '00', data changes for that channel will not flag a COS event and no data is stored in the FIFO. If interrupts are programmed and being serviced when a new event occurs, the logic continues to load the new state into the FIFO. The FIFO stores the new states until they are read by the host or the buffer becomes full.

1.5.1 Previous State Data Algorithm

The definition of previous state data is essential to a system that detects changes of state. Since all incoming data is compared to the previous state, what this previous state is and when it is stored is critical to the proper operation of the COS state machine.

A flagged Change-Of-State (COS) event occurs when one or more input channel's state changes in a way that the VMIVME-1184 has been programmed to detect. For example, if Channel 3 changes from a one (1) to a zero (0), and the COS Select Register has been programmed to detect falling edges for Channel 3, then Channel 3 causes a "flagged" COS event. A non-flagged COS event would occur if the logic level on Channel 3 changed from a zero (0) to a one (1), with falling edge detection enabled. Flagged COS data is the value of all of the input channels when one or more "flagged" changes of state have occurred. Non-flagged COS data is data for one or more channels that may have changed state, but are not flagged for saving.

1.5.2 "Simultaneous" Data Changes, and the Debounce "Stretching" Effect

A walking ones test is commonly used during design validation and product testing. In this test, all input channels are set to zero (0), and a one (1) is written to each successive channel in the following manner:

Table 1-2 Walking Ones Test

State 0	00000000
State 1	00000001
State 2	00000010
State 3	00000100

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During this test, two channels are actually changing value after State 1. In State 2, channel 0 has changed from a 1 to a 0, and channel 1 has changed from a 0 to a 1. Theoretically, these changes are simultaneous, and are viewed as a single COS event. The following, factors can be introduced to make the arrival of signals on different channels non-simultaneous:

- Comparators and Opto Couplers have different times on rising vs. falling edges.
- Traces, both inside and outside of FPGAs, can have slightly different lengths.
- Cables between sensors and I/O boards may not have precisely matched lengths.

If any of the above conditions occur, then data transmitted simultaneously on two or more channels may not arrive simultaneously at the COS detection circuitry.

The need for the COS inputs to be synchronized to a common clock also aggravates this situation. If two incoming signals arrive as little as 2 nanoseconds apart, the first signal may arrive prior to the synchronizing rising clock edge, and the second signal may arrive after the rising clock edge. If this occurs, the skew between the two signals is stretched to the period of the 16 MHz synchronizing clock. The debounce circuitry is another factor that can skew simultaneous events. Consider a situation where two incoming signals are skewed by one or more synchronizing clock cycles, the synchronized incoming signals can encounter another early-late condition (as was in the synchronizing clock) with the debounce circuitry. With the COS detection and FIFO circuitry running at the VMEbus clock rate, the first arriving signal will have been stored by the COS circuit, in the COS FIFO before the second arriving signal has passed the debounce circuitry. If the second signal is also flagged, the two COS events would be stored in the COS FIFO instead of one. This “double-hit” COS event can show what appears to be an invalid state condition.

Consider the following example:

1. Set Channel 5 for rising edge events and channel 4 to falling edge
2. Set the CSR to see SOE mode, the expected FIFO output is:

	Channel 5	**Channel 4**
Previous State 1	0	1
	01 to 10 change occurs here	
COS State 1	1	0

The actual FIFO output, due to skew introduced by cabling, synchronizing clock skewing, and/or debounce skewing, may appear as follows:

	Channel 5	**Channel 4**
Previous State 1	0	1
	01 to 10 change occurs here, but Channel 4 lags Channel 5 by 3nsec (New data appears on Channel 5, but old data still lingers on Channel 4)	
COS State 1	1	1

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	Channel 5	Channel 4
Previous State 2	1	1
COS State 2	1	0

The recovered COS FIFO data appears to have logically “anded”the previous state, and the current state of COS State 1 and Previous State 2, while the correct COS data does not appear until COS State 2. When viewed on a logic analyzer, the incoming data skew may be as little as 3 or 4 nsec, but due to synchronizing clock skew and the debounce skew, the saved COS sequence appears as two separate events.

If the Channel 4 COS detection circuitry had not been set to detect falling edges, a perceived erroneous result would still occur, but only Previous State 1 and COS State 1 would have occurred. This would still leave the tester with the impression that the values of the previous state (01) and final state (10) had somehow been logically “Anded” together.

A better approach to a walking ones test would be to reset the input channels to all zeros between walking a 1 from one channel to the next. This allows for the various skews to settle, and still allows the tester to detect channel cross-talk, which is one of the primary purposes of the walking ones testing.

Although the likelihood of problems being caused by this condition during “real world” operation is remote, it is still a possibility. The programer and system integrator should take this condition into consideration.

1.6 Inputs

The input circuit is easily configured by the user to be either Voltage Sensing or Contact Closure. ***Figure 1-3, Channels 1-30 Input Circuitry*** on page 19 shows the circuitry for input channels 1-30. For monitoring circuits which short the inputs, use the Contact Closure input circuit. Otherwise use the Voltage Sensing circuit. This can be configured differently for each bank of eight channels by inserting or removing the SIP for that bank.

The user can configure a circuit to monitor various external voltage levels by adjusting the position of the switch that controls the resistance of the input voltage divider resistor Rs1. Also shown in ***Figure 1-3*** is the voltage sensing input circuit and the contact closure input topology. For monitoring closed contacts or contacts-to-ground, use the contact closure input circuit configuration. To monitor circuits which supply power, use the voltage sensing input configuration.

1.6.1 Voltage Sensing

When using the Voltage Sensing configuration, the factory-installed SIP must be removed for that bank. Each of the 32 input channels can be set, in groups of two, to a different voltage selection. For example, the signal levels for input 1 and 2 could be set to a voltage input sensitivity of 5V, while inputs 3 and 4 could be set to 12V or 24/28V.

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1.6.2 Contact Closure

If the Contact Closure configuration is chosen, the user will need to insert a SIP resistor (provided) and set the appropriate pull-up voltage using either 5V, 12V or an external user-supplied voltage through contacts on channels 31 or 32.

NOTE
It is recommended that user supplied voltage not exceed 28V.

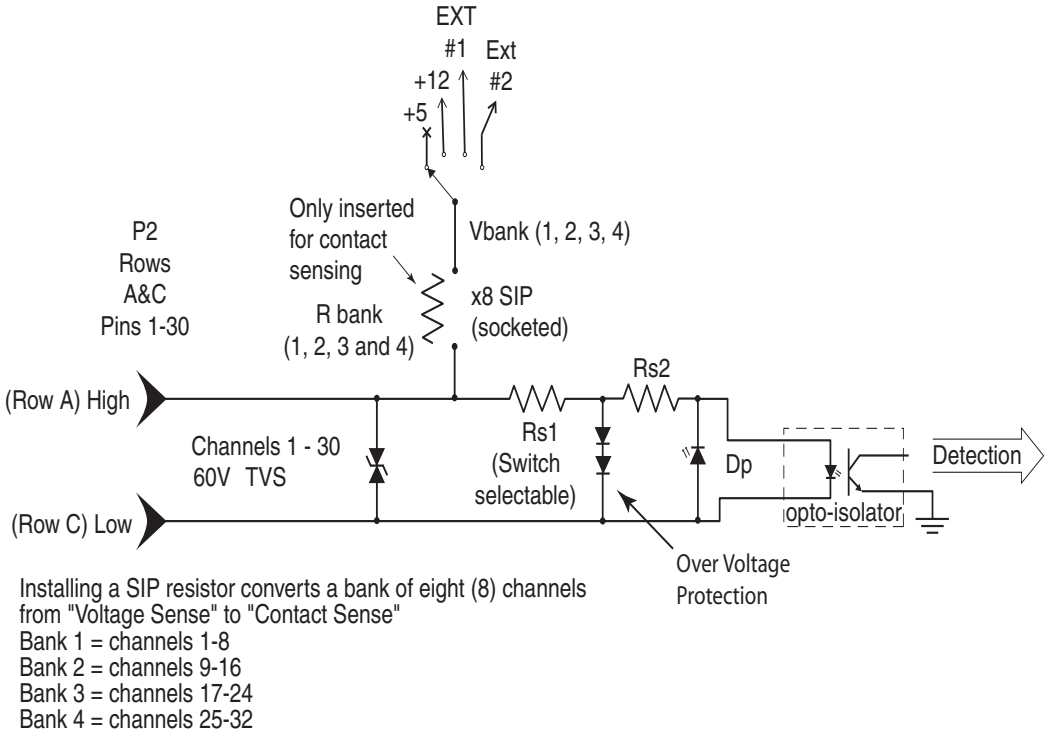
When using Contact Closure, all inputs for that group (1-8, 9-16, 17-24 or 25-32) are required to be set to the same voltage sensitivity level using the Voltage Selection switches. For example, to set the second bank (channels 9-16) for Contact Closure, install a SIP resistor in socket E6, rotate switch S27 to the preferred voltage, and set the four input sensitivity switches (S8, S9, S18 and S19) for the same voltage as S27. As shown in ***Figure 1-4, Channel 31 Input Circuitry (Channel 32 uses Vext #2)*** on page 20, inputs 31 and 32 can be sacrificed to provide two external voltages (Vext1 and Vext2) to the pull-up SIP resistors.

Table 1-3 Contact Closure SIP Resistors and Switch Assignments

Channels	SIP Resistor Socket	Voltage Source Switch
1 through 8	E34	S28
9 through 16	E35	S27
17 through 24	E36	S26
25 through 32	E37	S25

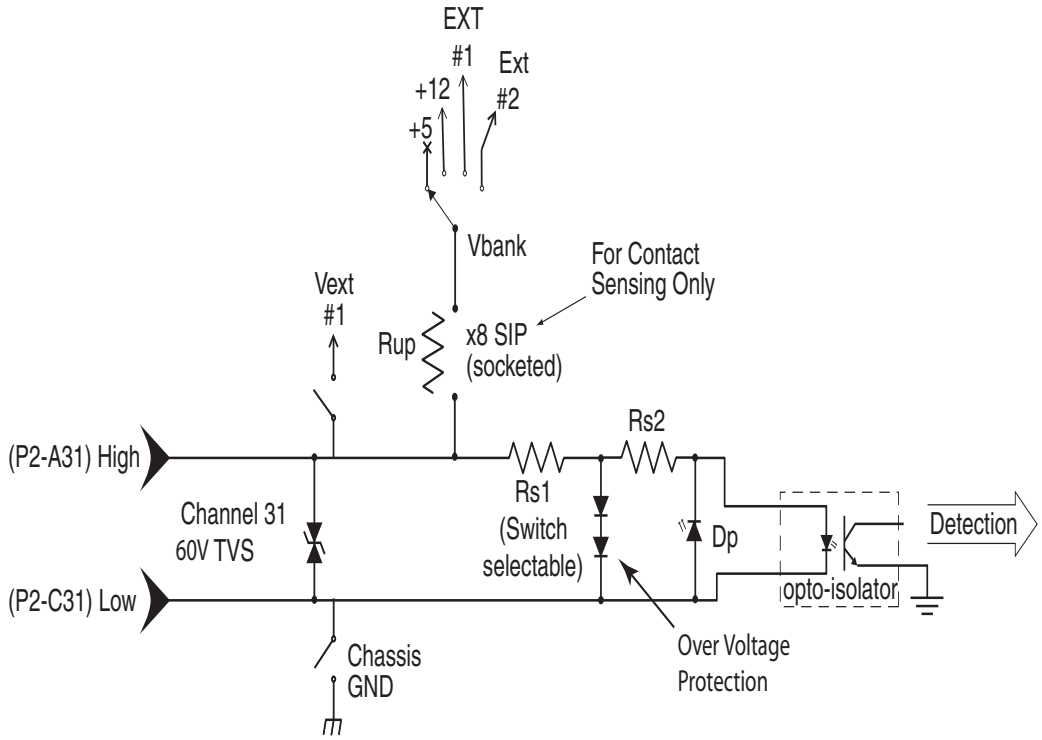
CAUTION
User supplied voltages should not exceed 28V for normal operation.

Figure 1-3 Channels 1-30 Input Circuitry



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Figure 1-4 Channel 31 Input Circuitry (Channel 32 uses Vext #2)



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2 • Configuration and Installation

2.1 Introduction

This chapter describes the installation and configuration of the board. Cable configuration, jumper/switch configuration and board layout are illustrated in this chapter.

2.2 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Customer Care together with a request for advice concerning the disposition of the damaged item(s).



CAUTION

Some of the components assembled on Abaco Systems products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

2.3 Physical Installation



CAUTION

Do not install or remove the boards while power is applied.

2.3.1 Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

1. Verify that all the desired jumpers/switches are in place and set to the desired position. To change the board address or address modifier, refer to *section 2.4.2, Board Address and Address Modifier Selection* on page 22.
2. Ensure the I/O cables, with the proper mating connectors, have been connected to the input/output connector P2 and P3.
   a. De-energize the equipment and insert the board into the appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

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2.4 Operational Configuration

The VMIVME-1184 Board's base address and I/O access mode are determined by user configurable switches. This section describes the use of these switches. The locations of the switches and jumpers on the VMIVME-1184 are shown in *Figure 2-1, Switch and Jumper Locations* on page 23.

2.4.1 Factory Installed Switches/Jumpers

Each VMIVME-1184 is configured at the factory with the specific switch/jumper arrangement shown in *Figure 2-1* on page 23. The factory configuration establishes the following functional baseline for the board, and ensures that all essential jumpers are installed.

- Base address is set to 0000 HEX
- Standard 24-bit Address Mode (S3-1 = On)
- All 32 channels are set for: Contact Sensing, 5V with a 10µs debounce

2.4.2 Board Address and Address Modifier Selection

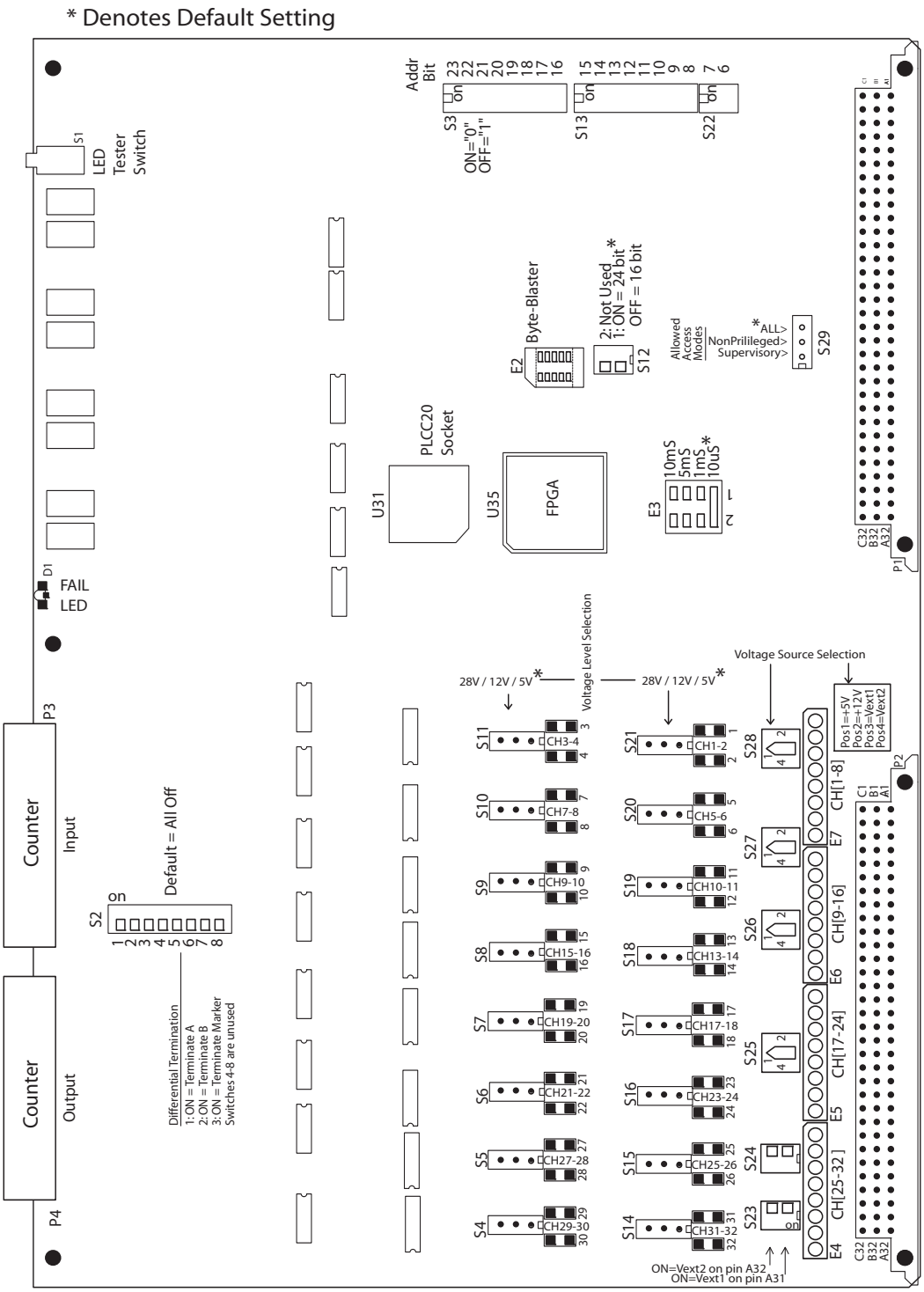
Switches S3, S13 and S22 set the address. The values of these bits is determined by the switch position. When a switch is ON the address bit value is zero "0" for a match. If the switch is OFF, the value is a one "1". Therefore, turn each switch ON for every zero "0" in the base address of the board.

This board is designed to respond to standard (A24) or short (A16) address ranges. S12-1 is used to establish the address range for the board. When set to OFF the board will operate in the short address region. In this mode, the upper 8 (A16 to A23) address lines will be ignored and the switch settings for those address lines are not used. If S12-1 is set to ON (standard), these lines will be decoded. Therefore, they must be configured according to the base address.

S29 determines which address modifier the board will respond to during data transfers. This switch determines supervisory or nonprivileged transfers. The middle position selects nonprivileged transfers only. In the bottom position the board responds only to supervisory accesses. The top (ALL) position allows both address modifiers.

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Figure 2-1 Switch and Jumper Locations



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Table 2-1 Voltage Thresholds

Voltage	25 C Exp Act	40 C Exp Act	80 C Exp Act	P/F
5V LO -> HI	1.2 1.3	1.3 1.4	1.6 1.9	P
12V LO -> HI	1.7 1.9	1.9 2.1	3.2 3.6	P
28V LO -> HI	2.5 2.9	3.1 3.6	6.1 7.3	P
5V HI -> LO	1.2 1.1	1.2 1.1	1.4 1.3	P
12V HI -> LO	1.5 1.5	1.7 1.6	2.6 2.3	P
28V HI -> LO	2.2 2.2	2.8 2.5	5.0 4.4	P

2.4.3 Debounce Timing

Input debounce is accomplished by an adjustable sample clock. The user chooses the frequency of this clock (which sets the debounce timing) by installing a jumper in one of the positions on E3. ***Figure 2-1, Switch and Jumper Locations*** on page 23 shows the jumpers and their timing values. The Change-of-State logic periodically takes a sample of the input level to determine the present state of the input channel. Unlike the input circuitry which continuously monitors the external world, the COS takes a sample of the outside environment at the VMEbus clock rate (16 MHz). The debounce times available have been chosen to provide control for a wide range of inputs. Fast times for high speeds and low electrical noise environments, slow times for noisier switches and relays.

Table 2-2 Jumper E3 (Extended Debounce Timing)

Pin#	Selection	Jumper
1-2	10 µs	Installed (Default)
3-4	1 ms	Omitted
5-6	5 ms	Omitted
7-8	10 ms	Omitted



NOTE

NOTE: If no jumper is installed the debounce time will be set to 1µs. Although the jumper setting is latched upon release of VMEbus “SYSRESET*”, the read/write register setting can be changed through software later.

2.5 Input Configurations

The input circuitry of the VMIVME-1184 can be configured to monitor a variety of external circuits. The user also has control over the threshold to use. ***Chapter 1, Theory of Operation*** discusses the various circuit configurations that can be accommodated by this design.

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2.6 Connector Description

Two 96-pin DIN connectors, P1 and P2 (*Figure 2-2, P1/P2 Connector Pin Layout* on page 26), provide the connections to the VMIVME-1184. P1 contains the address, data and control lines, plus all the additional signals necessary to control the VMEbus functions of the board. P2 provides the connections for the upper 16 data lines, additional power and ground pins, and the 32 channel digital acquisition inputs.

Orientation of the P1 and P2 connectors are shown in *Figure 2-1* on page 23. The P2 signal assignments are listed in *Table 2-4, P2 Pin Assignments* on page 27. The mating connector for P2 (Panduit Model 120-964-435E or equivalent) is designed to be used with a standard 64-wire ribbon-cable with conductor spacing of 0.050 inches. In environments where there is a high degree of electrical noise, a twisted-pair ribbon cable with an overall shield is recommended.

Two nine-channel connectors on the front panel (P3 and P4) provide the respective inputs and daisy-chain outputs for a 0 - 5V single-ended or differential quadrature counter with an optional marker pulse. A single channel (A) can be used to simply increment the counter. See *Figure 2-2* on page 26 for connector pinouts.

2.6.1 Barrier Terminal Transition Panels

The VMIVME-1184 can be used with Abaco's BT0X family of BT transitions panels. The VMIACC-BT01, 02, 03 and 04 family of BT transition panels meets ANSI/IEEE SWC TEST.

The BT transition panels provides a passive breakout of the discrete wires of the ribbon cables, allowing for a more efficient interface between external user equipment and Abaco's VMEbus-based interface boards. The BT transition panels eliminate the need for wire lugs and other bulky methods of wiring transitions.

The VMIACC-BT01 differential dual 64-pin transition panel facilitates 64 isolated pair circuits with no common ground (2-wire). The VMIACC-BT02 single-ended dual 64-pin transition panel facilitates 64 non-isolated pair circuits with the C-row tied to common ground E1 (2-wire). The VMIACC-BT03 differential dual 96-pin transition panel facilitates 64 isolated pair circuits with a common ground (3-wire). The VMIACC-BT04 dual 96-pin transition panel breaks out 192 individual circuits to terminal blocks. The BT transition panels are EIA RS-310C standard 19-inch rack mountable. The BT transition panels are compact and convenient to use even where space is a constraint. The panels will accommodate wire size from 22 AWG to 14 AWG stranded wire or to 12 AWG solid wire.

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Figure 2-2 P1/P2 Connector Pin Layout

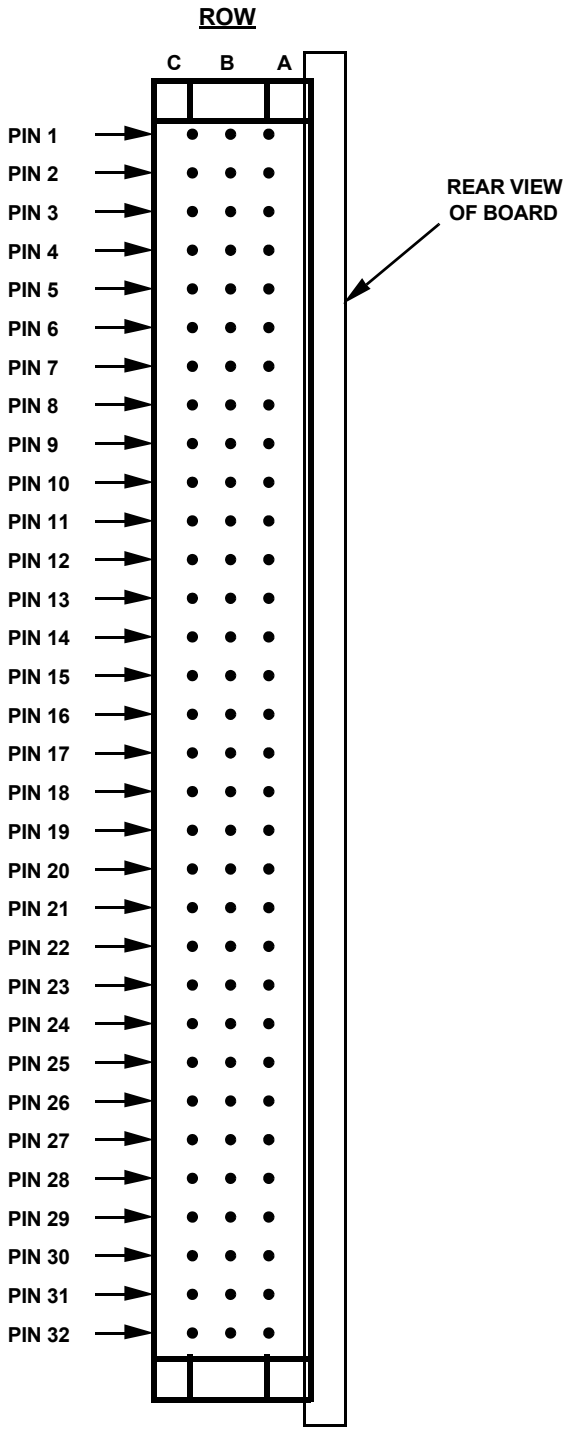


Table 2-3 P1 Pin Assignments

Pin	Function	Pin	Function	Pin	Function
C1	VME_D(8)	B1	N/C	A1	VME_D(0)
C2	VME_D(9)	B2	N/C	A2	VME_D(1)
C3	VME_D(10)	B3	N/C	A3	VME_D(2)
C4	VME_D(11)	B4	Tied to B5	A4	VME_D(3)
C5	VME_D(12)	B5	Tied to B4	A5	VME_D(4)
C6	VME_D(13)	B6	Tied to B7	A6	VME_D(5)

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Table 2-3 P1 Pin Assignments (Continued)

Pin	Function	Pin	Function	Pin	Function
C7	VME_D(14)	B7	Tied to B6	A7	VME_D(6)
C8	VME_D(15)	B8	Tied to B9	A8	VME_D(7)
C9	GND	B9	Tied to B8	A9	GND
C10	N/C	B10	Tied to B11	A10	VME_SYSCLK
C11	N/C	B11	Tied to B10	A11	GND
C12	VME_SYSRSTn	B12	N/C	A12	VME_DS1n
C13	VME_LWORDn	B13	N/C	A13	VME_DS0n
C14	VME_AM(5)	B14	N/C	A14	VME_WRITEn
C15	VME_D(23)	B15	N/C	A15	GND
C16	VME_D(22)	B16	VME_AM(0)	A16	VME_DTACKn
C17	VME_D(21)	B17	VME_AM(1)	A17	GND
C18	VME_D(20)	B18	VME_AM(2)	A18	VME_ASn
C19	VME_D(19)	B19	VME_AM(3)	A19	GND
C20	VME_D(18)	B20	GND	A20	N/C
C21	VME_D(17)	B21	N/C	A21	VME_IACKINn
C22	VME_D(16)	B22	N/C	A22	VME_IACKOUTn
C23	VME_D(15)	B23	GND	A23	VME_AM(4)
C24	VME_D(14)	B24	VME_IRQ(7)n	A24	VME_A(7)
C25	VME_D(13)	B25	VME_IRQ(6)n	A25	VME_A(6)
C26	VME_D(12)	B26	VME_IRQ(5)n	A26	VME_A(5)
C27	VME_D(11)	B27	VME_IRQ(4)n	A27	VME_A(4)
C28	VME_D(10)	B28	VME_IRQ(3)n	A28	VME_A(3)
C29	VME_D(9)	B29	VME_IRQ(2)n	A29	VME_A(2)
C30	VME_D(8)	B30	VME_IRQ(1)n	A30	VME_A(1)
C31	VCC_12.0	B31	N/C	A31	N/C
C32	VCC_5.0	B32	VCC_5.0	A32	VCC_5.0

Table 2-4 P2 Pin Assignments

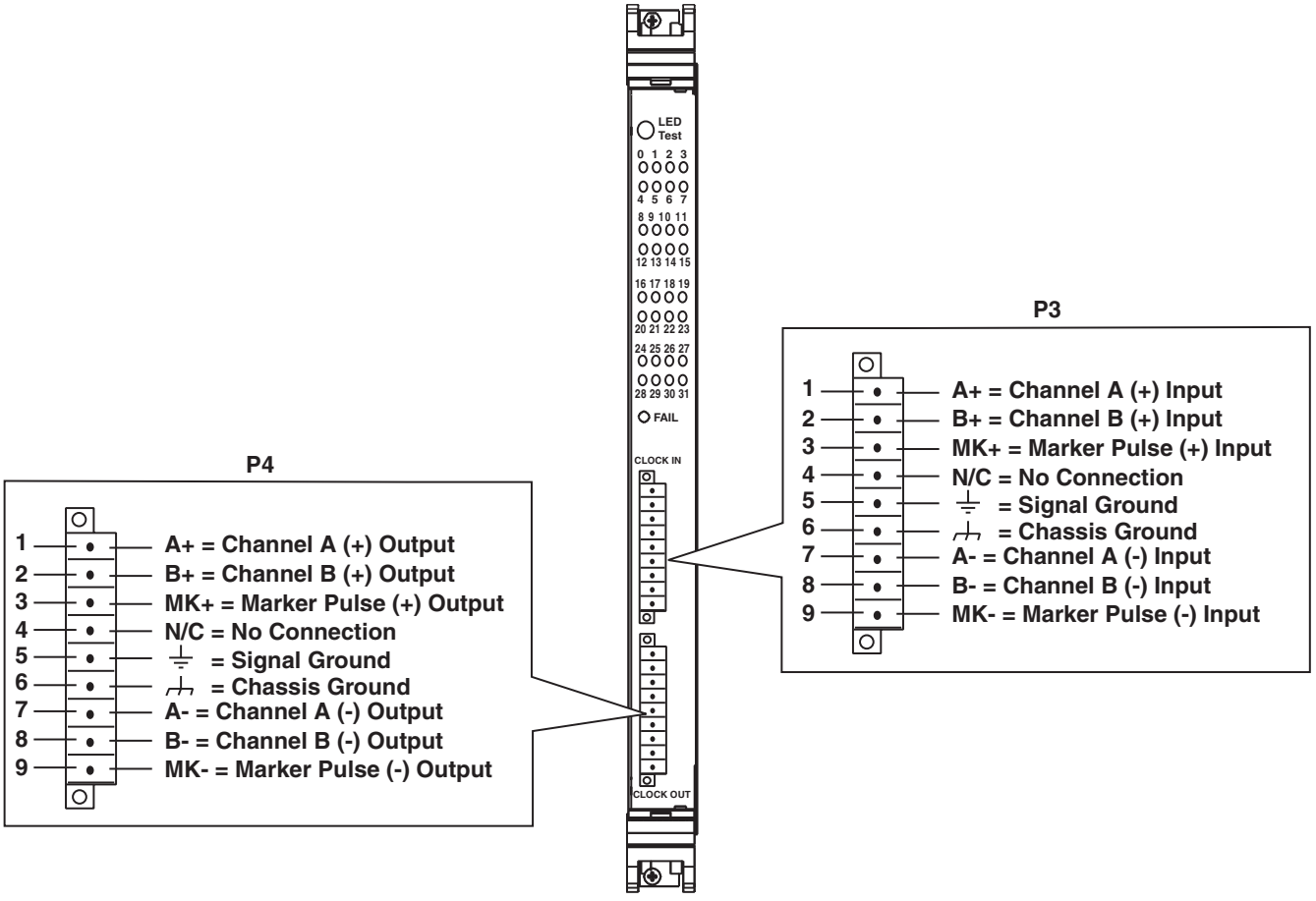
Pin	Function	Pin	Function	Pin	Function
C1	CH(1) INPUT-	B1	VCC_5.0	A1	CH(1) INPUT+
C2	CH(2) INPUT-	B2	GND	A2	CH(2) INPUT+
C3	CH(3) INPUT-	B3	N/C	A3	CH(3) INPUT+
C4	CH(4) INPUT-	B4	N/C	A4	CH(4) INPUT+
C5	CH(5) INPUT-	B5	N/C	A5	CH(5) INPUT+
C6	CH(6) INPUT-	B6	N/C	A6	CH(6) INPUT+
C7	CH(7) INPUT-	B7	N/C	A7	CH(7) INPUT+
C8	CH(8) INPUT-	B8	N/C	A8	CH(8) INPUT+
C9	CH(9) INPUT-	B9	N/C	A9	CH(9) INPUT+
C10	CH(10) INPUT-	B10	N/C	A10	CH(10) INPUT+
C11	CH(11) INPUT-	B11	N/C	A11	CH(11) INPUT+
C12	CH(12) INPUT-	B12	GND	A12	CH(12) INPUT+
C13	CH(13) INPUT-	B13	VCC_5.0	A13	CH(13) INPUT+
C14	CH(14) INPUT-	B14	VME_D(16)	A14	CH(14) INPUT+
C15	CH(15) INPUT-	B15	VME_D(17)	A15	CH(15) INPUT+
C16	CH(16) INPUT-	B16	VME_D(18)	A16	CH(16) INPUT+

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Table 2-4 P2 Pin Assignments (Continued)

Pin	Function	Pin	Function	Pin	Function
C17	CH(17) INPUT-	B17	VME_D(19)	A17	CH(17) INPUT+
C18	CH(18) INPUT-	B18	VME_D(20)	A18	CH(18) INPUT+
C19	CH(19) INPUT-	B19	VME_D(21)	A19	CH(19) INPUT+
C20	CH(20) INPUT-	B20	VME_D(22)	A20	CH(20) INPUT+
C21	CH(21) INPUT-	B21	VME_D(23)	A21	CH(21) INPUT+
C22	CH(22) INPUT-	B22	GND	A22	CH(22) INPUT+
C23	CH(23) INPUT-	B23	VME_D(24)	A23	CH(23) INPUT+
C24	CH(24) INPUT-	B24	VME_D(25)	A24	CH(24) INPUT+
C25	CH(25) INPUT-	B25	VME_D(26)	A25	CH(25) INPUT+
C26	CH(26) INPUT-	B26	VME_D(27)	A26	CH(26) INPUT+
C27	CH(27) INPUT-	B27	VME_D(28)	A27	CH(27) INPUT+
C28	CH(28) INPUT-	B28	VME_D(29)	A28	CH(28) INPUT+
C29	CH(29) INPUT-	B29	VME_D(30)	A29	CH(29) INPUT+
C30	CH(30) INPUT-	B30	VME_D(31)	A30	CH(30) INPUT+
C31	CH(31) INPUT-	B31	GND	A31	CH(31) INPUT+
C32	CH(32) INPUT-	B32	VCC_5.0	A32	CH(32) INPUT+

P3/P4 Connector Pinouts



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3 • Programming

3.1 Introduction

Throughout this manual the 32 input channels have been listed as 1-32. In this section the inputs are discussed on a logic level, and as such, will be referenced as 00-31.

The VMIVME-1184 can reside in short 16-bit I/O space or standard 24-bit data space. There are 18 switches used to establish the base address of the board. Table 3-1 lists the registers and their relative (or offset) addresses. The relative address is added to the base address to generate the actual address for the board's register. The board logic uses address lines A5 through A1 to decode the registers listed in ***Table 3-1***. The rest of the address lines used by the board are set using the address switches. In ***Chapter 2*** there is a detailed explanation of how to set these switches.

Programming the VMIVME-1184 involves setting up the IP (Interrupt processors) and the COS logic. When the board is first powered-up or after a system reset, all control registers are reset to their default values.

It is recommended to first set up the COS logic via the COS Select and the Channel Interrupt Enable registers. Then use the IP Control registers to set the IRE bits to start the interrupts. During interrupt acknowledge cycles, the IP supplies the service routine vector to the VMEbus.

The FIFOs and the BD ID registers are read-only. The board's read-only registers will not respond to writes, and the data will be ignored. During a read of the "current" Data registers, the board will sample the data received at the input (P2) and transfer that data to the VMEbus. Most registers, can be accessed using byte, word or longword transfers. The FIFO register, CTR_FIFO and the QUAD_CTR can only be accessed with longword transfers.

Table 3-1 VMIVME-1184 Address Map

Relative Address	Register Name	Register Function	R/RW
$00	BD ID	Identification number (BD ID = $6700)	R
$02	CSR1	Board Control bits and Status flags Register #1	RW
$04	Current Data Register	Input channels 31 through 0 (non-debounced)	R
$08	Data FIFO Register	COS data for channels 31 through 0	R
$0C	IP CTRL Register	Interrupt processor controls	RW
$0D	IP COS Vector Register	COS/SOE Interrupt Vector	RW
$0E	IP MKR Vector Register	Marker Pulse Interrupt Vector	RW
$10	CTR FIFO Register	Counter FIFO register	R
$14	Quad_CTR	Quadrature Counter Current Value	RW
$18	COS_SEL Register 0	COS Select Register for channels 31 through 24	RW
$1A	COS_SEL Register 1	COS Select Register for channels 23 through 16	RW
$1C	COS_SEL Register 2	COS Select Register for channels 15 through 8	RW
$1E	COS_SEL Register 3	COS Select Register for channels 7 through 0	RW
$20	FIFO_CNT	Number of unread samples in the COS FIFO	R
$22	CTR_FIFO_CNT	Number of unread samples in the Quad CTR FIFO	R

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Table 3-1 VMIVME-1184 Address Map (Continued)

Relative Address	Register Name	Register Function	R/RW
$24	CH_INT_ENA	Channel Interrupt Enable register	RW
$28	DB_Data	Debounced Data Register	R
$30	FREV	Firmware Revision ID	R
$34	CSR2	Control and Status Register #2	RW

3.1.1 Board ID (BD ID) Register

Table 3-2 Board ID Register Bit Map

BD ID: Offset $XXXX00 (fixed @ $6700)							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
0	1	1	0	0	1	1	1

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
0	0	0	0	0	0	0	0

3.2 Control and Status Registers

Table 3-3 Control and Status Register 1 Bit Map

CSR1: Offset $XXXX02 (fixed @ $6700)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Fail LED	Counter Reverse	FIFO Empty	FIFO Full	COS/SOE (0/1)	ROFE/ROAK (0/1)	EN CTR FIFO	Extend Debounce

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Debounce Time		Channel Enable	Double Count	CTR_FIFO_Full	CTR_FIFO_Empty	MRK_Reset	CTR_ENA

3.2.1 CSR1 Bit Definitions

The Offset for the Control and Status Register is $XXXX02.

Bit 15: **Fail LED** - Writing a one (1) to this bit will turn off the LED. Writing a zero (0) to this bit will turn on the LED. **Default is 0**.

Bit 14: **Counter Reverse** - Writing a one (1) to this will reverse the direction of the counter. Given a counter input, if the counter increment, it now decrements and visa versa. This applies to all 4 modes. **Default is 0 for normal direction**.

Bit 13: **Data FIFO Empty** – This bit is a read-only flag that when set, indicates that the COS/SOE FIFO is empty.

Bit 12: **Data FIFO Full** – This bit is a read-only flag that when set, indicates that the COS/SOE FIFO is full, and any additional COS/SOE events may be lost. An interrupt is generated at the COS level and vector.

Bit 11: **COS/SOE (0/1)** - Change-of-State/Sequence-of-Events: Bit 11 is set to zero (0) for the Change-of-State mode, and to a one (1) for the Sequence-of -Events mode. **Default is 0**.

Bit 10: **ROFE/ROAK(0/1)** - Release interrupt on FIFO Empty/Release Interrupt on Acknowledge. **Default is 0**.

Bit 09: **EN CTR FIFO** - Bit 9 enables storage of the Counter value each time a COS, or SOE event occurs. **Default is 0**.

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Bit 08: **Extend Debounce** - A one (1) sets the Debounce to the time indicated by bits 6 and 7. The original value is latched from onboard jumpers, but this condition can be changed through the software. Clearing this bit reduces debounce to 1µs.

Bits 07, 06: **Debounce Time** - The original value is latched from onboard jumpers at reset, but this can be changed later through software. Refer to the list below for correlating debounce times.

Table 3-4 Correlating Debounce Times

Bit 7	Bit 6	Time
0	0	10µs
0	1	1ms
1	0	5ms
1	1	10ms

Bit 05: **Channel Enable** - 1= Two channel (A and B) input (Quadrature mode)
0 = One channel input (channel A only, counter mode)
Default is 0.

Bit 04: **Double Count** - 1 = 2X counting
0 = 1X counting.
Default is 0.

Bit 03: **CTR_FIFO_FULL** - 1 = Counter FIFO is full.

Bit 02: **CTR_FIFO_EMPTY** - 1 = Counter FIFO is empty.

Bit 01: **MRK_Reset** - 1 = Marker Pulse resets counter.

Bit 00: **Counter Enable** - 1 = Enable the counter
0 = Disable counter (Default)

3.2.2 CSR2 Bit Definitions

The Offset for the Control and Status Register is $XXXX34.

The term "gating" means to qualify a signal. For some encoders, the marker pulse should be gated with the "A", or "B" channel in such a way as to qualify it. The actual marker signal could be quite long in duration, but it takes "A" and/or "B" to be a certain state before the marker is actually considered valid.

Table 3-5 Control and Status Register 2 Bit Map

CSR2: Register Offset $XXXX34							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved							

Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved					Set Debounce Time		Disable AB Debounce

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Reserved	Quad Counter Conn Warning	Broken Wire Counter Connectivity					

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Marker Int Gen	Cir Counter	Channel Enable		Marker Qualification			True Ungated Current Marker

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3.2.3 Counter Connectivity

Bits 31-19 and Bit 15: Unused (reserved for future use).

3.2.4 Quadrature Counter Decoder Bits (Bits 16, 17 and 18)

Bits 18 and 17 = Set debounce times

0 0 = 62.5nS

0 1 = 125nS

1 0 = 1uS

1 1 = 10uS

Bit 16: 1 = Disable AB debounce (note: Marker is always debounced per debounce times below)



NOTE

The minimum, or no debounce is used in quadrature mode to help the capture of quick AB transitions during equipment stoppage. Some debounce should be used in Counter modes. The use of differential signaling helps reduce noise problems in long cable runs or noisy motor environments.

Bits 14 - 08 below are used for Counter Connectivity.

Bit 14: RW, Counter Connectivity Warning.

0 = Okay

1 = Change or Conflict Warning.

The connectivity status for all six wires is latched-in as VME_SYSRESET goes away. If a conflicting configuration is attempted, this bit is set. For example, trying to use 2 channels without a "B" wire connected. Also, if a connectivity change occurs after RESET, then this bit is set as a warning indication. Writing a "0" to this bit forces a re-read of the latest wire status and may clear the warning, if it is not a conflict warning. Conflicts cannot be cleared without actually taking care of the conflict.

Some possible conflicts are:

No A+ connection

No B+ when CSR1_[5] (two channel operational mode) is set

No marker connection (+ or -) detected when CSR1_[1] (marker clear counter) is set or ip_ctl[31] (marker interrupt) is set.

Bits 13-08: Read only, "Broken Wire" Quadrature Counter input connectivity status.
"0" = okay, connected. "1" = Unconnected

13: A+ wire status

12: A- wire status

11: B+ wire status

10: B- wire status

09: M+ wire status

08: M- wire status

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3.2.5 Encoder Markers

The following bits are used to control or show the status of markers in the system.

Bit 07: **Marker Interrupt Generation** - R/W,

0 = Rising Edge only (default)

1 = Both edges



NOTE

If Bits 04 or 05 of CSR2 are set, then the qualified marker edges are used to generate the interrupt.

Bit 06: **Clear Counter (level/edge)** - R/W,

0 = Counter cleared by marker level. (default)

1 = Counter cleared by marker rising edge only



NOTE

Bit 06 requires CSR1_[1] to be set in order to function. If bits 4 or 5 of CSR2 are set, then the qualified marker is used.

Bits 05, 04: **Channel Enable** - R/W, Enables Channels for marker qualification/gating. ("M" channel is always enabled)

5: 1 = Use channel "A" to qualify marker; 0 = do not use "A" (default)

4: 1 = Use channel "B" to qualify marker; 0 = do not use "B" (default)

Bits 03, 02, 01:Marker Qualification - R/W, These bits are used in gating values for "A", "B", "M" channels, respectively. These are the values needed in order to recognize a true index/marker (0,0,1 is default).

Bit 00: **True Ungated "Current" Marker** - Read only, this indicates the status input directly from the encoder, 1 = High, 0 = Low

CSR 1 and 2 are used to control the basic functions of the board.

The Fail LED is user controlled and can be turned off when the board is working properly. Two bits of the CSR1 (Bits 13 and 12) are used to monitor the COS memory device (FIFO). Bit 12 (FIFO_Full) and Bit 13 (FIFO_Empty), allow the user to monitor the current condition of the FIFO. If a FIFO is full, any new flagged data will be lost. All bits in CSR1 are available during read operations. Bit 11 (COS/SOE) of CSR1, determines the mode of operation for the board.

The registers can be accessed on a byte, word or longword boundary. Please refer to the memory map in Chapter 3 for the relative address locations for these registers. The BD ID is at the base address of the board with the CSR1 stacked above it, followed by Data, COS/SOE FIFO, then the IP control and vector registers. Followed by the longword location where the current value of the SOE quadrature counter can be read. The COS Select 0 through 3 registers are placed next. COS Select registers 0 through 3 controls the monitoring mode (data only, rising/falling/any edge) of each channel. This allows you to read the BD ID and CSR1 in one longword access. You cannot read the odd byte of the BD ID and the even byte of CSR1 in one word transfer.

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3.3 Data FIFO Register

The Data FIFO register is a read-only register, containing the stored COS or SOE data. In the SOE mode of operation, the first read of this register will yield the value of the channel inputs previous to the change-of-state that triggered the storage of data. The second read yields the flagged data that triggered the storage of data. The Data FIFO register is readable by longword only.

NOTE
Reads of less than a longword are ignored.

Please remember, COS mode only stores the triggered event. SOE mode adds the additional previous data to the FIFO. Therefore, the 512 level FIFO can only store 256 events in SOE mode (two data for each trigger). Only one count is stored in the counter FIFO regardless of mode of operation.

- COS = 1, Read to capture the data
- SOE = 2, Read to capture the data

.

Table 3-6 Data FIFO Register Bit Map

FIFO Register Offset $XXXX08							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
CH15	CH14	CH13	CH12	CH11	CH10	CH09	CH08
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH07	CH06	CH05	CH04	CH03	CH02	CH01	CH00

3.4 Interrupt Processor Control Register

This Read/Write register is used to configure the operations of the Interrupt Processor.

Table 3-7 Interrupt Processor Control Register Bit Map

Interrupt Processor Control Register: Offset $XXXX0C							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
MKR_INT_ENA	Interrupt Levels			COS_INT_ENA	Interrupt Levels		
	0	0	0		0	0	0
	L2	L1	L0		L2	L1	L0

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3.4.1 Interrupt Levels

These three bits (L2 through L0) set the interrupt level that the IP will present to the host when a COS, or Marker request is made. The interrupt levels and the field values are:

Bits 7 through 4: Marker Interrupt Enable and Level bits.
Bits 3 through 0: COS Interrupt Enable and Level bits.

Table 3-8 Interrupt Level Bits

L2	L1	L0	IRQ Level
0	0	0	Disabled
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

The interrupt for the COS/SOE is cleared automatically when one of the following conditions is met:

#1: ROAK mode - Interrupt Acknowledged
#2: ROFE mode - FIFO is emptied
#3: Interrupt enabled bit is cleared

The Quadrature Marker Pulse interrupt is cleared when its interrupt is acknowledged, or when the MKR_INT_ENA bit is cleared.

3.5 Interrupt Processor COS Vector Register (Offset: $XXXX0D)

This is a read-write register, programmed by the user with the interrupt vector value desired for the COS interrupt bits 7 through 0. **Default is $00**.

3.6 Interrupt Processor Marker Vector Register (Offset: $XXXX0E)

This is a read-write register, programmed by the user with the interrupt vector value desired for the Marker interrupts bits 7 through 0. **Default is $00**.

3.7 Counter FIFO Register (Offset: $XXXX10)

This read-only 32-bit data register contains the value of the counter at the time that the data capture was triggered. It should be read once with each read to the Data register (two reads when used in SOE mode) so that time stamp/data alignment will be maintained. This will result in the complete data structure as shown:

In COS mode:

- Counter_Value
- COS_Input_Data

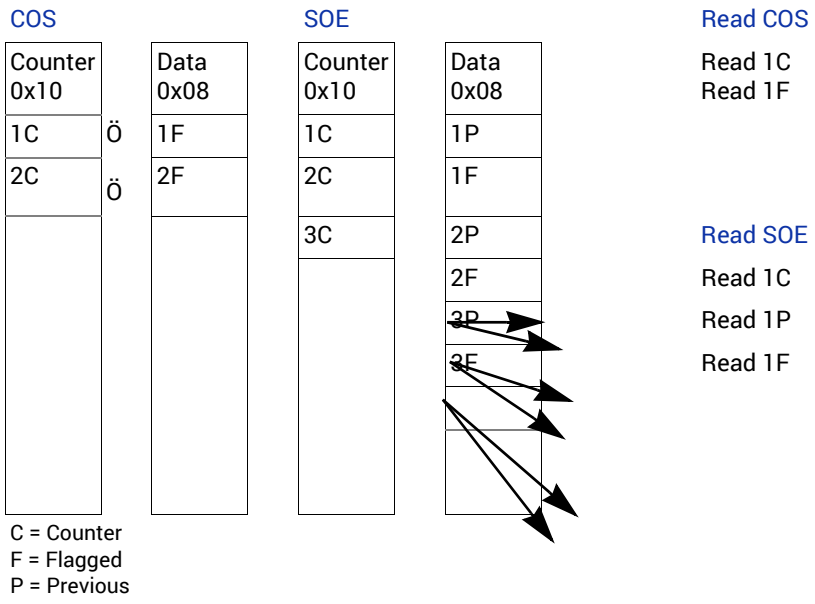
Setting Bit 9 in the CSR to one (1) enables this register.

In SOE mode, there are two data FIFO reads:

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- Counter_Value
- PREV_Input_Data
- COS_Input_Data

Figure 3-1 COS and SOE Registers



3.7.1 Counter Register (Offset: $XXXX14)

This register contains the current count derived from the front panel input (P3). The Counter register is a longword read/write register, so the user can begin the count with a predetermined value by writing directly to the register.

3.7.2 COS SEL B/A

Channel x

These bits work as a pair for the stated channel. They define the COS trigger condition for the associated channel. Their states and functions are:

Table 3-9 COS SEL B/A

B/A	Function
00	No interrupts (data only)
01	Rising edge interrupts only
10	Falling edge interrupts only
11	Any edge interrupt

Example:

Setting Bits 15 and 14 of address $XXXX1E will cause a COS trigger on any edge occurrence for channel 7.

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3.7.3 COS Select Register 0

This register's bits are used to select the COS trigger condition for bits 31 through 24.

Table 3-10 COS Select Register 0 Bit Map

COS Select Register 0 $XXXX18							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
31B	31A	30B	30A	29B	29A	28B	28A
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
27B	27A	26B	26A	25B	25A	24B	24A

3.7.4 COS Select Register 1

This register's bits are used to select the COS trigger condition for bits 23 through 16.

Table 3-11 COS Select Register 1 Bit Map

COS Select Register 0 $XXXX1A							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
23B	23A	22B	22A	21B	21A	20B	20A
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
19B	19A	18B	18A	17B	17A	16B	16A

3.7.5 COS Select Register 2

This register's bits are used to select the COS trigger condition for bits 15 through 8.

Table 3-12 COS Select Register 2 Bit Map

COS Select Register 0 $XXXX1C							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
15B	15A	14B	14A	13B	13A	12B	12A
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
11B	11A	10B	10A	9B	9A	8B	8A

3.7.6 COS Select Register 3

This register's bits are used to select the COS trigger condition for bits 7 through 0.

Table 3-13 COS Select Register 3 Bit Map

COS Select Register 0 $XXXX1E							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
7B	7A	6B	6A	5B	5A	4B	4A
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
3B	3A	2B	2A	1B	1A	0B	0A

3.7.7 FIFO Count Register (FIFO_CNT)

This 16-bit register contains the count of the number of samples in the COS FIFO.



NOTE

If SOE is enabled, the FIFO count will be twice the number of flagged COS events since the FIFO contains both the previous state, and the changed state for each event.

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Table 3-14 FIFO Count Register Bit Map

FIFO_CNT: Offset $XXXX20							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00

3.7.8 Counter FIFO Count Register (CTR_FIFO_CNT)

This 16-bit register contains the count of the number of samples in the quadrature counter FIFO.

Table 3-15 Counter FIFO Count Register Bit Map

CTR_FIFO_CNT: Offset $XXXX22							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00

3.8 Channel Interrupt Enable Register (CH_INT_ENA)

This 32-bit register allows the user to select which channels will trigger an interrupt. If the bit corresponding to a particular channel is set to a one (1), and that channel has a valid event, then the data is stored in the appropriate FIFO's, and a interrupt is set. If the corresponding bit is set to zero (0), the event is stored in the appropriate FIFO's, but no interrupt is set.

The interrupt for a particular channel corresponds to the channel number, i.e. setting Bit 23 will enable the interrupts for events occurring on input channel 23.

Table 3-16 Channel Interrupt Enable Register Bit Map

CH_INT_ENA Register: Offset $XXXX24							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
CH31	CH30	CH29	CH28	CH27	CH26	CH25	CH24
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
CH23	CH22	CH21	CH20	CH19	CH18	CH17	CH16
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit10	Bit 09	Bit 08
CH15	CH14	CH13	CH12	CH11	CH10	CH09	CH08
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
CH07	CH06	CH05	CH04	CH03	CH02	CH01	CH00

3.9 Firmware Revision Register (FREV)

The Firmware Revision register is a 32-bit, read-only register located at offset $30. It is accessible as byte, word or longword. For example, if the firmware revision is 1.2.17, a read from the register is 00 01 02 17.

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3.10 Counter Feature

The VMIVME-1184 has the capability of accepting a counter input (either single-ended or differential) at the P3 connector on the front panel. A single channel (A) can be used for incremental counting. Two channels are required to function as full Quadrature. The maximum input of this input is 48V. There is a marker input, which the VMIVME-1184 can treat as a counter reset signal, and optionally generate an interrupt. The use of the marker is optional. The marker input can be configured for logic level high or low. For single-ended signaling, connect to the (+) input. The switches on S2 are used to terminate the last device, for RS422 differential signaling ***only***. Single-ended signals should not be terminated.



CAUTION

Using termination on voltages higher than 5V could result in damage to equipment

Table 3-17 Differential Termination (S28)

Switch	Position	Use
1	*On	Places 120 ohms across A+ & A-
2	*On	Places 120 ohms across B+ & B-
3	*On	Places 120 ohms across M+ & M-
4-8	*Off	
* OFF is the default.		



NOTE

NOTE: All three channels (A, B and M) have a maximum input change rate of 100ns. If changes on these channels occur faster, then missed changes or counting errors may occur.

3.11 Counter Operation

Four counter modes are selected based on the resolution required by the application and the encoder used. The VMIVME-1184 utilizes two simple incremental counter modes (1X and 2X) and two quadrature types (2X and 4X).

3.11.1 CSR1_[5, 4] Definitions

Bits 5, 4 = Counter Mode

00 = 1X Counter, increments on rising edge of “A”
01 = 2X Counter, increments on any change of “A”
10 = 2X Quadrature, moves* on any change of “A”
11 = 4X Quadrature, moves* on any change of “A” or “B”

*Direction determined by channel “A” to “B” phase relationship.
A leading B, increments the counter
B leading A, decrements the counter

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Figure 3-2 Leading Edge Example

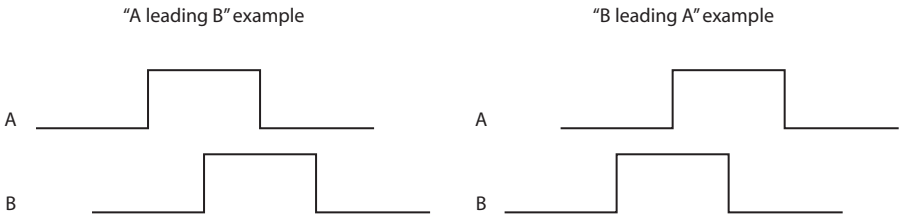


Figure 3-3 1x Counter Mode

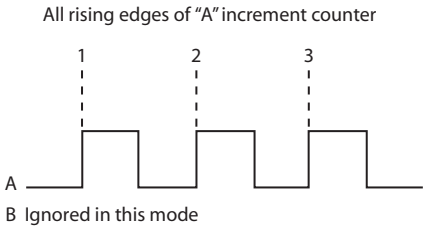
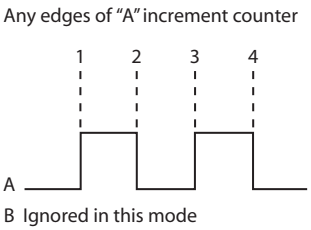


Figure 3-4 2x Counter Mode



3.11.2 2X Quadrature Mode

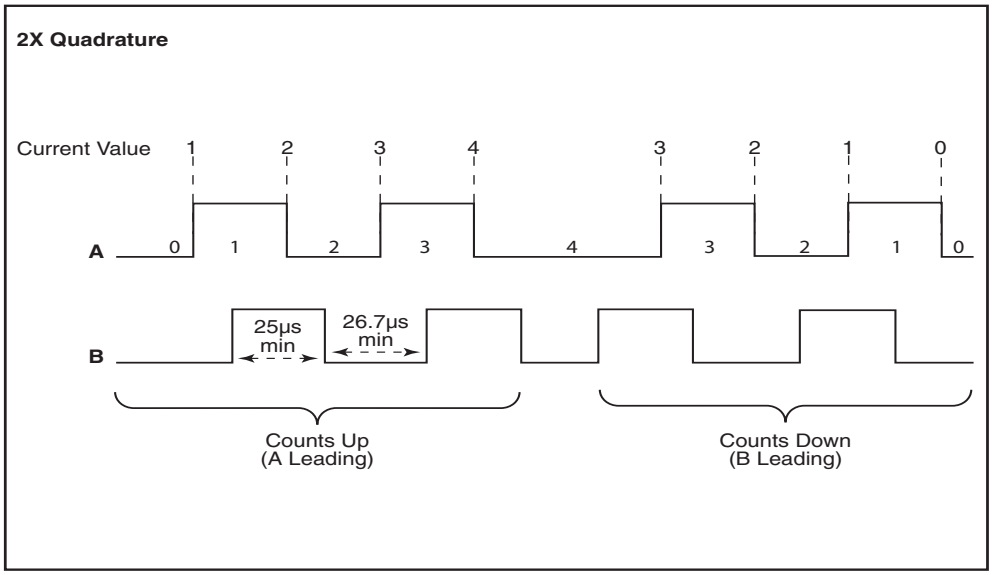
If input A leads input B, the module counts up on both rising and falling edges of input A. If input B leads input A, the module counts down on both rising and falling edges of input A. This mode is set through CSR1 Bits 5 and 4.

CRS1_[5] = 1

CSR1_[4] = 0

Figure 3-5 illustrates the relationship between inputs A and B and the count value in the 2X quadrature mode.

Figure 3-5 2X Quadrature



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3.11.3 4X Quadrature Mode

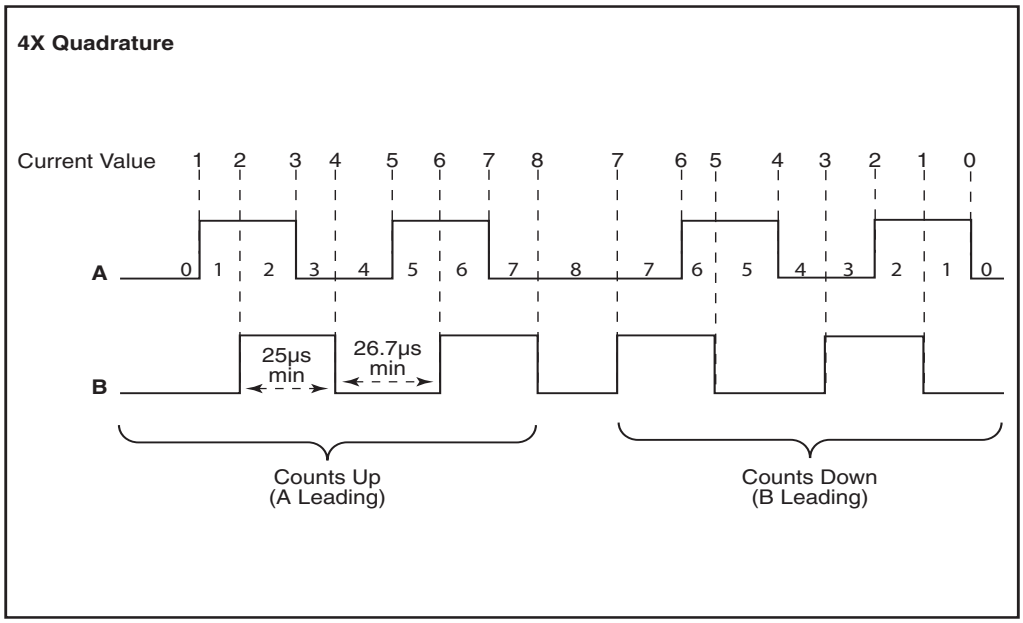
If input A leads input B, the module counts up on both rising and falling edges of inputs A and B. If input B leads input A, the module counts down on the rising and falling edges of inputs A and B. This mode is set through CSR1 Bits 5 and 4.

CRS1_[5] = 1

CSR1_[4] = 1

Figure 3-6 illustrates the relationship between inputs A and B and the count value in the 4X quadrature mode.

Figure 3-6 4X Quadrature



The VMIVME-1184 passes all counter signals to the output connector (P4). Regardless of whether single-ended or differential inputs are provided to P3, P4 always outputs differential which can then be used either way for daisy-chaining.

3.12 Initialization

Due to the nature of computers using VMEbus, the following example is just a descriptive outline of what needs to be done in your program. The descriptions assume an understanding of the VMEbus priority interrupt system.

The following is an example setup of the VMIVME-1184. Since each input channel is individually programmable regarding the type of transition that will trigger an event, caution should be used.

We will program four inputs for each of the COS/SOE operating modes. We will configure Channel 31 for data event storage only. It will NOT generate any interrupts. Channel 28 will cause an interrupt on rising edge transitions. This occurs when a data bit goes from a logic zero (0) to a logic one (1). Channel 26 will cause/generate falling edge interrupts. This is the opposite of Channel 28. Channel 25 will cause an interrupt on any transition (rising or falling).

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The board will operate in SOE mode, with a counter (using the Marker to reset the counter) input through the front panel connector P3.

To program the interrupts, assign an interrupt level and vector for the COS and Marker. We will assign interrupt level 4 to COS/SOE interrupts, and a interrupt vector value of $83. Since we will be using this board in the SOE mode, with a counter (with marker pulse) input to the front of the VMIVME-1184, we will set the marker pulse interrupt to level 2, with an interrupt vector of $45. The board will be set to ROFE mode.

The board in this example is addressed in A16 mode, and is jumper configured to base address $8000.

The required writes to the VMIVME-1184 board are shown in ***Table 3-18***.

Table 3-18 Example Setup of the VMIVME-1184

Address	Register	Value	Task
$XXXX8002	CSR1	0x8A03	Set up CSR1
$XXXX8018	COS_SEL0	0x012C	Set monitoring conditions for Channels 31, 28, 26 and 25
$XXXX800D	IP_COS_VECT	0x83	Set COS/SOE interrupt vector
$XXXX800E	IP_MKR_VECT	0x45	Set Marker Interrupt Vector
$XXXX8024	CH_INT_ENA	0x16000000	Enable COS Interrupts (CH 28, 26 and 25)
$XXXX800C	IP_CTRL_REG	0xAC	Set level for marker and COS interrupts

After completing the previous steps, the board is ready for operation. A write of $8A03 to CSR1 will turn off the FAIL LED and leave the board operating in SOE mode with the counter FIFO enabled.

The board is now ready to start looking for events. Although data can be processed at any time, the interrupt enable bits should only be set when you are ready to handle interrupts. At this time the COS/SOE interrupt, and Marker interrupt enable bits have to be set. One way is to write the entire byte of data again, only this time with the enable bits set. For this example, the value to write would be $AC. Now the board will issue interrupts as the COS logic and Marker dictate.

3.13 VMIVME-1184 Inputs

Table 3-19 Input Connectivity

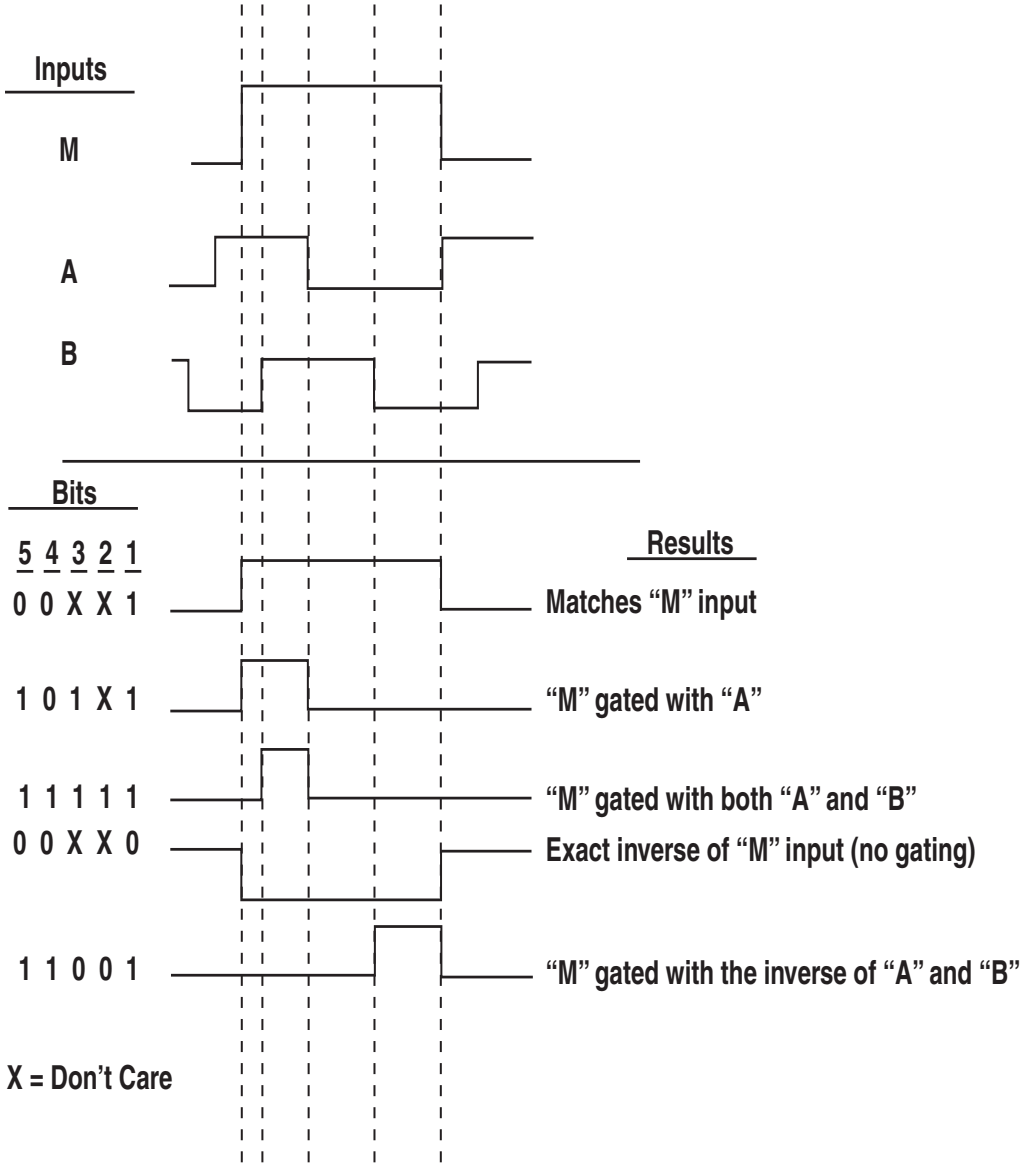
Minimum Connectivity Needed	Modes Supported
A+ (Single-Ended)	Counter
A+, B+ (Single-Ended)	Counter and Quadrature
A+, A- (Differential)	Counter
A+, A-, B+, B- (Differential)	Counter and Quadrature

Regardless of the wiring configuration (single-ended versus differential), only channel “A” is used for counter modes, while both “A” and “B” are necessary for Quadrature mode. Use of the Marker is optional. Differential wiring and transmitter equipment (encoders) are preferred to reduce common mode noise from noisy environments. Differential termination switch S2 should only be used for RS-422 signaling (last device in the chain).

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3.14 Marker Gating

Figure 3-7 Marker Gating Diagram



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