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Product Manual

VMIVME-9081* Intelligent I/O Controller

Publication No. 500-009081-000 Rev. E.0

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Document History

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Waste Electrical and Electronic Equipment (WEEE) Returns



Abaco Systems is registered with an approved Producer Compliance Scheme (PCS) and, subject to suitable contractual arrangements being in place, will ensure WEEE is processed in accordance with the requirements of the WEEE Directive.

Abaco Systems will evaluate requests to take back products purchased by our customers before August 13, 2005 on a case-by-case basis. A WEEE management fee may apply.

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About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a "D" subscript and binary numbers have a "b" subscript. The prefix "0x" shows a hexadecimal number, following the 'C' programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers "k", "M" and "G" have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$ respectively. The only exception to this is in the description of the size of memory areas, when "K", "M" and "G" mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.


NOTE
When describing transfer rates, "k", "M" and "G" mean $x10^3$, $x10^6$ and $x10^9$ *not* $x2^{10}$, $x2^{20}$ and $x2^{30}$.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde ("~") denote active low signals; all other signals are active high. "N" and "P" denote the low and high components of a differential signal respectively.

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www.abaco.com

Abaco Documents

This document is distributed via the Abaco website. You may register for access to manuals via the website.


LINK
www.abaco.com/products/vme-9081

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You can find technical assistance contact details on the website Embedded Support page.


LINK
www.abaco.com/embedded-support

Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:


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support@abaco.com

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If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.


LINK
www.abaco.com/embedded-support

Do not return products without first contacting the Abaco Repairs facility.

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Additional Notes

Abaco's VMIVME-9081* is an Intelligent I/O Controller (IIOC) implemented on the V7768* or VMIVME-7700/VME-7700RC* single board computer. The VMIVME-9081 is the third generation IIOC, combining the functionality of the legacy VMIVME-9064/32* and VMIVME-9066/32* embedded VMEbus host IIOCs. The VMIVME-9081 communicates with a host computer via Reflective Memory, Ethernet, or over the backplane to VMEbus-based hosts or hosts with a built-in VMEbus.

The VMIVME-9081 IIOC combines the intelligence to ease integration and simplify maintenance with the power to significantly reduce the impact of real time I/O on your host computer resources. The IIOC provides a high density, high throughput, low cost solution to the data acquisition and control problem by off loading the I/O scanning, scaling computation, and engineering unit conversion tasks from host computer computational resources. The IIOC provides a user friendly, easily maintained I/O subsystem. Extensive offline diagnostics and real time loopback testing of all I/O points provide quick fault detection and isolation to the I/O channel level, enhancing system reliability and maintainability.

References

V7768/V7769 VME SBC Product Manual
Doc. No. 500-9300007768-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

VMIVME-7700/VME-7700RC VME SBC Product Manual
Doc. No. 500-007700-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

IIOC Family Instruction Manual
Doc. No. 500-009000-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

VMIVME-5550 VME Reflective Memory Product Manual
Doc. No. 500-005550-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

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VMIVME-5565 VME Reflective Memory Product Manual
Doc. No. 500-005565-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

VMIVME-5576 VME Reflective Memory Product Manual
Doc. No. 500-005576-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

VMIVME-5588 VME Reflective Memory Product Manual
Doc. No. 500-005588-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

Physical Description and Specifications

VMIVME-9081 Intelligent I/O Controller Specification
Doc. No. 800-009081-000
Abaco Systems
12090 South Memorial Pkwy.
Huntsville, AL 35803-3308
(800) 322-3616

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture and intended use of this product.

Abaco assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to Abaco for service and repair to ensure that safety features are maintained.

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1 • Handling and Installation

This chapter describes the configuration options available with the VMIVME-9081. The user should carefully read this chapter to ensure the VMIVME-9081 and any host interface board are properly jumpered for the system configuration required.

The VMIVME-9081 IIOC is a functional replacement for the legacy VMIVME-9064/32 and VMIVME-9066/32 IIOCs. The VMIVME-9064/32 uses Reflective Memory as the host interface, and the VMIVME-9066/32 functions as an "embedded" IIOC, residing on the same VMEbus as the host computer. The VMIVME-9081 IIOC functions in both configurations, and also supports Ethernet as a host interface.

After connecting a CRT-based control panel to the serial port on the VMIVME-9081, the user selects one of the three host interface configurations from the Setup Menu. The Setup Menu is shown in *Figure 1-1, IIOC Setup Menu* on page 13.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to Abaco Systems Customer Care.

1.2 Handling Precautions



CAUTION

Some of the components assembled on Abaco products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

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Figure 1-1 IIOC Setup Menu

```
NODE: 1        VMIVME-9081-002-000   Intelligent I/O Controller
                Copyright 2005-2012   Abaco Systems
                          Version 05.05  15 Jun 2012

                                   SETUP MENU

    >>>  SETUP MENU EXIT OPTIONS       Save settings and reboot

         DIGITAL INPUT OPTIONS
           Polarity                    Standard
           Filter Speed                None

         HOST INTERFACE TYPE           Reflective Memory
           RFM Type                    RFM2g - VME-5565
```

1.3 Reflective Memory Host Interface

The VMIVME-9081 IIOC can communicate with a host computer using Abaco's Reflective Memory line of products:

- VMIVME-5550*
- VMIVME-5565*
- VMIVME-5576*
- VMIVME-5588*
- VMIVME-5588DMA*

The VMIVME-9081 is configurable as a functionally equivalent replacement of the VMIVME-9064/32 embedded IIOC. Reflective Memory boards can be ordered and installed in the IIOC master chassis and the host computer.

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Use the Setup Menu to select Reflective Memory as the VMIVME-9081's host interface:

1. Press the ENTER key until the cursor is positioned at SETUP MENU EXIT OPTIONS.
2. Press the SPACE key until Save settings and reboot is selected.
3. Press the ENTER key until the cursor is positioned at HOST INTERFACE TYPE.
4. Press the SPACE key until Reflective Memory is selected as the HOST INTERFACE TYPE.
5. Press the ENTER key until the cursor is positioned at RFM type.
6. Press the SPACE key to select RFM2g* for the VMIVME-5565 Reflective Memory, or RFM1* for VMIVME-5550, VMIVME-5576, VMIVME-5588 or VMIVME-5588DMA Reflective Memory products.
7. Press Control-Z to exit the Setup Menu. The configuration settings are stored in nonvolatile memory.
8. Answer Y to the prompt, “Do you want to reboot the IIOC? [Y/N]” to make the host interface setup take effect.

The host communications interface is a memory-mapped control window with an interrupt protocol. Thus, the interface appears to be locally resident with the host computer. Reflective Memory provides a software transparent interface to the VMIVME-9081 IIOCs from any host computer equipped with its own Reflective Memory. A single host computer can control up to fifteen VMIVME-9081 IIOCs with a single Reflective Memory link. In addition, a VMIVME-9150 Communications Controller is available for use with a VMIVME-9081 system. The VMIVME-9150 assumes much of the work done by the host when controlling and synchronizing multiple VMIVME-9081s.

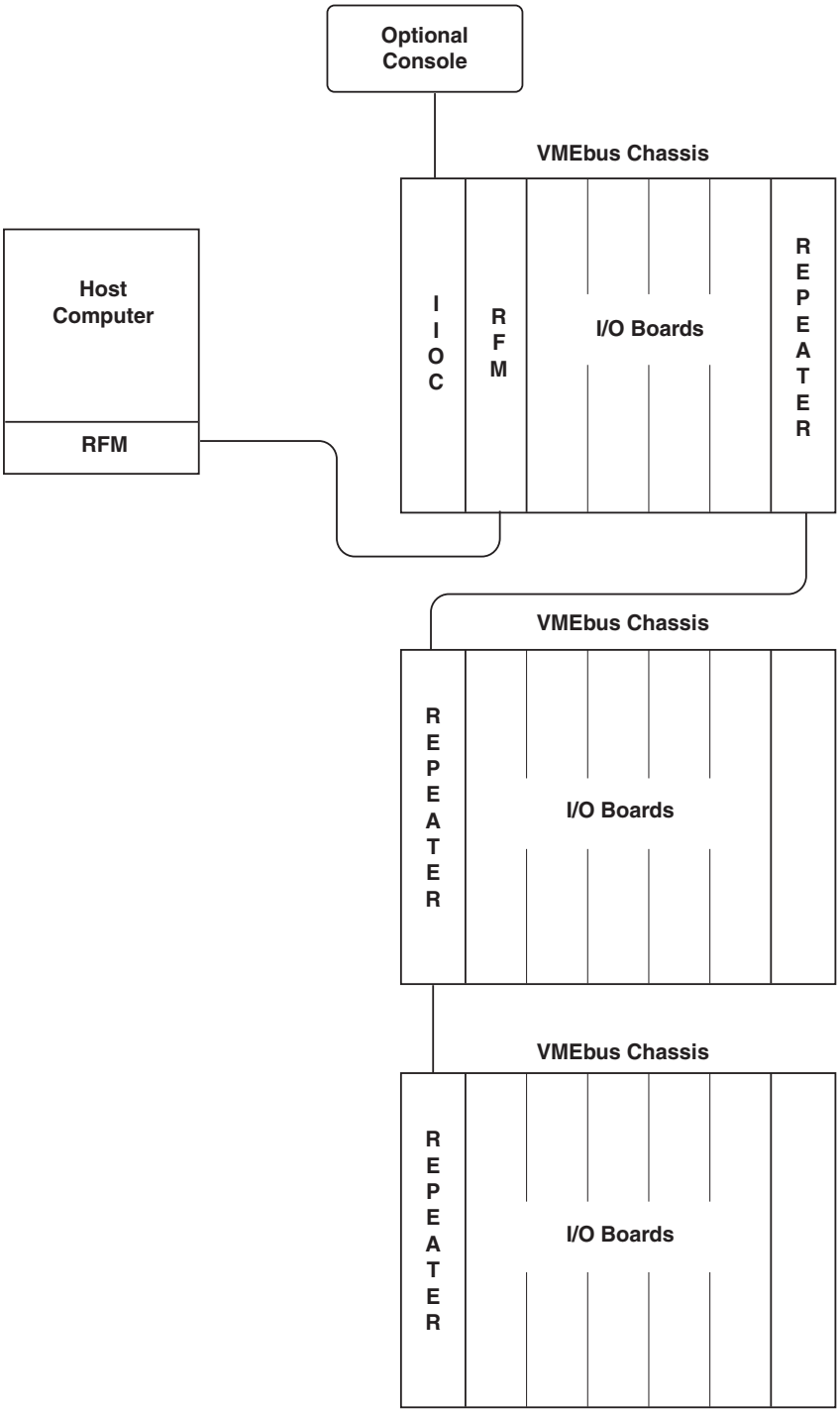
The Reflective Memory used with the VMIVME-9081 IIOC is addressed at 0x7B000000 in the A32 Supervisory Data space.

Each IIOC uses a node ID read from the local Reflective Memory as an index to locate its control window and buffer space. The node ID for the IIOC in a single-node system must be one (1). In multi-node systems, the node ID numbers must be one (1) through n, where n is the number of IIOCs. The node ID number of the Reflective Memory installed in the host computer must not be used by any other node on the network. Each node’s ID on the network must be unique to that particular node. ***Figure 1-2, IIOC System Configuration with Reflective Memory Host Interface*** on page 15 is a block diagram of a VMIVME-9081 IIOC system using a Reflective Memory host interface.

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1.3.1 System Configuration

Figure 1-2 IIOC System Configuration with Reflective Memory Host Interface



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1.4 VMIVME-5550 Reflective Memory

The following tables indicate the factory default jumper settings for the VMIVME-5550 Reflective Memory board as installed in the VMIVME-9081. Five configurations are defined in the following tables. These correspond to five memory size options of 256 KByte, 512 KByte, 1 MByte, 2 MByte, and 4 MByte. Refer to the VMIVME-5550 Product Manual (Doc No. 500-005550-000 available from Abaco) for the location of the jumper fields.

Table 1-1 Default Jumper Settings for a 256 KByte VMIVME-5550

Jumper	Description	Default Configuration
J1	Onboard Memory	1-2: Installed
J2	Onboard Memory	Installed
J3	Onboard Memory	Installed
J4	Onboard Memory	1-2: Installed
J6	AP20	Installed
J7	AP21	Installed
J8	AP19 AP18 A23 A22 A21 A20 A19 A18	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Installed
J9	Node ID (Node 1), Max Node ID (unused)	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Omitted
J10	Address Modifier = Supervisory	Omitted
J11	VME Addressing Mode = Extended	Installed
J12	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J13	Speed Selection = 20 MByte/s forceable length less than or equal to 50 ft.	Installed
J14	SRAM Decode	1-2: Installed
J15	SRAM Decode	1-2: Installed
J16	Link Reset Mode = Reset FIFO Only (Mode D)	Installed

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Table 1-1 Default Jumper Settings for a 256 KByte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J17	Extended Address = 7B	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J18	Memory Selection	Omitted
J19	Memory Selection	Omitted
J20	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

Table 1-2 Default Jumper Settings for a 512 KByte VMIVME-5550

Jumper	Description	Default Configuration
J1	Onboard Memory	1-2: Installed
J2	Onboard Memory	Installed
J3	Onboard Memory	Omitted
J4	Onboard Memory	1-2: Installed
J6	AP20	Installed
J7	AP21	Installed
J8	AP19 AP18 A23 A22 A21 A20 A19 A18	1-2: Installed 3-4: Omitted 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Omitted
J9	Node ID (Node 1), Max Node ID (unused)	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Omitted
J10	Address Modifier = Supervisory	Omitted
J11	VME Addressing Mode = Extended	Installed
J12	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J13	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed

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Table 1-2 Default Jumper Settings for a 512 KByte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J14	SRAM Decode	1-2: Installed
J15	SRAM Decode	1-2: Installed
J16	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
J17	Extended Address = 7B	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J18	Memory Selection	Omitted
J19	Memory Selection	Omitted
J20	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

Table 1-3 Default Jumper Settings for a 1 MByte VMIVME-5550

Jumper	Description	Default Configuration
J1	Onboard Memory	1-2: Installed
J2	Onboard Memory	Omitted
J3	Onboard Memory	Omitted
J4	Onboard Memory	1-2: Installed
J6	AP20	Installed
J7	AP21	Installed
J8	AP19 AP18 A23 A22 A21 A20 A19 A18	1-2: Omitted 3-4: Omitted 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Omitted 15-16: Omitted
J9	Node ID (Node 1), Max Node ID (unused)	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Omitted
J10	Address Modifier = Supervisory	Omitted
J11	VME Addressing Mode = Extended	Installed

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Table 1-3 Default Jumper Settings for a 1 MByte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J12	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J13	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J14	SRAM Decode	1-2: Installed
J15	SRAM Decode	1-2: Installed
J16	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
J17	Extended Address = 7B	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J18	Memory Selection	Omitted
J19	Memory Selection	Omitted
J20	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

Table 1-4 Default Jumper Settings for a 2 MByte VMIVME-5550

Jumper	Description	Default Configuration
J1	Onboard Memory	2-3: Installed
J2	Onboard Memory	Installed
J3	Onboard Memory	Omitted
J4	Onboard Memory	2-3: Installed
J6	AP20	Omitted
J7	AP21	Installed
J8	AP19 AP18 A23 A22 A21 A20 A19 A18	1-2: Omitted 3-4: Omitted 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Omitted 13-14: Omitted 15-16: Omitted

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Table 1-4 Default Jumper Settings for a 2 MByte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J9	Node ID (Node 1), Max Node ID (unused)	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Omitted
J10	Address Modifier = Supervisory	Omitted
J11	VME Addressing Mode = Extended	Installed
J12	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J13	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J14	SRAM Decode	2-3: Installed
J15	SRAM Decode	2-3: Installed
J16	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
J17	Extended Address = 7B	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J18	Memory Selection	Installed
J19	Memory Selection	Installed
J20	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

Table 1-5 Default Jumper Settings for a 4 MByte VMIVME-5550

Jumper	Description	Default Configuration
J1	Onboard Memory	2-3: Installed
J2	Onboard Memory	Omitted
J3	Onboard Memory	Omitted
J4	Onboard Memory	2-3: Installed
J6	AP20	Omitted
J7	AP21	Omitted

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Table 1-5 Default Jumper Settings for a 4 MByte VMIVME-5550 (Continued)

Jumper	Description	Default Configuration
J8	AP19 AP18 A23 A22 A21 A20 A19 A18	1-2: Omitted 3-4: Omitted 5-6: Installed 7-8: Installed 9-10: Omitted 11-12: Omitted 13-14: Omitted 15-16: Omitted
J9	Node ID (Node 1), Max Node ID (unused)	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Omitted
J10	Address Modifier = Supervisory	Omitted
J11	VME Addressing Mode = Extended	Installed
J12	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J13	Speed Selection = 20 MByte/s for cable length less than or equal to 50 ft.	Installed
J14	SRAM Decode	2-3: Installed
J15	SRAM Decode	2-3: Installed
J16	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
J17	Extended Address = 7B	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J18	Memory Selection	Installed
J19	Memory Selection	Installed
J20	Link Reset Mode = Reset FIFO Only (Mode D)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

1.5 VMIVME-5565 Reflective Memory

The VMIVME-5565 is configured for Small Memory Mode when used in an IIOC system. In this configuration, 512 KByte of SDRAM is available. The first SDRAM memory address is fixed at offset 0x3000 from the base address of the board. ***Table 1-6*** below indicates the factory default settings for the VMIVME-5565 Reflective

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Memory board as installed in the VMIVME-9081. Refer to the VMIVME-5565 Product Manual (Doc No. 500-005565-000 available from Abaco) for the locations of the switches and jumpers field.

Table 1-6 Default Switch and Jumper Settings for VMIVME-5565

Switch/Jumper	Description	Default Configuration
Switch S2	Small Memory Mode (512 KByte, registers inside the memory area)	1: On 2: Off 3: On 4: On 5: On 6: Off 7: Off 8: Off
Switch S3	Standard Address Field (A23-A16)	All On
Switch S4	Register Set (A32 Supervisory)	1: On 2: Off 3: On 4: Off 5: Off 6: Off 7: On 8: On
Switch S5	Not used	All Off
Switch S6	Node ID (Node 1)	1: Off 2: On 3: On 4: On 5: On 6: On 7: On 8: On
Switch S7	Extended Address Field (A32-A24, 0x7B000000)	1: Off 2: Off 3: On 4: Off 5: Off 6: Off 7: Off 8: On
Switch S8	Not used	All Off
Jumper E5	Fast Mode (Fast Mode enabled, Rogue Master Disabled)	1-2: Installed 3-4: Installed 5-6: Installed 7-8: Omitted

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1.6 VMIVME-5576 Reflective Memory

Table 1-7, *Table 1-8* on page 24 and *Table 1-9* on page 25 illustrate the factory default jumper settings for the VMIVME-5576 Reflective Memory board installed in the VMIVME-9081. Three memory options of 256 KByte, 512 KByte and 1 MByte are defined in the tables. Refer to the VMIVME-5576 Product Manual (Doc No. 500-005576-000 available from Abaco) for the location of the jumper fields.

Table 1-7 Default Jumper Settings for a 256 KByte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	Installed
J2	Address Pass Through Field - Depth 2	Installed
J3	Mask Field (INT0 Transfer Error Interrupt Enabled)	Installed
J4	Extended Address Jumper Field A31-A24 (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J5	Link Speed Selection (6.2 MByte)	Omitted
J6	Spare	Omitted
J7	Standard Address Jumper Field (0x000000)	AP19: Installed AP18: Installed A23: Installed A22: Installed A21: Installed A20: Installed A19: Installed A18: Installed
J8	Address Mode (Supervisory)	Omitted
J9	Node ID (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
J10	Standard/Extended Address Selection (Extended)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

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Table 1-8 Default Jumper Settings for a 512 KByte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	Installed
J2	Address Pass Through Field - Depth 2	Omitted
J3	Mask Field (INT0 Transfer Error Interrupt Enabled)	Installed
J4	Extended Address Jumper Field A31-A24 (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J5	Link Speed Selection (6.2 MByte)	Omitted
J6	Spare	Omitted
J7	Standard Address Jumper Field (0x000000)	AP19: Installed AP18: Omitted A23: Installed A22: Installed A21: Installed A20: Installed A19: Installed A18: Omitted
J8	Address Mode (Supervisory)	Omitted
J9	Node ID (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
J10	Standard/Extended Address Selection (Extended)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

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Table 1-9 Default Jumper Settings for a 1 MByte VMIVME-5576

Jumper	Description	Default Configuration
J1	Address Pass Through Field - Depth 1	Omitted
J2	Address Pass Through Field - Depth 2	Omitted
J3	Mask Field (INT0 Transfer Error Interrupt Enabled)	Installed
J4	Extended Address Jumper Field A31-A24 (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
J5	Link Speed Selection (6.2 MByte)	Omitted
J6	Spare	Omitted
J7	Standard Address Jumper Field (0x000000)	AP19: Omitted AP18: Omitted A23: Installed A22: Installed A21: Installed A20: Installed A19: Omitted A18: Omitted
J8	Address Mode (Supervisory)	Omitted
J9	Node ID (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
J10	Standard/Extended Address Selection (Extended)	Installed
A1	Address Line	Installed
A2	Address Line	Installed
A3	Address Line	Installed

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1.7 VMIVME-5588 Reflective Memory

Table 1-10 through *Table 1-14* illustrate the factory default jumper settings for the VMIVME-5588 Reflective Memory board installed in the VMIVME-9081. Five memory configurations are defined and correspond to five memory options available (256 KByte, 512 KByte, 1 MByte, 2 MByte and 4 MByte) for the VMIVME-5588. Refer to the VMIVME-5588 Product Manual (Doc No. 500-005588-000 available from Abaco) for the location of the jumper fields.

Table 1-10 Default Jumper Settings for a 256 KByte VMIVME-5588

Jumper	Description	Default Configuration
E1	Extended Address Field	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E2	Extended Address Jumper	Installed
E3	Address Modifier Select	Omitted
E4	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Installed A19: Installed A18: Installed
E5	Link SYSRESET Enable	Omitted
E6	Fast Field	Installed
E7	Mask Field	Omitted
E8	Optical Relay Bit (P2) Disconnect	Omitted
E9	Board Node ID Field (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
E10	Loop-Back Enable	Omitted

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Table 1-11 Default Jumper Settings for a 512 KByte VMIVME-5588

Jumper	Description	Default Configuration
E1	Extended Address Field	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E2	Extended Address Jumper	Installed
E3	Address Modifier Select	Omitted
E4	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Installed A19: Installed A18: Omitted
E5	Link SYSRESET Enable	Omitted
E6	Fast Field	Installed
E7	Mask Field	Omitted
E8	Optical Relay Bit (P2) Disconnect	Omitted
E9	Board Node ID Field (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
E10	Loop-Back Enable	Omitted

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Table 1-12 Default Jumper Settings for a 1 MByte VMIVME-5588

Jumper	Description	Default Configuration
E1	Extended Address Field	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E2	Extended Address Jumper	Installed
E3	Address Modifier Select	Omitted
E4	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Installed A19: Omitted A18: Omitted
E5	Link SYSRESET Enable	Omitted
E6	Fast Field	Installed
E7	Mask Field	Omitted
E8	Optical Relay Bit (P2) Disconnect	Omitted
E9	Board Node ID Field (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
E10	Loop-Back Enable	Omitted

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Table 1-13 Default Jumper Settings for a 2 MByte VMIVME-5588

Jumper	Description	Default Configuration
E1	Extended Address Field	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E2	Extended Address Jumper	Installed
E3	Address Modifier Select	Omitted
E4	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Omitted A19: Omitted A18: Omitted
E5	Link SYSRESET Enable	Omitted
E6	Fast Field	Installed
E7	Mask Field	Omitted
E8	Optical Relay Bit (P2) Disconnect	Omitted
E9	Board Node ID Field (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
E10	Loop-Back Enable	Omitted

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Table 1-14 Default Jumper Settings for a 4 MByte VMIVME-5588

Jumper	Description	Default Configuration
E1	Extended Address Field	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E2	Extended Address Jumper	Installed
E3	Address Modifier Select	Omitted
E4	Standard Address Field	A23: Installed A22: Installed A21: Omitted A20: Omitted A19: Omitted A18: Omitted
E5	Link SYSRESET Enable	Omitted
E6	Fast Field	Installed
E7	Mask Field	Omitted
E8	Optical Relay Bit (P2) Disconnect	Omitted
E9	Board Node ID Field (Node 1)	ID7: Installed ID6: Installed ID5: Installed ID4: Installed ID3: Installed ID2: Installed ID1: Installed ID0: Omitted
E10	Loop-Back Enable	Omitted

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1.8 VMIVME-5588DMA Reflective Memory

The following tables indicate the factory default jumper settings for the VMIVME-5588DMA Reflective Memory board as installed in the VMIVME-9081. Five configurations are defined in the following tables. These correspond to five memory size options of 256 KByte, 512 KByte, 1 MByte, 2 MByte and 4 MByte. Refer to the VMIVME-5588DMA Product Manual (Doc No. 500-105588-000 available from Abaco) for the location of the jumper fields.

Table 1-15 Default Jumper Settings for a 256 KByte VMIVME-5588DMA

Jumper	Description	Default Configuration
E2	Loop-Back Enable	Installed
E3	Optical Relay Bit (P2) Disconnect	Omitted
E4	Rogue Packet Elimination	Omitted
E18	Extended Address Jumper	Installed
E19	Link SYSRESET Enable	Omitted
E20	Address Modifier Select	Omitted
E36	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Installed A19: Installed A18: Installed
E37	Extended Address Field (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E38	Fast Field	Installed
E39	Data Error Mask Field	Omitted
E40	Transmitter Half-Full Mask Field	Omitted
E42	Board Node ID Field (Node 1)	1-2: Omitted 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Installed
E43	VMEbus Time-Out Enable	Omitted

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Table 1-16 Default Jumper Settings for a 512 KByte VMIVME-5588DMA

Jumper	Description	Default Configuration
E2	Loop-Back Enable	Installed
E3	Optical Relay Bit (P2) Disconnect	Omitted
E4	Rogue Packet Elimination	Omitted
E18	Extended Address Jumper	Installed
E19	Link SYSRESET Enable	Omitted
E20	Address Modifier Select	Omitted
E36	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Installed A19: Installed A18: Omitted
E37	Extended Address Field (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E38	Fast Field	Installed
E39	Data Error Mask Field	Omitted
E40	Transmitter Half-Full Mask Field	Omitted
E42	Board Node ID Field (Node 1)	1-2: Omitted 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Installed
E43	VMEbus Time-Out Enable	Omitted

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Table 1-17 Default Jumper Settings for a 1 MByte VMIVME-5588DMA

Jumper	Description	Default Configuration
E2	Loop-Back Enable	Installed
E3	Optical Relay Bit (P2) Disconnect	Omitted
E4	Rogue Packet Elimination	Omitted
E18	Extended Address Jumper	Installed
E19	Link SYSRESET Enable	Omitted
E20	Address Modifier Select	Omitted
E36	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Installed A19: Omitted A18: Omitted
E37	Extended Address Field (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E38	Fast Field	Installed
E39	Data Error Mask Field	Omitted
E40	Transmitter Half-Full Mask Field	Omitted
E42	Board Node ID Field (Node 1)	1-2: Omitted 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Installed
E43	VMEbus Time-Out Enable	Omitted

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Table 1-18 Default Jumper Settings for a 2 MByte VMIVME-5588DMA

Jumper	Description	Default Configuration
E2	Loop-Back Enable	Installed
E3	Optical Relay Bit (P2) Disconnect	Omitted
E4	Rogue Packet Elimination	Omitted
E18	Extended Address Jumper	Installed
E19	Link SYSRESET Enable	Omitted
E20	Address Modifier Select	Omitted
E36	Standard Address Field	A23: Installed A22: Installed A21: Installed A20: Omitted A19: Omitted A18: Omitted
E37	Extended Address Field (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E38	Fast Field	Installed
E39	Data Error Mask Field	Omitted
E40	Transmitter Half-Full Mask Field	Omitted
E42	Board Node ID Field (Node 1)	1-2: Omitted 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Installed
E43	VMEbus Time-Out Enable	Omitted

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Table 1-19 Default Jumper Settings for a 4 MByte VMIVME-5588DMA

Jumper	Description	Default Configuration
E2	Loop-Back Enable	Installed
E3	Optical Relay Bit (P2) Disconnect	Omitted
E4	Rogue Packet Elimination	Omitted
E18	Extended Address Jumper	Installed
E19	Link SYSRESET Enable	Omitted
E20	Address Modifier Select	Omitted
E36	Standard Address Field	A23: Installed A22: Installed A21: Omitted A20: Omitted A19: Omitted A18: Omitted
E37	Extended Address Field (0x7B)	A31: Installed A30: Omitted A29: Omitted A28: Omitted A27: Omitted A26: Installed A25: Omitted A24: Omitted
E38	Fast Field	Installed
E39	Data Error Mask Field	Omitted
E40	Transmitter Half-Full Mask Field	Omitted
E42	Board Node ID Field (Node 1)	1-2: Omitted 3-4: Installed 5-6: Installed 7-8: Installed 9-10: Installed 11-12: Installed 13-14: Installed 15-16: Installed
E43	VMEbus Time-Out Enable	Omitted

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1.9 Ethernet Host Interface

The VMIVME-9081 IIOC supports Ethernet as a host interface, using TCP/IP as the protocol. At bootup, the IIOC will initialize a server socket that listens for a connect attempt initiated by the host computer.



NOTE

The TCP/IP protocol guarantees data delivery, but not the speed of the data transfer. It is normal for data transfers to sometimes take hundreds of milliseconds. This interface is not recommended unless I/O buffer transfer timing is not required to be deterministic. For best performance when using the Ethernet host interface, use a peer to peer connection between the IIOC and the host computer.

Use the Setup Menu to select Ethernet as the VMIVME-9081's host interface.

1. Press the ENTER key until the cursor is positioned at SETUP MENU EXIT OPTIONS.
2. Press the SPACE key until Save settings and reboot is selected.
3. Press the ENTER key until the cursor is positioned at HOST INTERFACE TYPE.
4. Press the SPACE key until Ethernet is selected as the HOST INTERFACE TYPE.
5. Press the ENTER key until the cursor is positioned at IP Address. Enter an IP address, such as 192.168.0.10.
6. Press the ENTER key until the cursor is positioned at Port Number. Enter a port number, or accept the default value of 9081.
7. Press the ENTER key until the cursor is positioned at Send Buffer Size. Enter a size (in bytes), or accept the default value of 8192.
8. Press the ENTER key until the cursor is positioned at Recv Buffer Size. Enter a size (in bytes), or accept the default value of 8192.
9. Press the ENTER key until the cursor is positioned at Connection Reset. This setting determines when the IIOC resets the Ethernet connection following a period of time with no interaction from the host computer. Press the SPACE key to select Never, 5 seconds, 30 seconds, or 60 seconds.
10. Press Control-Z to exit the Setup Menu. The configuration settings are stored in nonvolatile memory.
11. Answer Y to the prompt, "Do you want to reboot the IIOC? [Y/N]" to make the host interface setup take effect.



NOTE

The IIOC's IP Address is a static address. Dynamic Host Configuration Protocol (DHCP) is NOT supported.

The IP address chosen for the IIOC must correspond to the address of the Ethernet adapter installed in the host computer. For example, if the Ethernet adapter in the host computer has a TCP/IP address of 192.168.0.1 and a subnet mask of 255.255.255.0, a valid address for the IIOC would be 192.168.0.10.



NOTE

The LAN1 connector on the VMIVME-9081 front panel is used for the Ethernet host interface.

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Figure 1-3 Ethernet Host Interface IIOC Setup Menu

```
              VMIVME-9081-002-000   Intelligent I/O Controller
               Copyright 2005-2012   Abaco Systems
                         Version 05.05  15 Jun 2012

                                  SETUP MENU

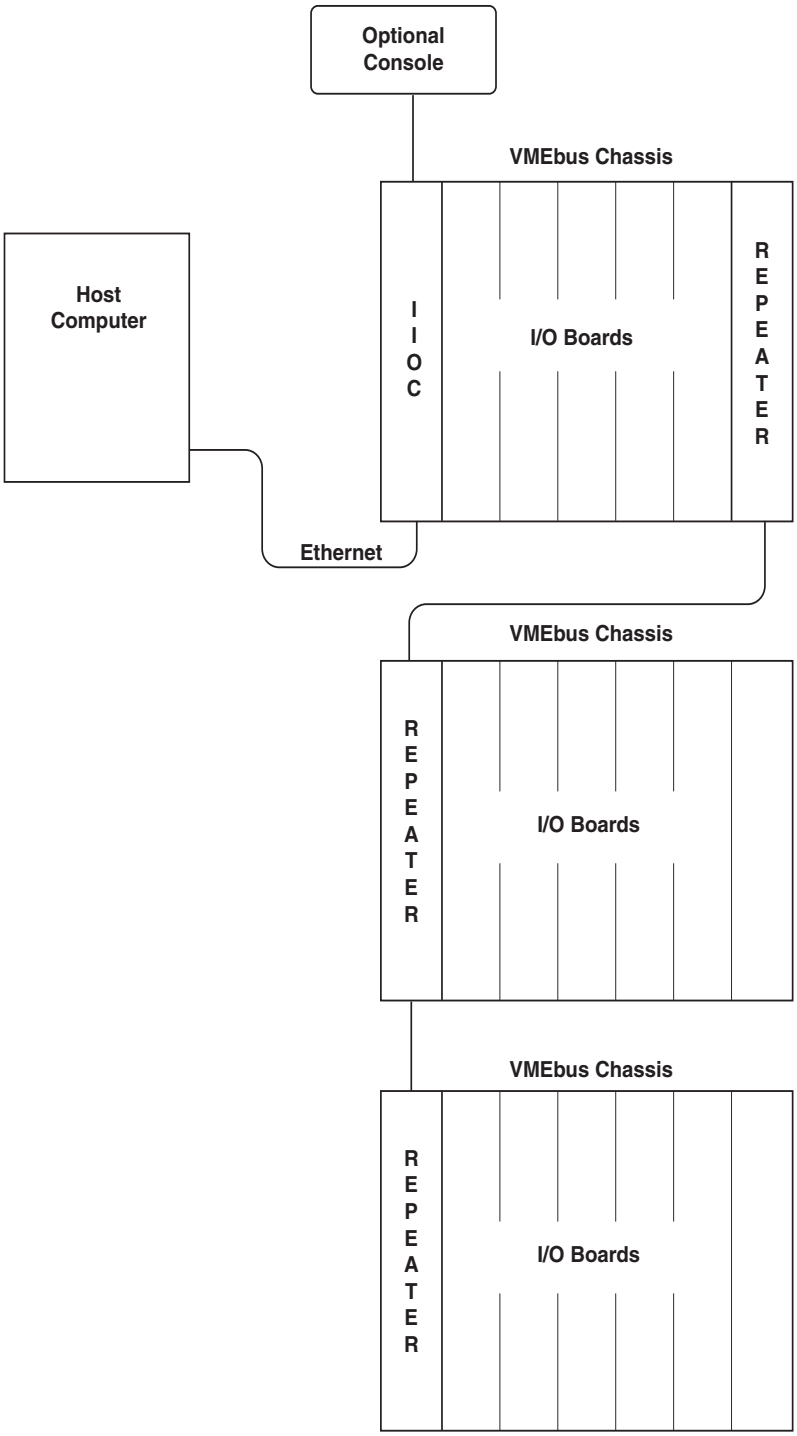
>>>  SETUP MENU EXIT OPTIONS       Save settings and reboot

     DIGITAL INPUT OPTIONS
       Polarity                   Standard
       Filter Speed               None

     HOST INTERFACE TYPE          Ethernet
       Ethernet Options
         IP Address               192.168.0.50
         Port Number              9081
         Send Buffer Size         8192
         Recv Buffer Size         8192
         Connection Reset         Never
```


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Figure 1-4 IIOC System Configuration with Host Ethernet Interface



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1.10 Embedded IIOC

A VMEbus system contains only one system controller board that resides in slot one of the VMEbus backplane. When the VMIVME-9081 is configured as an Embedded IIOC, it is typically not the system controller and does not reside in slot one. The host computer is usually a VMEbus single board computer and serves as the system controller. From the host computer's perspective, the Embedded IIOC appears as a RAM board on the VMEbus. The user may specify the base address at which the IIOC appears on the VMEbus. Other VMEbus parameters are specified to provide maximum flexibility between the IIOC and the host computer.

The Embedded IIOC shares a portion of its local RAM to the VMEbus. The shared RAM is visible to the host computer at a default base address of 0xF40C0000 in A32 Supervisory space. The user may change this default base VMEbus address on the IIOC via the Setup Menu.

In the Setup Menu, the default base address is shown as 0xF4000000, not 0xF40C0000. The Embedded IIOC adds an offset of 0x000C0000 to the base address chosen by the user. The 0x000C0000 offset is necessary to maintain backward compatibility with the legacy VMIVME-9066 Embedded IIOC.

When setting the base VMEbus address of the IIOC, the user is allowed to change only the most significant byte of the address, for example, changing from 0xF4000000 to 0x55000000.

The default base address of 0xF4000000 is also specified in the IIOC Host Software Support Package installed on the host computer. If the base address is changed on the VMIVME-9081, the Host Software must be adjusted to use the new base address.

In addition to the shared RAM, the host computer uses Mailbox Interrupts to communicate with the Embedded IIOC. The Mailbox Interrupt Register on the VMIVME-9081 appears at an A16 VMEbus address. The host computer writes to this address to generate an interrupt on the VMIVME-9081.

By default, the VMIVME-9081's Mailbox Interrupt Register is at address 0xF348 in A16 Nonprivileged space. The user may change the address of the Mailbox Interrupt Register via the Setup Menu. Only the most significant four bits of the address may be changed, for example changing from 0xF348 to 0xC348.



NOTE

When the address of the Mailbox Interrupt Register is changed to a value lower than the default of 0xF348, the VMIVME-9081 must give up A16 address space normally reserved for I/O boards by reducing the maximum chassis number. In most systems this address is unused. The following table shows the valid Mailbox Interrupt Register addresses and the corresponding maximum chassis numbers:

Table 1-20 Mailbox Interrupt Register

Address of Mailbox Interrupt Register	Maximum Chassis
0xF348 (default)	12
0xE348	11
0xD348	10

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Table 1-20 Mailbox Interrupt Register (Continued)

Address of Mailbox Interrupt Register	Maximum Chassis
0xC348	10 (this address also limits Max Chassis to 10)
0xB348	9
0xA348	8
0x9348	7
0x8348	6

The default Mailbox Interrupt Register address of 0xF348 is also specified in the IIOC Host Software Support Package installed on the host computer. If the Mailbox Interrupt Register address is changed on the VMIVME-9081, the Host Software must be adjusted to use the new address.

Use the Setup Menu to configure the VMIVME-9081 as an embedded IIOC. ***Figure 1-5, Embedded IIOC Setup Menu*** on page 42 shows the user-selected options for the Embedded IIOC configuration.

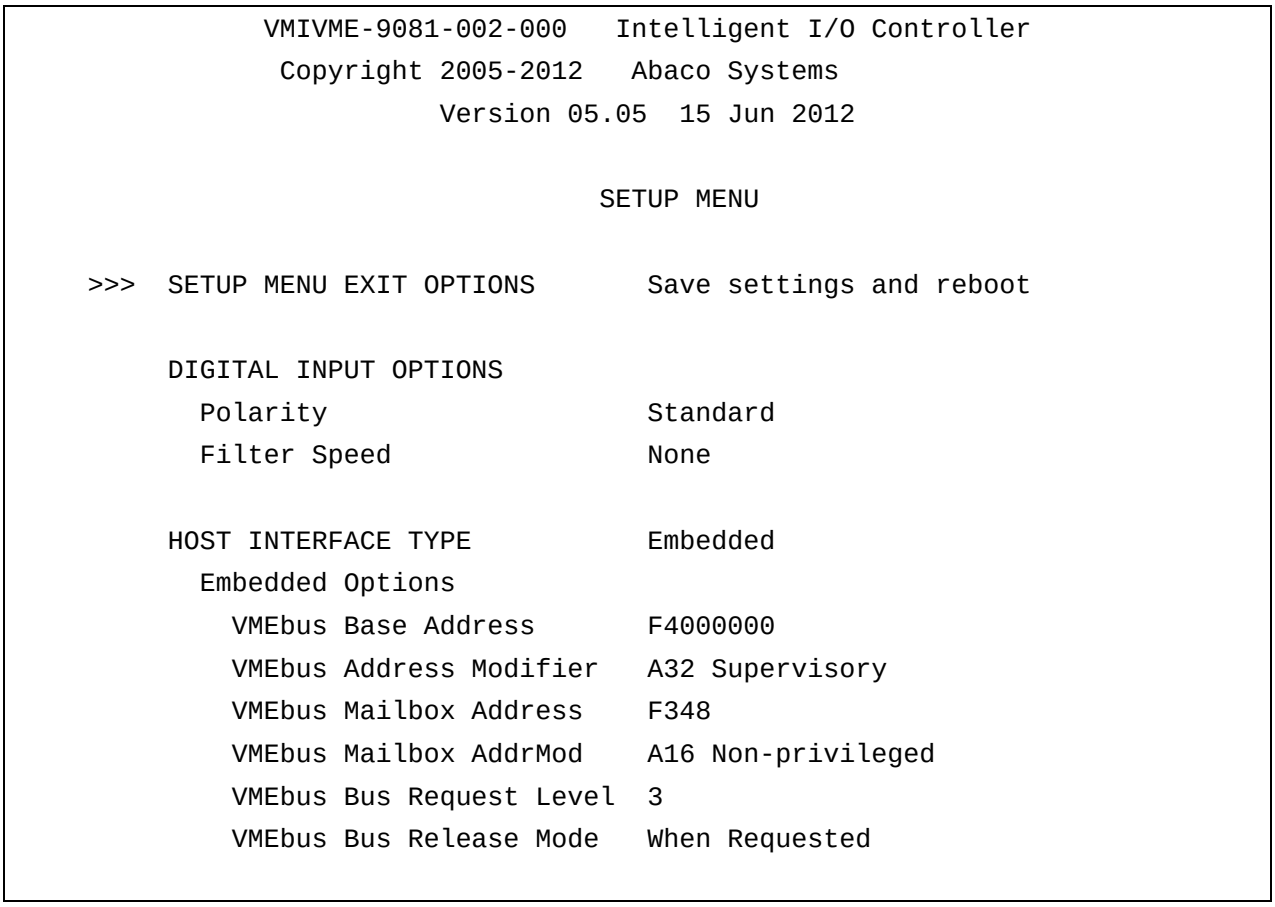
1. Press the ENTER key until the cursor is positioned at SETUP MENU EXIT OPTIONS.
2. Press the SPACE key until the Save settings and reboot is selected.
3. Press the ENTER key until the cursor is positioned at HOST INTERFACE TYPE.
4. Press the SPACE key until Embedded is selected as the HOST INTERFACE TYPE.
5. Press the ENTER key until the cursor is positioned at VMEbus Base Address. The VMIVME-9081 appears as a RAM board on the VMEbus at a user-specified A32 address. The user may specify only the upper byte of this address, i.e. address bits A31 through A24. Any 8-digit hexadecimal value can be used for the A32 address. The shared memory region of the VMIVME-9081 (local RAM visible to the VMEbus) begins at this A32 base address.
6. Press the ENTER key until the cursor is positioned at VMEbus Address Modifier. The VMIVME-9081 will respond to two VMEbus address modifiers: A32 Supervisory Data and A32 Nonprivileged Data. The user can select A32 Supervisory, A32 Nonprivileged, or both A32 Supervisory and Nonprivileged. The factory default is A32 Supervisory.
7. Press the ENTER key until the cursor is positioned at VMEbus Mailbox Address. The user may specify one of the Mailbox Interrupt Register addresses shown in the table above.
8. Press the ENTER key until the cursor is positioned at VMEbus Mailbox AddrMod. The VMIVME-9081's Mailbox Interrupt will respond to two VMEbus address modifiers: A16 Supervisory Data and A16 Nonprivileged Data. The user can select A16 Supervisory, A16 Nonprivileged, or both A16 Supervisory and Nonprivileged. The factory default is A16 Nonprivileged.
9. Press the ENTER key until the cursor is positioned at VMEbus Bus Request Level. The VMIVME-9081 provides four levels (0, 1, 2 or 3) of master bus request. The level selected for the IIOC should be determined from the characteristics of the system in which the IIOC is installed and the bus arbitration method used. The factory default is Level 3 bus request master.

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10. Press the ENTER key until the cursor is positioned at VMEbus Bus Release Mode. The VMIVME-9081 provides two bus release functions to arbitrate VMEbus mastership:
    - When Requested - This mode enables the IIOC to retain VMEbus bus mastership once it becomes master, until it detects a VMEbus request from another master. This relieves the IIOC from having to arbitrate for the VMEbus each time a VMEbus cycle is required. If no other master has requested the bus since the IIOC became master, the IIOC remains VMEbus master and avoids the bus arbitration time. The Release When Requested mode is the factory default release mode.
    - When Done - This mode causes a release of VMEbus mastership after the initiated transfer cycle has been completed. The IIOC must successfully gain VMEbus mastership for each transfer cycle. Abaco does not recommend the use of this release mode in an IIOC system.
11. Press the ENTER key until the cursor is positioned at the VMEbus Fair Mode. Fair Mode causes a VMEbus requestor to wait until the designated signal line for the selected request level is inactive before requesting the VMEbus. By default, the VMIVME-9081's Fair Mode is OFF.
12. Press the ENTER key until the cursor is positioned at VMEbus Arbitration Mode. The VMIVME-9081 provides two arbitration modes: Round Robin and Priority. These arbitration modes are used only when the IIOC is serving as the system controller.
    - Round Robin - This arbitration mode grants bus masters access to the VMEbus on a rotating priority basis. When the bus is granted to a master on bus request level BR(n), the highest priority for the next arbitration is assigned to bus request BR(n-1). This method of arbitration ensures that all requesting masters are given access to the bus in a timely fashion. Round Robin is the factory default.
    - Priority - This arbitration mode grants bus access to masters according to a fixed priority scheme. Bus request level 3 always has highest priority with decreasing priority to bus request level 0, which has the lowest priority. In a multimaster system, this method of arbitration may "starve" a master. Bus loading may become a factor to such an extent that a low bus request master may never be granted access to the bus. Abaco does not recommend the use of this arbitration method in an IIOC system.
13. Press Control-Z to exit the Setup Menu. The configuration settings are stored in nonvolatile memory.
14. Answer Y to the prompt, "Do you want to reboot the IIOC? [Y/N]" to make the host interface setup take effect.

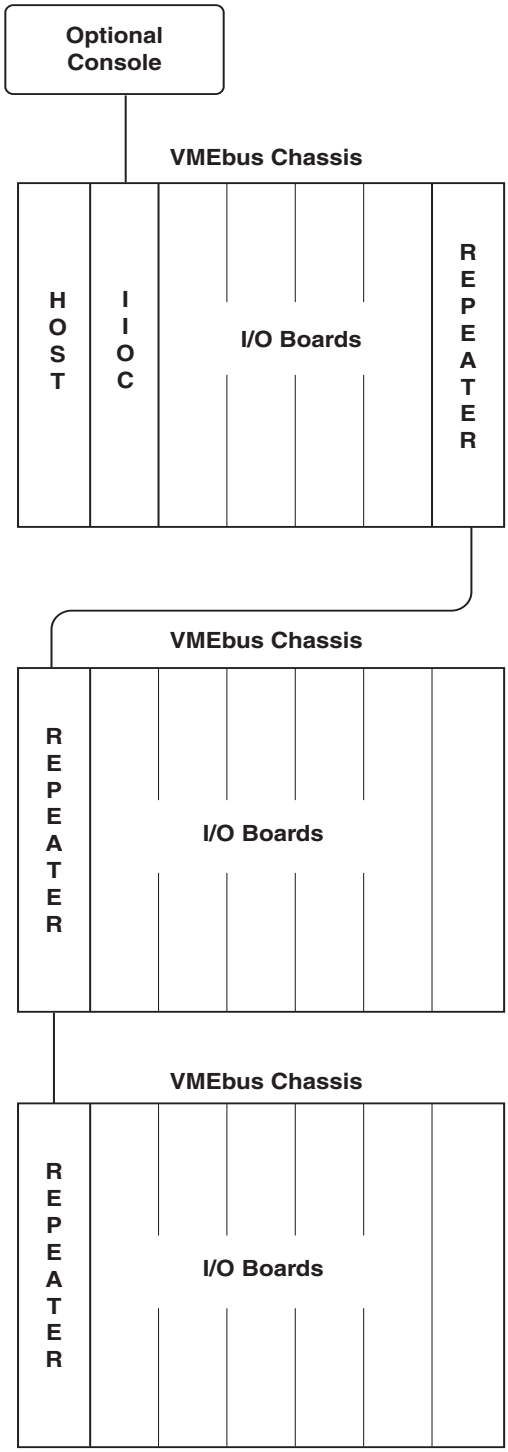
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Figure 1-5 Embedded IIOC Setup Menu



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Figure 1-6 Embedded IIOC System Configuration



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1.11 VMIVME-7700 Single Board Computer

The VMIVME-9081-001 IIOC consists of a VMIVME-7700-111-000 or VME-7700RC-111-000 Single Board Computer (SBC) preloaded with IIOC firmware.

The VMIVME-7700/VME-7700RC SBC is based on the Intel ultra low voltage Celeron processor. The enhanced Celeron processor has 256 KByte of on-die L2 cache. The thermal characteristics of the VMIVME-7700/VME-7700RC are well suited for embedded systems operating over a wide range of temperatures. The VMIVME-7700/VME-7700RC has 128 MByte of PC-100 memory, a 128 MByte CompactFlash memory containing the IIOC-CC firmware and operating system kernel, and front panel Ethernet and Serial ports. The VMEbus interface is based on the Newbridge/Tundra Universe IID high performance PCI-to-VMEbus interface.

The VMIVME-7700/VME-7700RC is tested for system operation and shipped with factory-installed jumpers. The physical location of the jumpers, switches and connectors for the SBC are illustrated in ***Figure 1-7, Jumper and Switch Locations for non-RoHS VMIVME-7700 (Assy. No. 332-007700)*** on page 45 and ***Figure 1-8, Jumper and Switch Locations for RoHS VME-7700RC (Assy. No. 332-9301007700)*** on page 48. The definitions of the SBC jumpers and connectors are included in ***Table 1-21*** on page 46 through ***Table 1-34*** on page 49.



NOTE

The VMIVME-9081-001 IIOC does not use all the features of the VMIVME-7700/VME-7700RC SBC.

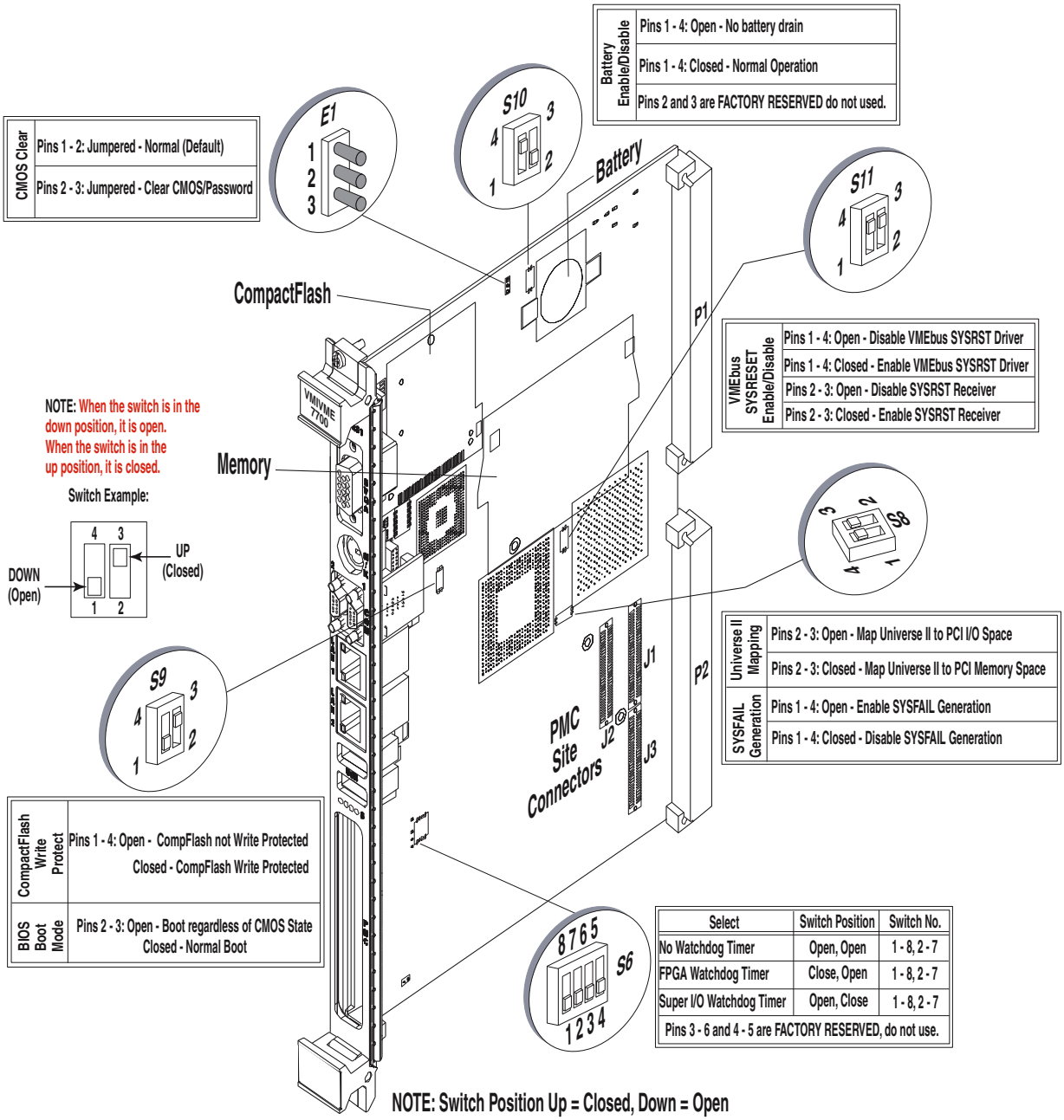


CAUTION

All jumpers and switches marked *User Configurable* in the following tables can be changed or modified by the user. The user should not modify jumpers marked *Factory Configured.* Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in damage to the unit. Modifying jumpers or switches not marked *User Configurable* will void the Warranty and may damage the unit. The default configuration of the VMIVME-7700/VME-7700RC for use as a VMIVME-9081-001 is expressed in ***Table 1-21*** on page 46 through ***Table 1-34*** on page 49 with bold text in the table cells.

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Figure 1-7 Jumper and Switch Locations for non-RoHS VMIVME-7700 (Assy. No. 332-007700)



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Table 1-21 Board Connectors and Headers for non-RoHS VMIVME-7700

Connector	Function
J7	*Mouse/Keyboard
J4, J5	Ethernet Ports 1 & 2*
P2	IDE (PRI)*, Floppy*
J8, J10	USB Connectors*
J9	Video*
E2, E4, E5, E6, E9, E10, E18	Factory Reserved DO NOT USE
E17	I^2C Header*
E1	CMOS Clear
J1, J2, J3	PMC Site Connectors
P4	CompactFlash Connector
P1, P2	VMEbus Backplane Connectors
* The connectors are not used by the IIOC.	

The VMIVME-7700's BIOS has the capability of password protecting casual access to the unit's CMOS set-up screens. This feature is disabled by default. The Password Clear jumper allows the user to clear the password in the case of a forgotten password.

To clear the CMOS password:

1. Turn off power to the unit.
2. Momentarily short the pins of E1 for approximately five seconds.
3. Power up the unit.

When power is reapplied to the unit, the CMOS password will be cleared.

Table 1-22 Non-RoHS VMIVME-7700 CMOS Clear (**User Configurable**) - Jumper (E1)

Select	Jumper Pin Positions
Normal	1-2
Clear CMOS/Password	2-3

Table 1-23 Non-RoHS VMIVME-7700 Watchdog Timer (**Factory Configurable**) - Switch (S6)

Select	Switch Position	Switch No.
No Watchdog Timer	Off, Off	1-8, 2-7
FPGA Watchdog Timer	On, Off	1-8, 2-7
Super I/O Watchdog Timer	Off, On	1-8, 2-7
Factory Reserved		3-6, 4-5

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Table 1-24 Non-RoHS VMIVME-7700 Universe II Mapping, SYSFAIL Generation (**Factory Configurable**) - Switch (S8)

Select	Switch Position	Switch No.
Map UNIV2 to PCI I/O Space	Off	1-4
Map UNIV2 to PCI Memory Space	On	1-4
SYSFAIL Generation Enabled	Off	2-3
SYSFAIL Generation Not Enabled	On	2-3

Table 1-25 Non-RoHS VMIVME-7700 CompactFlash Write Protect/BIOS Boot Mode (**Factory Configurable**) - Switch (S9)

Select	Switch Position	Switch No.
CompactFlash not Write Protected	Off	1-4
CompactFlash Write Protected	On	1-4
Boot Regardless of CMOS State	Off	2-3
Normal Boot	On	2-3

Table 1-26 Non-RoHS VMIVME-7700 Battery Enable/Disable (**User Configurable**) - Switch (S10)

Select	Switch Position	Switch No.
No Battery Drain	Off	1-4
Normal Operation	On	1-4

The VMIVME-9081-001 can drive SYSRESET on the VMEbus depending on the system configuration. In the Embedded configuration, it is usually undesirable to allow the IIOC to drive SYSRESET. This may reset everything on the VMEbus, including the host computer.

Table 1-27 Non-RoHS VMIVME-7700 VMEbus SYSRESET Enable/Disable (**User Configurable**) - Switch (S11)

Select	Switch Position	Switch No.
Disable VMEbus SYSRST Driver (see Note 1)	Off	1-4
Enable VMEbus SYSRST Driver (see Note 2)	On	1-4
Disable VMEbus SYSRST Receiver	Off	2-3
Enable SYSRST Receiver	On	2-3



NOTE

1. This is the default configuration for Embedded mode of operation.
2. This is the default configuration for the Reflective Memory and Ethernet Host Interfaces.

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Figure 1-8 Jumper and Switch Locations for RoHS VME-7700RC (Assy. No. 332-9301007700)

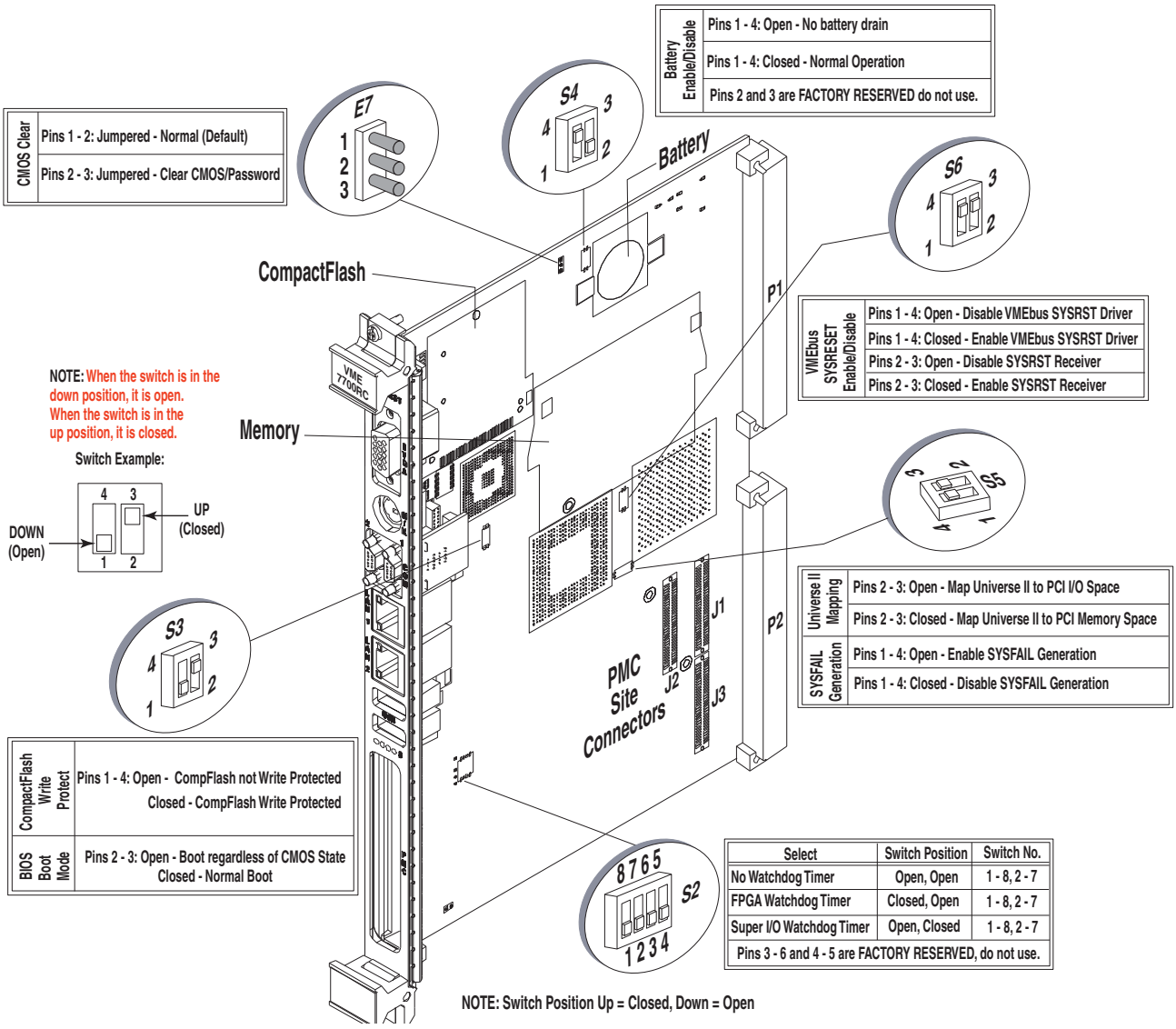


Table 1-28 Board Connectors and Headers for RoHS VME-7700RC

Connector	Function
J1	*Mouse/Keyboard
J5, J6	Ethernet Ports 1 & 2*
P2	IDE (PRI)*, Floppy*
J3, J4	USB Connectors*
J2	Video*
E1, E2, E3, E6, E7, E8, E9, E10	Factory Reserved DO NOT USE
E11	I^2C Header*
E7	CMOS Clear
J8, J9, J10	PMC Site Connectors
P4	CompactFlash Connector
P1, P2	VMEbus Backplane Connectors
* The connectors are not used by the IIOC.	

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Table 1-29 RoHS VME-7700RC CMOS Clear (**User Configurable**) - Jumper (E7)

Select	Jumper Pin Positions
Normal	1-2
Clear CMOS/ Password	2-3

Table 1-30 RoHS VME-7700RC Watchdog Timer (**Factory Configurable**) - Switch (S2)

Select	Switch Position	Switch No.
No Watchdog Timer	Off, Off	1-8, 2-7
FPGA Watchdog Timer	On, Off	1-8, 2-7
Super I/O Watchdog Timer	Off, On	1-8, 2-7
Factory Reserved		3-6, 4-5

Table 1-31 RoHS VME-7700RC Universe II Mapping, SYSFAIL Generation (**Factory Configurable**) - Switch (S5)

Select	Switch Position	Switch No.
Map UNIV2 to PCI I/O Space	Off	1-4
Map UNIV2 to PCI Memory Space	On	1-4
SYSFAIL Generation Enabled	Off	2-3
SYSFAIL Generation Not Enabled	On	2-3

Table 1-32 RoHS VME-7700RC CompactFlash Write Protect/BIOS Boot Mode (**Factory Configurable**) - Switch (S3)

Select	Switch Position	Switch No.
CompactFlash not Write Protected	Off	1-4
CompactFlash Write Protected	On	1-4
Boot Regardless of CMOS State	Off	2-3
Normal Boot	On	2-3

Table 1-33 RoHS VME-7700RC Battery Enable/Disable (**User Configurable**) - Switch (S4)

Select	Switch Position	Switch No.
No Battery Drain	Off	1-4
Normal Operation	On	1-4

Table 1-34 RoHS VME-7700RC VMEbus SYSRESET Enable/Disable (**User Configurable**) - Switch (S6)

Select	Switch Position	Switch No.
Disable VMEbus SYSRST Driver (see Note 1)	Off	1-4
Enable VMEbus SYSRST Driver (see Note 2)	On	1-4
Disable VMEbus SYSRST Receiver	Off	2-3
Enable SYSRST Receiver	On	2-3



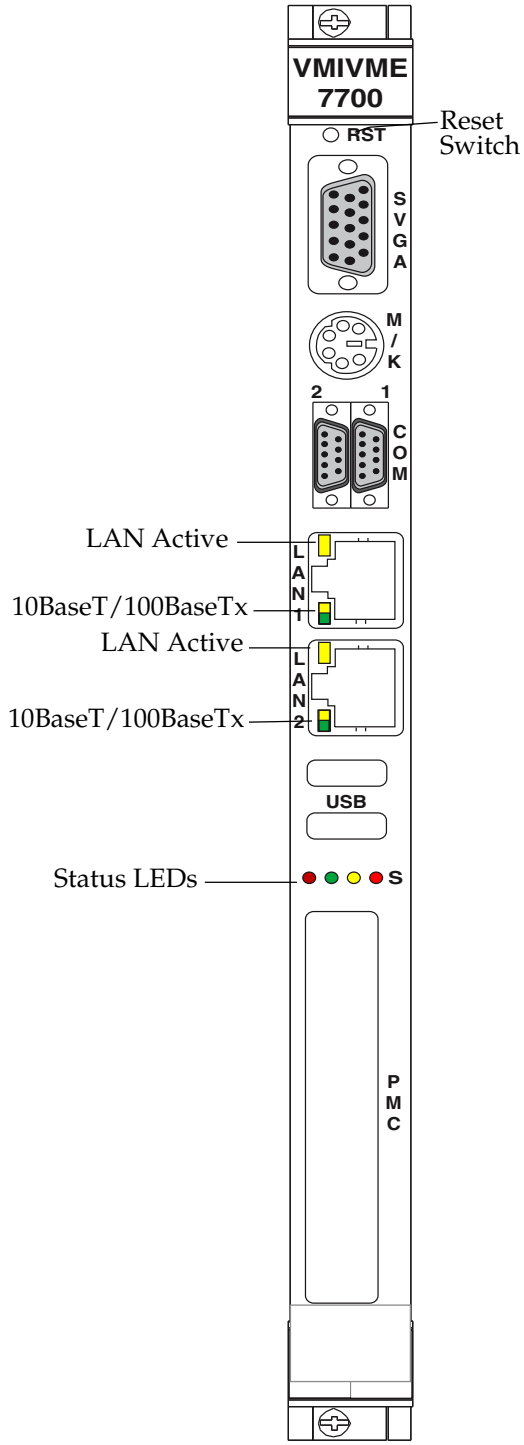
NOTE

1. This is the default configuration for Embedded mode of operation.
2. This is the default configuration for the Reflective Memory and Ethernet Host Interfaces.

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1.11.1 LED Definition

Figure 1-9 Front Panel LED Definitions



Reset Switch	*Reset* - Allows the system to be reset from the front panel.
LED R	*Reset* - Lights during reset condition, (Red LED).
LED P	*Power* - Indicates when power is applied to the board, (Green LED).
LED I	*IDE Indicator* - Indicates when IDE activity is occurring, (Yellow LED).
LED B	*Booting* - Indicates BIOS Boot is in progress. When LED is off, CPU has finished POST and is ready, (Red LED). Once booting has completed, any VME 'SYSFAILS' will be indicated by this LED.
LAN1 Active	Indicates the Ethernet is active, (Yellow LED).
LAN1 10/100BaseTx	Indicates whether 10BaseT or 100BaseTx mode. Yellow LED indicates 10BaseT, and Green LED indicates 100BaseTx.
LAN2 Active	Indicates the Ethernet is active, (Yellow LED).
LAN2 10/100BaseTx	Indicates whether 10BaseT or 100BaseTx mode. Yellow LED indicates 10BaseT, and Green LED indicates 100BaseTx.

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In addition, the front panel LEDs are used to indicate various modes of operational status that can occur with the VMIVME-7700. A summary of these indications is shown in ***Table 1-35***.

Table 1-35 Status Indications

State	Indication
Board is in Reset	"LAN 10BaseT/100BaseT" LED rapidly alternates Yellow/Green and the Red "Reset" LED is illuminated.
VME SYSFAIL	Red "B" LED illuminates with each VME SYSFAIL 'seen' on the bus. The LED will remain on as long as the failure lasts.
VRM Failure	Green "Power" LED is off and the Red "Reset" LED flashes at a rapid rate.
Normal Operation	LED R = Off (out of reset) LED P = On (power is good) LED I = Off, or Flashing (IDE activity) LED B = Off (boot completed)

1.12 VMIVME-7700 Control Terminal Connection

The IIOC supports an optional control terminal connected to serial port COM 1 on the VMIVME-7700 front panel. The control terminal provides the user with the capability to monitor and control I/O, initiate IIOC diagnostics, and display IIOC status independent of a host computer. Consult the *IIOC Family Instruction Manual* for a detailed description of IIOC control terminal operation.

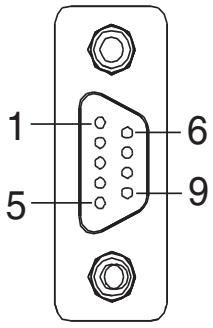
The control terminal may be any VT-100 compatible CRT or terminal emulation program supporting the ANSI Standard screen commands. The following communication setup is required on the control terminal:

- No Parity
- 8 Bits Per Character
- 1 Stop Bit
- 9600 Baud
- Asynchronous Protocol

The serial port is a Micro DB9 as shown in ***Figure 1-10, VMIVME-7700 Serial Port*** on page 52. An adapter is provided to transition the Micro DB9 to a standard DB9.

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Figure 1-10 VMIVME-7700 Serial Port



COM 1 and COM 2 SERIAL PORT CONNECTORS			
DB9 PIN	DIR	RS232 SIGNAL	FUNCTION
1	In	DCD	Data Carrier Detect
2	In	RX	Receive Data
3	Out	TX	Transmit Data
4	Out	DTR	Data Terminal Ready
5		GND	Signal Ground
6	In	DSR	Data Set Ready
7	Out	RTS	Request to Send
8	In	CTS	Clear to Send
9	In	RI	Ring Indicator
Shield			Chassis Ground

1.13 V7768 Single Board Computer

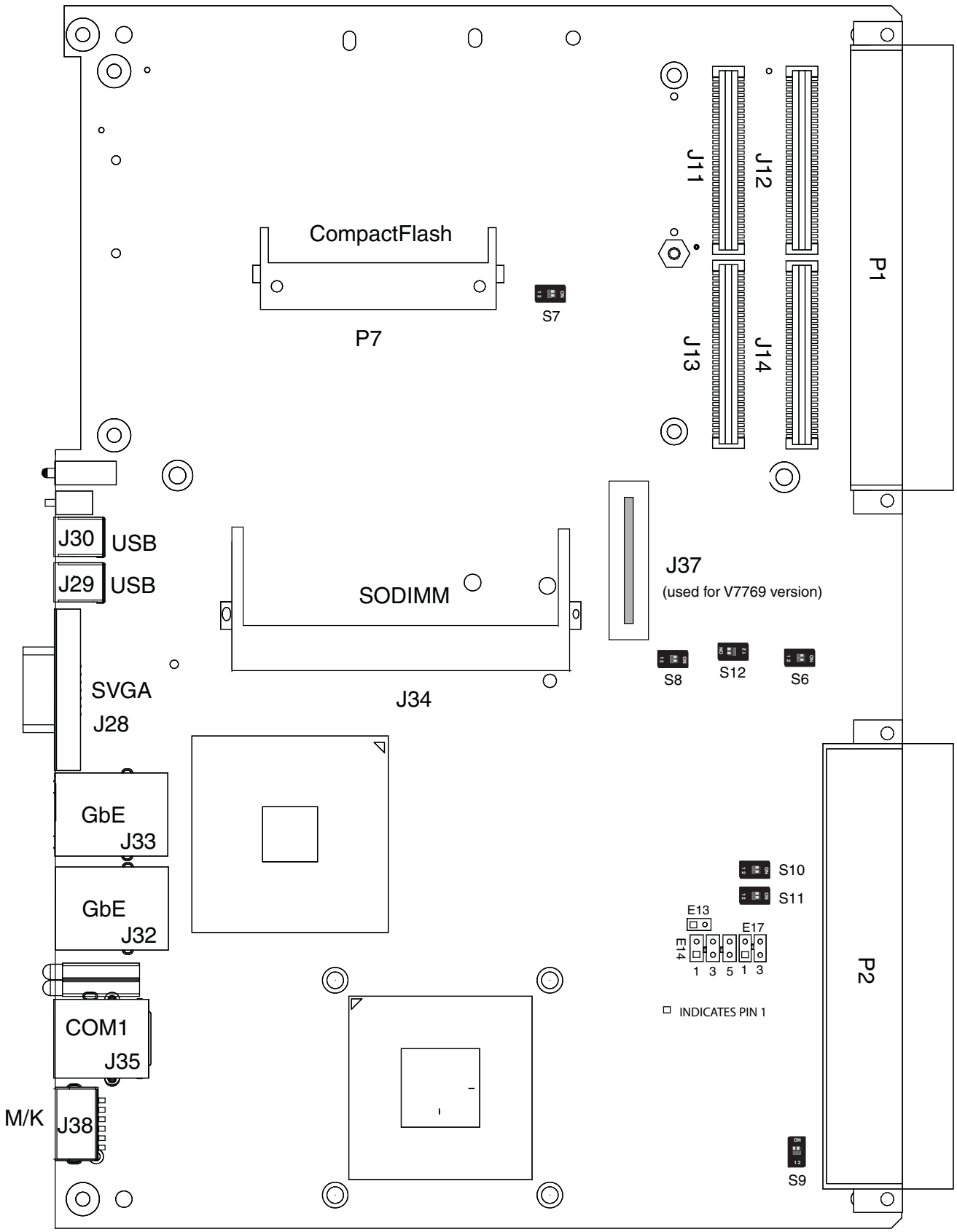
The VMIVME-9081-002 IIOC consists of a V7768-112000 SBC preloaded with IIOC firmware. The V7768 SBC is based on the Intel Celeron M processor with 1 MByte of on-die L2 cache. The thermal characteristics of the V7768 are well suited for embedded systems operating over a wide range of temperatures. V7768 has 512 MByte of DDR2 SDRAM memory, a 4 GByte CompactFlash memory containing the IIOC firmware and operating system kernel, and front panel Ethernet and Serial ports. The VMEbus interface is based on the Newbridge/ Tundra Universe IID high performance PCI-to-VMEbus interface. The V7768 is tested for system operation and shipped with factory-installed jumpers. The physical location of the jumpers, switches and connectors for the SBC are illustrated in ***Figure 1-11, V7768 Jumper and Switch Locations*** on page 53. The definitions of the SBC jumpers and connectors are included in ***Table 1-36*** on page 54 through ***Table 1-43*** on page 55.

NOTE
The VMIVME-9081-002 IIOC does not use all the features of the V7768 SBC.

CAUTION
Care must be taken when making jumper modifications to ensure against improper settings or connections. Improper settings may result in malfunction of the unit.

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Figure 1-11 V7768 Jumper and Switch Locations



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Table 1-36 V7768 Board Connectors and Headers

Connector	Function
P1	VME interface connector
P2	USB 2.0, Serial ATA, digital video, COM3, COM4, Gigabit Ethernet, GPIO *
P7	CompactFlash socket
J34	SODIMM socket
J29, J30	USB ports *
J38	Mouse/Keyboard PS/2 connector *
J32	Gigabit Ethernet LAN1 connector
J33	Gigabit Ethernet LAN2 connector *
J11, J12, J13, J14	PMC site connectors *
J35	Serial port connector (COM1)
J28	SVGA connector *
J37	Board to board connector for V7769 *
Header	**Function**
E13	COM1 configuration
E14	COM1 configuration
E17	COM1 (RS422 termination)
Switches	**Function**
S6	Mapping/SYSFAIL generation
S7	VMEbus SYSRESET
S8	Factory configurable
S9	Factory configurable
S10	System Controller
S11	Battery enable
S12	RTC reset and boot pause
* Not used by the IIOC.	

Figure 1-12 COM1 Configuration Headers (E13, E14, E17)

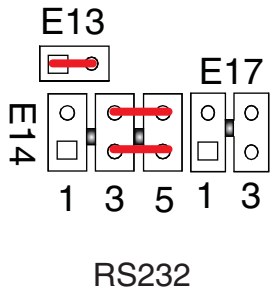


Table 1-37 Mapping/SYSFAIL Generation - Switch S6

Select	Switch Number	Switch Position
Disable SYSFAIL Generation	1	Off
Map UNIV2 to Memory Space	2	On

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The VMIVME-9081-002 can drive SYSRESET on the VMEbus depending on the system configuration. In the Embedded configuration, it is usually undesirable to allow the IIOC to drive SYSRESET because this may reset everything on the VMEbus, including the host computer.

Table 1-38 VME SYSRESET - Switch 7

Select	Switch Number	Switch Position
Enable VME SYSRESET Driver	1	On (when using RFM or Ethernet host interface)
Disable VME SYSRESET Driver	1	Off (when using Embedded host interface)
Enable SYSRESET Receiver	2	On

Table 1-39 Factory Configurable - Switch S8

Switch Number	Switch Position
1	On
2	On

Table 1-40 Factory Configurable - Switch S9

Switch Number	Switch Position
1	Off
2	Off

Table 1-41 System Controller - Switch S10

Select	Switch Number	Switch Position
Enable Auto System Controller	1	Off
Force non-syscontroller	2	Off

Table 1-42 Battery Enable - Switch S11

Select	Switch Number	Switch Position
Enable Battery	1	On
Factory Use Only	2	On

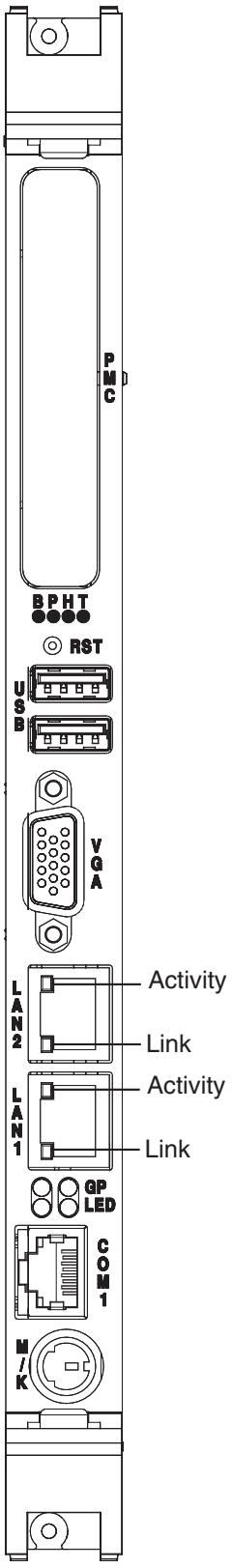
Table 1-43 RTC Reset and Boot Pause - Switch S12

Select	Switch Number	Switch Position
Normal	1	Off
Boot Halt on POST Errors	2	Off

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1.13.1 LED Definition

Figure 1-13 V7768 Front Panel Layout



Status LEDs (from left to right)

Boot Done (B) *Booting* - Indicates BIOS Boot is in progress. When LED is Off, CPU has finished POST and is ready (Red LED).

PWR (P) *Power* - Indicates when power is applied to the board, (Green LED).

IDE (H) *Activity Indicator* - Flashes when IDE activity is occurring, (Yellow LED).

Sysfail (T) *VME failure* - Lights during VME SYSFAIL condition, (Red LED).

RST Switch

Reset Allows the system to be reset from the front panel.

LAN1 and LAN2 LEDs

Activity	Indicates the Ethernet is active, (Yellow LED).	
Link	10Base-T	(LED Off)
	100Base-TX	(Yellow LED) or
	1000Base-T	(Green LED)

GP LED (User Configurable, general purpose LEDs)

Controlled by accessing I/O port 0xA4B bits 7-4.
The LEDs are turned off by setting the associated bit and turned on by clearing the associated bit.

Upper/Right LED	- Bit 7
Upper/Left LED	- Bit 6
Lower/Right LED	- Bit 5
Lower/Left LED	- Bit 4

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1.14 V7768 Control Terminal Connection

The IIOC supports an optional control terminal connected to serial port COM1 on the V7768 front panel. The control terminal provides the user with the capability to monitor and control I/O, initiate IIOC diagnostics, and display IIOC status independent of a host computer. Consult the *IIOC Family Instruction Manual* for a detailed description of IIOC control terminal operation.

The control terminal may be any VT-100 compatible CRT or terminal emulation program supporting the ANSI Standard screen commands. The following communication setup is required on the control terminal:

- No Parity
- 8 Bits Per Character
- 1 Stop Bit
- 9600 Baud
- Asynchronous Protocol

The serial port connector is a standard RJ45 connector as shown in ***Figure 1-14*** and its pinout in ***Table 1-44***.

Figure 1-14 Serial Connector (J35)

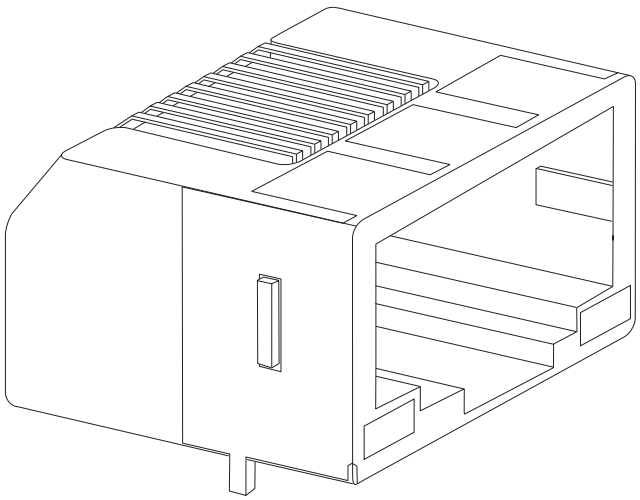


Table 1-44 Serial Connector (J35)

Pin	RS232 Signal
1	DCD
2	RTS
3	GND
4	TXD
5	RXD
6	GND
7	CTS
8	DTR

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2 • Standard Features

The VMIVME-9081 IIOC provides a flexible, compact solution including user friendly software utilities for the user requiring I/O products coupled with a preprogrammed single board computer (SBC) for an effective turnkey operation. Multiple VMIVME-9081 IIOCs can reside on a single Reflective Memory link.

Abaco Systems provides a complete product line of I/O boards designed specifically for the Simulation and Training industry. The I/O boards utilize state of the art building blocks organized around the VMEbus architecture, providing a high density, high throughput low cost solution to your I/O control problem. The real time interface equipment includes an IIOC designed to operate in parallel with customer-furnished/programmed SBCs and other customer-furnished hardware.

Abaco's I/O board-level product line, trademarked BITMODULES*, is comprised of digital I/O boards, analog I/O boards and synchro/resolver I/O boards. Some of Abaco's products are designed with an extensive Built-in-Test capability and a front panel Fail LED to enable quick fault detection and isolation. These products support both offline and real time fault detection and isolation.

Abaco's real time product line supports configuration of data, generated by a customer-furnished host computer, allowing user-definable scan lists, data conversion formats and service order of each I/O type. The system is expandable through the use of building block board-level products. As requirements change, the I/O system can be easily reconfigured. This configuration concept allows independent mapping of I/O points to memory, thus enabling the hardware configuration to change without changing the software interfaces.

The system provides extensive data type and engineering unit conversions. Digital data types can be represented as bit, byte, word or longword logicals. In addition, the host's definition of logical true may be designated as a least significant bit (LSB), most significant bit (MSB) on, or all bits on for byte, word, and longword digital points. Analog and synchro values can be represented as host floating-point format or integer numbers. Engineering unit conversions for analogs include: offset binary, scaled, first-, second-, and third-order polynomial, two's complement integer, sine, cosine, arcsine, arccosine, table lookup, natural log and common log. Engineering unit conversions for synchros include: offset binary, degrees +180 to -180, degrees 0 to 360, scaled, unscaled, and first-order polynomial. See the *IIOC Family Instruction Manual* for a full description of all the engineering unit conversions.

2.1 Intelligent I/O Controller (IIOC)

The IIOC consists of a high speed single board computer with factory-installed firmware. The IIOC system architecture provides for easy I/O system expansion in systems with Abaco board level building blocks.

The IIOC can control up to twelve chassis of I/O boards. The master chassis, containing the IIOC board, is numbered chassis 1 and can contain I/O boards in slots 2 through 20, although some slots may be occupied by a host interface board,

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repeater boards, or customer supplied boards. The slave chassis are numbered 2 through 12 and can contain up to nineteen I/O boards in slots 2 through 20.

In addition, a VMIVME-9150* Communications Controller is available for use in systems containing multiple VMIVME-9081 IIOCs. The VMIVME-9150 off loads much of the work done by the host computer when using large Reflective Memory links with multi-node IIOCs with high I/O point counts.

The basic IIOC system consists of one VMIVME-9081 IIOC in a chassis with power supplies, fans, VMEbus backplanes, and one or more Abaco I/O boards. Multiple chassis, bus repeaters to multiple chassis, and a control terminal may be purchased.

2.2 Host Interface

The VMIVME-9081 IIOC supports three methods of interfacing to a host computer:

- Reflective Memory
- Ethernet
- Embedded (i.e. the IIOC resides on the same VMEbus as the host computer)

2.2.1 Reflective Memory

The VMIVME-9081 IIOC communications protocol utilizes a simple, memory-mapped control window and interrupt scheme to simplify control by the Reflective Memory host computer. The host initializes a memory-mapped Reflective Memory allocation page and interrupts each VMIVME-9081 IIOC on the Reflective Memory link. Each IIOC uses its node ID, read from the local Reflective Memory as an index into the Reflective Memory allocation page to locate its control window and buffer space. The host can then write commands for the IIOC to the appropriate control window and issue a command interrupt. The IIOC fields the locally generated interrupt, interprets the command, and executes the requested action. After the I/O has been configured, the IIOC posts the locations and word count of the I/O buffers in the control window. The host and IIOC then read and write I/O data to these shared Reflective Memory buffers.

2.2.2 Ethernet

The VMIVME-9081 supports TCP/IP as a communications interface to a host computer. Stream sockets are used to ensure data integrity. The VMIVME-9081 initializes a server socket with a user-supplied TCP/IP address. The host computer connects to the IIOC using standard sockets calls. Commands and data are passed between the machines through the TCP sockets.



NOTE

The TCP/IP protocol guarantees data delivery, but not the speed of the data transfer. It is normal for data transfers to sometimes take hundreds of milliseconds. This interface is not recommended unless I/O buffer transfer timing is not required to be deterministic. For best performance when using the Ethernet host interface, use a peer to peer connection between the IIOC and the host computer.

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2.2.3 Embedded

The VMIVME-9081 IIOC communications protocol utilizes a simple memory-mapped control window and interrupt scheme to simplify control by the host computer. The host computer executes all IIOC commands, writing command codes and associated parameters to a global memory control window in the VMEbus extended supervisory data access area. This control window also provides IIOC status information for the host. After writing command information to the control window, the VMEbus host interrupts the VMIVME-9081 by performing an access to the IIOC mailbox interrupter, accessible from the VMEbus. The IIOC fields the locally generated interrupt, interrupts the command and performs the requested action. After I/O configuration, the IIOC posts the locations and sizes of the configured I/O buffers in the global control window. The host can then use the I/O buffers for its data manipulation, or request the IIOC perform data transfers to the host global memory.

2.3 Host Software Support Package

The Host Software Support Package (HSSP) for the IIOC product line is a set of host-resident tools and interface software. Tools are provided for configuring, documenting, and programming the IIOC in a manner that minimizes errors and facilitates changes. Programs within the HSSP work in conjunction to accomplish much of the data management necessary for an I/O system. An I/O point data file forms the central repository for information about the I/O points in a system. Data can be entered into the I/O point data file by two different means. The user can interactively enter the information using the I/O Point Manager. Alternatively, the user can import data from an ASCII text file using the Import Utility. The ASCII text file can be constructed from a database program, a text editor or a customer utility. From the I/O point data file, a binary configuration data file is generated which can be downloaded to the IIOC in an efficient manner. The Report Generator Utility generates several reports from the I/O point data file. In addition, user-defined ASCII files may be generated using the Export Utility.

The user's simulation application interfaces to the IIOC by way of the HSSP software library. The library provides I/O controller functions, such as initiating diagnostics, configuring scan lists, initiating I/O scans, reading and writing I/O data, and obtaining status and error information.

The HSSP is available in the C programming language. The software is constructed to be highly portable between host computers. The host-dependent functions are isolated and identified to facilitate porting the software. All source code is delivered to the user to allow maximum programming flexibility.

2.4 VMEbus

The IIOCs and a variety of Abaco's boards are based on the industry standard VMEbus. The VMEbus structure is based upon a 16-bit data path and 24-bit addressing, both expandable to 32 bits. The VMEbus can be summarized as a master/slave asynchronous, nonmultiplexed data transfer structure with four levels of master arbitration, seven levels of priority interrupts, control, and special data transfer cycles. Data transfer rates as high as 40 MByte/s are supported on the VMEbus. The VMEbus provides a cost-effective system bus that supports:

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- Complex systems through fault tolerance and diagnostic capability
- Multiple bus masters, such as processors, DMA devices, etc.
- High performance data rates and throughput
- Future growth

The Eurocard standard is used for printed circuit board format, and both single (3U) and double (6U) height boards are supported. The primary 96-pin connector (P1) contains 16 data lines, 23 address lines plus two data strobes to generate a 24-bit address, bus arbitration control lines, voltages and all additional signals necessary to control data transfer and other bus functions. The secondary 96-pin connector (P2) extends data and address busses to 32 bits and provides 64 user-defined pins.

For additional information regarding the VMEbus, see the VMEbus Specification. This publication is available from:

VITA
VFEA International Trade Associated
7825 E. Gelding Dr. #104
Scottsdale, Arizona 85206
(602) 951-8866
(602) 951-0720 fax

2.5 Multiple Chassis

IIOC systems consist of a single master chassis and multiple slave chassis. The master chassis contains the IIOC processor, host interface device, I/O boards and a VMEbus repeater for use when multiple slave chassis and additional I/O is required, with a maximum of twelve chassis supported. For small I/O systems, only the master chassis may be required. The master chassis is capable of supporting up to eighteen I/O boards.

2.6 VMEbus Repeater Link

The IIOC controls I/O boards in slave chassis through multiple VMEbus repeaters. Repeater products are available supporting 8-bit through 32-bit data transfers with up to 32-bit addressing and cable lengths of up to 2,000 feet. These products extend the master VMEbus chassis to all slave chassis, causing all I/O boards in the slave chassis to appear as though they reside on one continuous VMEbus. Only slave boards can reside in the slave chassis.

2.7 Control Terminal

Each IIOC supports an optional user friendly CRT based control terminal (ANSI compatible terminal) providing the system integrator or maintenance technician with the capability to control and modify all I/O points and initiate and control diagnostics offline (i.e., while the IIOC is not connected to or not communicating with the host). While online (actively controlled by the host), the control terminal allows the user to monitor I/O points and selectively freeze outputs. The control terminal displays IIOC status, errors detected through offline diagnostics or online real time background testing, and the current system hardware

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configuration. The control terminal facilitates maintenance, test, integration, and checkout of the IIOC independent of a host computer system. The *IIOC Family Instruction Manual* describes local control terminal operation of the IIOC in detail.

The control terminal may be any CRT supporting the ANSI-standard screen commands. The terminal must be connected to the RS232 serial port located on the front panel of the SBC in the IIOC master chassis. See ***Chapter 1, Handling and Installation*** for the location of the serial port on the SBC and wiring information for connection of the terminal. The following communications setup is required for the terminal:

- No Parity
- Eight Bits per Character
- One Stop Bit
- 9600 Baud
- Asynchronous Protocol
- VT-100 Emulation

Systems utilizing a VMIVME-9150 Communications Controller, which supports its own local control terminal, can remotely connect to the control terminals of each of the VMIVME-9081s on the Reflective Memory link through menu selections from the VMIVME-9150 control terminal.

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3 • IIOC Address Map

This chapter defines the address spaces utilized by the VMIVME-9081 IIOC. The user must ensure that special purpose resources (user-provided processors or special I/O) installed in the IIOC chassis are not configured to respond in the address spaces used by the IIOC.

3.1 IIOC Reserved Address Spaces

The IIOC reserved address spaces include:

- IIOC Reserved Short I/O Board Address Space
- IIOC Reserved Reflective Memory Address Space
- IIOC Reserved Global Memory Address Space
- IIOC Reserved Mailbox Interrupt Address Space

Table 3-1 lists the address spaces to be avoided by the user. Note that in the table "NP" stands for nonprivileged and "S" stands for supervisory.

Table 3-1 IIOC Reserved Address Spaces

Address Range	Address Space	IIOC Usage
0x0000 - 0xE3FF	Short NP I/O	I/O Boards
0x7B000000 - 0x7B0FFFFF	Extended S	Reflective Memory
0xF40C0000 - 0xF40FFFFF *	Extended S/NP	Global Memory (when configured as an Embedded IIOC)
0xF000 - 0xFFFF *	Short S/NP	Mailbox Interrupt (when configured as an Embedded IIOC)
* User configurable via the Setup Menu.		

3.2 IIOC Reserved Short I/O Board Address Space

The VMIVME-9081 IIOC uses memory mapping to determine the I/O board type and location for all IIOC-supported I/O boards. The IIOC reserves the entire VMEbus short I/O (A16) nonprivileged space for this purpose. Make sure the host system or user-supplied I/O devices do not respond to the VMEbus nonprivileged short I/O space. Use the VMEbus short supervisory space, except for the range from 0xF000 to 0xFFFF, for host system or user-supplied I/O devices.

3.3 IIOC Reserved Reflective Memory Address Space

If the VMIVME-9081 IIOC is configured to use Reflective Memory as the host interface, the address space used by the Reflective Memory is reserved. The Reflective Memory address space is occupied by the Reflective Memory board installed in the IIOC master chassis. The IIOC requires a section of this memory space for memory allocation structures initialized by the host computer. The *IIOC Family Instruction Manual* describes these structures in detail. The host has complete control of the allocation of the rest of the Reflective Memory space and

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may allocate portions of it for use by user-supplied masters installed in the IIOC system.

3.4 IIOC Reserved Global Memory Address Space

If the VMIVME-9081 IIOC is configured as an Embedded IIOC, a portion of the IIOC's local RAM is shared out to the VMEbus. The VMEbus-based host computer controls the IIOC and transfers I/O data via this shared memory region. The IIOC is accessed by the host computer at a factory default base address of 0xF40C0000 in the VMEbus extended (A32) supervisory address space. The default address of the IIOC global memory access window for the host computer is from 0xF40C0000 through 0xF40FFFFF in the VMEbus extended (A32) supervisory or nonprivileged data address space. Thus, the host system must have no devices that respond to this range of addresses in the extended (A32) data space. If the Setup Menu is used to change the default global memory access window address, then care must be taken to avoid address conflicts in this range as well.

3.5 IIOC Reserved Mailbox Interrupt Address Space

If the VMIVME-9081 IIOC is configured as an Embedded IIOC, the host computer uses the IIOC's mailbox interrupt for command processing. The IIOC is interrupted for command processing by the host computer writing a value to the mailbox interrupt address location, which by default is at 0xF348 in VMEbus Short I/O (A16) supervisory or nonprivileged data address space. The mailbox interrupt address is inside the register map of the Tundra Universe IID VMEbus interface. This register map is shared out to the VMEbus by default at 0xF000 to 0xFFFF in VMEbus Short I/O (A16) supervisory or nonprivileged data address space. Thus, the host system must have no devices that respond to this range of addresses. If the Setup Menu is used to change the default mailbox interrupt address, then care must be taken to avoid address conflicts in this range as well.

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4 • Host Communications

The VMIVME-9081 IIOC is user-configurable to operate with a Reflective Memory host interface, an Ethernet host interface, or as an embedded controller. When configured to use Reflective Memory or function as an embedded controller, the IIOC implements a memory-mapped control window and a local processor interrupt mechanism for host communications and control. When configured to use Ethernet as the host interface, the IIOC uses TCP/IP stream sockets to transfer data and commands.

4.1 IIOCs Using Reflective Memory Host Interface

The VMIVME-9081 IIOC implements a memory-mapped control window and Reflective Memory link interrupts for host communications and control. The control window and all commands implemented by the IIOC are described in detail in the *IIOC Family Instruction Manual*. The host defines the location of the VMIVME-9081 control window by initializing node allocation structures on the Reflective Memory and issuing an interrupt to each IIOC. The host then controls the IIOCs by writing commands and command parameters to the control windows and generating interrupts to the IIOC nodes.

The control window for the VMIVME-9081 IIOC is allocated in the Reflective Memory space by the host computer. The *IIOC Family Instruction Manual* provides a definition of the control window parameters and a complete description of host command protocol.

4.2 Addresses Posted in the Control Window

All addresses posted by the IIOC in the control window are IIOC access addresses. The global Reflective Memory is accessed by the IIOC SBC from a base address of 0x7B000000. In order to access the buffer addresses posted by the IIOC in the control window, the host must mask off the upper eight bits of the 32-bit address and offset the result by the base address of the host local Reflective Memory.

For example, assume the host local Reflective Memory is addressed by the host SBC at a base of 0xFF000000 and the IIOC has posted an analog input buffer base address of 0x7B003020. The host would access this buffer at a base address of 0xFF003020.

4.2.1 VMEbus Addresses for IIOC Data Transfers

Several commands to the IIOC require the IIOC to perform data transfers to or from the Reflective Memory board. When the host requires the IIOC to perform data transfers to or from the Reflective Memory, a full 32-bit absolute address within the IIOC Reflective Memory space must be provided in the control window.

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4.3 Embedded IIOCs

The VMIVME-9081 IIOC implements a memory-mapped control window and a mailbox interrupt generator for host communications and control. The control window and commands implemented by the IIOC are described in detail in the *IIOC Family Instruction Manual*. As described in this manual, the host controls the IIOC by:

- Writing commands and command parameters to the global memory-mapped control window
- Generating an IIOC SBC local interrupt

The VMIVME-9081 IIOC has no method of generating interrupts to the host. Thus, the host must poll control window locations to determine when the IIOC has completed command processing.

4.3.1 VMIVME-9081 Control Window

The control window for the VMIVME-9081 IIOC is accessed by the host computer in the VMEbus extended (A32) supervisory or nonprivileged data space at a factory default base address of 0xF40C0018. Chapter 5 of the *IIOC Family Instruction Manual* provides a definition of the control window parameters and a complete description of host command protocol.

4.3.2 Addresses Posted in the Control Window

Addresses posted by the IIOC in the control window are relative to the IIOC access address. The global memory on the IIOC SBC is accessed by the SBC relative to a base address of 0x00000000. To access the buffer addresses in the control window, the host must offset the addresses posted by the IIOC by 0xF4000000 or the user-specified base address to obtain the VMEbus access address.

4.3.3 IIOC Mailbox Command Interrupt

As described in Chapter 5 of the *IIOC Family Instruction Manual*, the host controls the IIOC by writing commands and command parameters into the IIOC control window and then generating the command interrupt to the IIOC. The IIOC fields this interrupt, interprets the command, and performs the commanded function. The mailbox interrupt generated is local to the IIOC SBC board. A VMEbus interrupt is not generated, however, so a special system configuration is not required for the host computer.

The command interrupt is generated by the host writing a byte to the default address 0xF348 in VMEbus short I/O (A16) nonprivileged data space. Consult the host system or SBC manual to obtain the full address of the VMEbus short I/O space of the host system being used.

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4.4 IIOCs Using Ethernet Host Interface

TCP/IP is an industry standard set of communication protocols that allows computers to share information and commands between processes. The TCP/IP network transports information from machine to machine. TCP/IP protocol is supported by the VMIVME-9081 IIOC through the Ethernet connector LAN1 on the front panel of the IIOC.

The IIOC initializes a server socket upon boot up. When the host computer calls the appropriate socket connect routines, the Ethernet connection is established between the host computer and the IIOC.

Commands from the host computer to the IIOC are passed in 8-byte command packets containing the 16-bit command word, one 16-bit command parameter, and one 32-bit command parameter. All data transfers are initiated from the host computer; the IIOC itself reads and writes data to the Ethernet connection only when commanded to do so by the host computer.



NOTE

The TCP/IP protocol guarantees data delivery, but not the speed of the data transfer. It is normal for data transfers to sometimes take hundreds of milliseconds. This interface is not recommended unless I/O buffer transfer timing is not required to be deterministic. For best performance when using the Ethernet host interface, use a peer to peer connection between the IIOC and the host computer.

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