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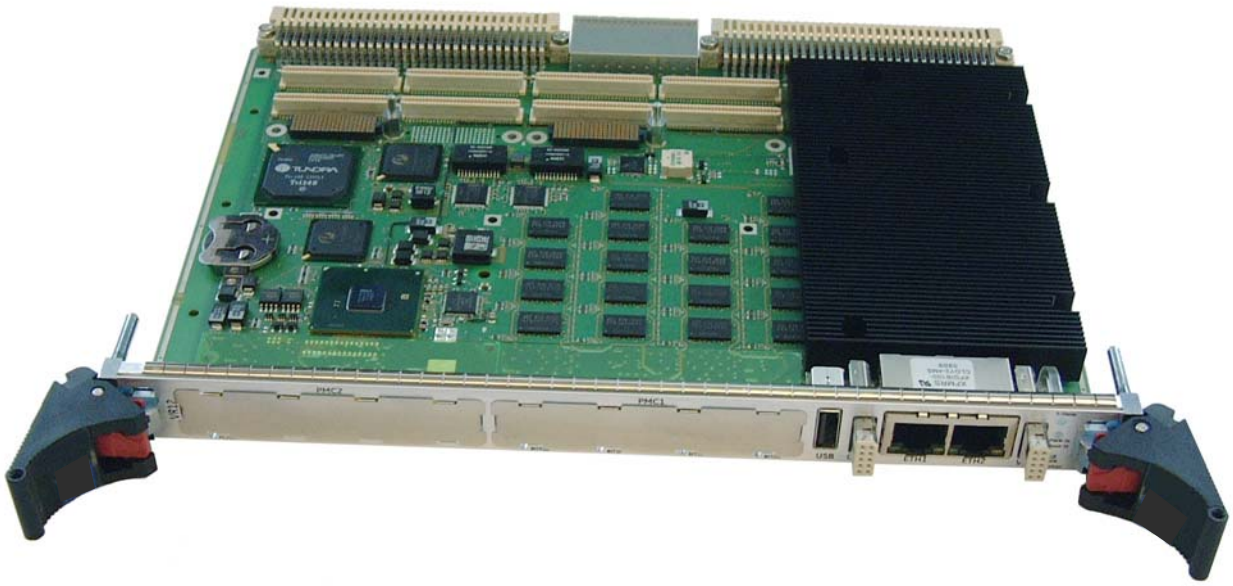
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Hardware Reference Manual

VR12*, VP12* 6U VME Single Board Computer

Publication No. VR12-HRM Rev. K.0



abaco SYSTEMS

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Document History

Revision	Date	Description
Preliminary	22 Feb 2010	Preliminary issue
First	21 Jun 2010	corrections
		changes for VR12 V1 and VTM24 V1
		replace several pictures in Chapters 1, 8 and Appendix A; replace Arrandale with i5/i7 name; correct spelling of har-Link®
		Cosmetic changes; new photos
		chapter 8: correct shock/vibration parameters
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		replace board photos on front page & in chapter 1
		Add note about HDD GPIO description and GPIO electrical characteristics 4.3 Booting 8.5 +/-12V Imax changed
		Corrections per emails MF (15 Dec) & PS (16 Dec)
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Eighth	02 Apr 2012	remove ref. to 'Board Specific Hardware Programmer's Manual'
Ninth	24 June 2013	remove reference to 'programming manual'
K.0	February 2017	Rebranded to Abaco Systems

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NOTE

This manual applies to version V1 (First Edition) and higher of VR12 and VP12. For version V0 (Preliminary Edition) consult the PE version manual.

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About This Manual

Conventions

Notices

This manual may use the following types of notice:


WARNING
Warnings alert you to the risk of severe personal injury.


CAUTION
Cautions alert you to system danger or loss of data.


NOTE
Notes call attention to important features or instructions.


TIP
Tips give guidance on procedures that may be tackled in a number of ways.


LINK
Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. Where confusion may occur, decimal numbers have a “D” subscript and binary numbers have a “b” subscript. The prefix “0x” shows a hexadecimal number, following the ‘C’ programming language convention. Thus:

One dozen = 12_D = 0x0C = 1100_b

The multipliers “k”, “M” and “G” have their conventional scientific and engineering meanings of $x10^3$, $x10^6$ and $x10^9$, respectively, and can be used to define a transfer rate. The only exception to this is in the description of the size of memory areas, when “K”, “M” and “G” mean $x2^{10}$, $x2^{20}$ and $x2^{30}$ respectively.

In PowerPC terminology, multiple bit fields are numbered from 0 to n where 0 is the MSB and n is the LSB. PCI terminology follows the more familiar convention that bit 0 is the LSB and n is the MSB.

Text

Signal names ending with a tilde (“~”) denote active low signals; all other signals are active high. “N” and “P” denote the low and high components of a differential signal respectively.

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This document is distributed via the Abaco website. You may register for access to manuals via the website, whose link is given above.


LINKS
https://www.abaco.com/products/vr12-vme-sbc
https://www.abaco.com/products/vp12-vme-sbc

Third-party Documents


NOTE
Technical literature describing components used on the VR12 and VP12 is available from the manufacturers' websites.

Legal Information

Regulatory Compliance

Products sold or transferred between companies or operated on company premises (factory floor, laboratory) do not need CE, FCC or equivalent certification. Boards or subsystems which cannot provide a useful function on their own do not need certification.

Certification can only be granted to complete and operational systems. There are authorized testing agencies, regulatory organizations and laboratories who will issue certificates of compliance after system testing.

Abaco designs and tests all their products for EMI/EMC conformance. Where Abaco supplies a complete/functional system for use by end users a certificate will be cited in the manuals/documents which are provided with the products.

Products manufactured by Abaco should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign or additional filtering. However, the systems might not conform to specific regulations once assembled and used. The system integrator or installer must test for compliance as required in his country or by the intended application and certify this to the end user.

ESD/EMI Issues

ESD (Electro-Static Discharge) and EMI (Electro-Magnetic Interference) issues may show up in complete and operational systems. There are many ways to avoid problems with these issues.

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Any operational system with cables for I/O signals, connectivity or peripheral devices provides an entry point for ESD and EMI. If Abaco does not manufacture the complete system, including enclosure and cables, it is the responsibility of the system integrator and end user to protect their system against potential problems. Filtering, optical isolation, ESD gaskets and other measures might be required at the physical point of entry (enclosure wall of box or rack). For example it is state-of-the-art that protection can not be done at the internal connector of an RTM if a cable is attached and routed outside the enclosure. It has to be done at the physical entry point as specified above.

Products manufactured by Abaco should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign. However, the systems might be subject to problems and issues once assembled, cabled and used. The end user, system integrator or installer must test for possible problems and in some cases show compliance to local regulations as required in his country or by the intended application.

CE Conformance Declaration

CE certification is required in EU countries for equipment which is used or operated by the end user. Products sold or transferred between companies or operated on company premises (factory floor, laboratory) do not need CE certification.

CE certification can only be granted to complete and operational systems. Boards or subsystems which cannot provide a useful function on their own do not need CE certification.

Abaco designs and tests all their products for EMI/EMC conformance. Products manufactured by Abaco should normally be suitable for use in properly designed and produced customer equipment (system boxes or operational systems) without any major redesign or additional filtering. The system integrator or installer must, in any case, test for CE compliance and certify this to the end user.

Information to the User

The following statement applies to the products covered in this manual, unless otherwise specified herein. The statement for other products will appear in the accompanying documentation.



NOTE

This equipment has been tested and found to comply with the limits for a class A digital device, pursuant to Part 15 of the FCC Rules and meets all requirements of the Canadian Interference-Causing Equipment Standard ICES-003 for digital apparatus. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Abaco is not responsible for any radio television interference caused by unauthorized modifications of this equipment or the substitution or attachment of connecting cables and equipment other than those specified by Abaco. The correction of interference caused by such unauthorized modification, substitution or attachment will be the responsibility of the user.



NOTE

The use of shielded I/O cables is required when connecting this equipment to any and all optional peripheral or host devices. Failure to do so may violate FCC and ICES rules.

Where Abaco supplies a complete/functional system for use by end users in EU countries a CE certificate will be cited in the manuals/documents which are provided with the products. The CE (and year of certification) symbol is shown on the equipment, typically on the type or S/N label or close to the power cable entry.



WARNING

This is a class A device. This equipment may cause interference in a residential installation. In this case the user is encouraged to perform appropriate measures to correct the interference.

Abaco has tested their boards using their own card cages (chassis). Test results of these tests are available upon request.

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Product Properties

Certification

The product or products described in this technical manual cannot be operated by themselves. They are components for integration into operational systems or add-ons to such systems. The products have been designed to meet relevant regulatory standards like FCC and CE. As mandated by these standards conformance to these standards can only be certified for complete operational systems. This has to be done by the end-user or by the systems integrator in their operational systems. Abaco has tested some products in their own systems. Upon request information is available which products have been tested and about the specific environment under which Abaco has tested these components.

Altitude

Altitude, air pressure, and ambient temperature influence the thermal operation of the components described in this manual. They have been developed and tested at about 500 m (1650 ft.) above sea level at a typical ambient temperature of 20 °C (68 °F). Because of only marginal variations within a limited range of altitudes these products operate as specified within altitudes from sea level to 1000 m (3300 ft.). This is with reference to temperature ranges of air-cooled versions. Abaco can assist the user of these components in planning operation outside this altitude range upon request.

Options

This manual describes the basic product plus all options. Your product may not have all options implemented. Please verify with your purchase contract which options are implemented. Descriptions of options which are not implemented obviously do not apply to your product.

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Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:

LINK
support@abaco.com

Returns

If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Embedded Support page.

LINK
https://www.abaco.com/embedded-support

Do not return products without first contacting the Abaco Repairs facility.

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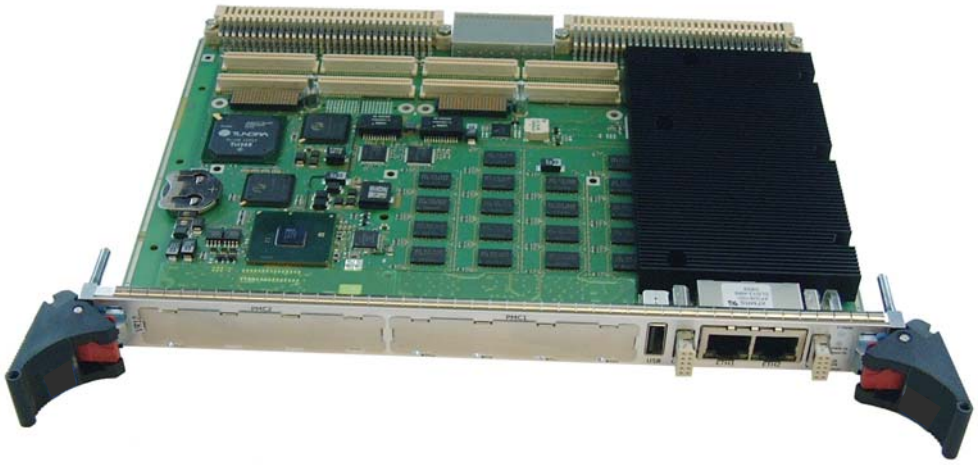
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1 • Introduction

Chapter Scope

This chapter describes features, capabilities, and compatibilities of the VR12 and VP12 VME Single Board Computer (SBC). The two boards are based on the same PCB. All further occurrences of the board's names will be referred to as the VR12. Any further specification in this document referring to VR12 can be applied to VR12 and VP12 unless otherwise noted.

Figure 1-1 VR12 board



1.1 Board Design

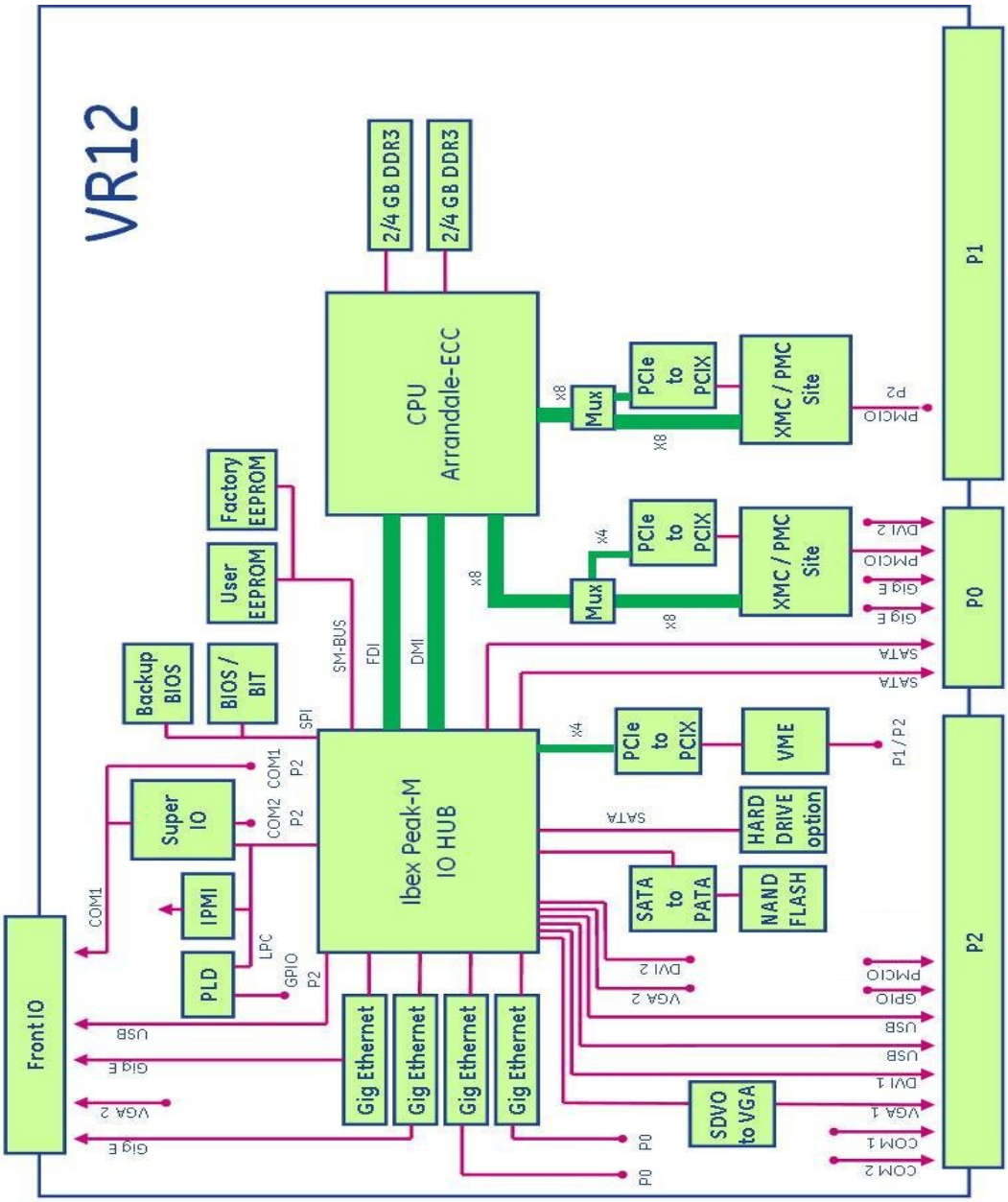
The VR12 is a fully IBM®-AT compatible stand-alone PC. It is equipped with many functions a conventional Personal Computer can only offer after the installation of several add-in cards. Extension boards can be connected via the VME interface. The minimal board size and the large number of I/Os and functions allow the VR12 to be used in many applications.

The VP12 is based on the VR12 but dual slot and provides with a mezzanine card two hard disk bays. The usage of PMC2 and XMC2 is limited see description of these interfaces.

See the following block diagram for the boards design.

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Figure 1-2 VR12 Block Diagram



1.1.1 Design Features

The VR12 VME Single Board Computer features:

Microprocessor

Intel® Core™ i5/i7 mobile processor (up to 4 MB Level3 cache) with integrated dual channel ECC Memory Controller, integrated graphic and PCIe channels

Supported CPUs

i7-610E	2.53 GHz 35 W	SV (Standard Voltage)
i5-520E	2.4 GHz 35 W	SV (Standard Voltage)
i7-620LE	2.0 GHz 25 W	LV (Low Voltage)
i7-620UE	1.06 GHz 18 W	ULV (Ultra Low Voltage)

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Chipset PCH

Intel Series 5 Enhanced Mobile QM57 Peripheral Controller Hub (PCH)

with PCIe channels, SATA, USB, graphic ports, SMBus, LPC, SPI

PCIexpress

Seven PCIexpress links onboard, two XMC x8 slots

SDRAM

onboard soldered, two 72-bit channels, 1 GB to 8 GB DDR3 1066/800 MHz with ECC

SPI Flash UEFI Firmware with Back-up UEFI Firmware

Easy updating, in-system programmable Flash ROM, automatic system configuration, write protected Back-up UEFI Firmware with automatic swap

UEFI Firmware.

Integrated VGA, SATA RAID and Ethernet PXE ROM BIOS

USB mass storage support, password protection, headless support

remote console via serial port

EEPROM (Serial)

512 Kbit for user data via SMBus

CMOS RAM

242 byte non-volatile RAM for UEFI Firmware configuration storage

Hard/Flash Disk

Onboard mountable 2.5″ SATA (3 GB/s) hard disk or FlashDrive.



NOTE

For environmental restrictions please see chapter Specifications.

Keyboard/Mouse

On USB connector, with PS/2 style emulation

USB

One front (not in conduction cooled level) and two rear USB 2.0 ports

Super I/O

SMSC SCH3114 Super I/O with integrated UART ports and System control logic

Watchdog

Watchdog implemented in Super I/O

High Resolution Timer

High-Precision Event Timer (HPET) allows 'Real Time Functions' implemented in PCH chipset, legacy PC-AT timer.

Realtime clock

RTC 146818 compatible, Lithium battery (not with Level C, D, E boards)

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Graphics

Intel Core i5/i7 Mobile CPU integrated Graphic, with four graphic ports at chipset PCH, one front VGA (not with conduction cooled levels), rear with two DVI and one VGA interface

CAUTION

The DVI ports at rear are shared with some PMC2IO signals and GPIO signals.

The rear DVI2 is only available in the configuration with partial PMC-IO or without PMC2.

Make sure, that the PMC-IO pins on the PMC-module don't conflict with the DVI-signals!

Gigabit Ethernet (GigE)

Four 10/100/1000BaseT Ethernet channels (with x1 PCIe interfaces) two front (not with conduction cooled) and two rear, compliant to ANSI/VITA 31.1-2003

SATA

Six SATA, RAID 0/1/10 capable interfaces, two SATA interfaces for onboard devices, and two interfaces at rear I/O (optional four interfaces) and one device for onboard soldered Flash Disk drive (NANDrive). SATA interface is generation 2 (3 Gb/s).

Important note:

CAUTION

The SATA signals at rear are shared with PMC2IO signals.

The rear SATA is only available in the configuration with partial PMC2-IO or without PMC2.

Make sure, that the PMC-IO pins on the PMC-module don't conflict with the SATA-signals!

Internal Flash Disk (NANDrive™)

Onboard soldered Flash Disk (NANDrive) connected via SATA-PATA controller

Floppy

Via USB

Serial I/O

Three asynchronous 16550 compatible full duplex channels with 16 byte FIFO. Two COM ports at rear I/O, transfer rates up to 115.2 KBaud, user selectable RS232/422/485 in UEFI Firmware setup. One COM port RS232 available at front (not with conduction cooled levels D, E)

GPIO

12 GPIO input or output (10 GPIOs pins shared with DVI1; GPIO(0..9) and DVI1 exclude each other)

Write Protection

Hardwire Write Protection of all non-voltage memories, UEFI Firmware flashes, User EEPROM, Flash Disk (NANDrive), Config EEPROMS of PCI bridges and Ethernet controllers

PMC slots

PMC1 and PMC2 with 64 bit/133 MHz PCI-X (3.3 V IO voltage signaling only); PCI mezzanine connector for standard PMC with front and rear IO. IO signals are available at the rear connectors.

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Compliant to ANSI/VITA 20-2001

Non-Monarch option compliant to ANSI/VITA 32-2003

PMC front I/O not available in conduction cooled

PMC bus is not available if a XMC card is installed

XMC slots

Two XMC slot at the PMC location with x8 PCIe lanes each. The PCIe lanes for the XMC are shared with PCIe for the PMC-PCI bridges. If a XMC module is installed the PMC/PCI part is disabled.

VMEbus

PCI bus to VMEbus controller, up to 60 MByte/s transfer rates

FIFOs for write posting, DMA controller with linked list support

Geographical addressing

VMEbus system controller

Master (including RMW) and Slave (including RETRY*) transfer modes:

BLT, ADOH, RMW, RETRY

A64 / A32 / A24 / A16

D64 (MBLT, 2eVME, 2eSST) / D32 / D16 / D8 (SCT, BLT)

IPMI Controller

Hitachi controller for support of Intelligent Platform Management Interface. Implementation according to VITA 38.

Temperature Sensors

Integrated sensors which measure the temperatures of the CPU and PCH dies and in the SuperI/O device for board temperature. The CPU die sensors are software readable in 1 °C increments from 0 °C to +105 °C, the PCH sensor from 59 °C to 125 °C.

Front panel I/O

2 x GigE, VGA2, PMC1 or XMC1, PMC2 or XMC2, USB, Power Button,
LEDs for boot-up and power status indication red/amber/green and four LEDs for BIT status.
For restrictions or conditions see appropriate chapters in this manual

Rear I/O

Via Transition Module VTM24
DVI1, DVI2, VGA1, SATA 4-5, (SATA2-3 please ask factory), COM1-2, two USB, PMC1 I/O and PCM2 I/O, GPIO [0...11], Write Protection, two status LEDs, 2x GigE, Power Button

For restrictions or conditions see appropriate chapters in this manual

Software

Windows®, Linux®, VxWorks®, Solaris®, Integrity (on request)

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Mechanical

6U, 1 slot (4 HP), conduction cooled is IEEE 1101.2-1992 compliant (VR12)

6U, 2 slots (8 HP), air cooled (VP12)

Shock and vibration

Stiffener bars and wedge locks depending on board level

Designed to meet ANSI/VITA 47 classes EAC1, EAC3, EAC6 and ECC4

Conformal coating

Optional

RoHS

Compliant

MTBF

Calculations are available in accordance with MIL-HDBK-217

Safety

Designed to meet standard UL1950, CE class A, FCC-A

Table 1-1 Levels available

VR12 (RoHS)	A	B	C**	D	E	F
low temperature	0°C	-20°C	-40°C	-40°C	-40°C	-40°C
high temperature*						
Front panel	yes	yes	yes			yes
Parts soldered			yes	yes	yes	
Stiffener			yes			
Conformal coating		yes	yes	yes	yes	
Conduction cooling				yes	yes	
Lithium battery	yes	yes				yes



WARNING

The ambient high temperature is very much dependent on the used CPU, air flow and other conditions. See Chapter 8.4 Envrionmental Condition for more details.

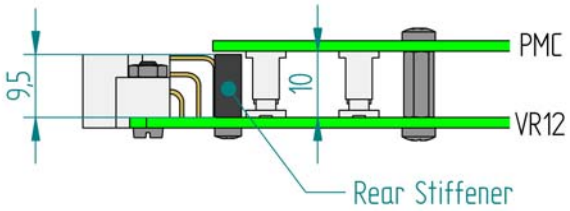


WARNING

** The stiffener (height 9.5 mm) as used in Level C may conflict with components if mounted on the very rear end behind PMC connectors (see drawing below). Check carefully for possible damage or electrical short circuit before installing a PMC mezzanine card. The clearance between the Rear Stiffener and the PMC board is only 0.5 mm. There should be no components in this area.

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Figure 1-3 Rear Stiffener



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2 • Unpacking and Inspection

Chapter Scope This chapter covers the suggested inspection and preparation considerations and background information necessary prior to using the VR12. Unpacking, initial inspection, and first-time operation of the VR12 are covered. Following the procedures given in the chapter is recommended, since they will verify proper operation after shipping and before the product is integrated into your system.

2.1 Delivery Volume

Please check that the delivered package contains the following items:

Table 2-1 Delivery volume

Qty.	Item	Purpose
1	VR12 or VP12	VME Single Board Computer
1	CD-ROM	Technical Product Information with driver software and manuals in Adobe Acrobat (PDF) format:

The manual files are also available through the website:
https://www.abaco.com

2.2 Available Options

The following table lists accessories (options) which are available for the VR12:

Table 2-2 Available options

Item	Purpose
VTM24	Transition module, 4U x 4HE/HP
YLB-CR12-01	10 pin har-Link® to COM Port Sub-D 9 pins adapter cable
YLB-CR12-02	10 pin har-Link to VGA Sub-D15 pins adapter cable

Please contact the Abaco sales department or your sales representative for latest information on options and accessories.

Accessories are subject to change without notice.

2.3 ESD

Electrostatic Discharge Notice

The discharge of static electricity, known as Electro-Static Discharge or ESD, is a major cause of electronic component failure. The VR12 has been packed in a static-safe bag which protects the board from ESD while the board is in the bag. Before removing the VR12 or any other electronic product from its static-safe bag, be prepared to handle it in a static-safe environment.

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You should wear a properly-functioning anti static strap and ensure you are fully grounded. Any surface upon which you place the unprotected VR12 should be static-safe, usually facilitated by the use of anti-static mats. From the time the board is removed from the anti-static bag until it is in the card cage and functioning properly, extreme care should be taken to avoid 'zapping' the board with ESD. You should be aware that you could 'zap' the board without you knowing it; a small discharge, imperceptible to the eye and touch, can often be enough to damage electronic components. Extra caution should be taken in cold and dry weather when static easily builds up.

Only after ensuring that both you and the surrounding area are protected from ESD, carefully remove the board or module from the shipping carton by grasping it by the front panel and the connectors. Place the board, in its antistatic bag, flat down on a suitable surface. You may then remove the board from the anti static bag by tearing the ESD warning labels.

2.4 Warning

This is an FCC Class A product for use in an industrial environment. In a home or residential environment this product may cause radio interference in which case the user may be required to take adequate measures.

NOTE
Drain static electricity before you install or remove any parts. Installing or removing modules without observing this precaution could result in damage to this and/or other modules in your system.

2.5 Initial Inspection

After unpacking the VR12, you should inspect it for visible damage that could have occurred during shipping or unpacking. If damage is observed (usually in the form of bent component leads or loose socketed components), contact Abaco for additional instructions. Depending on the severity of the damage, it may necessary to return the product to the factory for repair.

DO NOT apply power to the board if it has visible damage.

Doing so may cause further, possibly irreparable damage, as well as introduce a fire or shock hazard.

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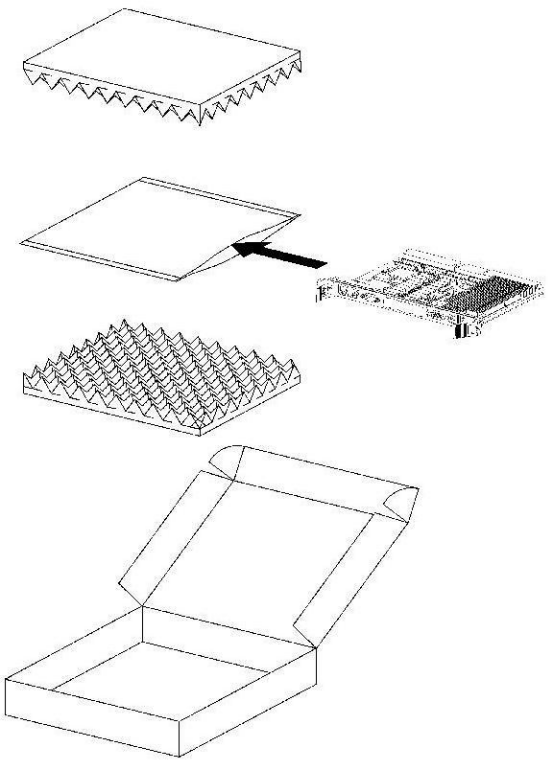
2.6 Unpacking

Please read the manual carefully before unpacking the board or module or fitting the device into your system. Also adhere to the following:

- Please read this manual carefully before unpacking the module or fitting it into your system. This will certainly save time and avoid trouble.
- Observe all precautions for electrostatic sensitive modules
- If the product contains batteries, please do not place the board on conductive surfaces, antistatic plastic, or sponge, which can cause shocks and lead to battery or board trace damage.
- Please do not exceed the specified operational temperatures. Note that batteries and storage devices might also have temperature restrictions.
- Keep all original packaging material for future storage or warranty shipments of the board.

Although the VR12 is carefully packaged to protect it against the rigors of shipping, it is still possible that shipping damages can occur. Careful inspection of the shipping carton should reveal some information about how the package was handled by the shipping service. If evidence of damage or rough handling is found, you should notify the shipping service and Abaco as soon as possible.

Figure 2-1 Board packaging



Retain all packing material in case of future need.

NOTE

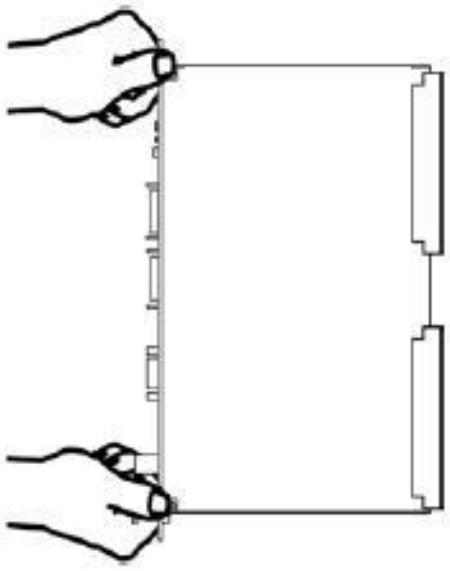
Before installing or removing any board, please ensure that the system power and external supplies have been turned off.

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2.7 Handling

Proper handling of the board or module is critical to ensure proper operation and long-term reliability. When unpacking the board, and whenever handling it thereafter, be sure to hold the board by the front panel as shown. Do not hold the board by the circuit card edges, the heat sink, or the connectors.

Figure 2-2 Handling the VMEboard



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3 • Installation

Chapter Scope This chapter covers the installation of the VR12 VME Single Board Computer on a VME backplane and initial power-on operations.

3.1 Installation preparation

The Character Catalog contains tags that provide predefined styles to modify selected text. Character tags include the following:

Use the following steps to install your Abaco hardware.

- Before installing or removing any board, please ensure that the system power and external supplies have been turned off.
- Check that the jumpers and mezzanines are correctly configured for your application.
- Mount the board/mezzanine/transition module very carefully. See also additional advisories for VMEbus and CompactPCI products below.
- Connect all IO cables.
- Once you are certain that all modules are correctly fitted into the system and all connections have been made properly, restore the power.

3.2 General advice

Please observe all safety procedures to avoid damaging system and protect operators and users.

Before installing or removing any board, please ensure that the system power and external supplies have been turned off.

Check that jumpers and mezzanines are correctly configured for your application. Mount the board, mezzanine, or transition module very carefully. See also sections on additional advisories below.

Do not restore power until you are sure that all modules are fitted correctly and all connections have been made properly.

3.2.1 Advice on VMEbus products

On a standard VMEbus backplane, remove the jumpers on the IACKIN - IACKOUT interrupt daisy-chain (1 jumper) and on the BGxIN - BGxOUT bus grant daisy-chains (4 jumpers) for the slot where the board is to be mounted. The daisy-chain jumpers on the VMEbus backplane should be mounted on all free slots.

Setting jumpers is not necessary for the Abaco Auto-Daisy-Chain VMEbus backplane (order number: VBUSxxAD). Please read additional advisories within the manual.

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A board with system controller functionality must be fitted into slot 1 (for Abaco products, see additional notes within the manual).

The backplane must supply +3.3 V and +5 V.

Because the board is available in several options the description in this chapter is related to the standard configuration.

Mount the CPU board carefully in the VME slot. Note that on some boards connectors are used for I/O purposes and should not be inserted into a VME backplane. A transition module must be used instead.

3.2.2 Advice on Batteries

There is danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by Abaco.

Dispose of used batteries according to instructions of Abaco and applicable local regulations.

3.3 Required items

The following items are required to start the board in a standard configuration:

3.3.1 Backplane and Power Supply

You will need a standard VME backplane wired into a regulated power supply capable of providing stable low noise +5 V and +3.3 V sources. Make sure that the supply is capable of meeting the total power requirements of the VR12. Please refer to chapter 'Specifications' for details.

Initially, you may plug the board into your 3U or 6U system slot of your VMEbus system. Please make sure that you do not have the power supply turned ON while plugging the board into your backplane.

3.3.2 Keyboard and Mouse

You should have a compatible keyboard for initial system operation. Depending on your application, this keyboard may be a standard keyboard, or one which utilizes membrane switches for harsh environments. The keyboard is attached via a USB connector.

3.3.3 Video Monitor

Any VGA-compatible video monitor can be used initially for display output. The VR12 offers front side access to the video signal with har-Link to VGA adapter. Video is also available via the P2/P0 VME connector. In order to get access to these pins it is necessary to use the transition module VTM24*.

3.4 Minimum System Requirements

The VR12 has been thoroughly tested, and is nearly ready for usage in the target system. In order to verify VR12 operation for the first time, it is suggested that you only configure a minimal system. It is not necessary to have disk drives, a

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Flash disk or other accessories connected in order to perform the VR12 POWER-ON-SELF-TEST (POST).

3.4.1 The POST

Each time the computer boots up it must pass the POST (Power-On Self Test). The following is the procedure of the POST:

** The first step of POST is the testing of the Power Supply to ensure that it is turned on and that it releases its reset signal.

** CPU must exit the reset status mode and thereafter be able to execute instructions

** UEFI Firmware was readable

** UEFI Firmware checksum must be valid, meaning that it must be readable.

** CMOS RAM is readable

** CPU must be able to read all forms of memory such as the memory controller, memory bus, and memory module

** The first 1 MB of memory must be operational and have the capability to be read and written to and from, and capable of containing the POST code

** I/O bus / controller must be accessible

If the computer does not pass any of the above tests, the board will fail the POST. An irregular POST presents a beep code which is different from the standard situation which can be either no beep at all or a combination of different beeps indicating what is causing the computer not to pass the POST.

Beep codes can only be heard if the user has a speaker which is either on the board or connected to a transition module.

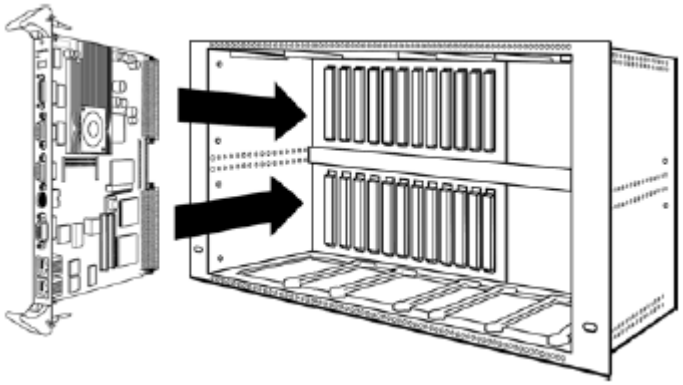
Because the boards are available in several configurations the description in this chapter is related to the standard configuration. See other sections of this document for standard and optional configurations and their influence on initial operation.

3.5 Installation of a plug-in board

Boards are installed in a CPCI or VMEbus chassis by carefully sliding them into the guide rails, inserting them all the way until the handles can be operated to seat and lock the board in place. Handles typically have a lock (snap lever) to unlock them when extracting a board. Older boards may have screws instead of handles to secure the board in place.

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Figure 3-1 6U board insertion into VME box



3.6 Installation of the Rear Transition Module (VTM24)

The VTM24 is a 6U x 80 mm rear I/O module which has to be plugged into the VR12 with the backplane between. This transition module has a DVI or VGA connector which can be used for monitor connection.

Plug the monitor into this connector. Make sure that your selected chassis supports this type of rear I/O transition module.

After making sure that you have installed the VR12 properly into your VME backplane, apply power to your monitor and then the VME supply. When the board is completely reset, the processor should begin executing initial UEFI Firmware-resident routines.

NOTE
If the VR12 was ordered without video onboard, you can use an external video VME card or a video PMC module. Consult the technical descriptions of these boards for required voltage and power consumption in the system.

Please see the chapter 'Interfaces' for details on onboard interfaces where the location of the VR12 interfaces are shown.

3.7 Initial Power-On Operation

After a few seconds, the VR12 system UEFI firmware banner will display on the screen and the LED on the front will switch to non-blinking green.

If you have seen all the on-screen messages to this point, you can be confident that the board is running properly and is ready to be installed and to be set up for your application.

3.8 Entering the UEFI Firmware SETUP

To enter SETUP during the initial power-on sequence, press the DELETE key during the boot up sequence. Also see the applicable on-screen messages when prompted. Press the DELETE key when the LED changes from amber to blinking green.

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Consult the 'User's Manual for AMI UEFI Firmware Setup' for further information on how to change settings and configurations.

If the board does not perform as described above, some damage may have occurred in shipping or the board is not installed or setup properly. Contact Abaco technical support as described in chapter 'Support, Service, and Warranty Information' for further instructions.

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4 • Getting started

Chapter Scope This chapter gives some useful tips when using a board from VR12 family the first time. It might be also useful to read this chapter carefully, when problems came up in using the VR12.

4.1 Power supply

All boards of the VR12 family require up to 60 Watts from the power supply. For exact values please check the current manual in chapter 8 'Specifications', but for rough data a current of up to 10 A at the 5 V rail and 8 A at the 3.3 V rail must be taken into consideration. The VR12 doesn't use +/-12 V but are provided to the PMC connectors for mezzanine which use these voltages. If there are harddisk or PMC modules attached to the VR12, then their power consumption must also be calculated. Keep in mind that standard power supplies often require minimum loads on every supply voltage for proper operation. It might be necessary to add a load to the +12 V to ensure correct voltage levels on 3.3 V and 5 V.

If you ever see the board not starting well or doing resets at random states, please check the voltage of the two supply voltages at the backplane. When measuring there, you can use a standard digital multimeter and you have to attach it to the backplane at positions where no high current is flowing. So better use rear contacts of the bus connectors or unused power connectors to measure, because measuring the voltages at the used power connectors can result in wrong values, which are caused by the high current flowing.

The + 5 V and 3.3 V should reach their nominal value when measuring with a multimeter. If the voltages are less than 5.0 V or 3.3 V, then short voltage drops while the CPU or memory gets into high activities may result in resetting the VR12 board.

4.2 Status indicator, Postcode and Beeps

The VR12 family has dual color LEDs at the front panel (for conduction cooling at back side) for a quick status indicator usage. The possible colors are red, amber or green and the LED can blink in different frequencies or be on continuously.

While running its UEFI Firmware initialization all boards of the VR12 family write checkpoints to port 80h.

- Currently some more debug support is integrated on the VR12 family, which beeps the checkpoint code if the POST stops before the CRT is initialized. The beeps are long for a '1' and short for a '0'. They start with the highest bit 7 and beep 8 represents the lowest bit 0. After some seconds the beep sequence is repeated for an easier recognition. If the beep code is not repeated, then this beeps are issued within the UEFI Firmware execution to show some other failures (i.e. fails in memory detection or if no VGA is detected). For more information please check the UEFI Firmware Check Point and Beep Code List as well as the UEFI Firmware Error Messages.

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4.3 Booting

When switching-on the VR12 following steps are done by hardware:

- On the VR12 family, the voltages at the backplane are monitored until they reach a first trip point which is 3.3 V > 2.9 V and 5 V > 4.3 V. After this the onboard voltages are raised up in a controlled manner to the externally supplied value.
- The continuous red Status LED shows that all circuitry is in reset and the on-board voltages are ramped up.
- When all onboard supply voltages are at their correct values, the 'powergood' status is signaled to all onboard devices and the Status LED is switched to amber (voltages ok but board in reset). And the S-State LED indicates with red the S5 or with amber the S3/S4 state.
- After this the S5 or S3/S4 state changes to S0 and the S-State LED is green. The S0 state switch on the CPU voltage and if the CPU voltage is valid the reset is deasserted (Status LED is off) and the CPU start reading it first instructions from UEFI Firmware. The Status LED is now under control of the UEFI Firmware and is programmed to a red blinking state.

4.4 Setup

When you want to enter the UEFI Firmware Setup, you have to press the keyboard <DEL> or <F2> key at the right moment. Especially when using a slow starting monitor it might be too late to wait for the CRT to show the message 'Press DEL to enter Setup'. Better look for the LED and press <DEL> or <F2> as soon as the LED goes from amber to green blinking. When you are using add on cards with external Option ROM's UEFI Firmware, you can hit the DEL, F2 key while their program runs.

When you miss the right moment to press the <DEL> or <F2> key, please use the power button on the front panel to restart the power up sequence or switch off the power supply for a few seconds and restart it.

4.5 Unexpected Resets

Whenever the VR12 unexpectedly issues a reset and starts booting again, you may want to know the reset source. For this reason a set of special registers is implemented onboard. Every reset source set there a special bit and can be read in the next boot up.

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5 • Interfaces

Chapter Scope

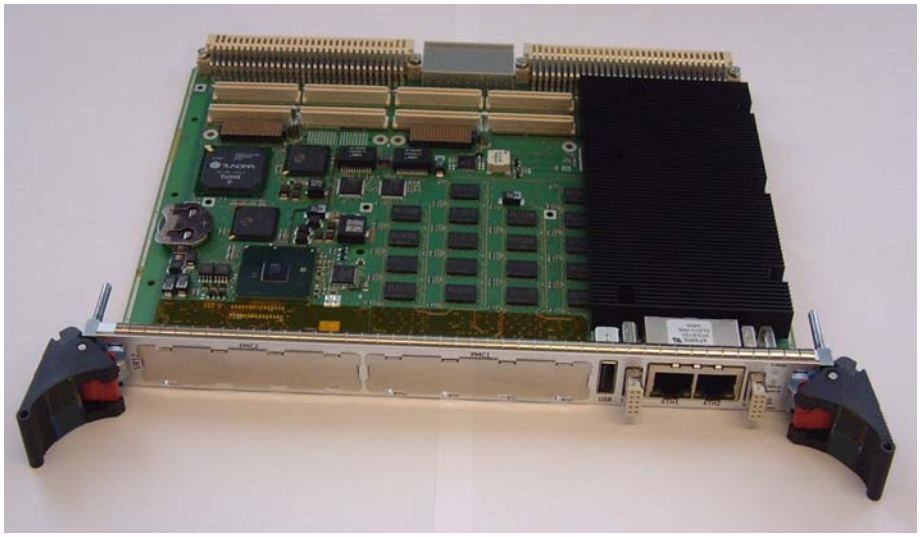
This chapter describes the interfaces of the VR12 VME Single Board Computer located top side on the board and on the front panel. Each section on a particular interface includes a graphical illustration of the connector and a pin assignment table as well as notes on certain signal line characteristics, if necessary.

For information on the interface of expansion and transition modules, please refer to the appropriate chapters in the appendices of this manual.

5.1 Onboard interfaces

Refer to the drawing for the location of interfaces at the VR12 board

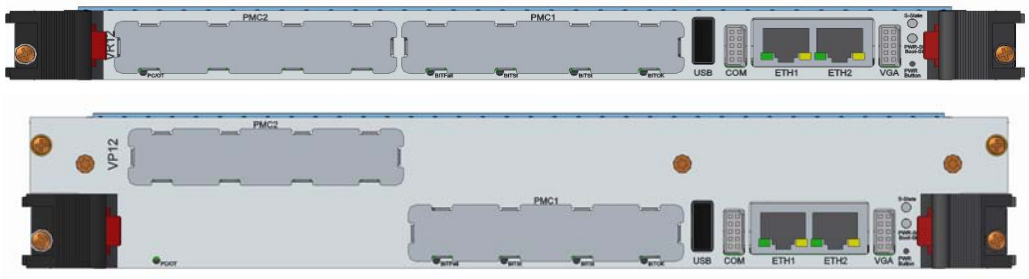
Figure 5-1 VR12 on-board interfaces



5.2 Front Panel Interfaces

Refer to the drawing for the location of interfaces on the front panel of the VR12 single slot board and VP12 dual slot board:

Figure 5-2 Front panel on single VP12 and dual slot board VR12



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5.3 VR12 Connectors

5.3.1 PMC I/O options

There are specific versions of PMC plug-on modules which require specific pin assignments on the VME connectors to be able to use the PMC I/O options and to avoid damage to the VMEbus carrier (base board), VR12 in this case. The correlation between PMC add-on modules and routing of I/O signals from/to the VME backplane via the VR12 needs to be compliant on both ends.

5.3.2 VMEbus Connector P1 (P7301)

The following table lists the pin assignments of connector P1. The connector is compatible to the P1 connector of the VMEbus specifications ANSI/VITA 1 (VME64), ANSI/VITA 1.1 (VME64x), and VITA 38 (System Management).

Table 5-1 VMEbus connector P1

	z	a	b	c	d
1	NC	VMED00	\VMEBBSY	VMED08	+5 V
2	GND	VMED01	\VMEBCLR	VMED09	GND
3	TCK	VMED02	\VMEACFAIL	VMED10	reserved
4	GND	VMED03	\VMEBG0IN	VMED11	reserved
5	TDO	VMED04	\VMEBG0OUT	VMED12	reserved
6	GND	VMED05	\VMEBG1IN	VMED13	reserved
7	TDI	VMED06	\VMEBG1OUT	VMED14	reserved
8	GND	VMED07	\VMEBG2IN	VMED15	reserved
9	TMS	GND	\VMEBG2OUT	GND	\GAP
10	GND	VMESYSCLK	\VMEBG3IN	\VMESYSFAIL	\GA0
11	reserved	GND	\VMEBG3OUT	\VMEBERR	\GA1
12	GND	\VMEDS1	\VMEBR0	\VMESYSRESET	+3.3 V
13	reserved	\VMEDS0	\VMEBR1	\VMELWORD	\GA2
14	GND	\VMEWRITE	\VMEBR2	VMEAM5	+3.3 V
15	reserved	GND	\VMEBR3	VMEA23	\GA3
16	GND	\VMEDTACK	VMEAM0	VMEA22	+3.3 V
17	reserved	GND	VMEAM1	VMEA21	\GA4
18	GND	\VMEAS	VMEAM2	VMEA20	+3.3 V
19	reserved	GND	VMEAM3	VMEA19	SMB_SCL
20	GND	\VMEIACK	GND	VMEA18	+3.3 V
21	reserved	\VMEIACKIN	IPMB_SCL	VMEA17	SMB_SDA
22	GND	\VMEIACKOUT	IPMB_SDA	VMEA16	+3.3 V
23	reserved	VMEAM4	GND	VMEA15	\SMB_ALERT
24	GND	VMEA07	\VMEIRQ7	VMEA14	+3.3 V
25	reserved	VMEA06	\VMEIRQ6	VMEA13	reserved
26	GND	VMEA05	\VMEIRQ5	VMEA12	+3.3 V
27	reserved	VMEA04	\VMEIRQ4	VMEA11	reserved
28	GND	VMEA03	\VMEIRQ3	VMEA10	+3.3 V
29	reserved	VMEA02	\VMEIRQ2	VMEA09	reserved
30	GND	VMEA01	\VMEIRQ1	VMEA08	+3.3 V
31	reserved	-12 V	+5 V STDBY	+12 V	GND
32	GND	+5 V	+5 V	+5 V	+5 V

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5.3.3 VMEbus Connector P2 (P7302)

The following table lists the pin assignments of connector P2. Row b of the connector is compatible to connector P2 of the VMEbus specifications ANSI/VITA 1 (VME64) and ANSI/VITA 1.1 (VME64x).

Rows a and c are compliant to the VMEbus specifications ANSI/VITA 1 (VME64) and ANSI/VITA 1.1 (VME64x), ANSI/VITA 35-2000 chapter 2.3 ´Mapping of Single PMC-P4 to VME-P2-Rows-A,C´.

Table 5-2 VMEbus connector P2

	z	a	b	c	d
1	USB1+	PMC1IO02	+5 V	PMC1IO01	DVI1TXC+ / GPIO0
2	GND	PMC1IO04	GND	PMC1IO03	DVI1TXC- / GPIO1
3	USB1-	PMC1IO06	\RETRY	PMC1IO05	DVI1TX0+ / GPIO2
4	GND	PMC1IO08	VMEA24	PMC1IO07	DVI1TX0- / GPIO3
5	USB0+	PMC1IO10	VMEA25	PMC1IO09	DVI1TX1+ / GPIO4
6	GND	PMC1IO12	VMEA26	PMC1IO11	DVI1TX1- / GPIO5
7	USB0-	PMC1IO14	VMEA27	PMC1IO13	DVI1TX2+ / GPIO6
8	GND	PMC1IO16	VMEA28	PMC1IO15	DVI1TX2- / GPIO7
9	\HW_WP	PMC1IO18	VMEA29	PMC1IO17	DVI1HOTPLG
10	GND	PMC1IO20	VMEA30	PMC1IO19	\PWR_BUT
11	\USB_OC	PMC1IO22	VMEA31	PMC1IO21	\SPEAKER
12	GND	PMC1IO24	GND	PMC1IO23	DVI1_SCL/GPIO8
13	\STAT_LED	PMC1IO26	+5 V	PMC1IO25	DVI1_SDA/GPIO9
14	GND	PMC1IO28	VMED16	PMC1IO27	GPIO10
15	\BITFAIL_LED	PMC1IO30	VMED17	PMC1IO29	GPIO11
16	GND	PMC1IO32	VMED18	PMC1IO31	C1_DSR
17	C1_DCD	PMC1IO34	VMED19	PMC1IO33	C1_RXD
18	GND	PMC1IO36	VMED20	PMC1IO35	C1_RTS
19	VGA1_SCL	PMC1IO38	VMED21	PMC1IO37	C1_TXD
20	GND	PMC1IO40	VMED22	PMC1IO39	C1_CTS
21	VGA1_SDA	PMC1IO42	VMED23	PMC1IO41	C1_DTR
22	GND	PMC1IO44	GND	PMC1IO43	C1_RI
23	VGA1_HSYNC	PMC1IO46	VMED24	PMC1IO45	C2_DCD
24	GND	PMC1IO48	VMED25	PMC1IO47	C2_DSR
25	VGA1_VSYN	PMC1IO50	VMED26	PMC1IO49	C2_RXD
26	GND	PMC1IO52	VMED27	PMC1IO51	C2_RTS
27	VGA1_BLUE	PMC1IO54	VMED28	PMC1IO53	C2_TXD
28	GND	PMC1IO56	VMED29	PMC1IO55	C2_CTS
29	VGA1_GREEN	PMC1IO58	VMED30	PMC1IO57	C2_DTR
30	GND	PMC1IO60	VMED31	PMC1IO59	C2_RI
31	VGA1_RED	PMC1IO62	GND	PMC1IO61	GND
32	GND	PMC1IO64	+5 V	PMC1IO63	+5 V

USB signals	USB...	VGA	VGA...
COM	C1_..., C2_...	DVI	DVI…

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5.3.4 VMEbus Connector P0 (P7300) with partial PMC-I/O

Table 5-3 VMEbus connector P0

	a	b	c	d	e	f
1	nc	nc	nc	nc	nc	GND
2	LPA_DA+	LPA_DA-	GND	LPA_DC+	LPA_DC-	GND
3	LPA_DB+	LPA_DB-	GND	LPA_DD+	LPA_DD-	GND
4	LPB_DA+	LPB_DA-	GND	LPB_DC+	LPB_DC-	GND
5	LPB_DB+	LPB_DB-	GND	LPB_DD+	LPB_DD-	GND
6	\MAACT	\MBACT	VTM+3.3V[1)]	\MALINK	\MBLINK	GND
7	SATATX2+[2)] / PMC2IO05	SATATX2-[2)] / PMC2IO04	PMC2IO03	PMC2IO02	PMC2IO01	GND
8	SATARX2+ [2)] / PMC2IO10	SATARX2-[2)] / PMC2IO09	PMC2IO08	PMC2IO07	PMC2IO06	GND
9	SATATX3+ [2)]/ PMC2IO15	SATATX3-[2)] / PMC2IO14	PMC2IO13	PMC2IO12	PMC2IO11	GND
10	SATARX3+ [2)] / PMC2IO20	SATARX3- [2)] / PMC2IO19	PMC2IO18	PMC2IO17	PMC2IO16	GND
11	PMC2IO25	PMC2IO24	PMC2IO23	PMC2IO22	PMC2IO21	GND
12	PMC2IO30	PMC2IO29	PMC2IO28	PMC2IO27	PMC2IO26	GND
13	PMC2IO35	PMC2IO34	PMC2IO33	PMC2IO32	PMC2IO31	GND
14	VGA2_SDA[2]/ PMC2IO40	PMC2IO39	PMC2IO38	PMC2IO37	PMC2IO36	GND
15	VGA2_RED[2]/ PMC2IO45	VGA2_GREEN[2] / PMC2IO44	VGA2_BLUE[2]/ PMC2IO43	VGA2_HSYNC[2] / PMC2IO42	VGA2_SCL[2]/ PMC2IO41	GND
16	DVi2TXC- / PMC2IO50	DVi2TC+ / PMC2IO49	SATARX5+ / PMC2IO48	SATARX5- / PMC2IO47	VGA2_VSYNC[2] / PMC2IO46	GND
17	DVi2TX0- / PMC2IO55	DVi2TX0+ / PMC2IO54	DVi2HTPLG/ PMC2IO53	SATATX5+ / PMC2IO52	SATATX5- / PMC2IO51	GND
18	DVi2TX1- / PMC2IO60	DVi2TX1+ / PMC2IO59	DVi2_SCL/ PMC2IO58	SATARX4+ PMC2IO57	SATARX4- / PMC2IO56	GND
19	DVi2TX2-	DVi2TX2+ / PMC2IO64	DVI2_SDA/ PMC2IO63	SATATX4+ / PMC2IO62	SATATX4- / PMC2IO61	GND

Signal groups:

DVI and VGA: DVI... and VGA....

Gigabit Ethernet LPA_… and LPB_…

Note

1. This is the only 3.3 VDC source for the Transition Module VTM24. Do not connect the +3.3V pin to +3.3 V backplane power.
2. SATA2/3 connection for VR11 compliant SATA pin-out and VGA2 at rear are only available at special request.

Note:

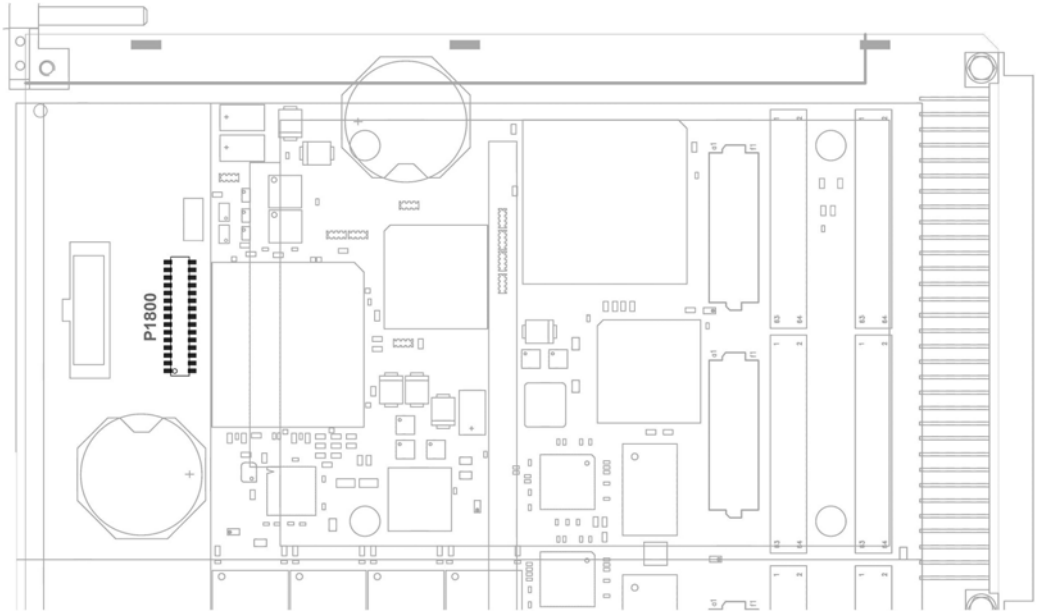
The LAN pin assignment is compliant to the VITA 31.1 specification 'Gigabit Ethernet on VME64x Backplanes'.

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5.3.5 SATA Connector (P1800)

Two onboard SATA interfaces are available at a 30 pin 1.27 mm pitch female onboard connector P1800. An adapter card (HD-ADAP3) provides the interface to a 2.5-inch SATA hard disc or for VP12 boards the SATA interfaces are available with a mezzanine card (HD-ADAP5).

Figure 5-3 SATA connector



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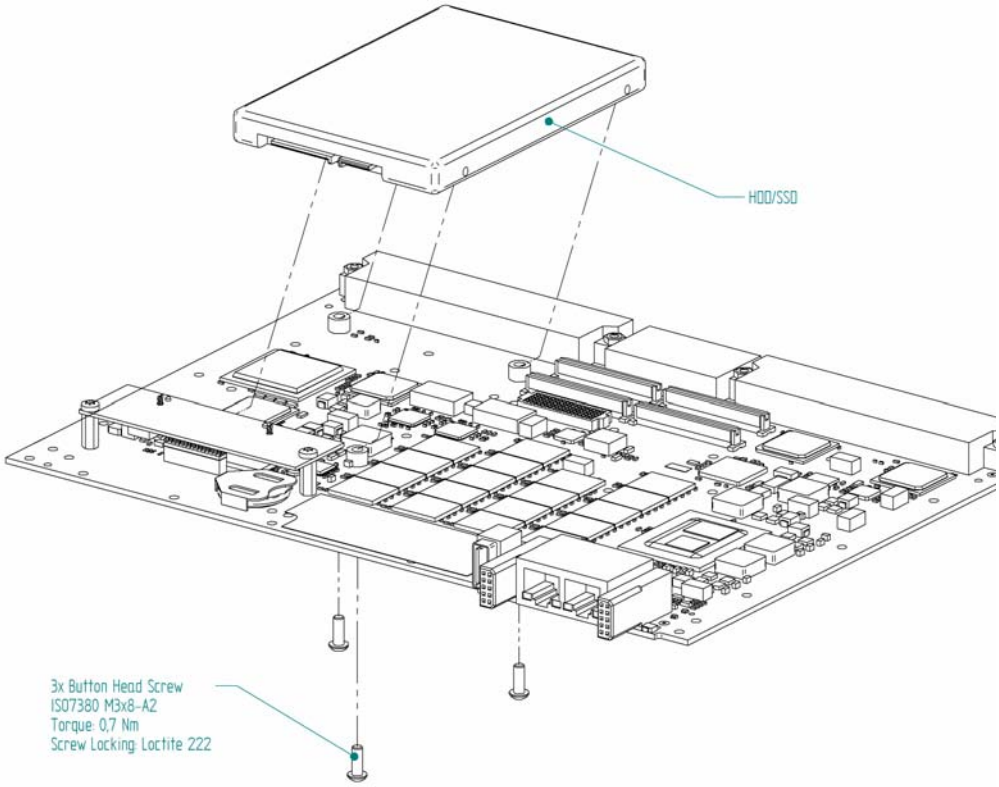
5.3.6 Customer-provided SATA HDD

There is a board option which enables the customer to supply his own hard disk. The mounting option, including required screws for fastening are shown in the drawing below. The customer provides the mounting screws.

WARNING

Abaco shall have no liability whether in contract, tort, negligence, or otherwise, to Customer with respect to non-Abaco manufactured products, or for any failure or damage caused by the interconnection or use of the product in combination with equipment, software or other devices not made or supplied by Abaco.

Figure 5-4 Mounting option for customer-supplied HDD



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5.3.7 Ethernet Interface (P5050)

The VR12 has four Gigabit Ethernet channels. Two Gigabit Ethernet channels with RJ45 jacks are available at front.

Figure 5-5 Ethernet connector

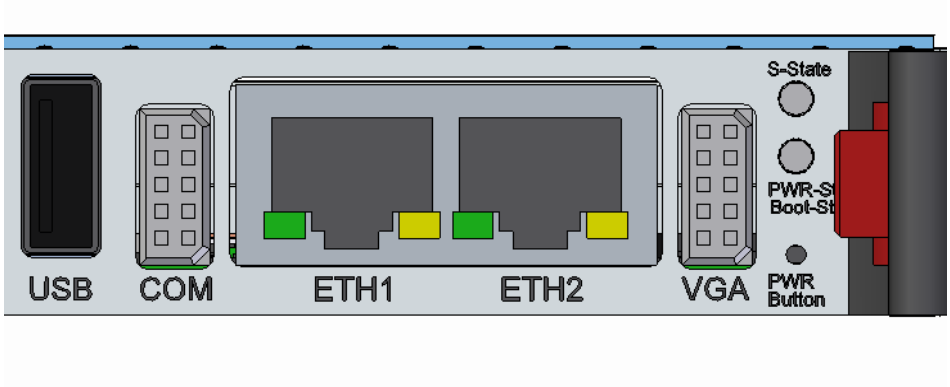


Table 5-4 Ethernet 1/2 connector

Name 10/100base	Name 1000base	Ethernet1, 2
TxD+	LP_DA+	1
TxD-	LP_DA-	2
RxD+	LP_DB+	3
NC	LP_DC+	4
NC	LP_DC-	5
RxD-	LP_DB-	6
NC	LP_DD+	7
NC	LP_DD-	8

Two LEDs (green and yellow) are integrated in each of the RJ45 connector. These LEDs indicate the link status of the interface.

Table 5-5 LEDs on Ethernet connector

LED green	Function
On	Link
Off	No link
LED yellow	Function
On, blink	Tx/Rx activity
Off	No activity

5.3.8 Serial Port COM3 (P2350)

The VR12 offers three serial ports. COM3 is accessible via the front panel har-Link connector. COM3 at front is RS232 only. A short cable is available to convert the 10 pin har-Link connector P2350 to a standard Sub-D9 connector.

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Figure 5-6 COM3 location



Table 5-6 COM3 pin assignments

Name RS232	P2350 (har-Link connector	DSUB male Connector
DSR	E1	6
DCD	E2	1
DTR	D1	4
GND	C2	5
RXD	A1	2
TXD	B1	3
CTS	D2	8
RTS	A2	7
RI	B2	9
RS232 driver disable*	C1	n/a
Shield	Z2	Shield

*: As the front VGA2 and COM3 are realized with the same connector type the pinning of the VGA har-Link cable disable the RS232 driver if the VGA cable is erroneously connected to a COM Port.

5.3.9 VGA2 Interface (P4100)

The VR12 offers four graphic ports. One of these ports is accessible as VGA2 at front. The front panel connector is a 10 pin har-Link connector.

A short cable is optionally available to convert the har-Link connector P4100 to a standard Sub-D15 female connector.

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Figure 5-7 VGA2 interface

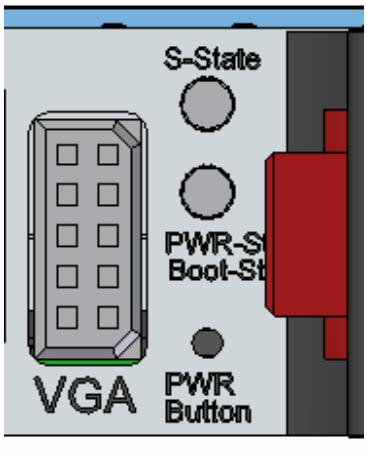


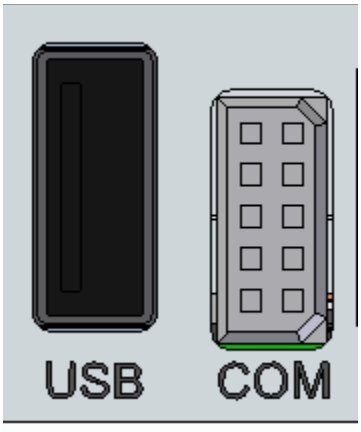
Table 5-7 VGA2 connector pin assignments

Name	P1200 (har-Link connector)	DSUB female connector
RED2	A2	1
GREEN2	B1	2
BLUE2	A1	3
HSYNC2	D1	13
VSYNC2	D2	14
DDC-Data2	E2	12
DDC-Clock2	E1	15
GND	C1, B2, C2	5, 6, 7, 8, 10
Shield	Z2	Shield

5.3.10 USB Interface (P1680)

One USB channel (USB9) is available at the front panel and two USB channels (USB0, USB1) are available on rear IO.

Figure 5-8 USB



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Figure 5-9 USB pin assignments

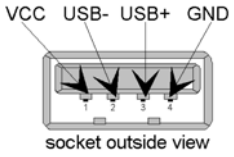


Table 5-8 USB pin assignments

Name	P1680
USB_VCC 1)	1
USB9-	2
USB9+	3
GND	4

1) the USB_VCC pin has a 2 A fuse. For normal operation don't exceed 100 mA current. The fuse automatically recovers if the over-current condition is removed.

5.3.11 PMC1 Connectors (P7101, P7102, and P7103)

The following table lists the pin assignments of the onboard PMC1 connector. The PMC1 slot is 64 bit and up to PCI-X 133 MHz capable and works with a PCIe-PCI bridge Pericom PI7C9X130. The PCI bridge and PMC1-bus is disabled when no PMC card is installed (\PRESENT pin is high) or a XMC card is installed at this slot. The PMC disabling can be overruled by UEFI Firmware Setup adjustments (see User Manual for AMI UEFI Firmware Setup).

The PMC is electrically and mechanically compliant to the specification IEEE 1386 and 1386.1 with enhancements of the Processor PMC Standard VITA 32-2003. These enhancements provide pins for a second device; (IDSELB and REQB/ GNTB) but they do not support a monarch PMC card.

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The PCI signaling voltage is fixed to 3.3 V but +5 V tolerant.

Table 5-9 PMC1 connector pin assignments

P7101	P7102	P7103	Pin	Pin	P7101	P7102	P7103
NC	+12 V	Reserved	01	02	-12 V	NC	GND
GND	NC	GND	03	04	\PMC1IRQA	NC	C/\BE7
\PMC1IRQB	NC	C/\BE6	05	06	\PMC1IRQC	GND	C/\BE5
\PRESENT	GND	C/\BE4	07	08	+5 V	Reserved	GND
\PMC1IRQD	Reserved	V(I/O)	09	10	Reserved	Reserved	PAR64
GND	PUP [a]	AD63	11	12	NC	+3.3 V	AD62
PCICLK	\PCIRST	AD61	13	14	GND	PDN [a]	GND
GND	+3.3V	GND	15	16	\GNT0	PDN [a]	AD60
\REQ0	\PME	AD59	17	18	+5 V	GND	AD58
V(I/O)	AD30	AD57	19	20	AD31	AD29	GND
AD28	GND	V(I/O)	21	22	AD27	AD26	AD56
AD25	AD24	AD55	23	24	GND	+3.3V	AD54
GND	AD24 (IDSEL)	AD53	25	26	C/\BE3	AD23	GND
AD22	+3.3 V	GND	27	28	AD21	AD20	AD52
AD19	AD18	AD51	29	30	+5 V	GND	AD50
V(I/O)	AD16	AD49	31	32	AD17	C/\BE2	GND
\FRAME	GND	GND	33	34	GND	AD25 (IDSELB)	AD48
PCIXCAP	\TRDY	AD47	35	36	\IRDY	+3.3 V	AD46
\DEVSEL	GND	AD45	37	38	+5 V	\STOP	GND
GND	\PERR	V(I/O)	39	40	\LOCK	GND	AD44
Reserved	+3.3 V	AD43	41	42	RES.	\SERR	AD42
PAR	C/\BE1	AD41	43	44	GND	GND	GND
V(I/O)	AD14	GND	45	46	AD15	AD13	AD40
AD12	M66EN	AD39	47	48	AD11	AD10	AD38
AD9	AD8	AD37	49	50	+5V	+3.3 V	GND
GND	AD7	GND	51	52	C/\BE0	\REQB	AD36
AD6	+3.3 V	AD35	53	54	AD5	\GNTB	AD34
AD4	Reserved	AD33	55	56	GND	GND	GND
V(I/O)	NC	V(I/O)	57	58	AD3	NC	AD32
AD2	GND	Reserved	59	60	AD1	\RSTOUT	Reserved
AD0	\ACK64	Reserved	61	62	+5 V	+3.3 V	GND
GND	GND	GND	63	64	\REQ64	NC	Reserved

[a] 330R pull-down (PDN) to GND and 4.7k pull-up (PUP) to VIO.

NC Not connected

Reserved Do not connect anything

V(I/O) I/O Voltage, connected with +3.3V

+12V/-12V Only available if connected at the VME backplane.

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5.3.12 PMC2 Connectors (P7201, P7202, and P7203)

PMC2 is available on a VR12 when there is no on-board SATA connector (P1800). On a dual slot VP12, the PMC2 is available in the second slot in this case the PMC is restricted to conventional PCI66.

The PCI signaling voltage is fixed to 3.3 V but +5V tolerant.

The following table lists the pin assignments of the PMC2 connector. The PMC2 slot is 64 bit and PCI-X 133 MHz capable and works with a PCIe-PCI bridge Pericom PI7C9X130. The PCI bridge and PMC2-bus is disabled when no PMC card is installed (\PRESENT pin is high) or a XMC card is installed at this slot. The PMC disabling can be overuled by UEFI Firmware Setup adjustments (see User Manual for AMI UEFI Firmware Setup).

The PMC is electrically and mechanically compliant to the specification IEEE 1386 and 1386.1 with enhancements of the Processor PMC Standard VITA 32-2003. These enhancements provide pins for a second device; (IDSELB and REQB/GNTB) but they do not support a monarch PMC card.

Table 5-10 PMC2 connector pin assignment

P7201	P7202	P7203	Pin	Pin	P7201	P7202	P7203
NC	+12 V	Reserved	01	02	-12 V	NC	GND
GND	NC	GND	03	04	\PMC2IRQA	NC	C/BE7
\PMC2IRQB	NC	C/BE6	05	06	\PMC2IRQC	GND	C/BE5
\PRESENT	GND	C/BE4	07	08	+5 V	Reserved	GND
\PMC2IREQD	Reserved	V(I/O)	09	10	Reserved	Reserved	PAR64
GND	PUP [a]	AD63	11	12	NC	+3.3 V	AD62
PCICLK	\PCIRST	AD61	13	14	GND	PDN [a]	GND
GND	+3.3V	GND	15	16	\GNT0	PDN [a]	AD60
\REQ0	\PME	AD59	17	18	+5 V	GND	AD58
V(I/O)	AD30	AD57	19	20	AD31	AD29	GND
AD28	GND	V(I/O)	21	22	AD27	AD26	AD56
AD25	AD24	AD55	23	24	GND	+3.3V	AD54
GND	AD24 (IDSEL)	AD53	25	26	C/\BE3	AD23	GND
AD22	+3.3 V	GND	27	28	AD21	AD20	AD52
AD19	AD18	AD51	29	30	+5 V	GND	AD50
V(I/O)	AD16	AD49	31	32	AD17	C/\BE2	GND
\FRAME	GND	GND	33	34	GND	AD25 (IDSELB)	AD48
PCIXCAP	\TRDY	AD47	35	36	\IRDY	+3.3 V	AD46
\DEVSEL	GND	AD45	37	38	+5 V	\STOP	GND
GND	\PERR	V(I/O)	39	40	\LOCK	GND	AD44
Reserved	+3.3 V	AD43	41	42	RES.	\SERR	AD42
PAR	C/\BE1	AD41	43	44	GND	GND	GND
V(I/O)	AD14	GND	45	46	AD15	AD13	AD40
AD12	M66EN	AD39	47	48	AD11	AD10	AD38
AD9	AD8	AD37	49	50	+5V	+3.3 V	GND
GND	AD7	GND	51	52	C/\BE0	\REQB	AD36

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Table 5-10 PMC2 connector pin assignment (Continued)

P7201	P7202	P7203	Pin	Pin	P7201	P7202	P7203
AD6	+3.3 V	AD35	53	54	AD5	\GNTB	AD34
AD4	Reserved	AD33	55	56	GND	GND	GND
V(I/O)	NC	V(I/O)	57	58	AD3	NC	AD32
AD2	GND	Reserved	59	60	AD1	\RSTOUT	Reserved
AD0	\ACK64	Reserved	61	62	+5 V	+3.3 V	GND
GND	GND	GND	63	64	\REQ64	NC	Reserved

[a] 330R pull-down (PDN) to GND and 4.7k pull-up (PUP) to VIO.

NC Not connected

Reserved Do not connect anything

V(I/O) I/O Voltage, connected with +3.3V

+12V/-12V Only available if connected at the VME backplane.

5.3.13 PMC-I/O Connector (P7204 and P7204)

Pin 1 of the I/O connector is PMCxIO_01. Pin 2 is PMCxIO_02 and so on. The x denotes PMC1 or PMC2 respectively. All traces are not connected to any onboard signal, and signal routing is neither paired nor length-matched to the backplane connectors.

Important note:

CAUTION

Some PMC2IO signals to the rear connector are shared with rear SATA, DVI2 and VGA2 signals.

All PMC2IO signals are only available in the configuration with full PMC-IO.

Make sure that the PMC-IO pins on the PMC module do not conflict with the shared signals!

5.3.14 XMC1 Connector (P7105)

The following table lists the pin assignments of the onboard XMC1 connector. The XMC1 slot provides a x8 lane wide PCI Express interface. Only if a XMC mezzanine board is installed and set the signal \XMC1_PRESENT to low the PCI express lanes are muxed to the XMC slot otherwise these lanes are used for the PMC1 bridge.

The XMC is electrically and mechanically compliant to the specification VITA 42.0 and IEEE 1386.1.

Table 5-11 XMC1 connector pin assignments

Pin	A	B	C	D	E	F
1	PERX8P	PERX8N	+3.3V	PERX9P	PERX9N	+5V
2	GND	GND	not used	GND	GND	\XMCRSTIN
3	PERX10P	PERX10N	+3.3V	PERX11P	PERX11N	+5V
4	GND	GND	not used	GND	GND	\XMC2RSTO
5	PERX12P	PERX12N	+3.3V	PERX13P	PERX13N	+5V
6	GND	GND	not used	GND	GND	+12V
7	PERX14P	PERX14N	+3.3V	PERX15P	PERX15N	+5V
8	GND	GND	not used	GND	GND	-12V
9	NC	NC	NC	NC	NC	+5V
10	GND	GND	NC	GND	GND	GA0

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Table 5-11 XMC1 connector pin assignments (Continued)

Pin	A	B	C	D	E	F
11	PETX8P	PETX8N	+3.3V	PETX9P	PETX9N	+5V
12	GND	GND	GA1	GND	GND	\XMC1_PRESENT
13	PETX10P	PETX10N	+3.3V	PETX11P	PETX11N	+5V
14	GND	GND	GA2	GND	GND	SDA
15	PETX12P	PETX12N	NC	PETX13P	PETX13N	+5V
16	GND	GND	XMCWP	GND	GND	SCL
17	PETX14P	PETX14N	NC	PETX15P	PETX15N	NC
18	GND	GND	NC	GND	GND	NC
19	CKXMC1P	CKXMC1N	NC	\WAKE	NC	NC

5.3.15 XMC2 Connector (P7205)

The following table lists the pin assignments of the onboard XMC2 connector. The XMC2 slot provides a x8 lane wide PCI Express interface. Only if a XMC mezzanine board is installed and set the signal \XMC2_PRESENT to low the PCI express lanes are muxed to the XMC slot otherwise these lanes are used for the PMC2 bridge. XMC2 is not available with VP12 configuration

The XMC is electrically and mechanically compliant to the specification VITA 42.0 and IEEE 1386.1.

Table 5-12 XMC2 connector pin assignments

Pin	A	B	C	D	E	F
1	PERX0P	PERX0N	+3.3V	PERX1P	PERX1N	+5V
2	GND	GND	not used	GND	GND	\XMCRSTIN
3	PERX2P	PERX2N	+3.3V	PERX3P	PERX3N	+5V
4	GND	GND	not used	GND	GND	\XMC1RSTO
5	PERX4P	PERX4N	+3.3V	PERX5P	PERX5N	+5V
6	GND	GND	not used	GND	GND	+12V
7	PERX6P	PERX6N	+3.3V	PERX7P	PERX7N	+5V
8	GND	GND	not used	GND	GND	-12V
9	NC	NC	NC	NC	NC	+5V
10	GND	GND	NC	GND	GND	GA0
11	PETX0P	PETX0N	+3.3V	PETX1P	PETX1N	+5V
12	GND	GND	GA1	GND	GND	\XMC2_PRESENT
13	PETX2P	PETX2N	+3.3V	PETX3P	PETX3N	+5V
14	GND	GND	GA2	GND	GND	SDA
15	PETX4P	PETX4N	NC	PETX5P	PETX5N	+5V
16	GND	GND	XMCWP	GND	GND	SCL
17	PETX6P	PETX6N	NC	PETX7P	PETX7N	NC
18	GND	GND	NC	GND	GND	NC
19	CKXMC2P	CKXMC2N	NC	\WAKE	NC	NC

5.4 Transition Module

Please refer to the appendix A for interface location and connector pin assignments for the optional extension boards and transition modules.

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6 • Resources

Chapter Scope This chapter describes system resources, such as memory mapping, register set and default interrupt request assignments.

6.1 Memory Map

The table below shows the memory address area used by the VR12.

Table 6-1 Memory map

Address	Size	Used by
$0 - $9_FFFF	640 KBytes	System RAM
$A_0000 - $B_FFFF	128 KBytes	Video RAM (if enabled)
$C_0000 - $D_FFFF	128 KBytes	Used by PCI ROMs, Add-on cards
$E_0000 - $F_FFFF	128 KBytes	UEFI Firmware
$10_0000 - $EFFF_FFFF	depends on available DRAM	Extended RAM
$4000_0000 - $FFBF_FFFF	depends on available DRAM	Dynamically used by PCI devices
$FF80_0000 - $FFFF_FFFF	8 MBytes	SPI ROM (UEFI Firmware and descriptors)

6.2 Register Set

The following section provides an overview of the registers located in the I/O address area of the VR12.

NOTE
The address locations of the PCI devices, such as SCSI or Ethernet, are not described in the following tables, because the UEFI Firmware automatically configures all PCI devices.

6.2.1 Standard Register Set

The standard register set is equal to all standard PC/AT systems. The table below provides an overview of the address ranges occupied by these registers.

Table 6-2 Standard register set

I/O Address Range (Hex)	Function
$00h – $0Fh	DMA Controller 1
$20h – $21h	Interrupt Controller 1
$40h – $43h	Counter / Timer
$60h	Keyboard Controller
$61h	NMI Status and Control
$64h	Keyboard Controller
$70h – $71h	RTC, NMI Mask
$80h – $8Fh	DMA Page register
$A0h – $A1h	Interrupt Controller 2
$B2h – $B3h	Power Management
$C0h – $DEh	DMA Controller 2
$F0h – $F1h	Coprocessor

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Table 6-2 Standard register set (Continued)

I/O Address Range (Hex)	Function
$170h – $177h	Secondary SATA
$1F0h – $1F7h	Primary SATA
$2E8h – $2Efh	COM port [a]
$2F8h - $2FFh	COM port [a]
$3E8h – $3Efh	COM port [a]
$3E8h – $3Efh	COM port [a]
$680h – $68Fh	VR12 specific [b]

[a] Via setup four address ranges can be defined for the serial interfaces.
[b] Used for onboard programmable options. They are not intended to be used by normal users.

6.3 Interrupts

The interrupt routing for standard components such as COM1/2 is in compliance with standard PC/AT systems. Unused interrupts can be used for add-on cards or other board specific PCI devices such as SCSI and Ethernet.

Table 6-3 Interrupt assignments

Hardware IRQ	IRQ Source
INTC1	
IRQ00	System Timer
IRQ01	Keyboard [a]
IRQ02	Cascade from INTC2
IRQ03	COM2 / COM1 [b]
IRQ04	COM1 / COM2 [b]
IRQ05	COM3[b]
IRQ06	
IRQ07	
INTC2	
IRQ08	Real Time Clock
IRQ09	Power Management Control
IRQ10	PnP/PCI [b]
IRQ11	PnP/PCI [b]
IRQ12	PS/2 Mouse [a]
IRQ13	Numeric Coprocessor
IRQ14	External IDE [d]
IRQ15	Onboard IDE [e]
NMI	Parity Error, ECC Error, System Error

[a] Emulated interrupt from USB keyboard/mouse.
[b] Interrupts are available for Plug and Play PCI devices
[d] This interrupt is available for other devices when the primary IDE is disabled in SETUP or when IDE is configured to 'native PCI' mode.
[e] This interrupt is available when the secondary IDE is disabled in SETUP or when IDE is configured to 'native PCI' mode.

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6.4 APIC Controller

The VR12 supports APIC (Advanced Programmable Interrupt Controller). This handling of the APIC interrupt services must be supported by the operating system. The I/O APIC handles interrupts very differently than the standard interrupt controller. Briefly, these differences are:

- Method of Interrupt Transmission. The I/O APIC transmits interrupts through processor FSB, and interrupts are handled without the need for the processor to run an interrupt acknowledge cycle.
- Interrupt Priority. The priority of interrupts in the I/O APIC is independent of the interrupt number. For example, interrupt 10 may be given a higher priority than interrupt 3.
- More Interrupts. The three I/O APICs in the VR12 support a total of 24 independent interrupt sources.

6.5 Message Signaled Interrupts

The VR12 supports Message Signaled Interrupts (MSI) on all its PCIe links for transporting interrupts from PCIe devices towards the CPU.

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7 • Function Blocks

Chapter Scope This section gives a brief overview of the VR12 VME Single Board Computer onboard devices software interfaces.

7.1 Processor

The Intel dual core i5/i7 processor family provides high performance with low power and features integrated memory hub and 2D/3D graphic controller. Enhanced Intel® Turbo Boost® technology which provides the ability to dynamically adjust the power and performance of the processor based on CPU and graphic demand. This results in optimal performance without compromising the power performance of the VR12.

The processor die is thermally protected by two thermal monitor features. When reaching a maximum safe operating temperature the Thermal Control Circuit in the processor activates a frequency reducing feature and reduces the voltage and frequency dynamically. If this feature is active, the VR12 will indicate it with short clicks at the speaker and short blinks at the PC/OT LED. In case of a catastrophic die overheating (above 125 °C), the VR12 switches off the processor core voltage. Recovery from this catastrophic event can be done with a power off-on cycle or Power Button.

Overview of processor feature

- Two execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data second-level cache (L2) for each core
- Up to 4-MB shared instruction/data third-level cache (L3), shared among all cores
- Intel Virtualization Technology (Intel VT-x)
- Intel Virtualization Technology for Directed I/O (Intel VT-d)
- Intel Trusted Execution Technology (Intel TXT)
- Intel Streaming SIMD Extensions (Intel SSE4.1, 4.2)
- Intel Hyper-Threading Technology (Intel HT Technology)
- Intel 64 architecture
- 6 Advanced Encryption Standard New Instructions (AES-NI)
- Intel Turbo Boost Technology
- Gen1 (2.5 GT/s) PCI Express frequency is supported
- Gen1 Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- DMI interface to the maximum theoretical bandwidth on interface of 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s when DMI x4
- The integrated graphics controller contains a refresh of the fifth generation graphics core
- Intel Dynamic Video Memory Technology (Intel DVMT) support

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- Intel Graphics Performance Modulation Technology (Intel GPMT)
- Intel Smart 2D Display Technology (Intel S2DDT)
- Intel Clear Video Technology
- 12 Execution Units
- Dedicated analog and digital display ports are supported through the Intel 5 Series Chipset PCH
- FDI bus carries display traffic from the integrated graphics controller in the processor to the legacy display connectors in the PCH with a transfer rate of 2.7 GT/s.
- Support of ACPI C-states as implemented by the following processor C-states:
  - C0, C1, C1E, C3 (no C6 support)
- Enhanced Intel SpeedStep® Technology
- S0, S3, S4, S5 States

7.2 Memory Controller

The CPU integrated dual channel memory controller in the VR12 supports double data rate synchronous DRAM (DDR3) with a data bus width of 64 bits + ECC. One, two or four banks are provided by the VR12 with a size of either 1 GByte or 2 GByte. This results in a minimum memory size of 1 GByte and a maximum size of 8 GByte.

Memory Controller features:

- One or two channels of DDR3 memory with a maximum of two ranks per channel
- Single- and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- Memory DDR3 data transfer rates of 800 MT/s (ULV) and 1066 MT/s (SV,LV)
- 64-bit wide channels and 8 bit ECC
- DDR3 I/O Voltage of 1.5 V
- unbuffered DDR3
- Theoretical maximum memory bandwidth of:
  - 12.8 GB/s in dual-channel mode assuming DDR3 800 MT/s
  - 17.1 GB/s in dual-channel mode assuming DDR3 1066 MT/s
- 1-Gb, and 2-Gb DDR3 DRAM technologies are supported for x8 devices.
- Using 2-Gb device technologies, the largest memory capacity possible is 8 GB,
- Up to 32 simultaneous open pages, 16 per channel (assuming 4 Ranks of 8 Bank Devices)

7.3 Chipset

The CPU is supported by the Chipset Intel Series 5 PCH QM57 which provides extensive I/O support of the VR12. This includes:

- PCI Express Base of 5 ports
- ACPI Power Management Logic Support, Revision 3.0b

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- Enhanced DMA controller, interrupt controller, and timer functions
- Integrated Serial ATA host controllers with independent DMA operation on up to six ports
- USB host interface; two EHCI high-speed USB 2.0 Host controllers and 2 rate matching hubs
- System Management Bus (SMBus)
- Supports Intel Rapid Storage Technology
- Supports Intel Active Management Technology
- Supports Intel Virtualization Technology for Directed I/O
- Supports Intel Trusted Execution Technology
- Supports buffered mode generating extra clocks from a clock chip
- Analog and Digital Display ports
  - Analog CRT
  - DVI
  - SDVO
- Low Pin Count (LPC) interface
- Serial Peripheral Interface (SPI) support

7.4 Interrupt Controller

The Interrupt controller on a standard PC consists of two 82C59A devices with eight interrupt request lines each. The two controllers are cascaded so that 14 external and two internal interrupt sources are available. The master interrupt controller provides IRQ [7...1]; the slave interrupt controller provides IRQ [15...8]. IRQ2 is used to cascade the two controllers, IRQ0 is used as a system timer interrupt and is tied to interval timer 1, counter 0. The remaining 14 interrupt lines are mapped to various onboard devices. Each 82C59A provides several internal registers. The interrupts on the IRQ input lines are handled by two registers, the interrupt request register IRR and the in-service register ISR. For programming details see the 82C59A data sheet. The VR12 support also the Interrupt handling of the APIC (Advanced Interrupt Controller). This handling of the APIC interrupt services must be supported by the operating system. The I/O APIC handles interrupts very differently than the 8259.

7.5 Timer

VME Single Board Computers like the VR12 are equipped with an 8254 compatible timer. This timer contains three counters. Each counter output provides a key system function. Counter 0 is connected to interrupt controller input IRQ0 and provides a system timer interrupt for time-of-day, floppy disk timeout and other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the sound for the speaker.

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The following table gives an overview over the 8254 functions.

Table 7-1 Interval timer functions

Interval Timer Functions	
Function	Counter 0 (System Timer)
Gate	Always on
Clock In	1.193 MHz (OSC/12)
Out	IRQ0 (INT1)
Function	Counter 1 (Refresh Request)
Gate	Always on
Clock In	1.193 MHz (OSC/12)
Out	Refresh Request
Function	Counter 2 (Speaker Tone)
Gate	Programmable via Port $061
Clock In	1.193 MHz (OSC/12)
Out	Speaker

The counter/timers are programmed by I/O accesses. A single control word register controls the operation of all three counters. For more information on programming and a detailed register description see the 8254 data sheet.

7.6 Real Time Clock

The RTC is a low-power clock that provides a time-of day clock and a 100-year calendar with alarm features and battery backed operation. The time-of-day function includes 14 control registers. Other features include maskable interrupt sources and 242 bytes of general purpose CMOS RAM used by system UEFI Firmware. Valid RAM data and time can be maintained after power down through the use of an external battery source. The RTC is software compatible to the Dallas DS1287, Motorola MC146818 and the Freescale equivalent.

7.7 UEFI Firmware – Backup UEFI Firmware

The VR12 provides two 8 MByte SPI flash device for the UEFI Firmware code and Management Engine firmware. The two devices content the standard and a back-up code. Integrated logic switch between the standard UEFI Firmware and back-up UEFI Firmware device. Only the standard UEFI Firmware can be programmed by the user, the back-up UEFI Firmware chip is read-only and can be only updated at the factory. This feature prevent the customer from hang-ups at standard UEFI Firmware updates.

Switching procedure between standard and back-up UEFI Firmware are controlled by the IPMI controller. See IPMI manual (tbd) for switching between standard and back-up UEFI firmware.

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7.8 BIT

The standard UEFI Firmware code will have space for a Built In Test (BIT). For operation description see the UEFI Firmware document. The BIT controls several BIT status LEDs, two yellow BIT status LED, a green BIT OK LED and a red BIT fail LED. This function is currently not available.

7.9 IPMI

A Baseboard management controller (BMC) is implemented on the VR12, the interfacing between host processor and the system management network. This controller can also work as a Peripheral management controller (PM). The BMC is mapped into the local CPUs I/O address space. The functionality of the IPMI controller is described in the ‘Intelligent Platform Management Interface for VR12 User’s Manual’.

If the power of the VR12 is off the IPMI controller may be supplied by the +5VSTBY power pin. A blinking green ‚heartbeat‘ LED indicates active and running IMPI code.

For information about the System Management in VME systems, please refer to the VITA 38 and PICMG® 2.9 'System Management Specification'. More information about IPMI can be found on the Intel website.

7.9.1 IPMB

The Intelligent Platform Management Bus (IPMB) is an I2C-based bus that provides a standardized interconnection between different VME-boards within a chassis. The standardized connection to the backplane is shown below:

Table 7-2 IPMB backplane pin assignments

P1	Name	Description
B21	IPMB_SCL	Serial Clock
B22	IPMB_SDA	Serial Data
B31	+5VSTDBY	Power Supply for all IPMI-devices

7.9.2 SMB

The System Management Bus (SMB) is an I2C-based bus that provides a standardized interconnection between the BMC and other I2C devices on the chassis. The standardized connection to the backplane is shown below:

Table 7-3 IPMB backplane pin assignments

P1	Name	Description
D19	SMB_SCL	Serial Clock
D21	SMB_SDA	Serial Data
D23	\SMB_ALERT	SMB Alert signal to IMPI controller

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7.10 Super I/O

The Super I/O SMSC SCH3114 provides four UARTs, Watchdog Timer, and system monitoring of voltages and board temperature to the system.

Voltage monitoring of +5V and +12V(backplane power), and CPU core voltage.

The temperature sensor shows the local onboard temperature (ambient temperature) and is located beneath the heatsink. The SCH3114 has an over-temperature output integrated, which can be used to take actions like reducing the CPU speed. For programming information please see the 'UEFI Firmware Programmer's Manual'.

More information on the SCH3114 can be found in the data sheet from SMSC.

7.11 Keyboard and Mouse

The communication between the PC and the keyboard and mouse is managed by a USB connection. A legacy 8042 interface is available via emulation for USB-unaware OS.

7.12 SATA Interface

The VR12 offers five SATA channels. They can transfer up to 300 MBytes/s. The controllers support RAID 0/1/5/10.

The SATA0 and SATA1 are connected to the on-board SATA connector, to provided a one or two HDD mounted at the VR12 or VP12. SATA2 is connected to an optional on-board NANDrive™. SATA4, SATA5 are routed to the rear connector (see rear pinout for availability). SATA2 and SATA3 may optional available at rear at special requests.

The VR12 UEFI Firmware automatically detects connected SATA Drives or flash disks and enters the corresponding drive parameters into the UEFI Firmware setup.

Using SATA and SCSI devices: The PC allows the simultaneous use of SATA and SCSI hard disks. UEFI Firmware setup allows reordering drives to boot from either SCSI or SATA drives.

7.13 PCI Express Interfaces

The Intel CPU Core i5/i7 and Intel PCH is offering several PCI Express interfaces. The PCI Express channels are dedicated to following devices.

Table 7-4 PCI Express channels

Device	Channel	Function
Intel Core I5/i7 mobile CPU	PCIe (0:3)	PCIe/PCI Bridge to PMC2 (x4) or XMC2 (0:3) (x8)*
	PCIe (4:7)	XMC2 (4:7) (x8) *

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Table 7-4 PCI Express channels (Continued)

	PICe (8:11)	PCIe/PCI Bridge to PMC1(x4) or XMC1 (0:3) (x8) *
	PCIe (12:15)	XMC1 (4:7) (x8)*
PCH	PCIe (1:4)	PCIe/PCI Bridge to VME controller
	PCIe (5)	Ethernet Controller 3
	PCIe (6)	Ethernet Controller 4
	PCIe (7)	Ethernet Controller 1
	PCIe (8)	Ethernet Controller 2

* If an XMC board is mounted the PCI Express lanes are muxed to the XMC slots and the PMC bridge is disconnected from the PCI Express bus.

7.14 VME

The VME interface is provided with IDT Tundra Tsi148 controller. It contains a complete high performance 64-bit 2esst capable VMEbus interface with 64-bit PCI-X master/slave capability. A system controller is implemented in the Tsi148 to allow the Vx12 to reside in slot 1 without the necessity of an extra system controller. The VME controller is connected via a 64bit PCI-X 133Mhz PCIe/PCI bridge Pericom PI7c9x130.

Tsi148 Register

All of the controlling registers are located in the Tsi148. The VME related registers for are memory mapped and after Power-On the base address is assigned dynamically by the software.

The PCI related registers can be found in the PCI configuration space.

Tsi148 PCI bus Address Space

By default the VMEbus interface is disabled. In this case the PCI address space reserved for the VMEbus is available. If the VR12 needs to access the VMEbus, the PCI address spaces must be defined in the UEFI Setup screen.

7.14.1 Features

- 64 bit, 133 MHz PCI-X local bus interface
- high performance 64 bit VMEbus interface
- Integral FIFOs for write posting and read pre-fetching to maximize bandwidth utilization
- Programmable DMA controller with linked list support
- VMEbus ‘real life’ transfer rates of up to 200 MByte/s (2esst)
- Complete suite of VMEbus address and transfer modes
- A64 / A32 / A24 / A16 master and slave
- D64 (MBLT)/D32/D16/D8 master and slave
- 2esst, 2eVME, BLT, ADOH, RMW, LOCK
- Flexible register set, programmable from both the PCI and VMEbus ports
- Full VMEbus system controller functionality

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7.14.2 VME \SYSRESET Direction

The VR12 provides a non-volatile UEFI setup screen of the VME \SYSRESET direction. In the setup screen the user can decide whether the VR12 can drive the VME \SYSRESET and also decide whether the VME \SYSRESET should be used as an input.

7.15 Serial Interface

The serial interface are provided by the Super I/O SCH3114. The VR12's serial ports are fully compatible with the NS16450 and NS16550. This means that each serial interface provides a 16 byte FIFO and therefore offers a higher performance than earlier used standard serial interfaces. The UARTs have programmable baud rate generators capable of 50 to 115200 baud. There are four address locations defined for serial interfaces on standard PCs. The serial interfaces are I/O mapped and can occupy four address ranges.

COM1 and COM2 to the rear are software selectable either RS232 or RS422/485 compliant. In RS485 mode the output drivers can be enabled or disabled with the DTR signal. An active DTR means the driver are always enabled. When using RS422 setting the output drivers are always enabled and the DTR signal is not used. The mode of the serial interface is controlled in an UEFI setup screen.

COM3 is an RS232 only interface. It is located on the front of non-conduction cooled boards.

7.16 Graphics Controller

The VR12 uses the integrated 2D/3D Graphic solution in the Intel Core i5/i7 mobile processor and PCH. The Graphic controller is in the Core i5/i7 mobile CPU and the PCH supports the analog and digital display ports. Graphic interconnection between Graphic controller and PCH display ports is established with the Flexible Display Interface (FDI).

- The integrated graphics controller contains a refresh of the fifth generation graphics core
- Intel Dynamic Video Memory Technology (Intel DVMT) support
- Intel Graphics Performance Modulation Technology (Intel GPMT).
- Intel Smart 2D Display Technology (Intel S2DDT)
- Intel Clear Video Technology
- 12 Execution Units
- Dedicated analog and digital display ports are supported through the Intel 5 Series Chipset PCH

Four displays are provided at the VR12

- VGA2: Analog VGA port from the integrated RAMDAC. It supports up to 350MHz with a resolution of 2048x1536 @75Hz. this port is either connected to the front or the rear

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- VGA1: second analog VGA port with a SDVO/DAC controller Chrontel CH7317 supporting pixel rate of 165MHz or resolution up to 1920x1200. This port is connected to the rear.

NOTE

Termination resistors of the VGA RGB lines are on the VR12 board for front only. For rear interfaces the termination (75 Ohm to ground) resistors must be located at a possible interface board i.e. Transition Module VTM24.

- DVI1 to rear is connected to Display Port C of the PCH. Maximal pixel rate 165MHz at 1920x1200.
- DVI2 to the rear is connected to Display Port D of the PCH. Maximal pixel rate 165MHz at 1920x1200.

At higher resolutions the cable and connectors have great influence on picture quality. Use very good quality cables and connectors or reduce resolution to get a stable display of good quality. This is especially important for the highest resolutions.

7.16.1 Software Installation

The Technical Product Information CD-ROM supplied with the VR12 includes the most commonly used software drivers and utilities.

7.17 PMC/XMC Interface

The two PCI Mezzanine Card (PMC) or XMC interfaces create additional slots for parallel mounted expanders or option cards. The PCI busses for the two PMCs are provided by Pericom PI7c9x130 PCIE/PCI bridges and have a 64bit wide bus with PCI-X 133Mhz capability. If no PMC module is installed the PMC bridges are disabled and not visible in the PCI scan. If an XMC mezzanine card is mounted at the slot the PCI Express lanes of the PCIE/PCI bridge are disconnected and muxed to the XMC connector, so the PMC PCI bus is not usable.

Please see chapter 'PCI Mezzanine Card (PMC)' of this manual for further details.

7.18 Ethernet Interface

The four Ethernet controllers 82574 from Intel used with the VR12 are high performance Gigabit Ethernet 10/100/1000 Mbit PCIe controller. Two interfaces are at front and two interfaces are at rear. For registration and identification of a workstation in a LAN, a unique ID number is required. Each network card is assigned a unique ID number which resides in an Ethernet address ROM on the VR12.

An Ethernet boot option can be enabled in UEFI Firmware setup.

7.18.1 Software Installation

The drivers available for the Ethernet controller 82574 support a large number of operating systems.

The Technical Product Information CD-ROM supplied with the VR12 includes the most commonly used software drivers and utilities.

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7.19 Additional devices

7.19.1 VR12 Programmable Logic Device

The VR12 has a Program Logic Device (PLD) to control power sequence, reset sources and generation and a set of registers to control VR12 specific features.

7.19.2 SMBus devices

The VR12 uses a serial 2-wire I2C bus to communicate with several onboard devices:

Table 7-5 Additional devices

Device	Designation	SMBus address
Clock synthesizer *	U1000	1101 001Xb
SPD EEPROM *	U1981	1010 00XXb
Factory EEPPROM *	U1981	1010 01XXb
User Eeprom 24C512	U1983	1010 110Xb

Devices marked * are handled by UEFI Firmware. It is strongly recommended not to access these devices via the user software.

An X at bit 0 represents the R/\W bit.

7.19.3 Temperature Sensor

Temperature sensors are integrated in the CPU die, PCH die and Super I/O. The sensor of the Super I/O shows the local onboard temperature of the VR12 and is located beneath the CPU heat sink. The Super I/O sensor has an over-temperature output integrated and this can be used to take actions like reducing the CPU speed.

The die sensors of the CPU and PCH may be programmed to take actions to protect the devices from over-heating. The CPU temperature sensor has a catastrophic protection which shut down the CPU core voltage if the die temperature reaches +125 °C.

7.19.4 Serial EEPROM

For storage of user data a serial EEPROM is implemented on the VR12 board. The user EEPROM is a 24C512 type with 64 KBytes of memory. More information about writing and reading the contents can be found in the data sheets from the manufacturer (e.g. Microchip Technology, SGS Thomson, Atmel, Catalyst and many others).

7.19.5 Geographic Addressing

If the backplane supports geographic addressing, the VR12 can detect the unique address in a VME System with the GA [5...0] pins on the VME connector P1 (P7301).

7.19.6 GPIO (0...11)

Twelve GPIO-Pins are available on the VME connector P2 (P7302). These pins can be used for I/O functions with output 3.3 V signals as well as 5 V tolerant inputs.

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GPIO0..9 can be used only when the DVI1 is not installed. GPIO0..9 and DVI1 are mutually exclusive ordering options. GPIO(10..11) are always available.

The GPIOs are realized as open drains with a pull-up of 1kOhm to 3.3V. That means if the corresponding bit in the GPIO control register is set to one (default after power-up) the GPIO is high-Z and driven to one by the pull-up resistor. A zero to the control register drives the GPIO to low. For input usage the coresponding control register bit must be set to one (GPIO high-Z), so an external driver can force the GPIO.

The GPIO control register is also used as GPIO read input register, please note that these read bits represent the logic level at the pin, regardless whether the pin is driven by from the GPIO control register or from an external driver.

7.19.7 LED

The VR12 has a set of status LEDs for indicating Power/startup and BIT status. All LEDs are available at front. Two status lines for LEDs are connected to rear.

Figure 7-1 VR12 front panel LEDs



Table 7-6 Front bi-color S-State LED

Status	LED
S0 running	green
S1 ACPI sleep	yellow
S3 suspend to RAM	yellow
S4 suspend to disk	yellow
S5 soft off	red

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Table 7-7 Front bi-color Power-State, Boot-State LED

Status	LED
board power missing	red
board in reset	amber
board out of reset	off
UEFI Firmware early init	Blink red 1Hz
UEFI Firmware memory init done	Blink amber 1Hz
UEFI Firmware DXE phase starts	Blink green 1 Hz
UEFI Firmware start OS	green

Table 7-8 Front PC/OT LED

Status	LED
Checkpoint, Post Codes (PC)	Output checkpoint with red blinking
Overtemperature (OT) CPU >105°C	short blink

Table 7-9 Front BIT status LED

Status	LED
BITFail	Red on
BITStatus 1,0 (see Note below)	red
BITOK	green



NOTE

For encoding of the BIT status LEDs see BIT manual (tbd).

The rear status LED signals provide the board status for external LEDs. The signal already implemented serial resistors on the VR12.

Table 7-10 Rear BITFail status LED

\BITFAIL_LED Status	LED (1kOhm serial resistor)
Build In Test Fail	active low on (1kOhm serial resistor)

Table 7-11 Rear status LED

\STAT_LED Status	LED (330Ohm serial resistor)
UEFI Firmware started	active low blinking
loading OS	active low steady on



NOTE

The LED color of the rear status LED is under control of the VR12 user. At the VR12 transition module VTM24 the rear STATUS LED is green.

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7.19.8 Power Button

There is a Power Button onboard. An external Power button may be connected between the appropriate IO connector at the back side and GND.

With a short Pressing at the power Button the operating system tries to shut down the VR12 to State S5. If the operating system doesn't react a long pressing (>5 sec) will shutdown the VR12 to State S5 without operating system support.

State S5 will switch off the CPU core power and hold the VR12 in reset. The state S5 is indicated at the S-State LED. At this state it is possible to reactivate the VR12 with a short press at the Power Button. The CPU core voltage is switched on and the boards restarts.

7.19.9 Speaker

An internal buzzer is implemented on the VR12 except on a VR12 Level D, E.

An external standard PC compatible speaker may be connected between the appropriate IO connector at the rear side and +5 V.

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8 • Specifications

Chapter Scope This chapter contains the detailed specifications for the VR12 Single Board Computer.

8.0.1 PCB

FR4 Multilayer

8.0.2 Size

Total board size: 6U, 4 HP (VR12)

Total size with optional extension board 8HP (VP12)

8.0.3 Dimensions

PCB: 233.35 mm x 178 mm x 20 mm (VR12 single Slot)

PCB: 233.35 mm x 178 mm x 40 mm (VP12 dual Slot)

8.0.4 Weight

VR12 Level A,B,C* boards:	approx. 550 g (with front panel and heatsink)
VP12 Level A* boards:	approx. 750g (with front panel and heatsink)
VR12 Level D boards:	approx. 685 g (with conduction cooling plate)
VR12 Level E boards:	approx. 775 g (with conduction cooling plates)

* if applicable add weight of mounted Hard Disk Drive(s) or Solid State Drive(s)

8.0.5 RoHS compliance

VR12 is available in RoHS

8.1 Power Consumption

The following two tables are intended to help you calculate the power consumption of a VR12 system. Select power consumption, depending on configuration, in both tables and add them together for total power consumption. Also add any other extra power consumption as described in the footnotes of both tables.

For measurement purposes, the VR12 board is mounted on a VME backplane. During measurement, the power consumption of the backplane, keyboard and the hard disk drive are deducted from the results. The values measured are typical.

The Intel Core i5 and i7 processors are available in three power consumption classes. These classes are regardless of other classification like frequencies or cores.

- SV Standard Voltage with up to 35 W CPU power consumption
- LV Low Voltage with up to 25 W CPU power consumption
- ULV Ultra Low Voltage with up to 18 W CPU power consumption

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Table 8-1 Power consumption CPU-dependent

VR12	DOS, one core running full cache access, one core idle, CPU die around +75 °C*	Windows VISTA, both CPU cores running a TDP design power consumption instruction mix at +100 °C die temperature
	+5 V	**+5 V**
2.53 GHz (SV) i7-610E 2.40 GHz (SV) i5-520E	5.0 A	8.8 A
2.00 GHz (LV) i7-620LE	4.2 A	6.7 A
1.06 GHz (ULV) i7-620UE	3.7 A	3.9 A

* for every 25 °C more please add around 10 %

** estimated values

Table 8-2 Power consumption DRAM-dependent

VR12 valid for all kind of CPUs	DOS prompt or CPU running full cache access, mid range temperature all four Gigabit linked **	Peak value UEFI Firmware during memory initialization*, **	Windows VISTA, 3D graphics active, four Gigabit Ethernet channels linked, Memory Workload **
	+3.3 V	**+3.3 V**	**+3.3 V**
1GB (1 bank, 9 devices)	4.0 A	3.8 A	4.7 A
2 GB (2 banks, 18 devices)	4.1 A	4.4 A	5.1 A
4 GB (4 banks, 36 devices)	4.2 A	5.0 A	5.5 A

* for every Ethernet channel linked to gigabit please calculate 0.25 A

** for every enabled PMC bridge add 0.45 A

- When using onboard PMC modules don't forget to add the power of the enabled PMC bridges and the PMC module power consumption
- With an onboard hard disk drive please add the following values to the +5 V current:
  - During power up 0.9 A max.
  - In an idle condition 0.13 A typical
  - During read/write access 0.42 A typical

Values are taken from the Fujitsu MHT 2060 AT datasheet

- For keyboard, mouse, etc. please add 0.1 A (typical) to the +5 V current
- USB connector P1680 provides fused VCC voltage (+5 V). The total current drawn from this source may not exceed 1.0 A

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8.2 Onboard Lithium Battery

An onboard battery BR2032 (190 mAh) supplies the VR12 RTC. The VR12 RTC has a current consumption of 6 µA (board non-operating). The estimated battery life time depends on temperature and power status. See Table 8-3 for battery life at non operating (VR12 power off, RTC supplied by battery) and operating (VR12 power on, RTC supplied by power rail).

8.2.1 Battery lifetime

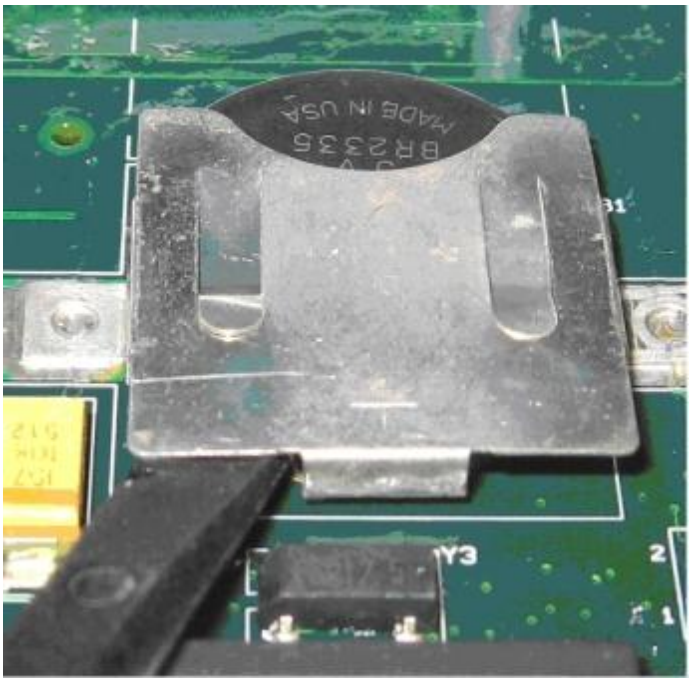
The battery lifetime varies with the temperature range.

Table 8-3 Battery lifetime

Mode	Temperature range	Years lifetime
non operating	+10 °C to +85 °C	5.5
non operating	-10 °C to +10 °C	4.0
non operating	< -10 °C	3.0
operating	-40 °C to +85 °C	10.0

The battery fits into a user accessible holder on the VR12.

Figure 8-1 Battery removal



NOTE
If the battery is exchanged by the customer, please use the same type of battery and ensure correct polarization.

For operating without battery please check the following description of the external battery input.

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8.2.2 Battery removal and replacement

Locate battery on the computer. Reference the product manual if it is not easily located. On some of the dual slot SBCs, the top board may need to be removed to make it easier to remove the battery. Once the battery is located, take a non-conductive tool and push at the back of the battery holder. Gently apply pressure in order to not break the socket. The battery should slide forward out of the holder. Pressure can be alternated between the two sides to get the battery to slide out of the socket. The battery should slide forward enough that it could be removed from the socket. A new battery can be installed by sliding it into the holder. Make sure to observe correct polarity.

8.3 +5VSTDBY

Pin +5VSTDBY located at the VME connector P1 (P7301) pin B31 can optionally supply current to the RTC and the IPMI controller during VR12 non-operating.

Without battery and without this +5VSTBY supply voltage, the real time clock oscillator has to be started at each power up. This time gets longer when operating at lower temperatures and can be up to around 30 seconds (at -40 °C). At normal ambient temperatures this delay is below one second.

When ordering a battery-less VR12, the setup information is stored automatically within an onboard EEPROM and is updated via the standard UEFI Firmware Setup function. It is still recommended to use an external supply voltage to this battery input to avoid the power-on oscillator start time and to keep the date and time information.

The optional +5VSTBY supplies also the IPMI controller during VR12 non-operating mode. Please refer to the IPMI User Manual for functionality.

See Table 8-4 for +5VSTBY current consumption.

Table 8-4 +5VSTBY Current

+5VSTBY	RTC	IPMI
at VR12 operating	0 mA	0 mA
at VR12 non-operating	2 mA	85 mA

8.4 EMC Compliance

8.4.1 Information to the user

The following statement applies to the products covered in this manual, unless otherwise specified herein. The statement for other products will appear in the accompanying documentation.

NOTE

This equipment has been tested and found to comply with the limits for a class A digital device, pursuant to Part 15 of the FCC Rules and meets all requirements of the Canadian Interference-Causing Equipment Standard ICES-003 for digital apparatus. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications.

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However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/T.V. technician for help.

Abaco is not responsible for any radio television interference caused by unauthorized modifications of this equipment or the substitution or attachment of connecting cables and equipment other than those specified by Abaco. The correction of interference caused by such unauthorized modification, substitution or attachment will be the responsibility of the user.



NOTE

The use of shielded I/O cables is required when connecting this equipment to any and all optional peripheral or host devices. Failure to do so may violate FCC and ICES rules.



WARNING

This is a class A device. This equipment may cause interference in a residential installation. In this case the user is encouraged to perform appropriate measures to correct the interference.

8.5 Environmental Conditions

Ambient temperatures and humidity values for theVR12:

Table 8-5 Environment conditions

	Level A	Level B	Level C,D	Level E
High Temperature - Storage* - Operating (see diagram below)	+85 °C	+100 °C	+100 °C	+105 °C
Low Temperature - Storage * - Operating	-40 °C 0 °C	-50 °C -20 °C	-50 °C -40 °C	-55 °C -40 °C
Temperature Shock - Storage - Operating	+/-10 °C/min +/-5 °C/min	+/-10 °C/min +/-5 °C/min	+/-20 °C/min -+/-10 °C/min	+/-20 °C/min +/-10 °C/min
Relative Humidity - Storage, Operating	up to 95 % non-condensing	up to 95 % non-condensing 10 cycles, 240 h	up to 95 % non-condensing 10 cycles, 240 h	up to 95 % non-condensing 10 cycles, 240 h

* Limited to -40 °C/+85 °C if the product includes a battery

VP12 only supports level A,B.

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Shock and vibration values for the VR12 designed to meet the values listed below:

Table 8-6 Shock & vibration parameters

	Level A, B, F	Level C	Level D, E
Vibration - Spectrum - Acceleration	 5 to 100 Hz 0.04 g²/Hz	 5 to 2000 Hz * 0.04 g²/Hz	 5 to21000 Hz ** 0.1 g²/Hz
Shock - half sine or sawtooth - Duration	 20 g 11 ms	 20 g 11 ms	 40 g 11 ms

VP12 only supports level A,B

* 3 dB/octave roll-off from 5 to 20 Hz and 6 dB/octave roll-off from 1000 to 2000 Hz

** no roll-off

NOTE

Values for shock & vibration are only valid for products without a hard disk drive (HDD) installed. For values of shock and vibration of HDDs please see the specifications of the HDD manufacturer. For further questions please consult the Abaco technical support team.

Maximum height usage for the VR12 is specified in the table below.

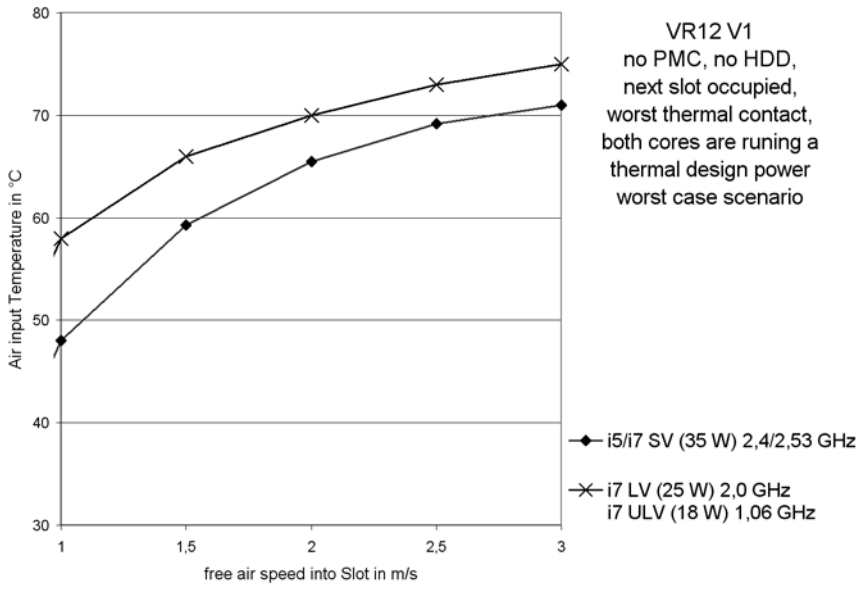
Table 8-7 Maximum height usage

	Level A, B, C	Level D, E
Maximum height - Operating - Storage	 4.5 km 12 km	 Vacuum Vacuum

Only the Level D,E boards are capable to be used in a vacuum environment. All other board levels contain either batteries and do not have the possibility to be cooled without airflow.

For highest operating temperatures (Level A, B, C) please refer to the following diagram:

Figure 8-2 Air temperature vs. airspeed



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This diagram is based on estimated data and may change.

- 0.5 m/s airflow means convection cooled only.
- The above diagram is valid for a usage at heights up to 1000 m above sea level. For higher heights the maximum temperature values have to be reduced in an appropriate way.
- The core temperature of the CPU can be read out via the die temperature sensors. The value must be kept below 105 °C for all operating conditions. This value is already included in the airspeed diagram above. If this temperature limit is violated, the Intel CPUs will start to reduce its internal frequency temporarily. This can be heard by a short click of the speaker which occurs every 0.8 seconds.
- When using an onboard hard disk drive (not with flash disk) the operating temperature is limited to 50 °C
- When using one or two PMC modules, please consider their power consumption and thermal limits in calculating the max. operating temperature

8.5.1 Card edge temperatures for VR12 conduction cooling (Levels D,E)

Table 8-8 Card edge temperatures for conduction cooling (Level D and E)

Processor	Card edge temperature Level D,E
SV-i5, SV-i7	Level D 70 °C Level E 80 °C (tbc)
LV-i7	Level D 75 °C Level E 85 °C (tbc)
ULV-i7	Level D 75 °C Level E 85 °C (tbc))

These values do not include temperature variations due to PMC modules.

For even more detailed information especially on the Level D and E versions, please check the thermal report document TR-HW-016 of the VR12.

8.6 Electrical Characteristics

The supply voltages are +5 V and 3.3 V.
+12 V and -12 V are required only if needed on the PMC slot.
The table below shows voltages with maximum current restrictions due to layout restrictions or fusing:

Table 8-9 Supply voltages

Name	U	Imax	Description	Fuse
+12V	+12 V	0.5 A	Supply for PMC-Module	
-12V	-12 V	0.2 A	Supply for PMC-Module	
USB_VCC	5 V	2.0 A	Supply for front panel USB	F1681 [b]
VTM+3.3V	3.3V	0.5 A	Supply for rear transition module logic	

[b] TPS2034D (Texas Instruments)

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8.6.1 Supply voltage range

The following ranges are defined by the VME64 specification ANSI/VITA 1-1994 for VME64 and ANSI/VITA 1.1-1997 for VME64 Extensions. The voltages have to be measured at the backplane.

Table 8-10 Supply voltage range

Supply	Voltage and tolerance
+5 V	5.0 V +0.250 V / -0.125 V
+5 V STDBY	5.0 V +0.250 V / -0.125 V
+3.3 V	3.3 V +0.150 V / -0.050 V
+12 V	12.0 V +0.60 V / -0.36 V

8.6.2 GPIO 0...11

This general purpose I/O pins can be used as inputs, with following signal levels:

Table 8-11 GPIO IN signal levels

level	voltage
low	-0.5 V ... +0.8 V
high	+2.0 V ... +5.5 V (absolute maximum rating)

When used as outputs (open drain), the following signal levels are supplied:

Table 8-12 GPIO OUT signal levels

level	voltage
low	+0.4 V at 6 mA sinking
high	1kOhm pull-up to 3.3V

8.6.3 Isolation

The Isolation of the Ethernet outputs whether front or rear is limited to 500 V peak against GND and any other supply voltage.

By itself the onboard digital ground GND and the front panel/chassis frame ground FGND are isolated on the VR12 with a layout distance of more than 0.3 mm in all PCB layers. However, most standard devices (keyboard, mouse, and monitor) except Ethernet will connect FGND and GND directly in the device. Also standard racks (our starter cage too) connect both grounds at the power supply for safety reasons.

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A • Transition Module VTM24

The VTM24 transition module is used for easy connection of I/O signals to standard connectors. Please refer to the drawing for the location of available interfaces:.

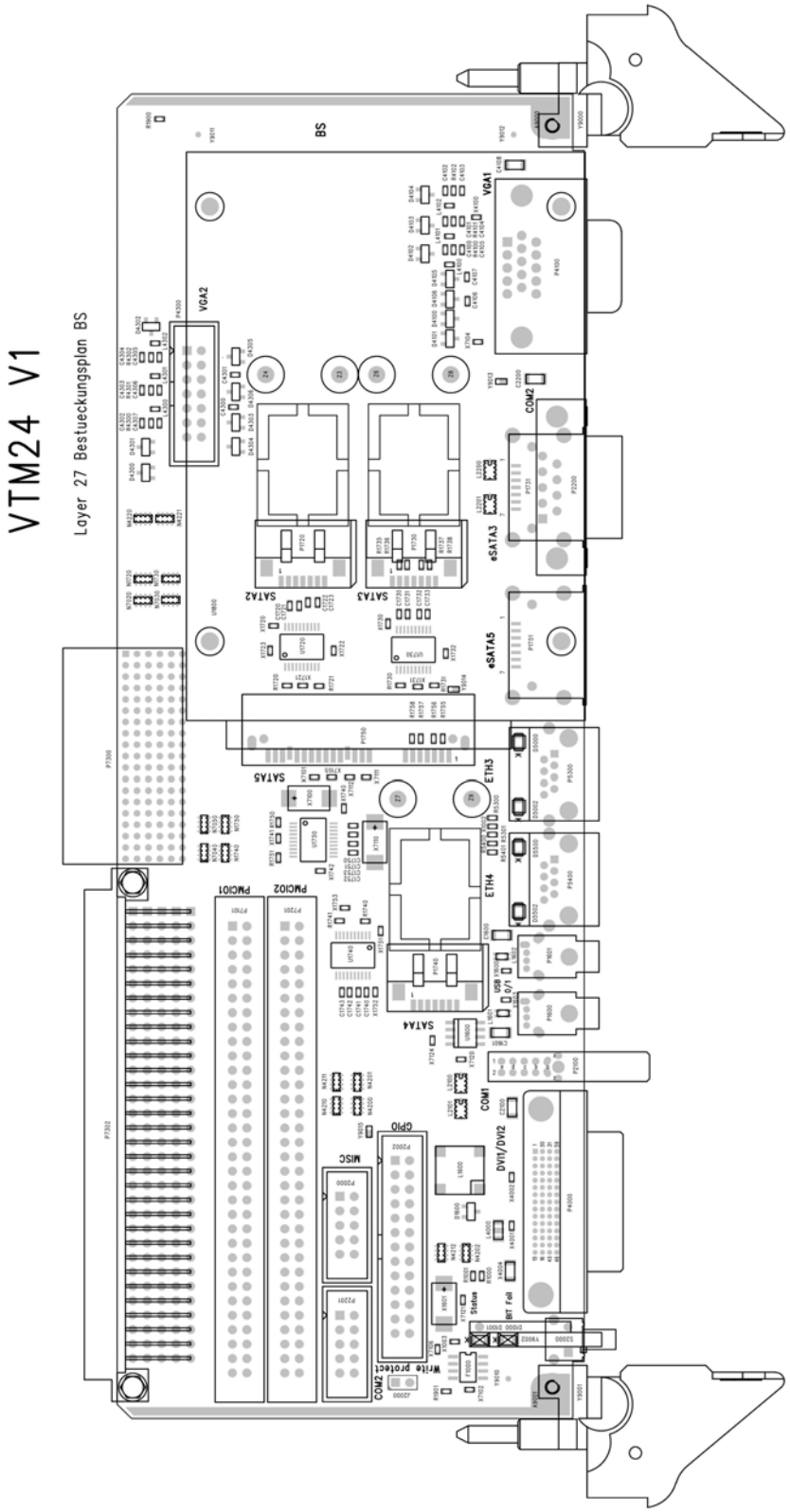


NOTE

The +3.3V pin 6c on P0 = P7300 is the only 3.3 VDC source for the Transition Module VTM24. Do not connect the +3.3V pin to +3.3 V backplane power plane.

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Figure A-1 VTM24 Transition Module



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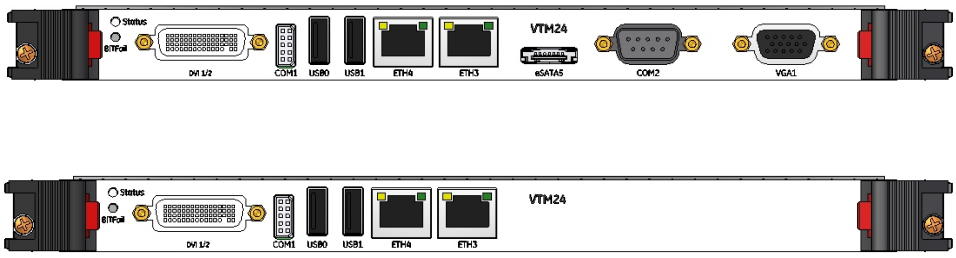
A.1 VTM Interfaces

This chapter describes all connector pin assignments on the VTM24 transition module.

A.1.1 VTM Front Panel

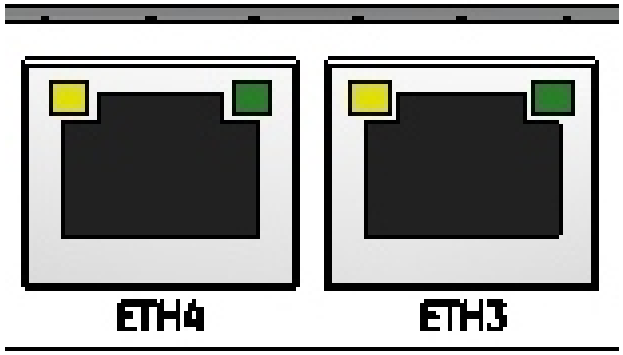
The VTM24 front panel has several connectors to accept appropriate interface cables. Two versions are available: Full-IO (top) and HDD integrated (lower).

Figure A-2 VTM24 Front Panel



A.1.2 Ethernet Interface 10/100/1000BaseT (P5000, P5500)

Figure A-3 Ethernet Interface 10/100/1000BaseT (P5300, P5400)



The Ethernet interfaces for RearI/O requires usage of CAT 5 cable for proper operation with 100/1000BaseT.

Table A-1 VTM24 Ethernet connectors

Name 10/100base	Name 1000base	Ethernet3, 4
TxD+	LP_DA+	1
TxD-	LP_DA-	2
RxD+	LP_DB+	3
NC	LP_DC+	4
NC	LP_DC-	5
RxD-	LP_DB-	6
NC	LP_DD+	7
NC	LP_DD-	8

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Two LEDs (green and yellow) are integrated in each of the RJ45 connector. These LEDs indicate the link status and activity of the interface.

Table A-2 VTM24 LEDs

LED green	Function
On	Link
Off	No link
LED yellow	Function
On, blink	Tx/Rx activity
Off	No activity

A.1.3 GPIO Connector (P2002)

Table A-3 VTM24 GPIO connector

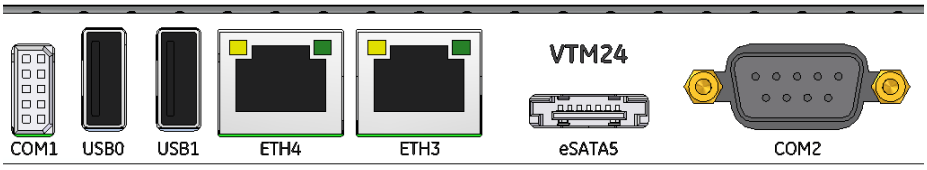
Name	P2002
DVI1_TXC+/GPIO0	3
DVI1_TXC-/GPIO1	5
DVI1_TX0+/GPIO2	7
DVI1_TX0-/GPIO3	9
DVI1_TX1+/GPIO4	11
DVI1_TX1-/GPIO5	13
DVI1_TX2+/GPIO6	15
DVI1_TX2-/GPIO7	17
DVI1_SCL/GPIO8	19
DVI1_SDA/GPIO9	21
GPIO10	23
GPIO11	25
FUSE_VCC	26*
GND	10,12,14,16,18,20,22
NC	1, 2, 4, 6, 8, 24

* FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

This connector shares the functions TMDS and GPIO. Only one function is available at the same time and is board specific.

A.1.4 Serial Interfaces COM1 (P2100) and COM2 (P2200, P2201)

Figure A-4 Serial interfaces COM1 & COM2



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COM1 and COM2 ports are accessible via the transition module. COM1 via a 10 pin har-Link connector, use adapter cable YA-CR12-01 for interface to 9 pin SUB-D connector.

COM2 is either at a 10 pole headers or 9 pin SUB-D connectors. The SUB-D for COM2 is only available if no hard disk is mounted at the transition module.

The ports are software selectable for RS232 or RS422/485 operation. The RS485 output drivers can be enabled or disabled with the DTR signal. An active DTR means the driver are always enabled. When using RS422 setting the output drivers are always enabled and the DTR signal is not used.

Table A-4 VTM24 COM1

Name RS232	Name RS422/485	P2100 har-Link
DCD	TXD-	1
DSR	TXD+	2
RXD	RTS-	3
RTS	RTS+	4
TXD	CTS+	5
CTS	CTS-	6
DTR	RXD+	7
RI	RXD-	8
GND		9
FUSE_VCC		10



NOTE

P2100 is har-Link, P2200 is pin header

* FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

Table A-5 VTM24 COM2

Name RS232	Name RS422/485	P2200	P2201
DCD	TXD-	1	1
DSR	TXD+	6	2
RXD	RTS-	2	3
RTS	RTS+	7	4
TXD	CTS+	3	5
CTS	CTS-	8	6
DTR	RXD+	4	7
RI	RXD-	9	8
GND		5	9
FUSE_VCC		-	10



NOTE

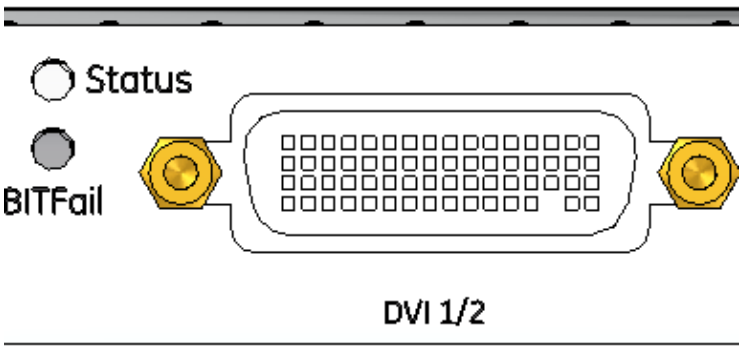
P2200 is DB9, P2201 is pin header

* FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

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A.1.5 DMS59 DVI connector (P4000)

Figure A-5 DMS59 connector



The VTM24 provides two DVI ports at a DMS59 connector (labeled DVI 1/2 on the VTM24 front panel). Use a split cable (part number DMS59A) to connect to compliant DVI connectors. The DVI connectors at the split cable has number at the DVI connector. Due to layout reasons the VTM24 physical DVI1 port is connected with split cable DVI connector with number „2“ and physical DVI2 port is connected with the split cable DVI connector with the number „1“.

As the DVI1 signals are shared with GPIO(0...9) and DVI2 are shared with PMC2IO the correct VR12 version must be selected for availability. For the digital signals the 'Transition Minimized Differential Signaling' (TMDS) is used.

Figure A-6 DMS59 connector layout

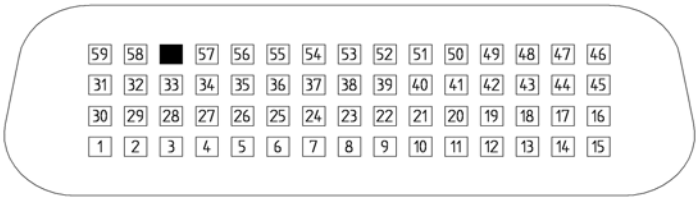


Table A-6 VTM24 DDMS59 connector digital pin assignments DVI1 and DVI2

Pin	Signal name	Pin	Signal name
1	GND	31	DVI2_TXC+
2	NC	32	DVI2_TXC-
3	NC	33	GND (DVI2_Data0 Shield)
4	GND	34	GND (DVI2_Data1 Shield)
5	FUSEVCC*	35	GND (DVI2_Data2 Shield)
6	DVI2_SCL	36	DVI2_HTPLG
7	DVI2_SDA	37	NC
8	GND	38	NC

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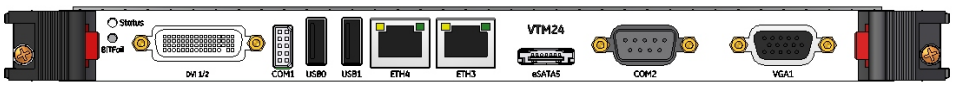
Table A-6 VTM24 DDMS59 connector digital pin assignments DVI1 and DVI2 (Continued)

Pin	Signal name	Pin	Signal name
9	DVI1_SCL	39	NC
10	DVI1_SDA	40	DVI1_HTPLG
11	FUSEVCC*	41	GND (DVI1_Data0 Shield)
12	GND	42	GND (DVI1_Data1 Shield)
13	NC	43	GND (DVI1_Data2 Shield)
14	NC	44	DVI1_TXC+
15	GND	45	DVI1_TXC-
16	DVI1_TX0+	46	GND
17	DVI1_TX0-	47	NC
18	DVI1_TX1+	48	NC
19	DVI1_TX1-	49	GND (DVI2_Clock Shield)
20	DVI1_TX2+	50	NC
21	DVI1_TX2-	51	NC
22	NC	52	GND
23	NC	53	NC
24	NC	54	GND
25	DVI2_TX0+	55	NC
26	DVI2_TX0-	26	NC
27	DVI2_TX1+	57	GND (DVI1_Clock Shield)
28	DVI2_TX1-	Key	-
29	DVI2_TX2+	58	NC
30	DVI2_TX2-	59	GND

* FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

A.1.6 VGA1 Interface (P4100)

The analog signals of VGA1 are available in any VR12 board version. The VTM24 provides these signal at a 15 pin SUB-D connector. The connector is only available if no Hard Disk is mounted. The RGB signals are terminated with 75 Ohm resistors at the transition module.



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Table A-7 VTM24 VGA1

Name	P4100
VGA1_RED	1
VGA1_GREEN	2
VGA1_BLUE	3
NC	4
GND	5
GND	6
GND	7
GND	8
FUSEVCC	9
GND	10
NC	11
VGA1_DDCData	12
VGA1_HSYNC	13
VGA1_VSYNC	14
VGA1_DDCClock	15

* FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

A.1.7 VGA2 Interface (P4300)

The VGA2 interface is available at a 14 pin header connector P4300. The RGB signals are terminated with 75 Ohm resistors at the transition module.

The connector is only available if no Hard Disk is mounted at the VTM24. The signal are shared with PMC2 I/O signals. For availability the correct version of VR12 and VTM24 must be selected.

Please ask factory for an interface cable from 14pin header to standard 15 pin SUB-D connector.

Table A-8 VTM24 VGA2

Name	P4300
VGA2_RED	2
VGA2_GREEN	4
VGA2_BLUE	6
VGA2_HSYNC	8
VGA2_VSYNC2	10
VGA2_DDCData	12
VGA2_DDCClock	13
NC	14
GND	1, 3, 5, 7, 9,11

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A.1.8 USB connectors (P1600, P1601)

Two channels are available at the standard USB connectors. FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

Figure A-7 USB connectors (P1600, P1601

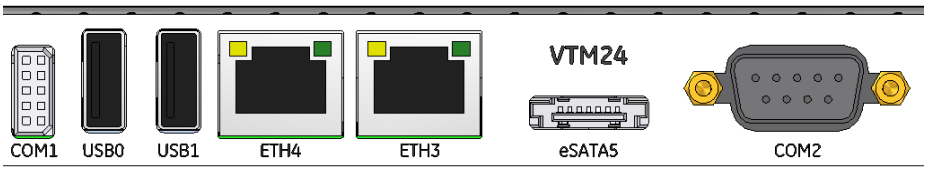


Table A-9 VTM24 USB0

Name	P1600
FUSE_VCC*	1
USB0-	2
USB0+	3
GND	4

Table A-10 VTM24 USB1

Name	P1601
FUSE_VCC*	1
USB1-	2
USB1+	3
GND	4

A.1.9 Miscellaneous connector (P2000)

Table A-11 VTM24 Miscellaneous Connector

Name	P2000	Name	
nc	1	2	nc
\HW_WP	3	4	\STATLED
\BITFAILR	5	6	GND
\PWRBUT	7	8	GND
\SPEAKER	9	10	FUSE_VCC*

* FUSE_VCC is fused with 2 A, but for normal operation don't exceed 1 A at this pin.

A.1.10 PMC I/O connectors

The PMC I/O signals of both the PMC slots are on a 64-pin male header (P7101/ P7201). Many signal s of PMC2IO are shared with other interfaces for availability the correct version of VR12 and VTM24 must be selected.

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The following table lists the pin assignment of the PMC I/O signals on the 64-pin header.

Table A-12 PMC I/O header

P7101/P7201	Pin	Pin	P7101/P7201
PMCx_IO01	1	2	PMCx_IO02
PMCx_IO03	3	4	PMCx_IO04
PMCx_IO05	5	6	PMCx_IO06
PMCx_IO07	7	8	PMCx_IO08
PMCx_IO09	9	10	PMCx_IO10
PMCx_IO11	11	12	PMCx_IO12
PMCx_IO13	13	14	PMCx_IO14
PMCx_IO15	15	16	PMCx_IO16
PMCx_IO17	17	18	PMCx_IO18
PMCx_IO19	19	20	PMCx_IO20
PMCx_IO21	21	22	PMCx_IO22
PMCx_IO23	23	24	PMCx_IO24
PMCx_IO25	25	26	PMCx_IO26
PMCx_IO27	27	28	PMCx_IO28
PMCx_IO29	29	30	PMCx_IO30
PMCx_IO31	31	32	PMCx_IO32
PMCx_IO33	33	34	PMCx_IO34
PMCx_IO35	35	36	PMCx_IO36
PMCx_IO37	37	38	PMCx_IO38
PMCx_IO39	39	40	PMCx_IO40
PMCx_IO41	41	42	PMCx_IO42
PMCx_IO43	43	44	PMCx_IO44
PMCx_IO45	45	46	PMCx_IO46
PMCx_IO47	47	48	PMCx_IO48
PMCx_IO49	49	50	PMCx_IO50
PMCx_IO51	51	52	PMCx_IO52
PMCx_IO53	53	54	PMCx_IO54
PMCx_IO55	55	56	PMCx_IO56
PMCx_IO57	57	58	PMCx_IO58
PMCx_IO59	59	60	PMCx_IO60
PMCx_IO61	61	62	PMCx_IO62
PMCx_IO63	63	64	PMCx_IO64

A.1.11 SATA connectors

All SATA interfaces have redrivers for improved signal quality.

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There are provisions for four SATA interfaces. In normal configuration two SATA interfaces (SATA port 4 and port 5) are available at the VTM24.

SATA4 has only a cable connector P1740. SATA5 has either an eSATA connector (P1751) or a connector for direct mounting (P1750) a hard disk at the transition module. In this case the front connector for COM2, VGA1 and the on-board connector VGA2 is not available.

SATA2 and SATA3 are only available at special request. SATA3 may have an cable connector P1730 or an eSATA P1731 connector at the COM2 space. SATA2 is only available at a cable connector P1720.

Table A-13 VTM24 SATA 2

Name	P1720
SATATX2	2
\SATATX2	3
\SATARX2	5
SATARX2	6
GND	1, 4, 7

Table A-14 VTM24 SATA 3 alternative with eSATA3

Name	P1730
SATATX3	2
\SATATX3	3
\SATARX3	5
SATARX3	6
GND	1, 4, 7

Table A-15 VTM24 eSATA 3 alternative with SATA3 cable connector

Name	P1731
SATATX3	2
\SATATX3	3
\SATARX3	5
SATARX3	6
GND	1, 4, 7

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Table A-16 VTM24 SATA 4

Name	P1740
SATATX4	2
\SATATX4	3
\SATARX4	5
SATARX4	6
GND	1, 4, 7

Figure A-8 eSATA5 connector

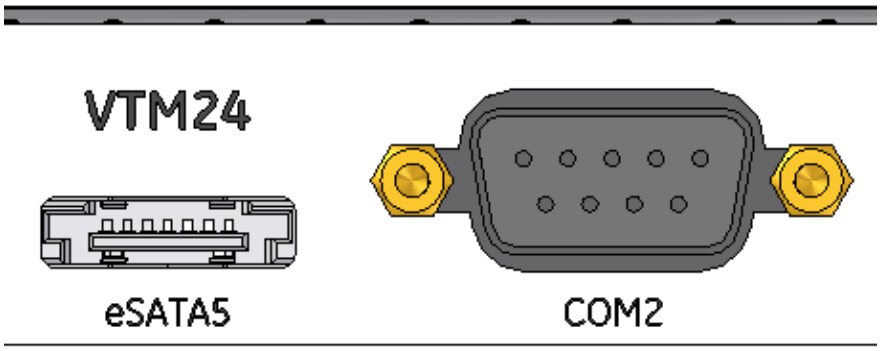


Table A-17 VTM24 eSATA 5 alternative with SATA5 HD direct

Name	P1751
SATATX5	2
\SATATX5	3
\SATARX5	5
SATARX5	6
GND	1, 4, 7

Table A-18 VTM24 SATA5 HD direct

Name	P1750-A
SATATX5	2
\SATATX5	3
\SATARX5	5
SATARX5	6
GND	1, 4, 7
Name	P1750-B
VCC3	1, 2, 3, 7, 8, 9
GND	4, 5, 6, 10, 11, 12
NC	13, 14, 15,

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A.1.12 Write Protection J2000

The VTM24 provides a Write Protection Jumper. If the jumper J2000 is closed all programmable devices of the VR12 are hardwired write protected.

A.1.13 LED

The rear status LED signals provide the board status at the VTM24. The signal already implemented serial resistors on the VR12.

Table A-19 Rear BITFail status LED

BITFAIL_LED Status	LED (1kOhm serial resistor at VR12)
Build In Test Fail	red (1kOhm serial resistor)

Table A-20 Rear status LED

STAT_LED Status	LED (330Ohm serial resistor at VR12)
UEFI Firmware started	green blinking
loading OS	green steady on

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B • PMC/XMC slot

The PCI Mezzanine Card (PMC/XMC) Interface is an additional slot for parallel mounted add on cards. The interface is compliant to the IEEE 1386.1 specification and is based on the electrical and logical layer of the PCI specification. PMC slots are 66/100/133 MHz PCI-X capable. The user definable I/O Pins are connected to the rear IO connector on the VR12, as defined in the VITA 36 specification.

- Both PMCs have a 3.3V key mounted, for 3.3 V compatible PMC cards.

B.1 Electrical characteristics

Table B-1 Electrical characteristics

Parameter	Comment	Value
I3.3 V	Max. current on 3.3 V Pins	1.5 A [c)]
I5 V	Max. current on 5 V Pins	1 A [c)]
I+12 V	Max. current on +12 V Pin	0.1 A
I-12 V [a)]	Max. current on -12 V Pin	0.1 A
V(I/O) [b)]	Voltage for PCI IO	3 or 5 V
P	Max. power consumption total	7.5 W

a) -12 V must be connected to the backplane.
b) the appropriate key has to be mounted.
c) total power dissipation on 3.3 V and 5 V rail is 7.5 W

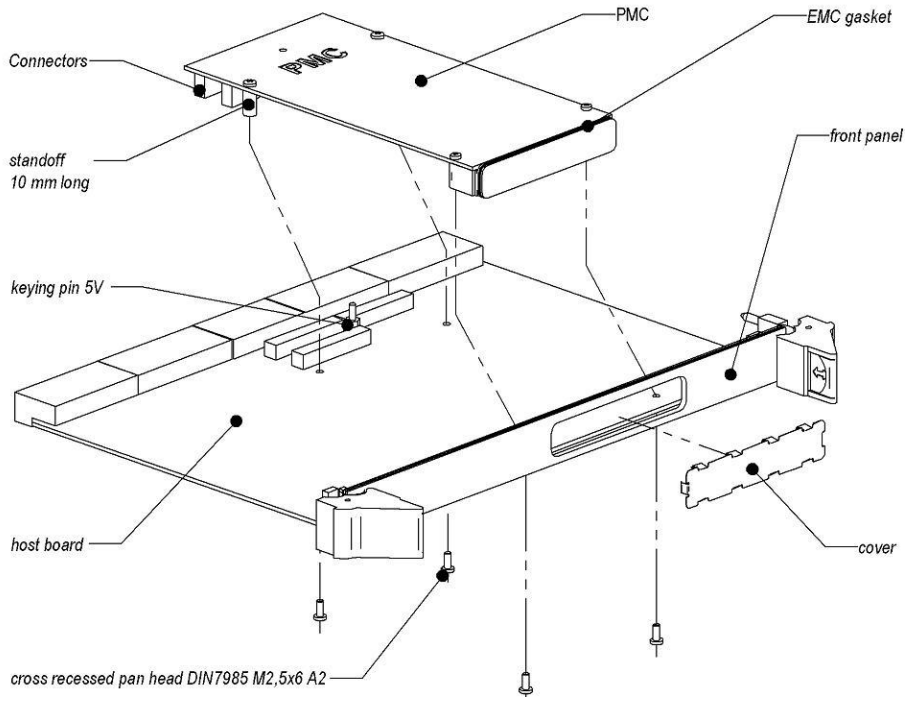
B.2 Mounting of PMC or XMC module

To mount a PMC or XMC board to the VR12, follow these steps:

1. Remove VR12 from system housing.
2. Remove the front panel cover of the PMC slot.
3. Take PMC/XMC from inside through front panel and push connectors together.
4. Verify correct installation of EMC gasket.
5. Fix PMC/XMC on host boards with 4 screws. Screws must be locked with Loctite 243.

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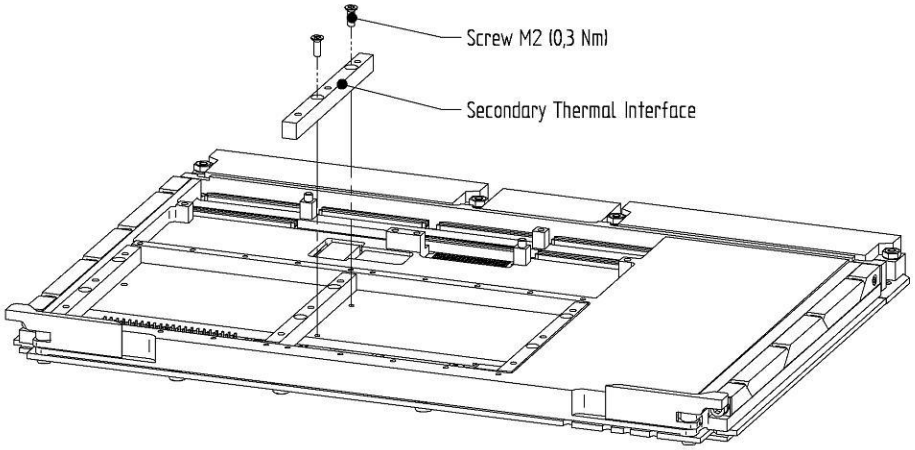
Figure B-1 Mounting of PMC/XMC module on VR12



B.3 Secondary Thermal Interface

On conduction-cooled versions of boards and mezzanines the PMC modules may be equipped with optional Secondary Thermal Interfaces. If the PMCs do not fit into their sockets on the VR12 base board then you can remove them. Use a matching TORX screw driver to remove the Secondary Thermal Interfaces. For mounting use a torque of 0.3 Nm to fix the screws or use minimum force to tighten the screws. Add only a short turn (~1/16th) when the screw starts to get tight.

Figure B-2 Mounting of Secondary Thermal Interface on PMC module



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C • Vx12 and Vx11 Compatibility

Chapter Scope The following sections describes compatibility issues between the Vx12 family and its predecessors Vx11.

C.1 Basic compatibility

Each Vx12 is as compatible as possible to the Vx11 family. Missing features on the Vx12 are the IDE and audio support.

The Vx12 offers dual core CPU technology with dual channel DRAM up to 4 GB. It has two XMC/PMC slots, two Gigabit Ethernet ports on the front and rear each, two onboard SATA channels and two SATA at rear, one USB, VGA, and COM port connector at the front panel, and a superior graphics solution.

The internal Vx12 hard disk are SATA only IDE is not longer supported.

The existing transition module VTM22 can be used for the Vx12 if no IDE and audio is used and the Vx12 SATA is configured for Vx11 compliance.

C.1.1 Front I/O

The VR12 front I/O interfaces are available regardless how many PMCs are there.

- Instead the Reset button of the Vx11 the VR12 has an Power Button.
- The Vx12 has always two Gigabit interfaces with RJ45 jacks
- The Vx12 has only one USB at the front
- The Vx12 has COM3 (RS232 only) instead COM1 (selectable RS232 or RS422/485) at the Vx11
- Vx12 COM port and VGA needs adapter cable from a har-Link connector to compliant interface connector
- Vx12 has BIT LEDs and different status LEDs

C.1.2 Rear I/O

The following table shows the rear I/O connection of the Vx12 and Vx11 families:

Table C-1 Rear I/O pin assignments for Vx11 & Vx12

				Rear I/O				
VP12	**VR12**	**VR12**				**VP11**	**VR11**	**VR11**
		CC						**CC**
√	√	√	P1	VME bus	P1	√	√	√
			P1		P1			
√	√			front Ethernet 1	P0	*2	*2	√
√	√			front Ethernet 2	P0	*2	*2	√
√	√	√	P0	rear Ethernet 3	-			
√	√	√	P0	rear Ethernet 4	-			

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Table C-1 Rear I/O pin assignments for Vx11 & Vx12 (Continued)

				Rear I/O					
			-	IDE primary **and/or**		P0	*3 *5	*3 *5	*3
				PMC 2 I/O					
√	√	√	P0	SATA4 and/or	PMC 2 /O	P0	√	√	√
				PMC 2 I/O					
√	√	√	P0	SATA5 and/or	PMC 2 /O	P0	√	√	√
				PMC 2 I/O					
			-	Audio and/or	PMC 2 /O	P0	√	√	√
				PMC 2 I/O					
√	√	√	P0	VGA2 and/or	PMC 2 /O	P0	√	√	√
				PMC 2 I/O					
√	√	√	P0	DVI2 and/or	PMC 2 /O	P0	√	√	√
				PMC 2 I/O					
*4	*4	*4	P2	DVI1 **or**		P2	*4	*4	*4
				GPIO					
√	√	√	P2	VGA1		P2	*1	*1	√
*4	*4	*4	-	GPIO/DVI1	Keyboard / Mouse	P2	√	√	√
				Reset		P2	√	√	√
√	√	√	P2	Power Button		-			
√	√	√	P2	LEDs		P2	√	√	√
√	√	√	P2	USB 0		P2	√	√	√
√	√	√	P2	USB 1		P2	√	√	√
√	√	√	P2	COM 1		P2	√	√	√
√	√	√	P2	COM 2		P2	√	√	√
√	√	√	P2	PMC 1 I/O		P2	√	√	√
√	√	√	P2	VME bus		P2	√	√	√

CC Conduction Cooled
*1 Rear DVI-I connector for DVI and VGA on transition module
*2 Front or Rear as an order option
*3 IDE primary and PMC 2 I/O use shared pins
Full PMC 2 rear I/O if IDE primary is not used
Partly PMC 2 rear I/O if IDE primary is used
*4 DVI-1 pins are shared with GPIO pins
*5 PMC 2 rear I/O is not possible if Ethernet 1 & 2 or VGA on the front are used because the PMC cannot installed on the SBC in this case



NOTE

If onboard hard disk/flash drive is used than no PMC 2 is available

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Glossary

ACPI	Advanced Configuration and Power Interface
APIC	Advanced Programmable Interrupt Controller
BIT	Built-In Test
CE	Conformité Européenne (European conformity)
CPU	Central Processing Unit
DDR3	Double-Data-Rate three
DMA	Direct Memory Access
DMI	Direct Media Interface
DOS	Disk Operating System
DRAM	Dynamic Random Access Memory
DVI	Digital Visual Interface
ECC	Error Correction Checking
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
EU	European Union
EU	Execution Unit
FCC	Federal Communication Commission (USA)
FDI	Flexible Display Interface
FSB	Front-Side Bus
GPIO	General Purpose I/O
GT	Giga Transfers
HP	Horizontal Position (1 HP = 5.08 mm)
I2C	Inter Integrated Circuit
I/O	Input / Output
IPMI	Intelligent Platform Management Interface
IRQ	Interrupt ReQuest
LAN	Local Area Network
LED	Light Emitting Diode
LPC	Low Pin Count
LV	Low Voltage
PCB	Printed Circuit Board
PCH	Peripheral Controller Hub

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PCI	Peripheral Component Interconnect
PCIe	Peripheral Component Interconnect Express
PICMG	PCI Industrial Computer Manufacturers Group
PLD	Programmable Logic Device
PMC	PCI Mezzanine Card
POST	Power-On Self Test
RAID	Redundant Array of Independent Disks
RMA	Return Material Authorization
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SBC	Single Board Computer
SCSI	Small Computer System Interface
SDVO	Serial Digital Video Out
SMB	System Management Bus
SPI	Serial Peripheral Interface
SV	Standard Voltage
TDP	Thermal Design Power
UART	Universal Asynchronous Receiver Transmitter
UEFI	Unified Extensible Firmware Interface
ULV	Ultra Low Voltage
USB	Universal Serial Bus
VGA	Virtual Graphics Array
VITA	VMEbus International Trade Association
VME	not a specific abbreviation (Versatile Modular Eurocard)
XMC	Switched Mezzanine Card
xU	Unit of vertical height of vertically mounted boards (1U = 44.45 mm)

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