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MODEL 104-AIO12-8
104-AI12-8
104-AO12-4

USER MANUAL

FILE: M104-AIO12-8.D5b

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Chapter 1: Introduction

Flexibility

The following functions are available in many configurations. This gives the user the ability to specify exactly what's needed in order to minimize costs. Interrupts from each circuit can eliminate the need for constant polling. Interrupts are individually enabled or disabled via software. A status register is provided to determine the interrupt source.

Analog In

The Analog Inputs feature software programmable gain with ranges of 0-5V, 0-10V, ±5V, and ±10V. The configuration employs an instrumentation pre-amplifier per channel which allows for true differential inputs, 200V Common Mode Rejection, and high input impedance. The gain may be set at the factory to accommodate low-level inputs from sensors. Also, any combination of channels may be factory configured to convert 4-20mA current. This feature includes a built-in offset to allow for full 12-bit resolution on the current input. The board may be ordered without the instrumentation amplifiers as a factory option if the inputs are from single-ended sources.

Analog Out

Output ranges of 0-5V, 0-10V, ±5V and ±10V, are field selectable with jumpers. Note that four conversions may take place at once.

Digital I/O

The circuit uses an 82C55A Programmable Peripheral Interface. Ports A and B (16 lines) are buffered and all 24 lines have pull-up resistors to 5V. As a factory option, lines can be pulled down to ground. Port C is not buffered and should normally be used only as inputs. Port C also features Change of State detection.

Counter/Timer

The circuit uses an 82C54 Programmable Interval Timer (3 sixteen bit counter/timers). The user has access to each counter/timer's gate, clock, and output signals. The output of counter one can be used to generate an interrupt. The Counter/Timer can be used to initiate A/D conversions for more precise timing between samples, thus eliminating "jitter" which can occur when initiating conversions via software command. The software package supports counting events, frequency output, pulse and frequency measurement.

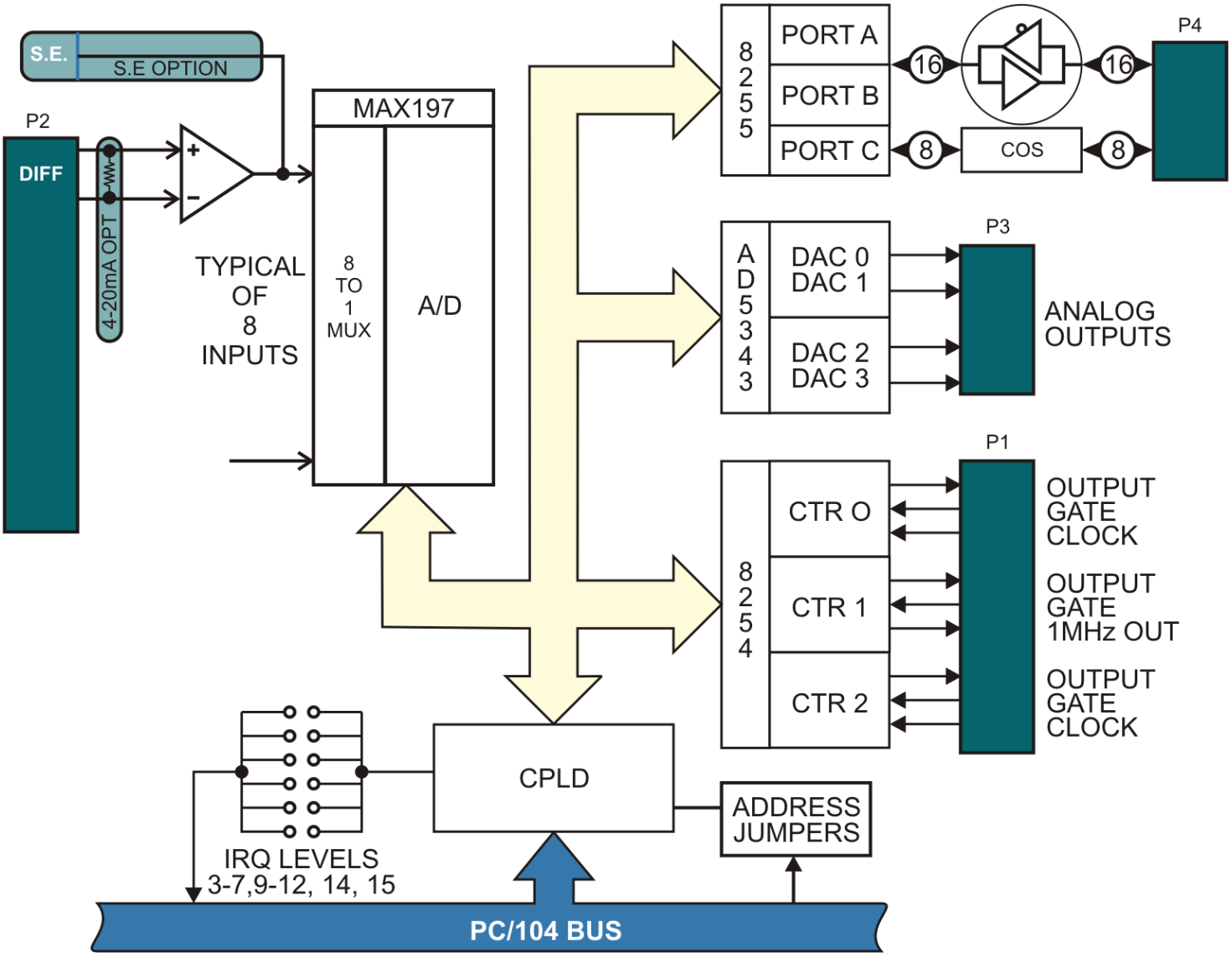


Figure 1-1: 104-AIO12-8 Analog Multifunction Board Block Diagram

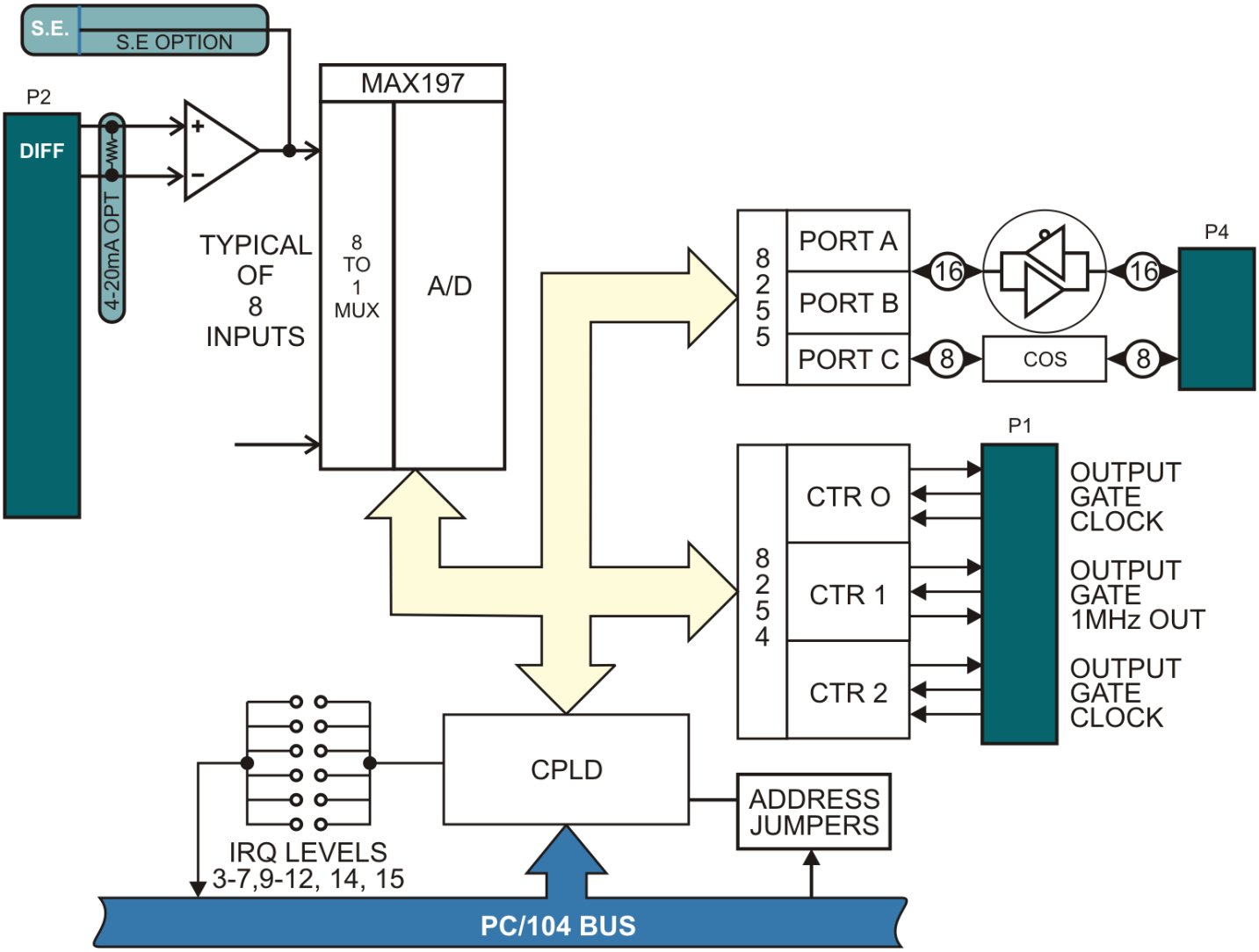


Figure 1-2: 104-AI12-8 Analog Input Board Block Diagram

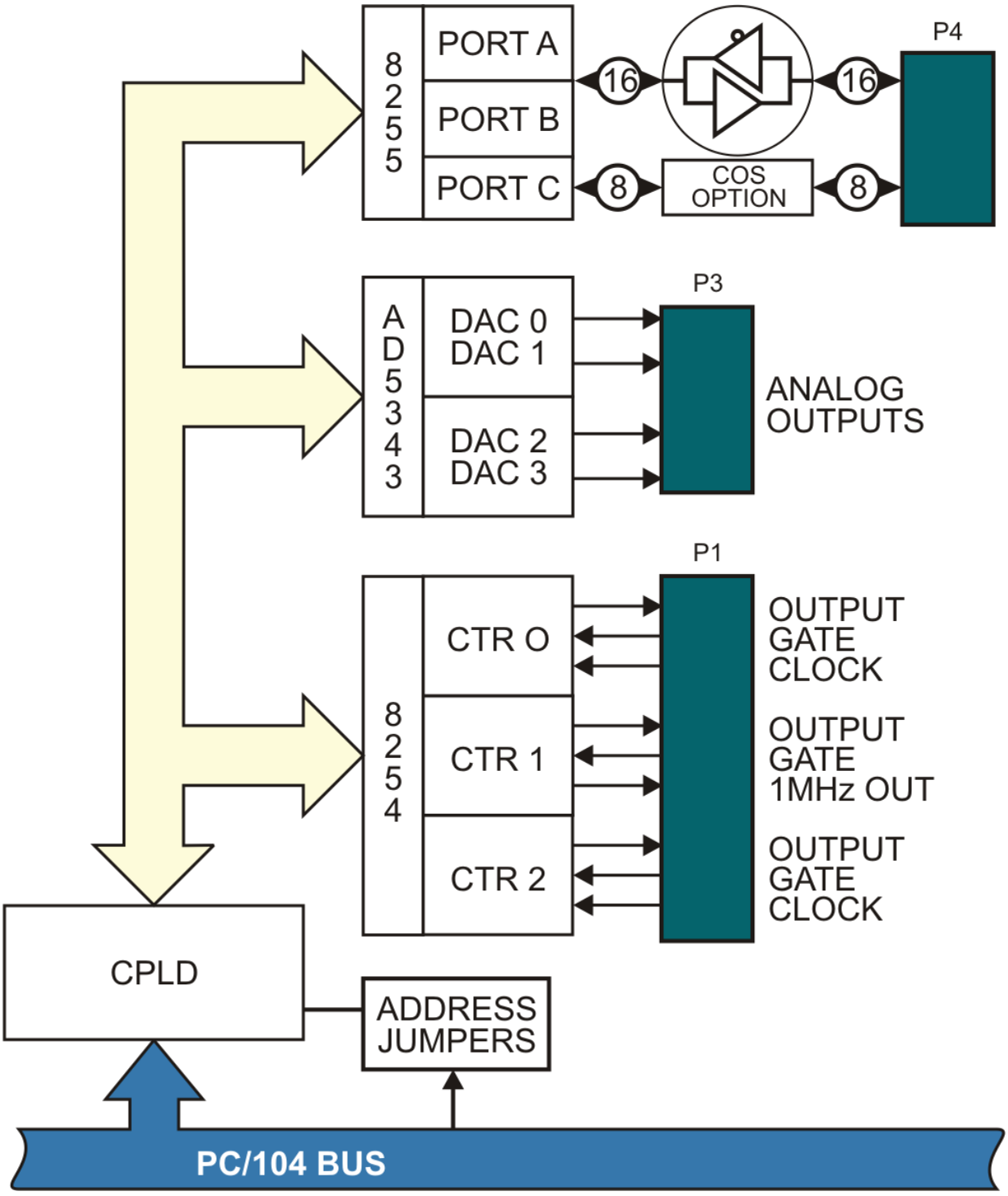


Figure 1-3: 104-AO12-4 Analog Output Board Block Diagram

Ordering Guide

- 104-AIO12-8 PC/104 12-Bit analog input/output multi-function board
- 104-AI12-8 PC/104 12-Bit analog input multi-function board
- 104-AO12-4 PC/104 12-Bit analog output multi-function board

Model Options

- 4-20mA inputs with offset
- Channel by channel pre-amplifier gains of 1-100
- Single-ended inputs
- +5VDC only operation
- -40 to +85°C extended operating temperature
- Pull-down resistors on digital I/O lines

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104 Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Installing the Hardware

Before installing the board, carefully read Chapter 3 and Chapter 4 of this manual and configure the board according to your requirements. The SETUP Program can be used to assist in configuring jumpers on the board. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. To help avoid this problem, refer to the FINDBASE.EXE program installed from the CD. The setup program does not set the options on the board, these must be set by jumpers.

To Install the Board

1. Install jumpers for selected options and base address according to your application requirements, as mentioned above.
2. Remove power from the PC/104 stack.
3. Assemble standoff hardware for stacking and securing the boards.
4. Carefully plug the board onto the PC/104 connector on the CPU or onto the stack, ensuring proper alignment of the pins before completely seating the connectors together.
5. Install I/O cables onto the board's I/O connectors and proceed to secure the stack together or repeat steps 3-5 until all boards are installed using the selected mounting hardware.
6. Check that all connections in your PC/104 stack are correct and secure then power up the system.
7. Run one of the provided sample programs appropriate for your operating system that was installed from the CD to test and validate your installation.

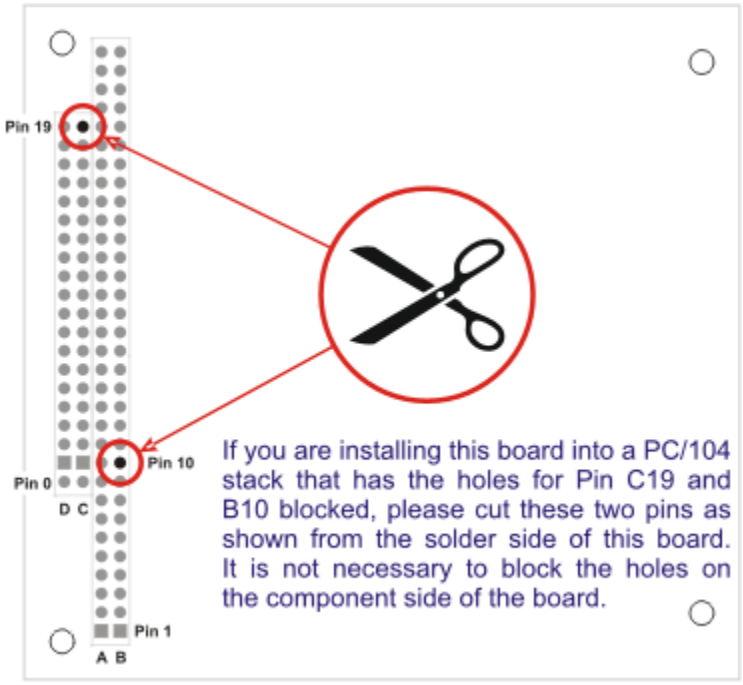


Figure 2-1: PC/104 Key Information

Chapter 3: Option Selection

Refer to the Setup Program on the provided CD for details of selecting appropriate options for your application. Jumpers are available on the board to configure the following functions:

1. Base address (jumpers labeled A5 through A9, see Chapter 4 for details)
2. IRQ level
3. DAC output voltage ranges
4. Mode 1 Digital Inversion (82C55) on Digital I/O
5. +/-12V Power Options (JP20, JP21)

As Factory Options, you can also order the board:

- for use with single-ended inputs (without instrumentation amplifiers)
- configured for any number of 4-20mA inputs (up to 8)
- configured with pull-down resistors on digital I/O lines
- ***with a DC/DC converter installed so the board operates on +5V only***
- to operate in an industrial temperature range

Your board also may be populated with any combination of functionality such as Digital I/O with four DAC channels, or Analog Inputs with 82C54 Counter/Timers. This is indicated by a label on the PC/104 connector that has a part number ending in -S0X, where X indicates a unique number identifying a special configuration.

The standard board has most of the functionality that the board is capable of with the exception of the following factory installed options: ±12V DC/DC converter and 4-20mA inputs.

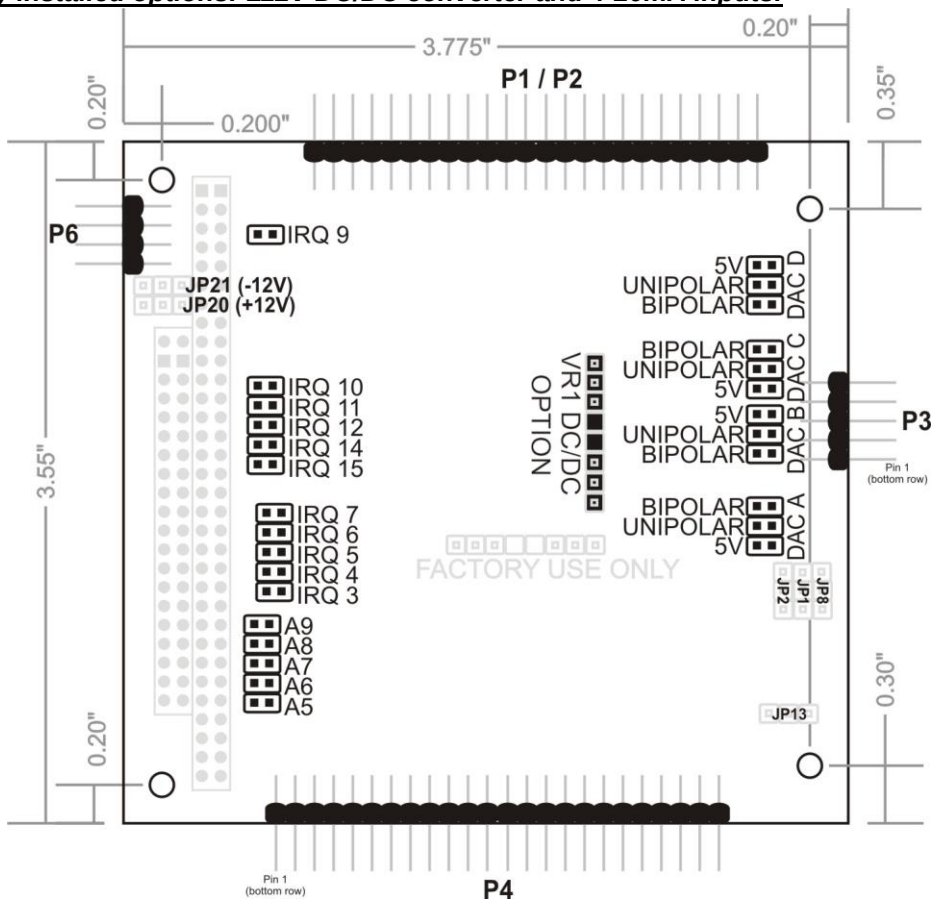


Figure 3-1: Option Selection Map

DAC Range:
Set these jumpers to select the range of each DAC. DACs A and C use the same layout (similar to the ones on the top), and DACs B and D use the same layout (similar to the ones on the bottom).

Analog Output
The card has four 12-bit analog output channels based on a pair of AD5343 dual D/A chips.

Analog Input and Counter/Timer
The card has an Integrated Multiplexer and A/D chip, which has 8 single ended inputs. Instrumentation amplifiers are populated on the standard board model for true differential readings. The board may be ordered without those differential amplifiers installed as a factory option, as well as offset circuitry and dropping resistors as a factory option to read 4-20mA signals. The card also has three 16-bit counter/timers based on an industry-standard 8254 chip (specifically, a Harris Semiconductor 82C54).

The A/D range is software-selectable to ±5V, 0-5V, ±10V, or 0-10V. In bipolar modes, the data is returned in standard two's-complement form. The gate, clock, and output pins for each counter are exposed on the connector. Counter 2's output can generate interrupts. Counter 1's clock has a 1MHz input. These counter/timers can be used for frequency generation, frequency measurement, pulse width measurement, and event counting, and can be cascaded together for larger counts.

Digital I/O
The card has 24 bits of digital I/O based on an industry-standard 8255 chip (specifically, a Harris Semiconductor 82C55A). All 8255 modes are supported by the card, with jumpers controlling the inversions necessary for Mode 1 operation.

Ports A and B are buffered. Port C features change-of-state detection. All pins have pull-ups to 5V.

Mode 1 Digital Inversion (JP2, JP1, JP8 and JP13)
These jumpers invert four bits of Port C of the 8255 digital I/O chip on the card. This is intended for 8255 Mode 1 operation; inverting bits 1 and 2 allows Port A to be a Mode 1 port talking to an uninverted Mode 1 port, and inverting bits 5 and 6 does the same with Port B.

The inverters treat bits 1 (JP1) and 5 (JP8) as outputs and bits 2 (JP2) and 6 (JP13) as inputs, which is how they're used in 8255 Mode 1. When uninverted, these bits can freely be inputs or outputs.

+/-12V Source (JP20 and JP21)
Set these jumpers to select where the card gets ±12V reference power. In the left position, they're taken from the PC-104 connector. In the right position, they're taken from P6, the eight-pin connector just below these jumpers; +12V is taken from pin 4 and -12V from pin 6.

DC/DC Converter (VR1) Factory Option
This option is needed when the PC/104 bus J1 (or P6) is not providing both +12V *and* -12V. If these voltages are not supplied to the board the A/D and D/A circuitry will not operate properly.

Chapter 4: Address Selection

The board base address on the I/O bus is set by JUMPERS next to the PC/104 connector. The jumper posts are marked A5 through A9 and A5 is the least significant bit of the address. The base addresses can be selected anywhere within the I/O address range 100-3FF provided that they do not overlap with other functions. The FINDBASE software utility provided on CD with your board will help you select a base address that does not conflict with other assignments. If in doubt, refer to the following table for a list of standard address assignments.

In order to configure the desired address, the hexadecimal address must be converted to a binary representation.

For example, as illustrated below, jumper selection corresponds to hex **2C0 (or binary 10 110xxxxx).** The "xxxxx" represents address lines A4 through A0 used on the board to select individual registers as described in the Chapter 5, Programming of the manual.

Hex Representation	2		C		
Conversion Factors	2	1	8	4	2
Binary Representation	1	0	1	1	0
Jumper Setting	Out	In	Out	Out	In
Jumper Label	A9	A8	A7	A6	A5

Table 4-1: Hex Representation

Please note that “1" = “out” (no jumper) and “0" = “in” (jumper installed).

Review the Address Selection Table carefully before selecting the board address. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. If you have doubts concerning available addresses in your particular computer, use the FINDBASE utility provided to determine available addresses.

HEX RANGE	USAGE
000-00F	8237 DMA Controller 1
020-021	8259 Interrupt
040-043	8253 Timer
060-06F	8042 Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Register
0A0-0BF	8259 Slave Interrupt Controller
0C0-0DF	8237 DMA Controller 2
0F0-0F1	Math Coprocessor
0F8-0FF	Math Coprocessor
170-177	Fixed Disk Controller 2
1F0-1F8	Fixed Disk Controller 1
200-207	Game Port
238-23B	Bus Mouse
23C-23F	Alt. Bus Mouse
278-27F	Parallel Printer
2B0-2BF	EGA
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	Serial Port
2F8-2FF	Serial Port
300-30F	
310-31F	
320-32F	Hard Disk (XT)
370-377	Floppy Controller 2
378-37F	Parallel Printer
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	Parallel Printer
3C0-3CF	VGA EGA
3D0-3DF	CGA
3E8-3EF	Serial Port
3F0-3F7	Floppy Controller 1
3F8-3FF	Serial Port

Table 4-2: Standard Address Assignments for Computers

Chapter 5: Programming

The board uses 24 consecutive registers in I/O space as follows:

Offset	Read Function	Write Function
00h	Board Status / Clear Board Status	IRQ Clear
01h	Interrupt Status	Interrupt Enables
02h	A/DC Low Byte	A/D Control / Start Conversion
03h	A/DC High Byte	
04h		D/AC 1 LSB
05h		D/AC 1 MSB
06h		D/AC 2 LSB
07h		D/AC 2 MSB
08h		D/AC 3 LSB
09h		D/AC 3 MSB
0Ah		D/AC 4 LSB
0Bh		D/AC 4 MSB
0Ch	Counter/Timer 0 Value	Counter/Timer 0 Load Value
0Dh	Counter/Timer 1 Value	Counter/Timer 1 Load Value
0Eh	Counter/Timer 2 Value	Counter/Timer 2 Load Value
0Fh		Counter Control
10h	Digital I/O Port A	Digital I/O Port A Output Value
11h	Digital I/O Port B	Digital I/O Port B Output Value
12h	Digital I/O Port C	Digital I/O Port C Output Value
13h	Digital I/O Status (Modes 1 & 2)	Digital I/O Command Byte
14h		Digital I/O Buffer Control
15h		A/DC Command
16h		Counter Trigger Enables
17h	COS Status / Clear COS Status	
18h		DAC Reference Enable* (also 4-20mA inputs)

Table 5-1: Register Address Map

*__NOTE__: Applies only to Revision D and above. ***Also used to enable 4-20mA input factory option.***

Base + 0h: **Board Status**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A/DC EOC	Port C Change of State	reserved	reserved	reserved	IRQ Enabled	reserved	reserved

This register shows the state of the two events that can generate interrupts (IRQs), and the state of the global interrupt enable. The interrupt enables/disables have no affect on the events shown in this register. All bits are active HIGH. Also, all of the event bits are latched; when an event occurs, its bit goes HIGH until this register is read. Reading this register clears it.

Writing to this register clears IRQs (see the description of IRQ enables).

Bit 7 goes HIGH when an A/D conversion completes (used for simple A/D acquisition).

Bit 6 goes HIGH when any DIO bit on Port C changes.

Bit 2 reflects the global interrupt enable written to Base + 1h. This is not an event, and is not cleared when read.

Base + 1h: **Interrupt Enables, Interrupt Status**

Operation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
READ	A/DC IRQ	Change of State IRQ	Counter 1 IRQ	Digital I/O Port C3 IRQ	Digital I/O Port C0 IRQ	IRQ Event	always zero	always zero
WRITE	A/DC IRQ Enable	Change of State IRQ Enable	Counter 1 IRQ Enable	Digital I/O Port C3 IRQ Enable	Digital I/O Port C0 IRQ Enable	Global IRQ Enable		

All bits are active HIGH. Reading this address accesses the Status register. Writing to this address affects the Enables register. Note that the register that's written to is not the same register that's read at this address.

Interrupts from this board can be shared. The IRQ driver will pull the PC/104 interrupt line LOW for 500nS, briefly drive it HIGH, and then tri-state. After an interrupt is generated another won't be allowed until the IRQ has been cleared (write to Base+0h) and the data read (for some event types).

If multiple enabled events occur (for example, an A/D end of conversion and a Port C change of state), and only one is cleared (for example, by reading the A/D data and writing to Base+0h but not reading the COS data), the other event will cause another interrupt.

Set bit 2 HIGH to enable interrupts from the board. The default after system RESET is LOW. Without this global enable set, the board will not generate interrupts of any kind. If an interrupt has been generated by the board, this bit will be HIGH when read.

Set bit 7 HIGH to enable interrupts from the A/DC. When read, bit 7 is HIGH if the A/DC generated an interrupt that was not yet cleared. Read Base+2h and Base+3h to get the A/D data, and write to Base+0h to clear the board's interrupt so it can generate another.

Set bit 6 HIGH to enable interrupts from the Change of State detection circuit at DIO Port C. When read, bit 6 is HIGH if a change of state generated an interrupt that was not yet cleared. Read Base+17h to get the COS data, and write to Base+0h to clear the board's interrupt so it can generate another.

Set bit 5 HIGH to enable interrupts from falling edges of Counter 1. When read, bit 5 is HIGH if the counter generated an interrupt that was not yet cleared. Write to Base+0h to clear the board's interrupt so it can generate another.

Set bits 4 and 3 HIGH to enable interrupts from rising edges of DIO Port C bits 3 and 0, respectively. When read, bit 4 is HIGH if this bit generated an interrupt that was not yet cleared. Write to Base+0h to clear the board's interrupt so it can generate another.

Port C Change-Of-State (COS)
If any bit of Port C changes state, this event is noted in the board status register (Base+0h), an interrupt is generated if enabled (at Base+1h), and the specific bit that changed is noted in the COS status register (Base+17h). Multiple changes are accumulated in the COS status register until read.

For example, if Port C changed from "50" to "40", bit 4 has changed, so the COS status register will contain the value "10" (bit 4 high). If Port C then changed to "60", bit 5 has changed, so the COS status register will contain the value "30" (bits 4 and 5 high). If it's then read, this "30" will be read, and it will be cleared to "00".

Base + 2h Write: **A/D Control / Start Conversion**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device Mode 1	Device Mode 0	Acquisition Mode	Range	Bipolar / Unipolar	Channel Selection Bit 2	Channel Selection Bit 1	Channel Selection Bit 0

USING THE ANALOG TO DIGITAL CONVERTER

This circuit is based on a Maxim ADC chip. Please refer to file MAX197.pdf in the \CHIPDOCS directory on the CDROM. A conversion begins when a control byte is written to the ADC. The control byte contains five bit fields: channel selection, bipolar/unipolar, range, acquisition mode, and device mode. Normally, the acquisition mode and device mode bits will be zero.

The two bits in the device mode field select the clock source and the power state. Before putting the ADC in a power down state, a conversion with Normal Operation selected should be triggered. The chip will 'remember' this clock setting if the Standby power-down mode is subsequently used. The Standby state is entered after a conversion is complete, there is no start-up delay on the next conversion. There is a 50mS start-up delay before a conversion from the full power-down state.

Bit 7	Bit 6	Device Mode
0	0	Normal Operation, selects the external (to the ADC) clock mode, a 2MHz clock frequency is applied
0	1	Internal clock mode, not appropriate for this circuit, unexpected events may occur if this mode is selected
1	0	Standby power-down, supply current will typically be 700uA
1	1	Full power-down, supply current will be 120uA worst case

The ADC has a Sample and Hold circuit controlled by the Acquisition Mode bit. A control byte with this bit set low will select an acquisition interval of 3uS after which a conversion will begin. A noisy signal may require more integration. A control byte with this bit set high will start a user-determined acquisition period, conversion will begin when a 2nd control byte is sent with bit 5 set low. Bits 0, 1, and 2 must be the same value but the power state may be changed. Bit 4, the range bit, doubles the input voltage range when set. Bit 3 selects bipolar mode when set.

Range (Bit 4)	Bipolar / Unipolar (Bit 3)	Input Range
0	0	0 - 5V
1	0	0 - 10V
0	1	±5V
1	1	±10V

The channel selection bits direct one of the eight analog inputs connected to the ADC's multiplexor to the Sample and Hold circuit. Bits 2, 1, and 0 make a binary value equal to the channel number.

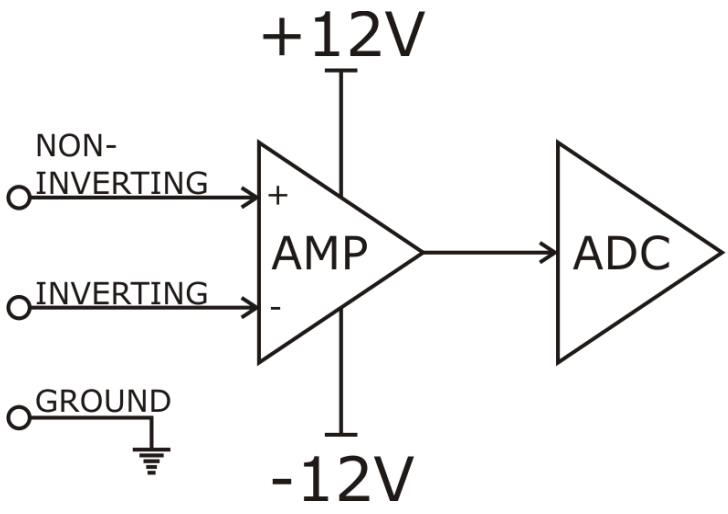


Figure 5-1: Differential Source to Differential Input

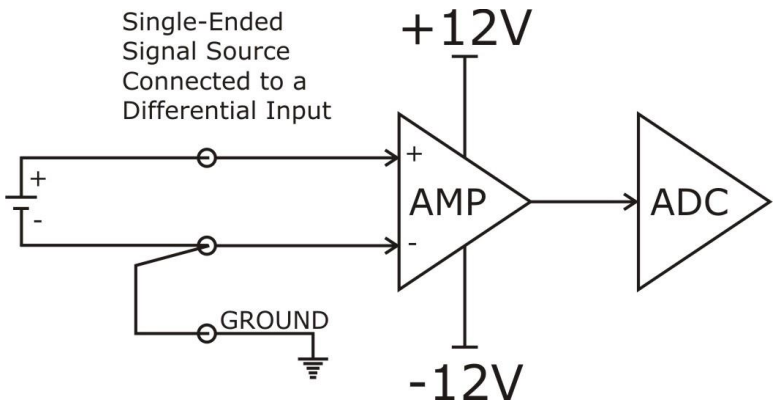


Figure 5-2: Single-Ended Source to Differential Input

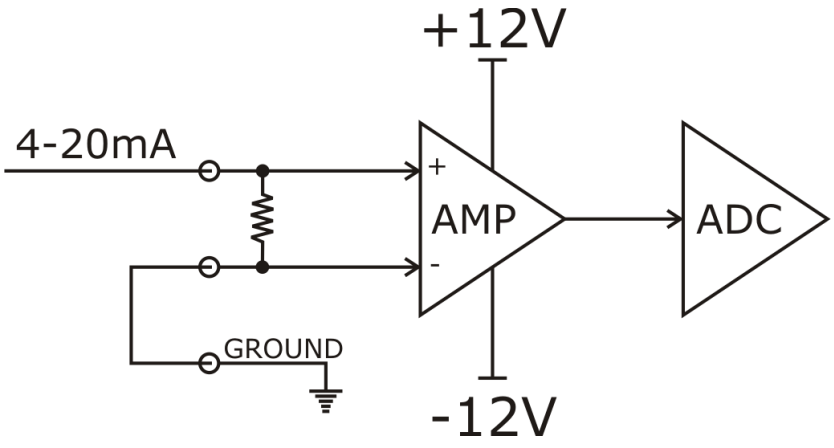


Figure 5-3: 4-20mA Source to Differential Input

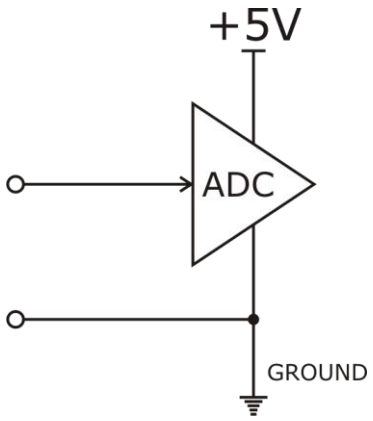


Figure 5-4: Single-Ended Input Stage

Base + 2h / 3h Read: **A/D Data**

Base + 3h (8 bit, rarely used)								Base + 2h (8 or 16-bit)							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
unused				d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

Reading base + 2h as a 16-bit value will return the results of the most recently completed A/D conversion. Although it is possible to read the two bytes comprising the value separately, it is not necessary, and is slower.

The data is in two's complement format in Bipolar modes, and is an unsigned 12-bit value in unipolar modes.

Base + 4h / 5h through Base + Ah / Bh: **DAC Output**

Base + 5h, 7h, 9h, Bh (8 bit, rarely used)								Base + 4h, 6h, 8h, Ah							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
unused				d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

No voltage can be generated by the DACs until the DAC reference enable register at Base +18h has been configured to enable the reference. Every system reset disables the DAC reference until enabled by your software.

Writing a 16-bit value to the DAC Output register will update that DACs output to the new value. Only the bottom 12-bits of the 16-bit data are significant (decimal values 0 through 4095).

The output voltage is given by:
V_{out} = (Gain * V_{ref} * Counts / 4096) + Offset

where V_{ref} = 4.096V and Counts = the decimal equivalent of the binary code written to the DAC (a number between 0 and 4095).

Jumper Selected DAC Range	0-5V	0-10V	±5V	±10V
Gain	1.22	2.44	2.44	4.88
Offset	0V	0V	-5V	-10V

On power-up, the DAC output values will be at the most negative for the selected range.

If bit 0 (DACTRIG) is set at Base + 16h, writing to these registers will not update the DACs. In this mode, DAC updates occur simultaneously on all DACs only when the trigger event occurs.

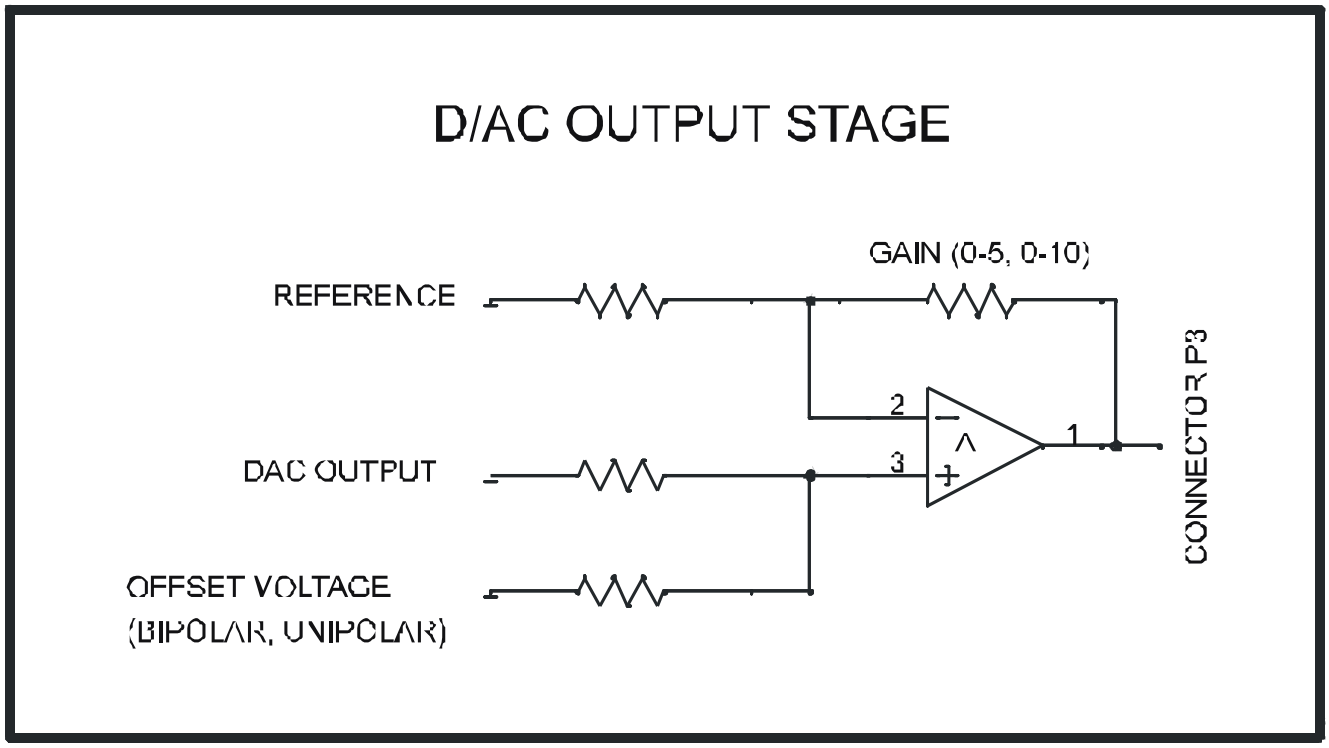


Figure 5-5: D/AC Output Stage

Base + Ch through Base + Fh: **8254 Counter Timer**

Please refer to Appendix B: 8254 for detailed information on using the full features of the 8254 chip.

USING COUNTER 1 TO TRIGGER A/D and D/A CONVERSIONS

In Mode 2 the Counter chip will generate a 1 microsecond negative going pulse at a programmed rate. If bit 1 of the Timer-Triggered Conversion Enable register (base address + 16h) is set high, the ADC chip will initiate conversions on the tick. If bit 0 is set high the DAC chip will initiate conversions on the tick.

The ADC chip needs a command byte to begin a conversion. This byte is stored in the ADC Command register at base + 15h. Note that only the lowest 5 bits are significant, the top 3 bits will automatically be zeros.

All of the DACs present will be updated simultaneously. Typically, the user would configure the board to generate an interrupt on the tick from counter 1; the user would also enable DAC conversions triggered by the same tick.

Base + 10h, +11h, +12h: **Digital I/O**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port Bit 7	Port Bit 6	Port Bit 5	Port Bit 4	Port Bit 3	Port Bit 2	Port Bit 1	Port Bit 0

Each of these three registers contains one 8-bit digital value. Base + 10h is the value associated with 8255 Port A. Base + 11h is Port B, and Base + 12h is Port C (also known as Chi / Clo).

Reading these registers will return either the current state of the inputs, or the current state of the outputs, depending on the current mode of each port.

Base + 13h: **Digital I/O Command Byte**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Mode Set Flag	Group A Mode	Group A Mode	Port A Direction	Port C Upper Direction	Group B Mode	Port B Direction	Port C Lower Direction
1 = Active	1 = Mode 2 0 = use Bit 5	1 = Mode 1 0 = Mode 0	1 = Input 0 = Output	1 = Input 0 = Output	1 = Mode 1 0 = Mode 0	1 = Input 0 = Output	1 = Input 0 = Output

This circuit is based on an 82C55A chip. Please refer to file 82C55.pdf in the \CHIPDOCS directory.

On power-up or on Reset the circuit will be in the mode 0 input state. That is, ports A and B (each 8 bits) and ports Chi and Clo (each 4 bits) will be readable, and any floating pins at connector P4 will be high.

To change Port A and Port B I/O configuration, there are two modes. In the default mode the buffers' direction is automatically set by the command-byte. This mode is designed to support 'off the shelf' software.

The cards are designed to use the PPI in mode 0 wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

The PPI contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. The PPI should be configured during initialization by writing to the control registers even if the ports are going to be used as inputs. Output buffers are automatically set by hardware logic according to the control register states. The control register is located at base address +13h. Bit assignments in this control register is as follows:

Bit	**Assignment**	**Function**
D0	Port C Lo (C0-C3)	1 = Input, 0 = Output
D1	Port B	1 = Input, 0 = Output
D2	Mode Selection	1 = Mode 1, 0 = Mode 0
D3	Port C Hi (C4-C7)	1 = Input, 0 = Output
D4	Port A	1 = Input, 0 = Output
D5,D6	Mode Selection	01 = Mode 1, 00 = Mode 0, 1X = Mode 2
D7	Mode Set Flag & Tristate	1 = Active & Tristate, 0 = Inactive

Table 5-2: Control Register Bit Assignments

Note
In Mode 0, do not use the control register byte for the individual bit control feature. The hardware uses the I/O bits to control buffer directions on this card. The control register should only be used for setting up input and output of the ports and enabling the buffer.

Programming Example

The following programming example is provided as a guide to assist you in developing your working software. In this example, the PPI base address is 2D0 hex and I/O lines of Port 0 are to be setup as follows:

port A	=	Input
port B	=	Output
port C hi	=	Input
port C lo	=	Output

Configure bits of the Control Register as:

D0	0	Port C Lo Output
D1	0	Port B Output
D2	0	Mode 0
D3	1	Port C Hi Input
D4	1	Port A Input
D5	0	Mode 0
D6	0	Mode 0
D7	1	Active Mode Set

This corresponds to 98 hex. If the PPI base address is 2D0 hex, use the BASIC OUT command to write to the control register as follows:

```
10    BASEADDR=&H2D0
20    OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C, use the BASIC INPUT command:

```
30    X=INP(BASEADDR)          'Read Port A
40    Y=INP(BASEADDR+2)/16     'Read Port C Hi
```

To set outputs high ("1") at Port B and the lower nybble of Port C:

```
50    OUT BASEADDR+1,&HFF      'Turn on all Port B bits
60    OUT BASEADDR+2,&HF       'Turn on all bits of Port C Lo
```

This circuit can, as a factory installed option, operate in 8255 programmed I/O Modes 1 and 2. Note that if Bit 6 is set then Bit 5 is unused.

Base + 14h: **Digital I/O Buffer Control**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
unused							TST

If the TST bit (bit 0) is set, the TRISTATE mode is entered. Clear bit 0 to exit TRISTATE mode.

When software configures an 8255 port to be an output the lines will immediately all go low (odd quirk of the chip). Since most control signals are active-low, this is considered sub-optimal. When in TRISTATE mode, this board will tri-state the associated buffer when it becomes an output. This allows the lines to be pulled high by the onboard pull-ups. Software would then initialize the outputs and re-enable the buffer(s), preventing a low-going glitch from occurring.

To re-enable the buffers, simply write the control byte a 2nd time, but with Bit 7 cleared. That is, if and only if you are in TRISTATE mode, every write to Base + 13h should be followed (after writing an initial output value to every port in output mode) by another write to Base + 13h, containing “the same command byte AND 0x7F.”

Base + 15h: **A/D Counter-Triggered Command Byte**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused			Range	Bipolar / Unipolar	Channel Selection Bit 2	Channel Selection Bit 1	Channel Selection Bit 0

The value written here is stored for use when starting conversions via the 8254 Counter 2 trigger output (see Base + 15h). The format of the data in bits 4 through 0 is identical to Base + 2, and the top 3 bits are handled internally, simply write 0s to these bits.

Note: The channel selected here will be used each time the 8254 counter 2 starts an A/D conversion. Base + 2h is ignored for this mode of operation.

Base + 16h: **Counter Trigger Enables**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused						ADTRIG	DACTRIG

Write to this register to enable Counter 1 to generate trigger events for the A/D and / or DAC circuit. Each negative going pulse from the output of Counter 1 will be used as a trigger for enabled events. Set Bit 1 (ADTRIG) to enable the output of counter 1 to generate Start A/D Conversion triggers. Set Bit 0 (DACTRIG) to use the output to trigger DAC Conversions.

Note the value loaded in Base +15h is used as the A/D control byte for counter triggered A/D conversions. If you wish to acquire timed data from more than this single channel, you must write a new A/D control value to Base + 15h before the next trigger output from CTR 1.

Base + 17h: **COS Status / Clear COS Status**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PC 7 COS	PC 6 COS	PC 5 COS	PC 4 COS	PC 3 COS	PC 2 COS	PC 1 COS	PC 0 COS

Each bit of this register indicates “Has this bit of Port C changed since I last checked?” when read.

The memory of COS events is cleared by reading the register.

That is, if you reset the board, toggle bit n of Port C any number of times and read this register, bit n of this register will be set high (1). If you then toggle any other bit of Port C any number of times and read this register, only the new bit will be set high.

Base + 18h: **DAC Reference Enable (also used for 4-20mA input Factory option)**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Unused							DAC Reference Enable

Bit 0 is set to zero at every board reset. In order to generate voltages with the DACs, you must first set Bit 0 (write "1" to Base + 18h).

If your board has the Factory option of 4-20mA inputs, the DAC Reference Voltage is used for the offset of the 4-20mA signals instead of the A/D reference. Therefore, you must set Bit 0 once at every board start-up prior to reading the 4-20mA input signals.

At power–on or reset, all DACs will be generating a near-ground voltage only because the DAC reference is disabled. The DAC chips themselves are trying to generate random voltages. If you simply re-enable the DAC reference after a reset your output voltages will be random. To avoid this, write known values to all DACs (via the Base +4h through Base +Bh registers) before enabling the DAC Reference here.

Note: this feature exists only on boards with Revision D and above.

Chapter 6: Connector Pin Assignments

IDC 10-Pin Header Male

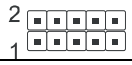


Table 6-1: P3 DAC				
Pin 2 DAC A Output	Pin 4 DAC B Output	Pin 6 4.096V Reference Output	Pin 8 DAC C Output	Pin 10 DAC D Output
Pin 1 Ground	Pin 3 Ground	Pin 5 Ground	Pin 7 Ground	Pin 9 Ground

Each DAC output can drive up to +10mA. Due to a limitation of the optional DC/DC converter power supply, the total drive of these four signals should be kept below 20mA. If ±12V power is supplied at the ISA bus connectors or at P6, there isn't a cumulative drive current limit.

Each DAC output has three configuration jumpers. If the jumper labeled 'DAC x 5V' (where x is either A, B, C, or D) is in place, the range is limited to 5V (0-5V or ±5V). If the jumper labeled 'UNIPOLAR' is in place the range is limited to 0-5V or 0-10V. If the jumper labeled 'BIPOLAR' is in place the range is either ±5V or ±10V. Note that 'UNIPOLAR' and 'BIPOLAR' are mutually exclusive.

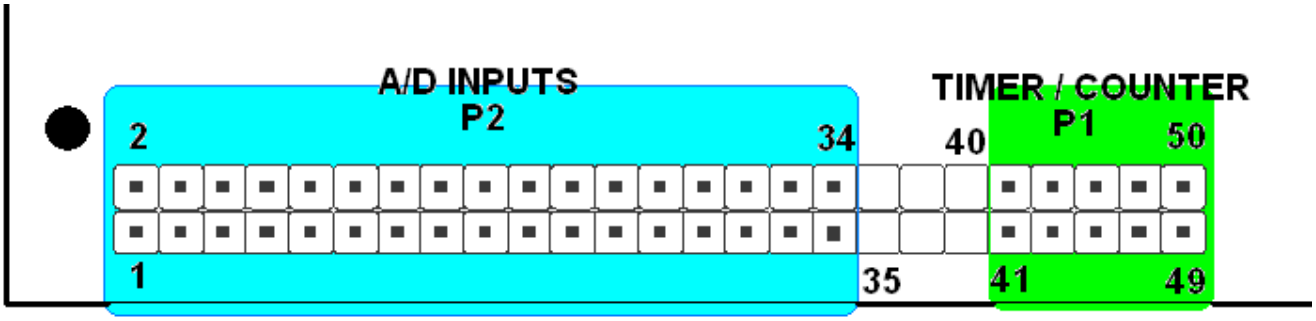


Figure 6-1: P2 Analog Inputs / P1 Timer Counter Arrangement Diagram

P1 and P2 are combined into one 50 pin connector. P1 starts where P2 ends (P2 is the A/D inputs and has 34 pins). P1 is the closest to you and pin 1 is on the bottom row (pin 41 in the combined arrangement). See also the next page for the pinout of P2. Pins 35-40 are not used.

Pins 42 and 48 are the clock or event inputs for the Programmable Interval Timer counters Zero and Two and are pulled-up to +5V through a 10K resistor. 8MHz is the maximum frequency. Pin 45 is an output of the 1MHz square wave applied to the clock input of counter one.

Pins 43, 46, and 49 are the gate inputs and are pulled-up to +5V through a 10K resistor. Pull these inputs low to pause/disable the counters.

Pins 44, 47, and 50 are the counter outputs and can not tri-state.

Either TTL or CMOS signal levels are acceptable at all inputs. The 1MHz clock signal (pin 45) is a CMOS output.

Table 6-2: P1 (P2 split) Timer-Counter					
Pin # P1	*Pin # P2*	Function	Pin # P1	*Pin # P2*	Function
1	*41*	Ground	6	*46*	Gate 1 Input
2	*42*	Clock 0 Input	7	*47*	Out 1 Output
3	*43*	Gate 0 Input	8	*48*	Clock 2 Input
4	*44*	Out 0 Output	9	*49*	Gate 2 Input
5	*45*	1MHz Output	10	*50*	Out 2 Output

The 4.096V reference on pin 1 is current-limited by a 620Ω resistor. The Reference Adjust input is limited by a 510KΩ resistor and may have from 1V to 5V applied.

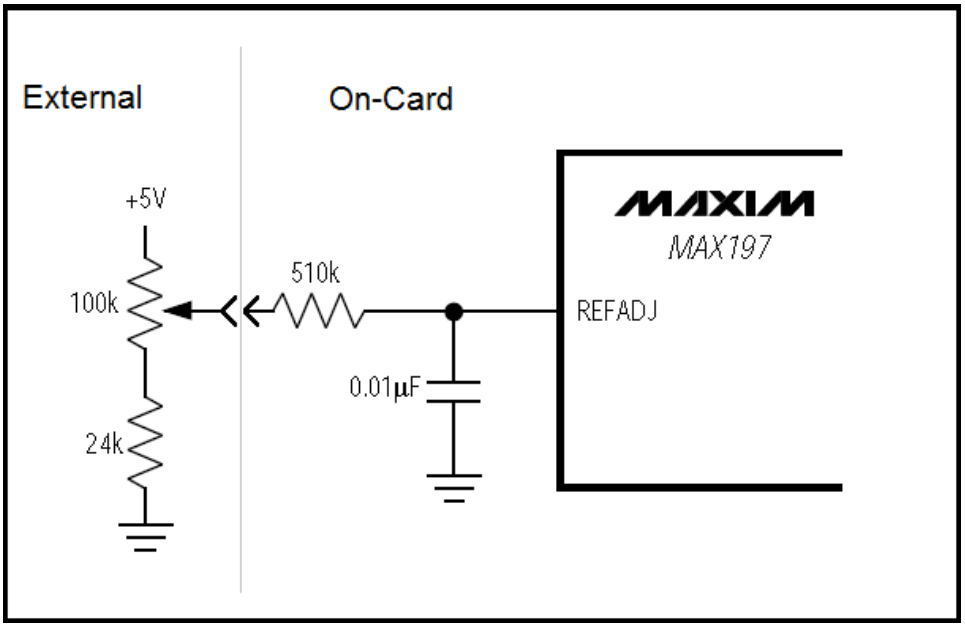


Figure 6-2: Internal Reference Adjust Circuit

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a 4.7µF capacitor to AGND and the REFADJ pin with a 0.01µF capacitor to AGND. The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit.

If the instrumentation amplifiers are present (as in the standard model), the inverting inputs are connected to ground through a 1M resistor. The non-inverting inputs are floating. Also, the instrumentation amplifier outputs are available at the Channel x Output pins (Ch 0-pin 6, Ch 1-pin 8, Ch 2–pin 14, Ch 3–pin 16, Ch 4–pin 22, Ch 5–pin 24, Ch 6–pin 30, Ch 7–pin 32). Use these pins with a Digital Multi-Meter to measure the output of the amplifier which should correspond to the input signal level. **Do not connect any signal source to these output pins!**

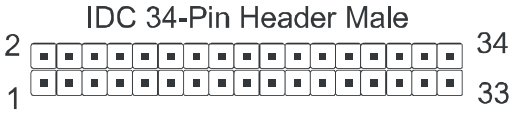


Table 6-3: P2 Differential Analog Inputs			
Pin 1	4.096V Reference Output	Pin 2	Reference Adjust Input
Pin 3	Ground	Pin 4	Channel 0 Non-inverting Differential Input
Pin 5	Channel 0 Inverting Differential Input	Pin 6	Channel 0 Differential Amplifier Output
Pin 7	Ground	Pin 8	Channel 1 Differential Amplifier Output
Pin 9	Channel 1 Inverting Differential Input	Pin 10	Channel 1 Non-inverting Differential Input
Pin 11	Ground	Pin 12	Channel 2 Non-inverting Differential Input
Pin 13	Channel 2 Inverting Differential Input	Pin 14	Channel 2 Differential Amplifier Output
Pin 15	Ground	Pin 16	Channel 3 Differential Amplifier Output
Pin 17	Channel 3 Inverting Differential Input	Pin 18	Channel 3 Non-inverting Differential Input
Pin 19	Ground	Pin 20	Channel 4 Non-inverting Differential Input
Pin 21	Channel 4 Inverting Differential Input	Pin 22	Channel 4 Differential Amplifier Output
Pin 23	Ground	Pin 24	Channel 5 Differential Amplifier Output
Pin 25	Channel 5 Inverting Differential Input	Pin 26	Channel 5 Non-inverting Differential Input
Pin 27	Ground	Pin 28	Channel 6 Non-inverting Differential Input
Pin 29	Channel 6 Inverting Differential Input	Pin 30	Channel 6 Differential Amplifier Output
Pin 31	Ground	Pin 32	Channel 7 Differential Amplifier Output
Pin 33	Channel 7 Inverting Differential Input	Pin 34	Channel 7 Non-inverting Differential Input

The 104-AIO12-8 can optionally be purchased for single-ended use, without the differential amplifiers. In this case, refer to the single-ended pinout table following where pins 6, 8, 14, 16, 22, 24, 30 and 32 are the inputs.

Table 6-4: P2 Single-Ended Analog Inputs

Pin 1	4.096V Ref: Output	Pin 2	Reference Adjust Input
Pin 3	Ground	Pin 4	N/C
Pin 5	N/C	Pin 6	Channel 0 Input
Pin 7	Ground	Pin 8	Channel 1 Input
Pin 9	N/C	Pin 10	N/C
Pin 11	Ground	Pin 12	N/C
Pin 13	N/C	Pin 14	Channel 2 Input
Pin 15	Ground	Pin 16	Channel 3 Input
Pin 17	N/C	Pin 18	N/C
Pin 19	Ground	Pin 20	N/C
Pin 21	N/C	Pin 22	Channel 4 Input
Pin 23	Ground	Pin 24	Channel 5 Input
Pin 25	N/C	Pin 26	N/C
Pin 27	Ground	Pin 28	N/C
Pin 29	N/C	Pin 30	Channel 6 Input
Pin 31	Ground	Pin32	Channel 7 Input
Pin 33	N/C	Pin 34	N/C

In the case where the 104-AIO12-8 is fully populated with the differential amps here is a comparison of how the external signals are connected to the I/O pins:

Table 6-5: S.E. and Diff Signal Source Connections to Standard Bd.

	Single Ended	**Differential**
Input / Output	N/C	N/C
Non-inverting Differential Input	Input	Non-inverting Input
Inverting Differential Input	Ground	Inverting Input
Ground	Ground	Ground

The digital I/O bits are arranged in an industry standard configuration.

Pin 1 can be identified by the square pad on the bottom of the board. Also, with the PC/104 connector closest to you, pin 1 of P4 is on the bottom row, closest to you.

IDC 50-Pin Header Male

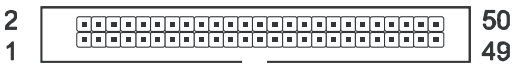


Table 6-6: P4, Digital I/O

Pin	Signal	Pin	Signal
50	All even numbered pins are GROUND	49	+5VFUSED
48		47	Port A Bit 0
46		45	Port A Bit 1
44		43	Port A Bit 2
42		41	Port A Bit 3
40		39	Port A Bit 4
38		37	Port A Bit 5
36		35	Port A Bit 6
34		33	Port A Bit 7
32		31	Port B Bit 0
30		29	Port B Bit 1
28		27	Port B Bit 2
26		25	Port B Bit 3
24		23	Port B Bit 4
22		21	Port B Bit 5
20		19	Port B Bit 6
18		17	Port B Bit 7
16		15	Port C Bit 0
14		13	Port C Bit 1
12		11	Port C Bit 2
10		9	Port C Bit 3
8		7	Port C Bit 4
6		5	Port C Bit 5
4		3	Port C Bit 6
2		1	Port C Bit 7

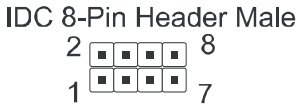


Table 6-7: P6, ±12V Power

Pin	Signal	Pin	Signal
1	GND	2	N/C
3	GND	4	+12V
5	GND	6	-12V
7	GND	8	N/C

Normally, the board takes ±12V power from the PC/104 bus. However, it can be used on a PC/104 stack that does not provide ±12V power by providing it here on P6.

Note: Pins 4 and 6 of P6 are connected to the corresponding lines of the PC/104 bus. If your PC/104 stack provides ±12V power, it will be sourced on these pins.

Appendix A: Technical Specifications

Analog Inputs

Feature	Value
Channels	8 True Differential
Conversion Frequency	100k Samples per Second
Differential Input Impedance S.E. (w/o pre-amp) Input Impedance	2MegΩ with pre-amp 21kΩ/16kΩ uni/bipolar
Gain Temperature Coefficient (typical)	6 ppm/°C, bipolar, 8ppm/°C unipolar
Common Mode Voltage	±200V
Integral Nonlinearity	±1 LSB maximum
Accuracy	0.2% of full scale
Noise levels	±1 LSB typical

Feature	Value
Programmable Voltage Ranges	0-5V, 0-10V, ±5V, ±10V (4-20mA as a factory option)
Resolution	12-Bit
Preamplifier gain	1 standard, up to 200 upon request
Reference Output Voltage	4.096V ±0.02V
Common Mode Rejection Ratio	86dB typical
Full Power-Down Mode Standby Power-Down Mode	1uA maximum 400uA maximum
Trigger Source(s)	Software selectable for program command or programmable timer

Analog Outputs

Feature	Value
Channels	4
Conversion Frequency	100k Conversions per second
Output Drive Capability	+10mA per channel
Relative Accuracy	2 LSB, typical

Feature	Value
Voltage Ranges	0-5V, 0-10V, ±5V, ±10V
Resolution	12-Bit
Power-Down Mode Current Draw	1uA, maximum
Trigger Source(s)	Software selectable for program command or programmable timer

Digital Input/Output

Feature	Value
Programmable Peripheral Interface	82C55A
Buffered Channels	16 (ports A & B)
Un-Buffered Channels	8 (port C)
Modes supported	mode 0 (1 and 2 factory options)

Feature	Value
Channels	24, (10KΩ to 5V, optional to ground)
Sink & Source Current	64mA & 32mA
Sink & Source Current	2.5mA (direct from 82C55A)
Change of State Detection	8 inputs (port C)

Counter/Timer

Feature	Value
Peripheral Interface Timer	Type 82C54
Clock Frequency Output	1 MHz
Native Modes	Pulse on terminal count, retriggerable one-shot, rate generator, square wave generator, software triggered strobe, hardware triggered strobe
Software support	Event counter, frequency output, frequency and pulse measurement

Feature	Value
Counters	3 x 16-Bit down counters
Inputs/Outputs	Fully Buffered

General

Feature	Value
Power Required:	+5V @ 40mA, +12V @ 30mA, -12V @ 30mA +5V @ 240mA w/optional ±12V DC/DC conv.
Interrupt Requests:	Eleven channels, IRQ 3-7, 9-12, 14, 15

Feature	Value
Environmental Operating Temperature	0 to +70°C standard, -40 to +85°C optional
Interrupt Status Register Interrupt Enable/Disable	Indicates source(s) of interrupt Software Controlled

Appendix B: 82C54 Counter Timer Operation

The board contains one type 8254 programmable counter/timer. The 8254 consists of three independent, 16-bit, presettable down-counters. Each counter can be programmed to any count between 2 and 65,535 in binary format, depending on the mode chosen. The programmed value is a divisor, the output frequency equals the input frequency divided by the programmed value.

In this manual these three counter/timers are designated Counter/Timer 0, Counter/Timer 1, and Counter/Timer 2.

OPERATIONAL MODES

The 8254 modes of operation are described in the following paragraphs to familiarize you with the versatility and power of this device. For those interested in more detailed information, a full description of the 8254 programmable interval timer can be found in the Intel (or equivalent manufacturers) data sheets. The following conventions apply for use in describing operation of the 8254 :

Clock:	A positive pulse into the counter's clock input.
Trigger:	A rising edge input to the counter's gate input.
Counter Loading:	Programming of a binary count into the counter.

Mode 0: Pulse on Terminal Count

After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing.

Mode 1: Retriggerable One-Shot

The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. Thus, this forms a re-triggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator

This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low.

Mode 3: Square Wave Generator

This mode operates periodically like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency syntheses are two possible applications for this mode. Note that in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the wave form.

Mode 4: Software Triggered Strobe

This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter. This mode can be used to provide a delayed software trigger for initiating A/D conversions.

Mode 5: Hardware Triggered Strobe

In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

PROGRAMMING

On this card the 8254 counters occupy the following addresses (hex):

Base Address + C: Read/Write Counter 0
Base Address + D: Read/Write Counter 1
Base Address + E: Read/Write Counter 2
Base Address + F: Write to Counter Control register

The counters are programmed by writing a control byte into a counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0-SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter 0
0	1	Program Counter 1
1	0	Program Counter 2
1	1	Read/Write Cmd.*

* See Chapter on READING AND LOADING THE COUNTERS.

RW0-RW1: These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0-M2: These bits set the operational mode of the selected counter.

MODE	M2	M1	M0
0	0	0	0
1	0	0	1
2	X	1	0
3	X	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (BCD = 0) or BCD (BCD = 1).

READING AND LOADING THE COUNTERS

If you attempt to read the counters on the fly when there is a high input frequency, you will most likely get erroneous data. This is partly caused by carries rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it is possible that carries will be propagated from the low to the high byte during the read cycle.

To circumvent these problems, you can perform a counter-latch operation in advance of the read cycle. To do this, load the RW1 and RW2 bits with zeroes. This instantly latches the count of the selected counter (selected via the SC1 and SC0 bits) in a 16-bit hold register. (An alternative method of latching counter(s) which has an additional advantage of operating simultaneously on several counters is by use of a readback command to be discussed later.) A subsequent read operation on the selected counter returns the held value. Latching is the best way to read a counter on the fly without disturbing the counting process. You can only rely on directly read counter data if the counting process is suspended while reading, by bringing the gate low, or by halting the input pulses.

For each counter you must specify in advance the type of read or write operation that you intend to perform. You have a choice of loading/reading (a) the high byte of the count, or (b) the low byte of the count, or (c) the low byte followed by the high byte. This last is of the most general use and is selected for each counter by setting the RW1 and RW0 bits to ones. Of course, subsequent read/load operations must be performed in pairs in this sequence or the sequencing flip-flop in the 8254 chip will get out of step.

The readback command byte format is:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	CNT	STA	C2	C1	C0	0

CNT: When is 0, latches the counters selected by bits C0-C2.
STA: When is 0, returns the status byte of counters selected by C0-C2.
C0, C1, C2: When high, select a particular counter for readback. C0 selects Counter 0, C1 selects Counter 1, and C2 selects Counter 2.

You can perform two types of operations with the readback command. When CNT=0, the counters selected by C0 through C2 are latched simultaneously. When STA=0, the counter status byte is read when the counter I/O location is accessed. The counter status byte provides information about the current output state of the selected counter and its configuration. The status byte returned if STA=0 is:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OUT	NC	RW1	RW2	M2	M1	M0	BCD

OUT: Current state of counter output pin.
NC: Null count. This indicates when the last count loaded into the counter register has actually been loaded into the counter itself. The exact time of load depends on the configuration selected. Until the count is loaded into the counter itself, it cannot be read.
RW1, RW0: Read/Write command.
M2, M1, M0: Counter mode.
BCD: BCD = 0 is binary mode, otherwise counter is in BCD mode.

If both STA and CNT bits in the readback command byte are set low and the RW1 and RW0 bits have both been previously set high in the counter control register (thus selecting two-byte reads), then reading a selected counter address location will yield:

1st Read:	Status byte
2nd Read:	Low byte of latched data
3rd Read:	High byte of latched data

After any latching operation of a counter, the contents of its hold register must be read before any subsequent latches of that counter will have any effect. If a status latch command is issued before the hold register is read, then the first read will read the status, not the latched value.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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