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MODEL 104-DA12-8

Analog Output Board

USER MANUAL

FILE: M104-DA12-8.A1e

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Chapter 1: Overview

Features

- Eight 12-Bit 10uS Digital to Analog Converters
- Counter/Timer with a 32-bit Divisor for Conversion Triggers
- Counter/Timer with a 16-bit Divisor for Interrupts
- 4-20mA Current Sink

Circuit Description

The board has eight 12-bit digital to analog converters. The circuit uses an Analog Devices AD5348 which has a single 12-bit input port, a 3-bit address port, and a shared 'start conversion' signal. The outputs are buffered by eight op-amps.

Two countdown timers (based on an i8254) are provided. The output of Counter/Timer 0 (16 bit, see appendix B) is available at connector P2 pin 4. The output of chained timers 1 & 2 (32 bit) provide the conversion trigger. The 16-bit timer has a 10MHz clock input while the 32-bit trigger timer has a 2MHz clock input, either may generate an interrupt.

The board has a 4-20mA current sink outputs. Each DAC may drive a 4-20mA sink with digital values from 0 (4mA) to 4095 (20mA). This is in addition to and in parallel with the op-amp driven outputs. The current is regulated with FETs, each source lead connects to the card's ground plane through a small resistance and each drain lead connects to the user's circuit.

A 4.096 volt reference is available at a connector pin (J1 Pin 35). Fused (resettable) +5 volts from the PC/104 bus and fused (resettable) +12 volts are also available. The +12 volts may come from the user's power supply if the PC/104 bus doesn't have it (some don't).

Note that on power-up the 4.096V reference is in standby mode. This ensures that all D/AC outputs are at zero volts. The user must set bit 6 at the card’s base address +10h. Clearing this bit at any time will cause all outputs to go to zero.

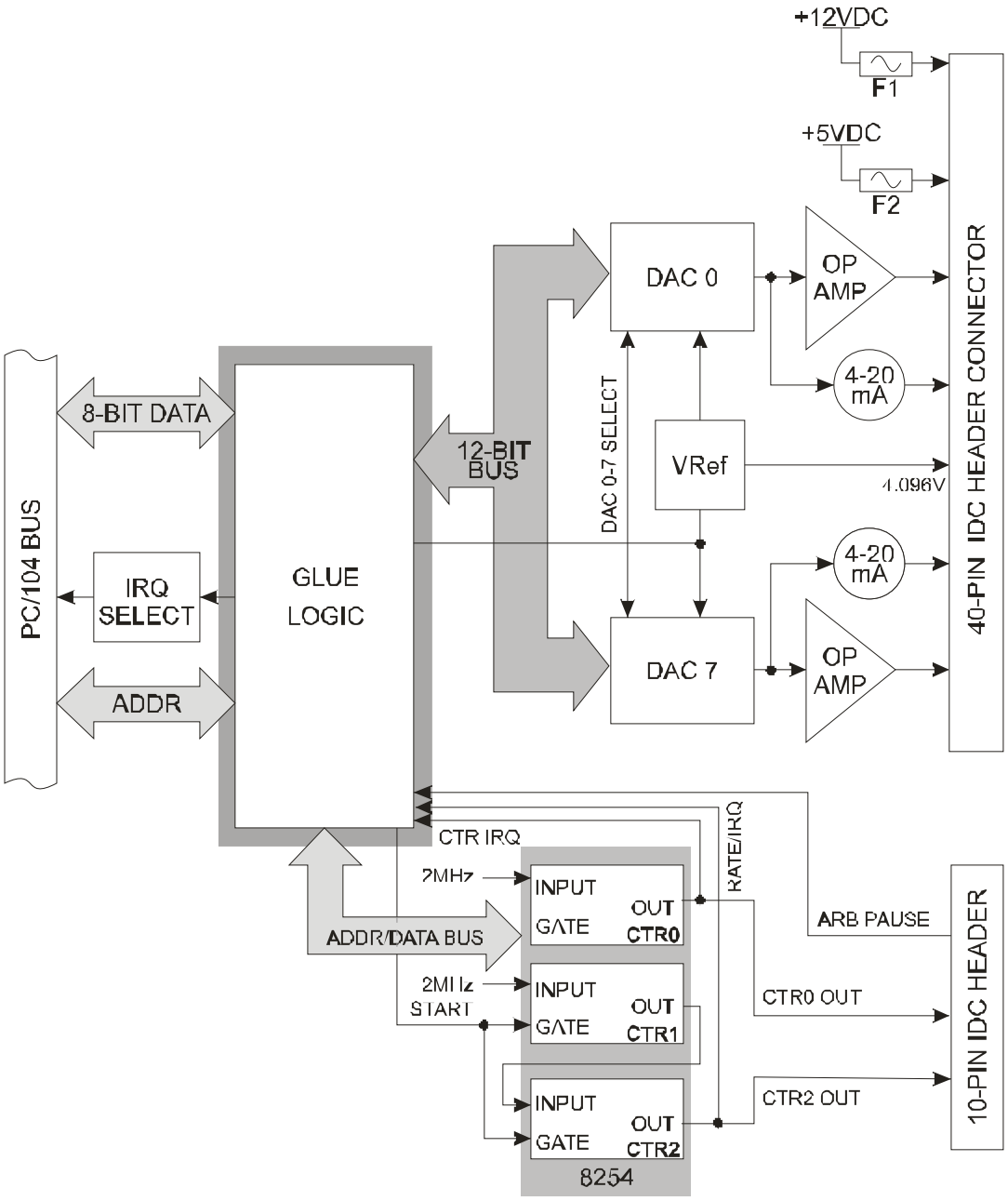


Figure 1-1: Block Diagram

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104 Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing serial ports under linux.

Installing the Hardware

Before installing the board, carefully read Chapter 3 and Chapter 4 of this manual and configure the board according to your requirements. The SETUP Program can be used to assist in configuring jumpers on the board. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. To help avoid this problem, refer to the FINDBASE.EXE program installed from the CD. The setup program does not set the options on the board, these must be set by jumpers.

To Install the Board

1. Install jumpers for selected options and base address according to your application requirements, as mentioned above.
2. Remove power from the PC/104 stack.
3. Assemble standoff hardware for stacking and securing the boards.
4. Carefully plug the board onto the PC/104 connector on the CPU or onto the stack, ensuring proper alignment of the pins before completely seating the connectors together.
5. Install I/O cables onto the board's I/O connectors and proceed to secure the stack together or repeat steps 3-5 until all boards are installed using the selected mounting hardware.
6. Check that all connections in your PC/104 stack are correct and secure then power up the system.
7. Run one of the provided sample programs appropriate for your operating system that was installed from the CD to test and validate your installation.

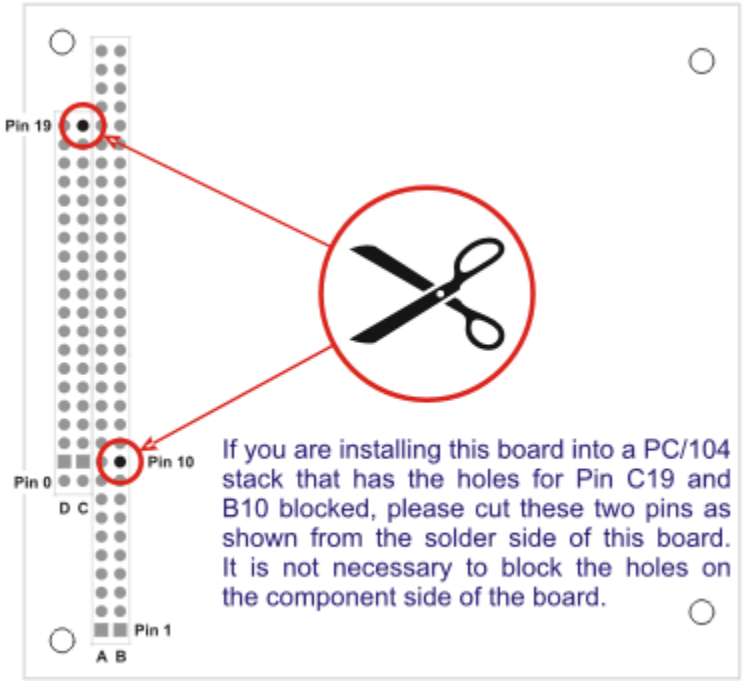


Figure 2-1: PC/104 Key Information

Chapter 3: Option Selection

Jumpers are available on the card to setup the following:

Base address
IRQ level
DAC output voltage ranges

Address Selection

The Card's Base Address is set by jumpers marked /A5 through /A9, and /A5 is the least significant bit of the address. The base addresses can be selected anywhere within the I/O address range 000-3E0 provided that they do not overlap with other functions. The FINDBASE software utility provided on the CD with your card will help you select a base address that does not conflict with other assignments.

This card requires a block of 32 addresses (20 hex). In order to configure the desired address, the hexadecimal address must be converted to a binary representation which is then selected by installing jumpers on the card.

For example, as illustrated below, switch selection corresponds to hex **2C0 (or binary 10 110x xxxx).** The "xxxxx" represents address lines A4 through A0 used on the card to select individual registers.

Hex Representation	2		C		
Conversion Factors	2	1	8	4	2
Binary Representation	1	0	1	1	0
Jumper Installed	NO	YES	NO	NO	YES
Jumper Label	A9	A8	A7	A6	A5

Table 3-1: Base Address Jumpers

Please note that "1" means that no jumper is installed and that "0" means that a jumper must be installed.

Consult the documentation for your system before selecting a card address.

The board occupies 32 bytes of I/O space. The board base address can be selected anywhere within the I/O address range 0-3E0 hex. If in doubt of where to assign the base address, refer to the following tables and the FINDBASE program to find an available address for your system.

HEX RANGE	USAGE
000-00F	8237 DMA Controller 1
020-021	8259 Interrupt
040-043	8253 Timer
060-06F	8042 Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Register
0A0-0BF	8259 Slave Interrupt Controller
0C0-0DF	8237 DMA Controller 2
0F0-0F1	Math Coprocessor
0F8-0FF	Math Coprocessor
170-177	Fixed Disk Controller 2
1F0-1F8	Fixed Disk Controller 1
200-207	Game Port
238-23B	Bus Mouse
23C-23F	Alt. Bus Mouse
278-27F	Parallel Printer
2B0-2BF	EGA
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	Serial Port
2F8-2FF	Serial Port
300-30F	reserved
310-31F	reserved
320-32F	Hard Disk (XT)
370-377	Floppy Controller 2
378-37F	Parallel Printer
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	Parallel Printer
3C0-3CF	VGA EGA
3D0-3DF	CGA
3E8-3EF	Serial Port
3F0-3F7	Floppy Controller 1
3F8-3FF	Serial Port

Table 3-2: Standard Address Assignments

IRQ Selection

The board can generate an interrupt on the DAC conversion or on the falling edge of Counter/Timer 0. The IRQ # is selected by a jumper placed on one pair of pins from the group labeled 'IRQ3' through 'IRQ15'. If you do not intend to use the IRQ, do not install a jumper on any IRQ pins. The locations of these jumpers is shown in the Option Selection map, as well as in the Setup Program provided with the card.

This interrupt can not be shared.

DAC Option Selections

Each DAC's op-amp circuit has two jumpers which configure it's voltage range. The user may select unipolar or bipolar outputs and 5 or 10 max voltage. In other words, the user may select four output ranges: 0 to 5V, 0 to 10V, -5V to +5V, -10V to +10V.

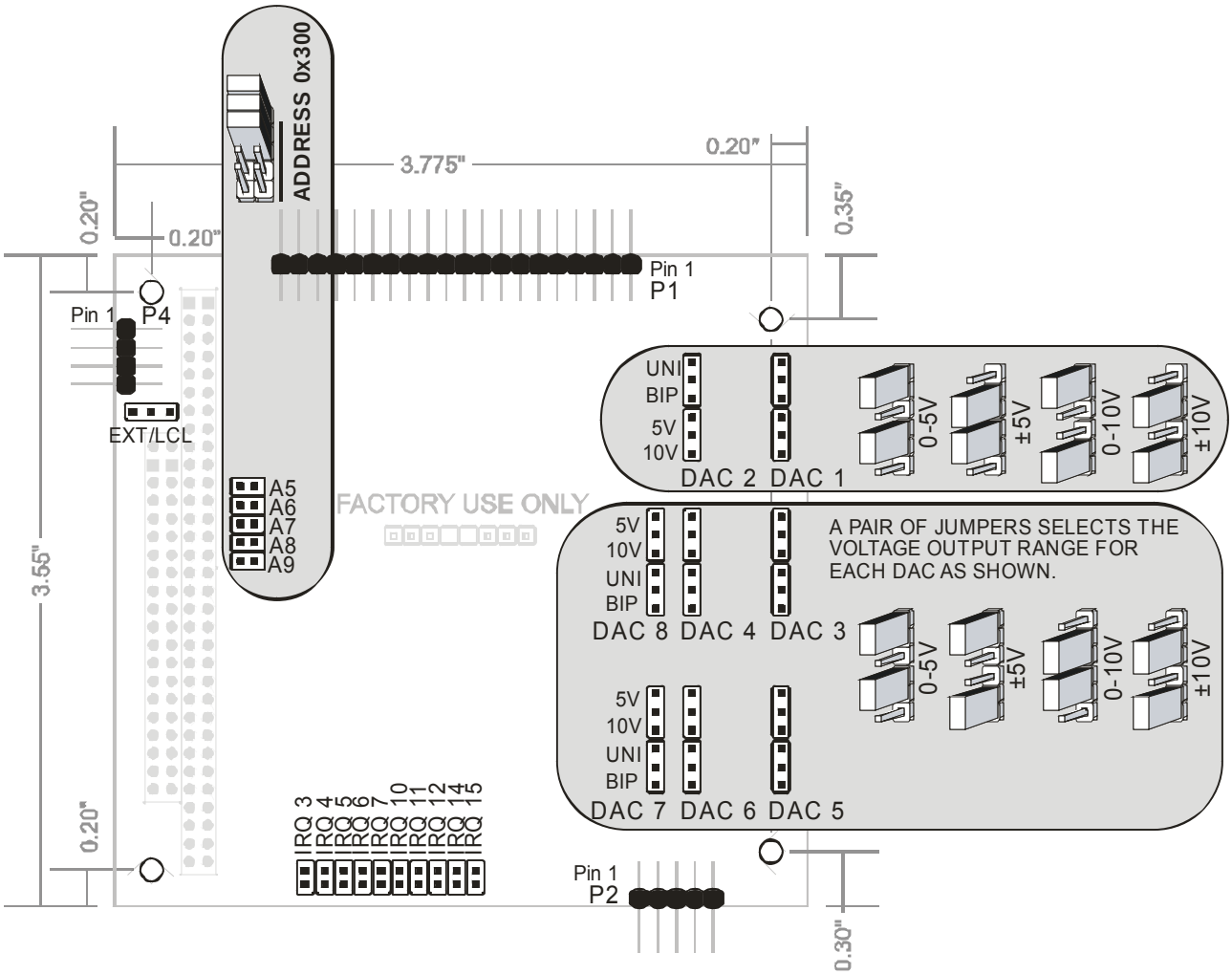


Figure 3-1: Option Selection

Chapter 4: Programming

Offset	Write Function	Read Function
0	DAC 0 LSB	
1	DAC 0 MSB	
2	DAC 1 LSB	
3	DAC 1 MSB	
4	DAC 2 LSB	
5	DAC 2 MSB	
6	DAC 3 LSB	
7	DAC 3 MSB	
8	DAC 4 LSB	
9	DAC 4 MSB	
A	DAC 5 LSB	
B	DAC 5 MSB	
C	DAC 6 LSB	
D	DAC 6 MSB	
E	DAC 7 LSB	
F	DAC 7 MSB	
10	Voltage REFerence Control	
11	IRQ Enable Register	IRQ Enable Readback
12		
13	DAC RESET	
14	Program Counter 0	Read Counter 0
15	Program Counter 1	Read Counter 1
16	Program Counter 2	Read Counter 2
17	Counter Control Register	
18		
19		
1A		
1B		
1C		
1D		
1E	IRQ Clear	
1F	Not used	

Table 4-1: Register Map
All offsets are in hexadecimal.

Register Descriptions

The card is controlled by reading and writing 8- or 16-bit registers in I/O Memory. The registers are described below. Please note, all offsets are hexadecimal.

Base+ 0 through Base + E, DACs 0-7 Direct Control Registers

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

These 8 word-sized registers allow you to update the DACs from software. If you're interested in simple DC voltage or current outputs you can ignore all the rest of the registers and just use these to control the outputs of the DACs.

Write a word to an even address in the range of (base +) 0 through 0xE to update the DAC with a new count value. Data is offset Binary: 0x0000 is the minimum value (in unipolar modes, 0Volts, in bipolar modes, the most-negative value possible). 0x0800 is the "middle" of the range (0V when in Bipolar modes), and 0x0FFF is the maximum positive voltage.

Bits D15 through D12 are unused and should be set to zero for future compatibility.

To calculate the counts for any given Desired Output Voltage use the following equation:

Given: SpanVolts is equal to the highest positive voltage minus the most negative voltage the range supports (ex: +5V is "5" - "-5" which is "5+5" or "10")
Unipolar: Counts = (DesiredVolts / SpanVolts) * 4096
Bipolar: Counts = (DesiredVolts / SpanVolts) * 2048 + 2048

Base + 10 Write, Reference Control

D7	D6	D5	D4	D3	D2	D1	D0
	REF						

Bit D6 REF: Set/clear to enable/disable the 4.096 DAC **REF**erence. While this bit is set DACs can generate signals, and P1 Pin 35 will have 4.096 volts output. At power-up this bit is cleared and all outputs are 0V.

Bits D0 through D5 and D7 are unused.

Reading this register will return the current state of the Reference Control bit.

All bits in this register power-on or reset to "zero"

Base + 11 Write, Interrupt Enable Register

D7	D6	D5	D4	D3	D2	D1	D0
						EICTR0	

Set/clear bits D0 through D7 to enable/disable an irq from each bit's IRQ source.

> **Bit D1 EICTR0: E**nables **I**RQs from the output of **C**oun**T**e**R 0**. Each time the output of Counter 0 goes low and this bit is set an IRQ will be generated. This counter, and its IRQ and output on the P2 connector (pin 4), are solely for use by the customer.

Reading this register will return the current state of these bits.

All bits in this register power-on or reset to "zero."

Base + 13, DAC Reset
Write any value to this register to clear the DACs and set all outputs to their most negative value. For example, if the range is -10V to +10V on DAC 1 it will go to -10V. If the range on channel 2 is 0V to 5V it will go to zero volts.

Base + 14, Program Counter/Timer 0 - (see Appendix B)
This is a 16-bit timer used as a timer-tick for external hardware. Its 10MHz input clock is divided by a load 16-bit value and output on P2 pin 4. This counter output can also generate an IRQ, if enabled (see base + 10.)

Base + 17, Counter/Timer Control Register - (see Appendix B)
Use this register to configure the 8254.

Base + 1E, IRQ Clear
Write any value to this address to clear a pending interrupt. Once the card generates an IRQ, no further IRQs will be requested until the pending IRQ has been cleared by writing to this address.

Chapter 5: Software

Software Driven DC DAC Mode:

There are two broad categories of software driven DAC usage: synchronous, or simultaneous, and asynchronous, or "automatic." Simultaneous mode is so named because all DACs will switch from their old voltage (or current) output levels to their newly programmed levels simultaneously, and synchronously with an event.

Asynchronous:

To use the DACs simply write desired count values to the DACs themselves, via Base + 0 through Base + E. The card powers up in this mode, so no other registers need to be manipulated.

Chapter 6: Connector Pinouts

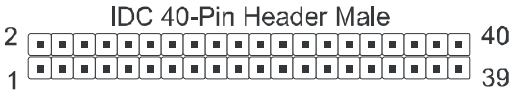


Table 6-1: Connector P1, 40-pin Male IDC Header

Pin	Function	Pin	Function
1	Ground	2	DAC 0 Voltage Output
3		4	DAC 0 4-20mA Output
5		6	DAC 1 Voltage Output
7		8	DAC 1 4-20mA Output
9		10	DAC 2 Voltage Output
11		12	DAC 2 4-20mA Output
13		14	DAC 3 Voltage Output
15		16	DAC 3 4-20mA Output
17		18	DAC 4 Voltage Output
19		20	DAC 4 4-20mA Output
21		22	DAC 5 Voltage Output
23		24	DAC 5 4-20mA Output
25		26	DAC 6 Voltage Output
27		28	DAC 6 4-20mA Output
29		30	DAC 7 Voltage Output
31		32	DAC 7 4-20mA Output
33		34	+12 Volts Fused
35	4.096V	36	+5 Volts Fused
37	Ground	38	n.c.
39	n.c.	40	n.c.

Note that pin 35 will be 0V if bit 6 of Control Register 2 is LOW.
Note also that pins 38, 39, and 40 are unused, such that connection via a standard 37-Pin DSub connector is simplified.

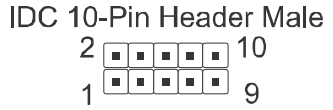


Table 6-2: Connector P2, 10-pin Male IDC Header

Pin	Function
1	Load DAC (output)
3	N/C
5	Ground
7	N/C
9	N/C

Pin	Function
2	N/C
4	Counter 0 Output
6	Ground
8	N/C
10	N/C

Pin 1, Conversion Trigger, output
Every time the DACs are updated a very short low-going pulse will be generated here. (<100nS).

Pin 4, Clock Tick, output
This is the output of counter/timer 0. The user may program this 16-bit count-down timer to generate a tick or a square wave etc. (see appendix B).

Pins 5 and 6 are connected to the ground.

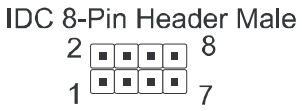


Table 6-3: Connector P4, 8-pin Male IDC Header

Pin	Signal
1	Ground
3	
5	
7	

Pin	Signal
2	n.c.
4	+12V
6	n.c.
8	n.c.

The board does not require +12V but the user's 4-20mA circuit might. +12V is brought to pin 34 of connector P1 through a resettable fuse. This +12V may come from the PC/104 bus or from an external source. If the voltage comes from the PC/104 bus then a jumper should be placed on the pins of JP32 (next to P4) labeled LCL (local). If the voltage comes from a source connected to P4 then a jumper should be placed on the pins of JP32 labeled EXT. Note that if the voltage for the user's 4-20mA circuit comes from an external source that it isn't limited to 12V.

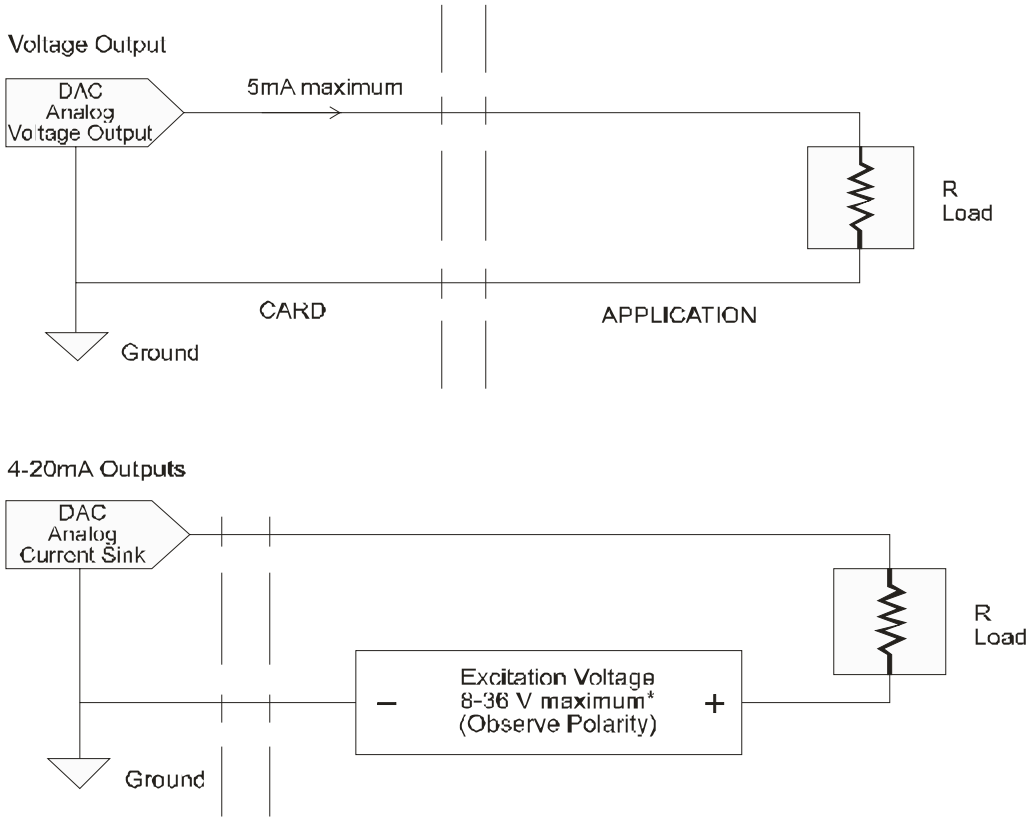


Figure 6-1: Signal Connection

Appendix A: Technical Specifications

ANALOG OUTPUTS

- 8 Channels
- 10µS per conversion, all channels simultaneously
- 12 Bit Resolution
- Output Ranges, 0-5V 0-10V +5V +10V
- Eight 4-20mA current sink outputs (external 8 to 36VDC excitation required)
- +2 counts D/AC Relative Accuracy (typical)
- 8uS D/AC Settling Time (typical, to 3/4 scale)
- +0.4 % of Full Scale D/AC Offset Error (typical)
- +0.1 % of Full Scale D/AC Gain Error (typical)
- Drive Capability of 5mA per channel, Outputs are Short-Circuit Protected
- 30mA cumulative total drive from all D/ACs
- 4.096V Voltage Reference

Counter/Timer

- Type 82C54
- 3 x 16-Bit Down-Counters
- Counter 0 is an IRQ source (clock-tick interrupt) and frequency source (counter 0 output is available at P2 connector pin 4)
- 10MHz Input Clock Frequency

General

- +5V @ 210mA Power Consumption (typical, no load on the outputs)
- On-board DC/DC Converter allows operation on +5V Power
- Interrupt requests may be generated on channels 3-7, 10-12 and 14-15
- Environment Tolerance: 0-70C, 5% to 95% Humidity (non-condensing)
  (-40 to +85C available with special order)

Appendix B: 82C54 Counter Timer Operation

The board contains one type 8254 programmable counter/timer. The 8254 consists of three independent, 16-bit, presettable down-counters. Each counter can be programmed to any count between 2 and 65,535 in binary format, depending on the mode chosen. The programmed value is a divisor, the output frequency equals the input frequency divided by the programmed value.

In this manual these three counter/timers are designated Counter/Timer 0, Counter/Timer 1, and Counter/Timer 2.

Counter/Timer 0 is a 16-bit counter with a 10MHz input clock. The output of Counter/Timer 0 is available at connector P2 pin 4. The gate signal for counters 1 & 2 is controlled via software at bit 1 (HIGH = off, LOW = count enabled = power-on default) of the register at Base + 10h. Counter/Timers 1 and 2 are concatenated by the card to form a single 32-bit counter. The input of the counter is fixed at 2MHz. The output of is available at connector P2 pin 1.

OPERATIONAL MODES

The 8254 modes of operation are described in the following paragraphs to familiarize you with the versatility and power of this device. For those interested in more detailed information, a full description of the 8254 programmable interval timer can be found in the Intel (or equivalent manufacturers) data sheets. The following conventions apply for use in describing operation of the 8254 :

Clock:	A positive pulse into the counter's clock input.
Trigger:	A rising edge input to the counter's gate input.
Counter Loading:	Programming of a binary count into the counter.

Mode 0: Pulse on Terminal Count

After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing.

Mode 1: Retriggerable One-Shot

The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. Thus, this forms a re-triggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator

This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low.

Mode 3: Square Wave Generator

This mode operates periodically like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency synthesis are two possible applications for this mode. Note that in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the wave form.

Mode 4: Software Triggered Strobe

This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter. This mode can be used to provide a delayed software trigger for initiating A/D conversions.

Mode 5: Hardware Triggered Strobe

In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

PROGRAMMING

On this card the 8254 counters occupy the following addresses (hex):

Base Address + 14: Read/Write Counter 0
Base Address + 15: Read/Write Counter 1
Base Address + 16: Read/Write Counter 2
Base Address + 17: Write to Counter Control register

The counters are programmed by writing a control byte into a counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows:

B7	B6	B5	B4	B3	B2	B1	B0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0-SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter 0
0	1	Program Counter 1
1	0	Program Counter 2
1	1	Read/Write Cmd.*

* See Chapter on READING AND LOADING THE COUNTERS.

RW0-RW1:These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0-M2: These bits set the operational mode of the selected counter.

MODE	M2	M1	M0
0	0	0	0
1	0	0	1
2	X	1	0
3	X	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (BCD = 0) or BCD (BCD = 1).

READING AND LOADING THE COUNTERS

If you attempt to read the counters on the fly when there is a high input frequency, you will most likely get erroneous data. This is partly caused by carries rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it is possible that carries will be propagated from the low to the high byte during the read cycle.

To circumvent these problems, you can perform a counter-latch operation in advance of the read cycle. To do this, load the RW1 and RW2 bits with zeroes. This instantly latches the count of the selected counter (selected via the SC1 and SC0 bits) in a 16-bit hold register. (An alternative method of latching counter(s) which has an additional advantage of operating simultaneously on several counters is by use of a readback command to be discussed later.) A subsequent read operation on the selected counter returns the held value. Latching is the best way to read a counter on the fly without disturbing the counting process. You can only rely on directly read counter data if the counting process is suspended while reading, by bringing the gate low, or by halting the input pulses.

For each counter you must specify in advance the type of read or write operation that you intend to perform. You have a choice of loading/reading (a) the high byte of the count, or (b) the low byte of the count, or (c) the low byte followed by the high byte. This last is of the most general use and is selected for each counter by setting the RW1 and RW0 bits to ones. Of course, subsequent read/load operations must be performed in pairs in this sequence or the sequencing flip-flop in the 8254 chip will get out of step.

The readback command byte format is:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	CNT	STA	C2	C1	C0	0

CNT: When is 0, latches the counters selected by bits C0-C2.
STA: When is 0, returns the status byte of counters selected by C0-C2.
C0, C1, C2: When high, select a particular counter for readback. C0 selects Counter 0, C1 selects Counter 1, and C2 selects Counter 2.

You can perform two types of operations with the readback command. When CNT=0, the counters selected by C0 through C2 are latched simultaneously. When STA=0, the counter status byte is read when the counter I/O location is accessed. The counter status byte provides information about the current output state of the selected counter and its configuration. The status byte returned if STA=0 is:

B7	B6	B5	B4	B3	B2	B1	B0
OUT	NC	RW1	RW2	M2	M1	M0	BCD

OUT: Current state of counter output pin.
NC: Null count. This indicates when the last count loaded into the counter register has actually been loaded into the counter itself. The exact time of load depends on the configuration selected. Until the count is loaded into the counter itself, it cannot be read.
RW1, RW0: Read/Write command.
M2, M1, M0: Counter mode.
BCD: BCD = 0 is binary mode, otherwise counter is in BCD mode.

If both STA and CNT bits in the readback command byte are set low and the RW1 and RW0 bits have both been previously set high in the counter control register (thus selecting two-byte reads), then reading a selected counter address location will yield:

1st Read:	Status byte
2nd Read:	Low byte of latched data
3rd Read:	High byte of latched data

After any latching operation of a counter, the contents of its hold register must be read before any subsequent latches of that counter will have any effect. If a status latch command is issued before the hold register is read, then the first read will read the status, not the latched value.

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com***. Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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