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10623 Roselle Street, San Diego, CA 92121 • (858) 550-9559 • Fax (858) 550-7322
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MODEL 104-DIO-48S
104-DIO-24S

USER MANUAL

FILE: m104-DIO-48S.B7i

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Chapter 1: INTRODUCTION

Features

- 48 or 24 Bits of Digital Input/Output.
- Interrupt Generation on Input Change of State.
- Change-of-state Interrupt Software Enabled in Six 8-Input Ports.
- All 48 or 24 I/O Lines Buffered on the Board.
- I/O Buffers Can Be Enabled/Disabled under Program Control.
- Four and Eight Bit Ports Independently Selectable for I/O.
- Pull-Ups on I/O Lines.
- +5V Supply Available to the User. Onboard resettable 0.5A fuse.
- Compatible with Industry Standard I/O Racks like Gordos, Opto-22, Potter & Brumfield, etc.
- Counter/Timer 82C54 chip, 3x16 bit.

Applications

- Automatic Test Systems.
- Laboratory Automation.
- Robotics.
- Machine Control.
- Security Systems, Energy Management.
- Relay Monitoring and Control.
- Parallel Data Transfer to PC.
- Sensing Switch Closures or TTL, DTL, CMOS Logic.
- Driving Indicator Lights or Recorders.

Description

The 48S or 24S board is a general purpose Digital Input/Output board with buffers on all I/O lines and with a very useful feature called Change of State Detection. The state of all inputs can be monitored by the board's hardware and, if any one or more bits change state, a latched interrupt request can be generated. Thus, it is not necessary to use software to continuously poll the inputs to detect a change of state. The change-of-state interrupt is enabled by a software WRITE to an interrupt-enable register. Six bits in that register each control an eight-bit port at one of two type 82C55-5 Programmable Peripheral Interface chips. The change-of-state interrupt latch can be cleared by a software WRITE.

Interrupts are directed to levels #3 through #7, #9 through #12, #14 and #15 by jumper installation.

The board was designed for industrial applications and can be installed in 16-or 8-bit PC/104 bus socket. Each I/O line is buffered and capable of sourcing 32mA or sinking 64mA (depending on the drivers chosen). The board contains two Programmable Peripheral Interface (PPI) chips of type 8255-5 to provide a computer interface to 48 I/O lines. There are three 8-bit ports A, B, and C per PPI. Each 8-bit port can be software configured to function as either inputs or latched outputs. Port C can also be configured as four inputs and four outputs. Pull-ups on the board assure that there are no erroneous outputs at power up.

Tristate I/O line buffers (HCT or LS or F) are configured automatically by hardware logic for input or output according to the direction assignment from a control register in the PPI. Further, if a software flag is set the tristate buffers are enabled/disabled under program control. (See the Option Selection section to follow.)

I/O wiring connections are via 50-pin headers on the board. Two flat I/O cables connect the board to termination. Also, this provides compatibility with OPTO-22, Gordos, Potter & Brumfield, and all module mounting racks. Every second conductor of the flat cables are grounded to minimize the effect of crosstalk between signals. If needed for external circuits, fused +5 VDC power (resettable) is available on each I/O connector pin 49.

The board occupies 32 bytes of I/O address space. The base address is selectable via jumpers anywhere within the range of 100-3E0 hex. An illustrated setup program is provided with the board. Interactive displays show locations and proper settings of jumpers to set up board address and interrupt levels. Also, sample programs in a variety of languages are described in the Software section of this manual and on CD or 3 ½" diskette.

The board optionally has an 82C54 Counter/Timer chip. This can be used for frequency measurement, frequency output, pulse width modulation, etc. Most pins are available on a connector for flexibility, and the input to Counter 1 has a dedicated 1MHz input.

SPECIAL NOTE FOR PROGRAMMERS:

> The one language **not** recommended for programming interrupt service routines is any version of Visual BASIC. The recommended programming languages for IRQ based applications are Delphi, C++ Builder or Visual C.

Specification

Digital Inputs (TTL Compatible)

- Logic High: 2.0 to 5.0 VDC.
- Logic Low: -0.5 to +0.8 VDC.
- Input Load (Hi): 20 uA.
- Input Load (Lo): -200 uA.

Digital Outputs

- Logic High: 2.5 VDC min., source 32 mA
- Logic Low: 0.5 VDC max., sink 64 mA

Optional Counter/Timers

- Type: 82C54 programmable interval counters.
- Output Drive: Sink 64mA, source 32mA.
- Input Gate: TTL/CMOS compatible.
- Clock Output: 1 MHz crystal-controlled oscillator.
- Active Count Edge: Negative edge.

General

- Power Output: +5 VDC from computer bus available on each 50 pin I/O connector (onboard resettable 0.5A fuse).
- Power Required: +5 VDC at 125 mA typical (depends on the driver type used).

Environmental

- Operating Temperature: 0 °C to +70 °C (optional -40 °C to +85 °C).
- Storage Temperature: -50 °C to +120 °C.
- Humidity: up to 95% RH, non-condensing.

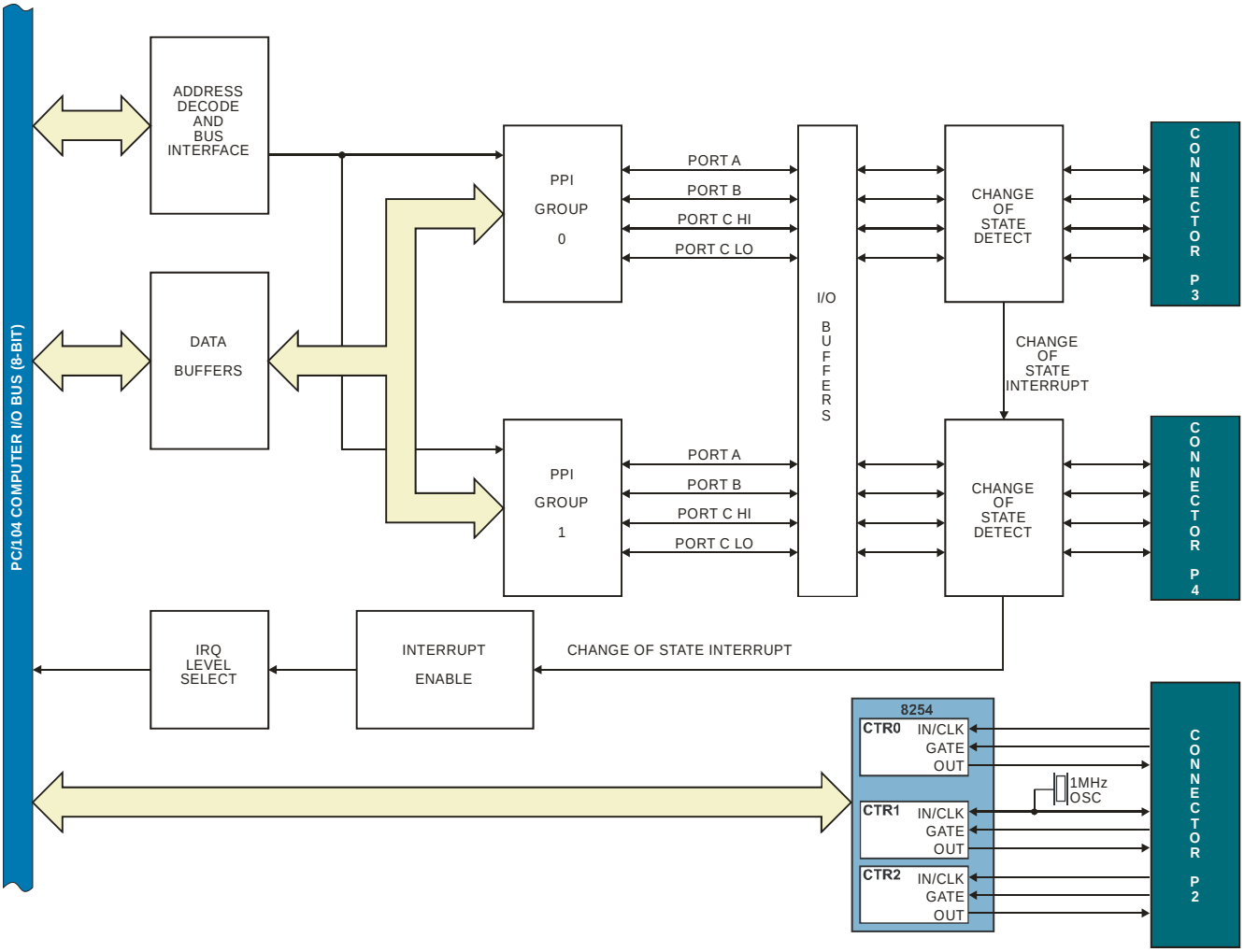


Figure 1-1: Block Diagram

Chapter 2: INSTALLATION

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104 Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Installing the Hardware

Before installing the board, carefully read Chapter 3 and Chapter 4 of this manual and configure the board according to your requirements. The SETUP Program can be used to assist in configuring jumpers on the board. Be especially careful with Address Selection. If the addresses of two installed functions overlap, you will experience unpredictable computer behavior. To help avoid this problem, refer to the FINDBASE.EXE program installed from the CD. The setup program does not set the options on the board, these must be set by jumpers.

To Install the Board

1. Install jumpers for selected options and base address according to your application requirements, as mentioned above.
2. Remove power from the PC/104 stack.
3. Assemble standoff hardware for stacking and securing the boards.
4. Carefully plug the board onto the PC/104 connector on the CPU or onto the stack, ensuring proper alignment of the pins before completely seating the connectors together.
5. Install I/O cables onto the board's I/O connectors and proceed to secure the stack together or repeat steps 3-5 until all boards are installed using the selected mounting hardware.
6. Check that all connections in your PC/104 stack are correct and secure then power up the system.
7. Run one of the provided sample programs appropriate for your operating system that was installed from the CD to test and validate your installation.

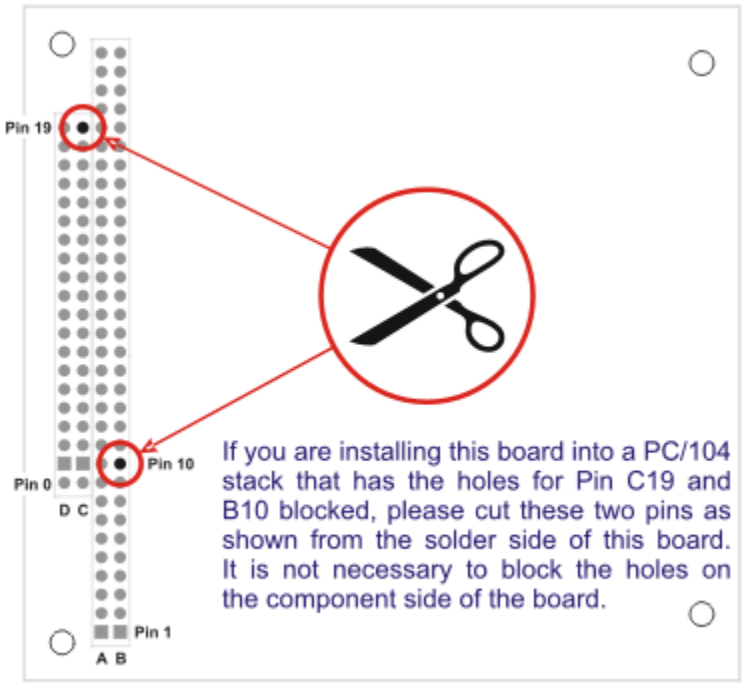


Figure 2-1: PC/104 Key Information

Chapter 3: OPTION SELECTION

The only options to select on the board are the IRQ level and the board's base address. All other options are selected via software.

Interrupts are directed to levels #3 through #7, #9 through #12, #14 and #15 by jumpers installed at locations labeled IRQ3 through IRQ7, IRQ10 through IRQ12, IRQ14 and IRQ15.

The 74xx245 (LS, F, HC, HCT type drivers are available as factory options for different power consumption requirements) input/output buffers are enabled or disabled under program control. (See the programming section of this manual for a description.) The buffers' directions are automatically configured.

The change-of-state Interrupt is enabled by writing to the board's register. (See the Programming section of this manual for details) The ports are individually enabled (Port C, Port B, Port A).

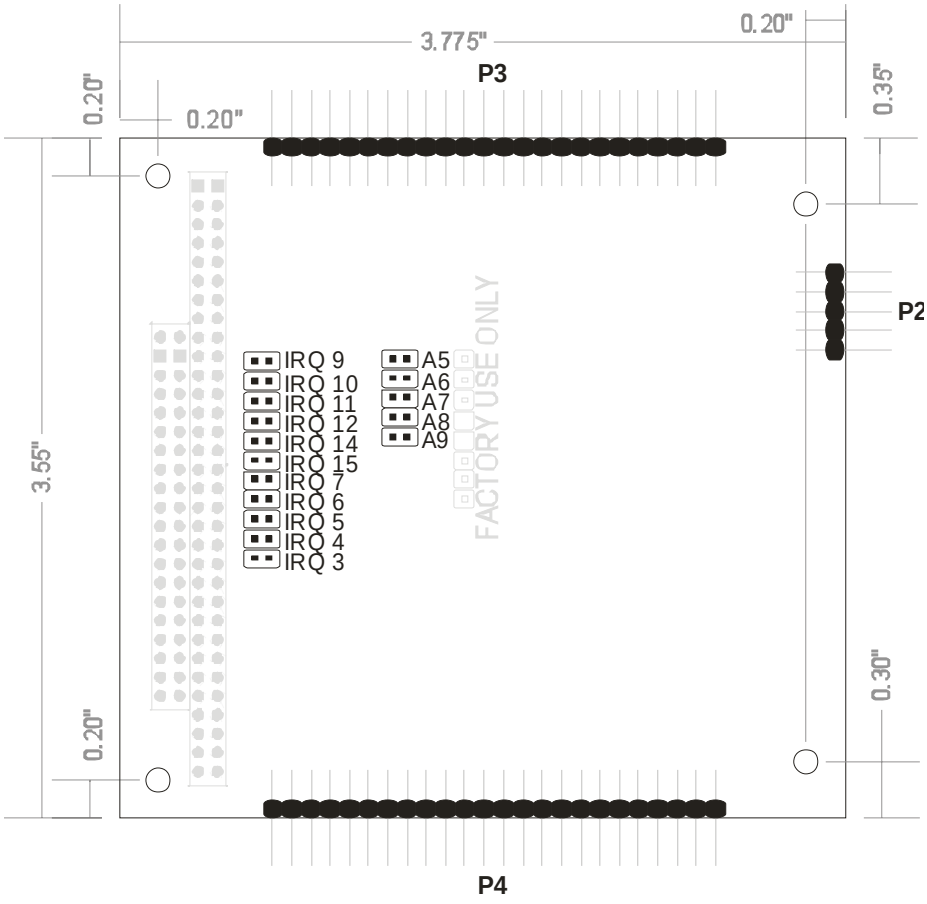


Figure 3-1: Option Selection Map

Chapter 4: ADDRESS SELECTION

The board occupies 32 bytes of I/O space. The board base address can be selected anywhere within the I/O address range 100-3E0 hex. If in doubt of where to assign the base address, refer to the following tables and the FINDBASE program to find an available address for your system.

HEX RANGE	USAGE
000-00F	8237 DMA Controller 1
020-021	8259 Interrupt
040-043	8253 Timer
060-06F	8042 Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Register
0A0-0BF	8259 Slave Interrupt Controller
0C0-0DF	8237 DMA Controller 2
0F0-0F1	Math Coprocessor
0F8-0FF	Math Coprocessor
170-177	Fixed Disk Controller 2
1F0-1F8	Fixed Disk Controller 1
200-207	Game Port
238-23B	Bus Mouse
23C-23F	Alt. Bus Mouse
278-27F	Parallel Printer
2B0-2BF	EGA
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	Serial Port
2F8-2FF	Serial Port
300-30F	reserved
310-31F	reserved
320-32F	Hard Disk (XT)
370-377	Floppy Controller 2
378-37F	Parallel Printer
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	Parallel Printer
3C0-3CF	VGA EGA
3D0-3DF	CGA
3E8-3EF	Serial Port
3F0-3F7	Floppy Controller 1
3F8-3FF	Serial Port

Table 4-1: Address Assignments for Standard Computers

To set desired board address, jumpers must be installed on the board. These jumpers are marked A5-A9 and form a binary representation of the address in negative-true logic. (assign '0' to all Address Setup jumpers installed, and assign '1' to all Address Setup jumpers left off.)

Base Address Table

To set the base address of the board, install the jumpers “ON” the posts for that address according to the table.

A9	A8	A7	A6	A5	Address Range
					3E0h - 3FFh
				On	3C0h - 3DFh
			On		3A0h - 3BFh
			On	On	380h - 39Fh
		On			360h - 37Fh
		On		On	340h - 35Fh
		On	On		320h - 33Fh
		On	On	On	300h - 31Fh
	On				2E0h - 2FFh
	On			On	2C0h - 2DFh
	On		On		2A0h - 2BFh
	On		On	On	280h - 29Fh
	On	On			260h - 27Fh
	On	On		On	240h - 25Fh
	On	On	On		220h - 23Fh
	On	On	On	On	200h - 21Fh
On					1E0h - 1FFh
On				On	1C0h - 1DFh
On			On		1A0h - 1BFh
On			On	On	180h - 19Fh
On		On			160h - 17Fh
On		On		On	140h - 15Fh
On		On	On		120h - 13Fh
On		On	On	On	100h - 11Fh

Caution

Carefully review the address selection reference table on the previous page before selecting the board address. If the addresses of two circuits overlap you will experience unpredictable computer behavior.

Chapter 5: PROGRAMMING

The board is an I/O-mapped device that is easily configured from any language and any language can easily perform digital I/O through the board's ports. This is especially true if the form of the data is byte or word wide. All references to the I/O ports would be in absolute port addressing. However, a table could be used to convert the byte or word data ports to a logical reference.

The recommended languages to program in to take advantage of the invaluable feature of Change-of-State detection are Delphi and C++ Builder. Visual C is more difficult to accomplish this in and Visual BASIC is *NOT* recommended for interrupt type programming.

Address	Port Assignment	Operation
Base Address	PA Group 0	Read/Write
Base Address +1	PB Group 0	Read/Write
Base Address +2	PC Group 0	Read Write
Base Address +3	Control Group 0	Write Only
Base Address +4	PA Group 1	Read/Write
Base Address +5	PB Group 1	Read/Write
Base Address +6	PC Group 1	Read/Write
Base Address +7	Control Group 1	Write Only
Base Address +8	Enable/Disable Buffer, Grp 0	Write Only
Base Address +9	Enable/Disable Buffer, Grp 1	Write Only
Base Address +A	Buffer Tristate Enable/Disable	Read/Write
Base Address +B	Enable Chg-of-St. Interrupt	Read/Write
Base Address +C	Selective Port Enable, Grp 0	Read/Write
Base Address +D	Selective Port Enable, Grp 1	Read/Write
Base Address +F	Clear Chg-of-St. Interrupt	Read/Write
Base Address + 10	Counter/Timer 0	Read/Write
Base Address + 11	Counter/Timer 1	Read/Write
Base Address + 12	Counter/Timer 2	Read/Write
Base Address + 13	Counter/Timer Mode Select	Write Only
Base Address + 14	Counter/Timer Interrupt	Read/Write
Base Address + 15	Counter/Timer IRQ Status	Read Only
Base Address + 16	Counter/Timer Interrupt Clear	Read/Write
Base Address + 17	not used	
Base Address + 18	Clear Chg-of-St. Interrupt	Read Only

Table 5-1: Address Selection Table

If you wish to gain a better understanding of the programs, then the information in the following paragraphs will be of interest to you. Refer to the data sheets and 82C55-5 specification provided in the “Chip Docs” directory of the CD.

The board uses two 82C55-5 PPIs to provide a total of 48 bits input/output. The board is designed to use each of these PPIs in Mode 0 wherein for each group:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

Each PPI contains a Control Register. This write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each PPI should be configured during initialization by writing to the Control Registers even if the ports are only going to be used as inputs. Output buffers are automatically set by hardware according to the Control Register states. Note that Control Registers are located at base address +3 and base address +7. Bit assignments in each of these Control Registers are as follows:

Bit	Assignment	Code
D0 Bit	Port C Lo (C0-C3)	1=Input, 0=Output
D1	Port B	1=Input, 0=Output
D2	Mode Select	1=Mode 1, 0=Mode 0
D3	Port C Hi (C4-C7)	1=Input, 0=Output
D4	Port A	1=Input, 0=Output
D5, D6	Mode Select	00=Mode 0, 01=Mode 1, 1X=Mode 2
D7	Mode Set Flag	1=Active

Table 5-2: 82C55 Control Register Bit Assignment

Note

Mode 1 and Mode 2 cannot be used by the board without modification (Consult the factory). Thus, bits D2, D5, and D6 should always be set to "0" and Bit D7 to "1".

Note

In Mode 0, do not use the control register byte for the individual bit control feature. The hardware uses the I/O bits to control buffer direction on this board. The control register should only be used for setting up input and output of the ports and enabling the buffer.

The board is initialized in the receive mode and buffer tristating is disabled by the computer reset command.

The 82C55 PPI chip doesn't have enough sink or source current for some applications and is intolerant of static and shorts. The board has a tri-state buffer for each port: A, B, C high, and C low. When a command changes the direction of one of the 82C55s, the buffers change direction to match. Thus the board behaves like two 82C55s with very strong drive.

When an 82C55 port is configured to be an output the port bits are set to zero. This may be inconvenient if the equipment controlled by the port has active-low signals. The Buffer Tristate Enable provide a work-around for this quirk of the chip. Enable either or both of them (base address +Ah bit 0 for Group 0, bit 1 for Group 1) and the board's port buffers will behave as follows:

a. When bit D7 of the Control Register is HIGH, direction of the three ports of the associated PPI chip as well as the mode can be set. For example, a write to Base Address +3 with data bit D7 HIGH programs port direction at Group 0 ports A, B, and C. If, for example, hex 80 is sent to Base Address +3, the Group 0 PPI will be configured in mode 0 with Ports A, B, and C as outputs.

b. At the same time, data bit D7 is also latched in a buffer controller for the associated PPI chip. A HIGH state disables the buffers and, thus, all four buffers will be put in the tristate mode; i.e. disabled. Pull-ups on the board will provide a HIGH at each bit of each port. Note that even ports configured as inputs will be tri-stated.

c. Now, if any of the ports are to be set as outputs, you may set the values with the outputs still in the tristate condition. (If all ports are to be set as inputs, this step is not necessary.)

d. When the data to be output are correct and it is desired to open the ports, it is necessary to send a byte with bit D7 LOW to base address +8 to enable the Group 0 buffers.

Those buffers will now remain enabled until another control byte with data bit D7 HIGH is sent to base address +3. The buffers for all ports of the group can be tristated without changing the PPI mode by writing to base address +8 with D7 HIGH.

Similarly, the Group 1 ports can be enabled/disabled via the control register at base address +7 or 9. The following program fragment in C language illustrates the foregoing:

```
const BASE_ADDRESS 0x300;
outportb(BASE_ADDRESS +0xA, 0x03); /*This instruction enables buffer tristating for both
                                    groups.*/
outportb(BASE_ADDRESS +3, 0x89);   /*This instruction sets the mode to Mode 0, ports A
                                    and B as output, and port C as input. Since bit D7 is
                                    high and buffer tristating is enabled for the group, the
                                    output buffers are set to tristate condition. See item b.
                                    above.*/

outportb(BASE_ADDRESS,0);
outportb(BASE_ADDRESS+1,0);        /*These instructions set the initial state of ports A and
                                    B to all zeroes. Port C is not set because it is
                                    configured as an input. See item c. above.*/
outportb(BASE_ADDRESS +8, 0x09);   /*Enable the buffers by writing a byte with bit D7 low.
                                    See item d. above.*/
```

A third method of buffer control, Selective Port Enable, is provided. When using the 'selective' mode the user would set the Buffer Tristate Enable bit for one or both groups, write a control word to the Control Register at Base Address +3 or +7, set the values of the output ports, and then enable selected ports with a WRITE of a bit mapped value to Base Address +C or +D. A HIGH bit will enable a port's buffer, A LOW bit will tristate it (pull-ups will hold lines HIGH, pull-downs are a factory installable option).

	D7	D6	D5	D4	D3	D2	D1	D0
Base + 0Ch	X	X	X	Port A Group 0	Port C High Group 0	X	Port B Group 0	Port C Low Group 0
Base + 0Dh	X	X	X	Port A Group 1	Port C High Group 1	X	Port B Group 1	Port C Low Group 1

Note that sending a command to the 82C55 will cause all port buffers in the group to be tri-stated, but a bit pattern written to a Selective Port Enable register can control the buffers individually.

Programming Example (Basic)

The following example in BASIC is provided as a guide to assist you in developing your working software. In this example, the board base address is 2D0 hex and the I/O lines of group 0 are to be setup as follows:

Port A = Input Port C Hi = Input
Port B = Output Port C Lo = Output

The first step is to configure the control register. Configure bits of the control register as:

D7	1	Active Mode Set
D6	0	Mode 0
D5	0	Mode 0
D4	1	Port A = Input
D3	1	Port C Hi = Input
D2	0	Mode 0
D1	0	Port B = Output
D0	0	Port C Lo = Output

This corresponds to 98 hex. If the board address is 2D0 hex, use the BASIC OUT command to write to the control register as follows:

```
10      BASEADDR=&H2D0
20      OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C:

```
30      X=INP(BASEADDR)          'Read Port A
40      Y=INP(BASEADDR+2)/16     'Read Port C Hi
```

To set outputs high (1) at Port B and the lower nybble of Port C:

```
50      OUT BASEADDR+1,&HFF     'Turn on all Port B bits
60      OUT BASEADDR+2,&HF      'Turn on all bits of Port C lower nybble
```

Change-of-state Interrupts

At power-up or Reset, a register that enables change-of-state interrupts is reset. This disables all 24 or 48 inputs from generating change-of-state interrupts. During software initialization this register should be programmed to enable interrupt generation by ports that you want to cause change-of-state interrupts. To program this Change-of-State Interrupt Enable Register, write to it at Base Address +B. Writing a "one" disables the port; writing a "zero" enables it. This register is latched and can be read back. Data bits D0 through D5 control ports A, B, and C of the 82C55 PPIs as shown in Table 6-3.

Bit	Port Controlled
D0	Group 0, Port A
D1	Group 0, Port B
D2	Group 0, Port C
D3	Group 1, Port A
D4	Group 1, Port B
D5	Group 1, Port C

Table 5-3: Change-of-state Interrupt Enable Register

To clear the IRQ status register at Base +F once it's been serviced by an ISR (Interrupt Service Routine, generic version provided on the CD), write any value to Base +F. You may first read from Base +F to determine *which* port had the change of state occurrence. Bit=0: No Change of State occurred, Bit=1: Change of State occurred. To read the IRQ status register and clear the interrupt at the same time, read Base +18.

Bit	Port Status
D0	Group 0, Port A
D1	Group 0, Port B
D2	Group 0, Port C lo
D3	Group 0, Port C hi
D4	Group 1, Port A
D5	Group 1, Port B
D6	Group 1, Port C lo
D7	Group 1, Port C hi

Table 5-4: Change-of-state interrupt status Register

Sharing Interrupts on the PC/104 (ISA) Bus

On occasion, a system application will require more interrupt levels than are available on the PC/104 (ISA) bus. While this is not recommended, IRQ sharing is possible. Each board that is going to share an IRQ must strictly adhere to a special standard for accessing the IRQ lines as follows:

1. The interrupt must be held in a high impedance state until asserting an interrupt.
2. The interrupt must be asserted in the form of a low signal lasting at least 500 nanoseconds followed by a rising edge and then immediately returning to a high impedance condition.
3. The board must contain a status register or flag of some kind to indicate that it generated the interrupt. There is an exception to this rule. This is the case where only one board (of those sharing the interrupt level) does not provide a status bit to indicate that it asserted the interrupt but is otherwise capable of sharing the IRQ. In this case, it may share the interrupt level with other boards if (a) it is the only board on that IRQ level that does not have a status bit and (b) it is installed onto the IRQ vector first. (This makes it the last board to be called in the vector chain.) This scheme will work because it can be assumed that if every other board in the vector chain did not cause the interrupt, then the last board must be the one that did.

Note

Note that if two boards assert the IRQ line within 500 nanoseconds of each other, the second board in the ISR chain will not be serviced. It is possible to alleviate this problem by writing a single ISR that can detect the bit flag on every board and therefore detect the fact that two boards (or more) report generating an interrupt even though only one interrupt was processed by the CPU.

Chapter 6: 8254 COUNTER/TIMER

These boards optionally contain one type 82C54 programmable counter/timer. This may be wired externally at connector P2 to allow the user to implement a 32-bit Event Counter or 48-bit Rate Generator (Frequency Output) functions. To do this connect the OUT1signal to the GATE0 input and to the CLK2 input. Connect the signal or event to be counted to the CLK0 input (P2 pin 1), connect the time period (pulse) to be measured to GATE1 (P2 pin 5). The frequency or rate generator output is at P2 pin 9. The rate generator is based on the 1MHz output (P2 pin 4) which is hard-wired internally to CLK1 input.

The 82C54 is a flexible but powerful device that consists of three independent 16-bit down counters. Each counter can be programmed to any count as low as 1 or 2 (depending on the mode chosen) and up to 65,535. For those interested in more detailed information, a full description can be found in the Intel (or equivalent manufacturer's) data sheet.

Operational Modes

The 8254 modes of operation are described in the following paragraphs to familiarize you with the versatility and power of this device. For those interested in more detailed information, a full description of the 8254 programmable interval timer can be found in the Intel (or equivalent manufacturers') data sheets. The following conventions apply for use in describing operation of the 8254 :

Clock:	A positive pulse into the counter's clock input
Trigger:	A rising edge input to the counter's gate input
Counter Loading:	Programming a binary count into the counter

Mode 0: Pulse on Terminal Count

After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing.

Mode 1: Retriggerable One-Shot

The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. This forms a retriggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator

This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low. This mode also works well as an alternative to mode 0 for event counting.

Mode 3: Square Wave Generator

This mode operates like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency synthesis are two possible applications for this mode. Note that in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the wave form.

Mode 4: Software Triggered Strobe

This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter.

Mode 5: Hardware Triggered Strobe

In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

Programming the 8254

The counters are programmed by writing a control byte into the counter control register. Refer to the previous register map for the base addresses of the counters and the counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows:

B7	B6	B5	B4	B3	B2	B1	B0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0-SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter #0
0	1	Program Counter #1
1	0	Program Counter #2
1	1	Read/Write Cmd.*

* See section on Reading and Loading the Counters.

RW0-RW1: These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0-M2: These bits set the operational mode of the selected counter.

Mode	M2	M1	M0
0	0	0	0
1	0	0	1
2	X	1	0
3	X	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (BCD = 0) or BCD (BCD = 1).

Reading and Loading the Counters

If you attempt to read the counters on the fly when there is a high input frequency, you will most likely get erroneous data. This is partly caused by carries rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it is possible that carries will be propagated from the low to the high byte during the read cycle.
To circumvent these problems, you can perform a counter-latch operation in advance of the read cycle. To do this, load the RW1 and RW2 bits with zeroes. This instantly latches the count of the selected counter (selected via the SC1 and SC0 bits) in a 16-bit hold register. (An alternative method of latching counter(s) that has an additional advantage of operating simultaneously on several counters is through a readback command to be discussed later.) A subsequent read operation on the selected counter returns the held value. Latching is the best way to read a counter on the fly without disturbing the counting process. You can only rely on directly read counter data if the counting process is suspended while reading by bringing the gate low.

For each counter you must specify in advance the type of read or write operation that you intend to perform. You have a choice of loading/reading (a) the high byte of the count, or (b) the low byte of the count, or (c) the low byte followed by the high byte. This last is most generally used and is selected for each counter by setting the RW1 and RW0 bits to ones. Subsequent read/load operations must be performed in pairs in this sequence or the sequencing flip-flop in the 8254 chip will get out of step. The readback command byte format is:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	CNT	STA	C2	C1	C0	0

CNT: When 0, latches the counters selected by bits C0-C2.
STA: When 0, returns the status byte of counters selected by C0-C2.
C0, C1, C2: When high, select a particular counter for readback. C0 selects Counter 0, C1 selects Counter 1, and C2 selects Counter 2.

You can perform two types of operations with the readback command. When CNT=0, the counters selected by C2 through C0 are latched simultaneously. When STA=0, the counter status byte is read when the counter I/O location is accessed. The counter status byte provides information about the current output state of the selected counter and its configuration. The status byte returned if STA=0 is:

B7	B6	B5	B4	B3	B2	B1	B0
OUT	NC	RW1	RW2	M2	M1	M0	BCD

OUT: Current state of counter output pin.
NC: Null count. This indicates when the last count loaded into the counter register has been loaded into the actual counter. The exact time of load depends on the configuration selected. Until the count is loaded into the counter, it cannot be read.
RW1, RW0: Read/Write command.
M2, M1, M0: Counter mode.
BCD: BCD = 0 is binary mode, otherwise counter is in BCD mode.

If both STA and CNT bits in the readback command byte are set low and the RW1 and RW0 bits have both been previously set high in the counter control register (thus selecting two-byte reads), then reading a selected counter address location will yield:

1st Read: Status byte
2nd Read: Low byte of latched data
3rd Read: High byte of latched data

After any latching operation on a counter, the contents of its hold register must be read before any subsequent latches of that counter will have any effect. If a status latch command is issued before the hold register is read, then the first read will read the status, not the latched value.

8254 Driver

A simple driver is provided to perform basic counter/timer operations on this board. Source code for the driver and a sample program showing how to use the functions are located in the DOS\CSAMPLES directory.

Note: In order to use the driver, you must connect the pins Output 1 (pin 6), Gate 0 (pin 2), and Clock 2 (pin 7). In this configuration, the output of counter 1 can enable/disable counter 0 and can be the timebase for counter 2, allowing the driver to use precise timing methods.

The following functions are provided:

Frequency Measure

The Frequency Measure function of the 8254 Counter Driver has the ability to measure an unknown frequency from 1KHz to 0.5MHz. This function requires as input the Base Address of the board. The unknown frequency is applied to the CLOCK IN pin of the board (P2 pin 1). The function will return the frequency as a long integer in Hz.

```
long frequency_measure(unsigned BaseAddress);
```

Event Counter

The Event Counter function has the ability to trace the number of events that have occurred. This function requires the Base Address and an additional parameter that identifies which features should be implemented on this call to the function. Each feature can be identified by its unique integer value. Multiple features can be run in a single call to the function by ORing the respective integer values together. Features will be executed in increasing integer order. The CLOCK IN pin of the board (P2 pin 1) is the point of application for the incoming events. (Note: This function is limited by the input speed of

the 8254 counter, and slow signals are preferred. Further only 65,535 events are possible without a RESET.) The function returns the number of events (based on priority) or 0 for those features that do not specify a return value.

Features:

INITIALIZE	= 1;	initialize the counter
START	= 2;	begin counting
SINCESTART	= 4;	return the number of events since the start
SINCELAST	= 8;	return the number of events since last check
STOP	= 16;	stop counting events
RESET	= 32;	reset number of events to 0

```
unsigned event_counter(unsigned BaseAddress, int feature);
```

Generate Frequency

The Generate Frequency function will generate a square wave (0 to +5V) with the desired frequency. The Base Address of the board as well as the frequency are required as input to the function. The counter can generate a frequency with a range of 1Hz to 250KHz. The square wave can be read on the CLOCK OUT pin (pin 9) of the board.

```
void generatefrequency(unsigned BaseAddress, unsigned long frequency);
```

Pulse Width

The Pulse Width function will measure the width of an applied event from its rise to its fall (effectively one half the period). The Base Address of the board is required as input to the function. The signal should be applied to the GATE IN pin of the board (P2 pin 5). Software latency will be affected by the operating system and will set a limit on the precision of the measurement.

```
unsigned pulse_width(unsigned BaseAddress);
```

Chapter 7: Connector Pin Assignments

Two 50-pin headers are provided on the board; one for each 24 I/O group. PPI Group 0 is on connector P3, and PPI Group 1 is on connector P4. The mating connector is an AMP type 1-746285-0 or equivalent. Connector pin assignments are listed below. Notice that every second line is grounded to minimize crosstalk between signals. One 10-pin header (P2) is provided for the Counter/Timer connections (see Table 7-2).



Assignment		Pin	Assignment	Pin
Port C Hi	PC7	1	All Even-Numbered Pins are Ground	2
	PC6	3		4
	PC5	5		6
	PC4	7		8
Port C Lo	PC3	9		10
	PC2	11		12
	PC1	13		14
	PC0	15		16
Port B	PB7	17		18
	PB6	19		20
	PB5	21		22
	PB4	23		24
	PB3	25		26
	PB2	27		28
	PB1	29		30
	PB0	31		32
Port A	PA7	33		34
	PA6	35		36
	PA5	37		38
	PA4	39		40
	PA3	41		42
	PA2	43		44
	PA1	45		46
	PA0	47		48
+5 VDC		49		50

Table 7-1: Digital I/O (P3 and P4) Connector Pin Assignments



Assignment	Pin
Clock 0 (in)	1
Gate 0 (in)	2
Output 0	3
1MHz Clock (out)*	4
Gate 1 (in)	5
Output 1	6
Clock 2 (in)	7
Gate 2 (in)	8
Output 2	9
Ground	10

* Internally hard-wired to Clock 1 (in)

Table 7-2: Counter/Timer (82C54) P2 Connector Pin Assignments

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

ACCES I/O PRODUCTS, INC.
10623 Roselle Street, San Diego CA 92121
Tel. (858)550-9559 FAX (858)550-7322
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