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10623 Roselle Street, San Diego, CA 92121 • (858) 550-9559 • (858) 550-7322
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MODELS P104-DIO-96, P104-DIO-48S, P104-DIO-48

PC/104 Plus High-Density Digital I/O with Change of State (COS) Detection

USER MANUAL

FILE: MP104-DIO-96.B2k

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Chapter 1: Introduction

Features

- PC/104 Plus or PCI-104 (no ISA connector)
- 96 or 48 Channel TTL-CMOS high speed digital I/O
- Software selectable port mode as Input or Output
- 8 bit and 4 bit wide ports
- Emulates up to 4 industry standard 8255 PPIs (mode 0)
- Full 32-bit PCI interface design
- Buffered circuits for higher current drive
- Change of State detection capability = Low CPU overhead
- Known power-up states
- Output port status read back
- Standard 50-pin male IDC connectors (x4)
- 0 to +70° C and -40 to +85° C versions available

Applications

- Kiosks and Robotics
- Machine control
- Embedded OEM
- Security systems and energy management
- Automatic test systems
- Rugged Military systems
- Driving indicator lights or recorders
- Contact monitoring and relay control
- Laboratory and industrial automation
- Parallel digital data communications via TTL, DTL, CMOS logic

Functional Description

Each I/O line of this board is buffered and capable of sourcing 32mA or sinking 64mA. The board emulates Programmable Peripheral Interface chips (Intel 8255 PPI) to provide a computer interface to digital I/O lines. Each PPI supports two 8-bit ports (A, B) and two 4-bit ports (C_{hi}, C_{low}). Each port can be configured to function as either inputs or output latches. The I/O line buffers (types 74ABT240 and 74ABT245) are configured automatically by hardware logic for input or output according to the PPI Control Register direction software assignment.

On power-up all I/O pins default as inputs. The I/O lines are pulled up through 10KΩ to +5VDC allowing inputs to easily monitor external dry contacts. With no cabling connected to the I/O headers the lines would read as logic HIGH.

These boards require both 5V and 3.3V power. The PCI to local bus controller uses 3.3V. The port I/O buffers use 5V, and the PCI bus signaling voltage may be either 5V or 3.3V depending on the host CPU. See chapter 7 for electrical specifications.

I/O wiring connections are via two right-angle 50-pin headers and two vertical 50-pin headers on the board to provide compatibility with solid-state module mounting racks. Every other conductor of the flat ribbon cables is grounded to minimize crosstalk. If needed for external circuits, +5VDC power is available on each I/O connector at pin 49. If you use this power, we recommend that you include a 1A fast blow fuse in your circuits in order to avoid possible damage to the host computer.

The C_{hi} port of each group on the “-96” version can provide 'Change of State' detection. If the voltage level at an enabled I/O pin changes for at least 1 microsecond then a bit in a status register flags the event and an interrupt is generated. There are 16 I/O pins/lines with this capability. All bits on the “-48S” version have this capability.

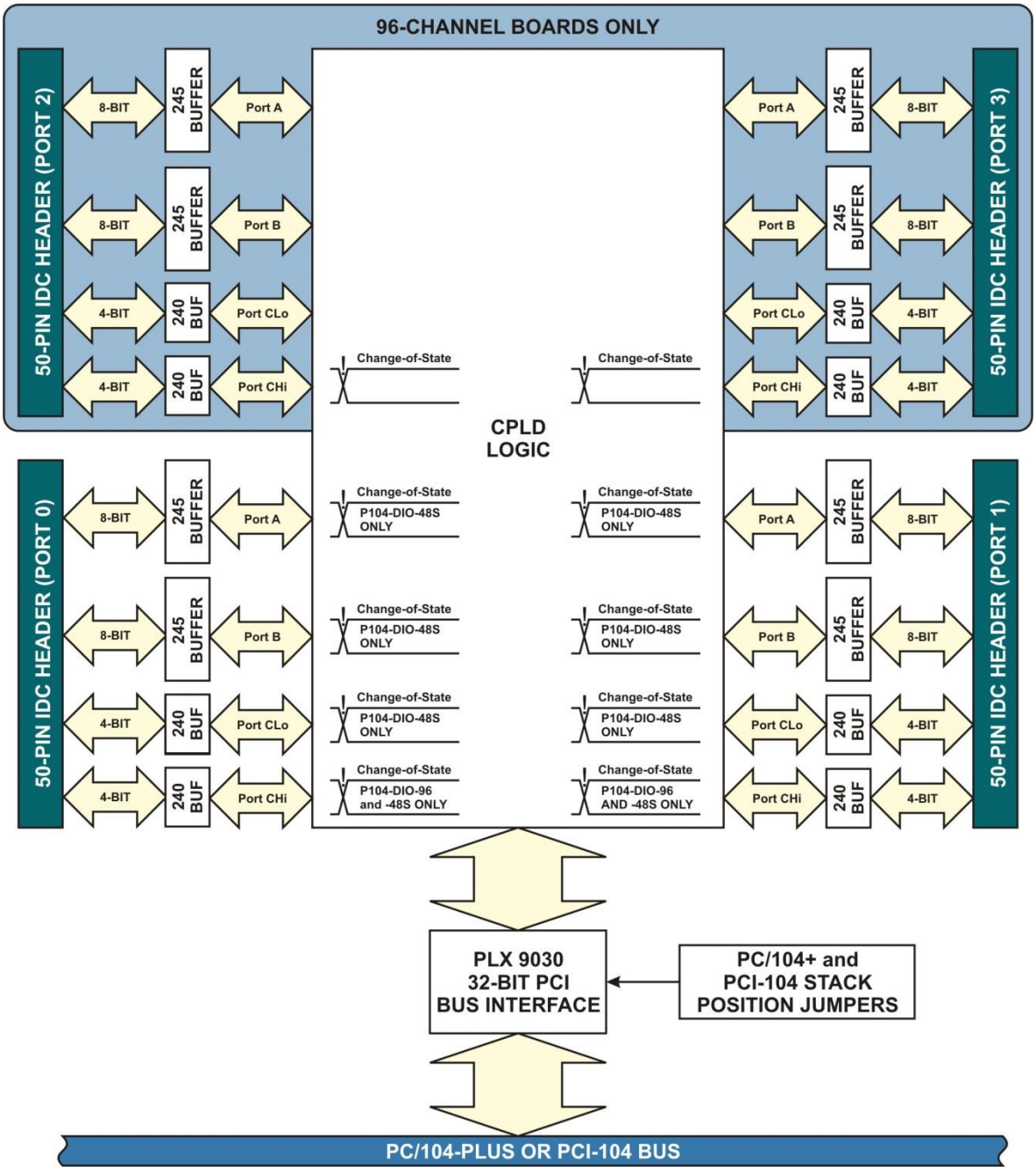


Figure 1-1: Block Diagram

Ordering Guide

- P104-DIO-96 PC/104 Plus 96-bit Digital I/O card with 16-lines of COS detection
- P104-DIO-48 PC/104 Plus 48-bit Digital I/O card
- P104-DIO-48S PC/104 Plus 48-bit Digital I/O card with COS detection on all lines

Model Options

- Extended Operating Temp (-40 to +85 degrees C)
- Pull up resistors removed
- PCI-104 Only

Special Order

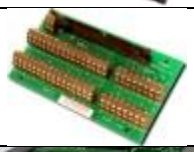
Please contact ACCES with your precise requirement such as conformal coating, latching connectors, custom software, etc., we'll work with you to provide it.

Included with your board

The following items are included with your shipment, depending on options ordered. Please take time now to ensure no items are damaged or missing.

- PC/104 Plus board
- Software Master CD
- I/O Quick-Start Guide

Optional Accessories

• PCI-P104-ADAP	Permits a PC/104-Plus board to be installed in a standard desktop PCI slot for development and software testing	
• UTBK-50	Screw terminal board plugs directly onto right-angle and vertical 50-pin male headers	
• CAB50F-6 or • CAB50-6	Six-foot ribbon cable assembly with 50-pin female connectors or with one 50-pin female header and one edge connector	
• STB-96CH	50-Pin Multi-Header Universal Screw Terminal Board for 96 Digital I/O Channels	
• STB-50	Screw terminal board, typically ships with standoffs but can also mount on SNAP-TRACK or DIN-SNAP	
• DIN-SNAP	One foot length of SNAP-TRACK with four clips, for mounting up to two STB-50 screw terminal boards on a DIN rail	

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the board for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this PC/104-Plus Board is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your CD-ROM where you see d: in the examples below.

CD Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Installing the Hardware

Before installing the board, please run Setup.exe. The Setup program can be used to assist in configuring the two switches on the board. Our setup program will lead the user through the process of setting the options on the board (the program does not set the options on the board).

The PCI bus clock trace length from the CPU to the cards in the stack is tuned so that the clock edge arrives at the interface when data is valid. Since boards in the PC/104 stack are at different distances from the CPU, provision is made on the CPU board to supply four clock signals with compensating trace lengths. Two signals from other groups must be likewise selected: IDSEL and INT. When the PCI bus is being initialized, the operating system will enable each card with a hard-wired select line and read it's configuration registers. An address is assigned, space in the memory map and I/O map is reserved, etc. Similarly, the CPU's interrupt controller resources (INTA, INTB, INTC, INTD) will be distributed among the cards in the stack. A set of four-to-one multiplexers and two slide switches are used to select which PCI clock, IDSEL and INT lines are routed to the board's PCI bus interface.

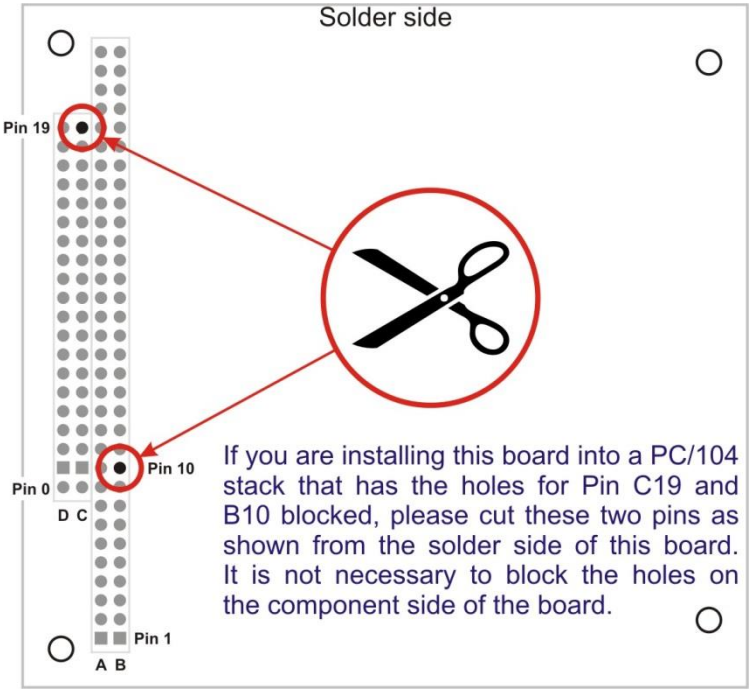


Figure 2-1: PC/104 Key Information

To install the board

1. Turn off the computer power.
2. Position the slide switches to select the clock, IDSEL, and interrupt signal group.
3. Install the card in a PC/104-Plus stack.
4. Install I/O cables or UTBK-50 screw terminal boards at P1, P2, P3 and P4 as appropriate.
5. Inspect for proper fit of the card and cable and then tighten the screws

Chapter 3: Option Selection

Most PCI bus signals are common to all four boards in the PCI stack. However, there are four unique signal groups, one for each board. The slide switches select which signal group goes to each card. The card in the stack closest to the CPU board must get signal group 0.

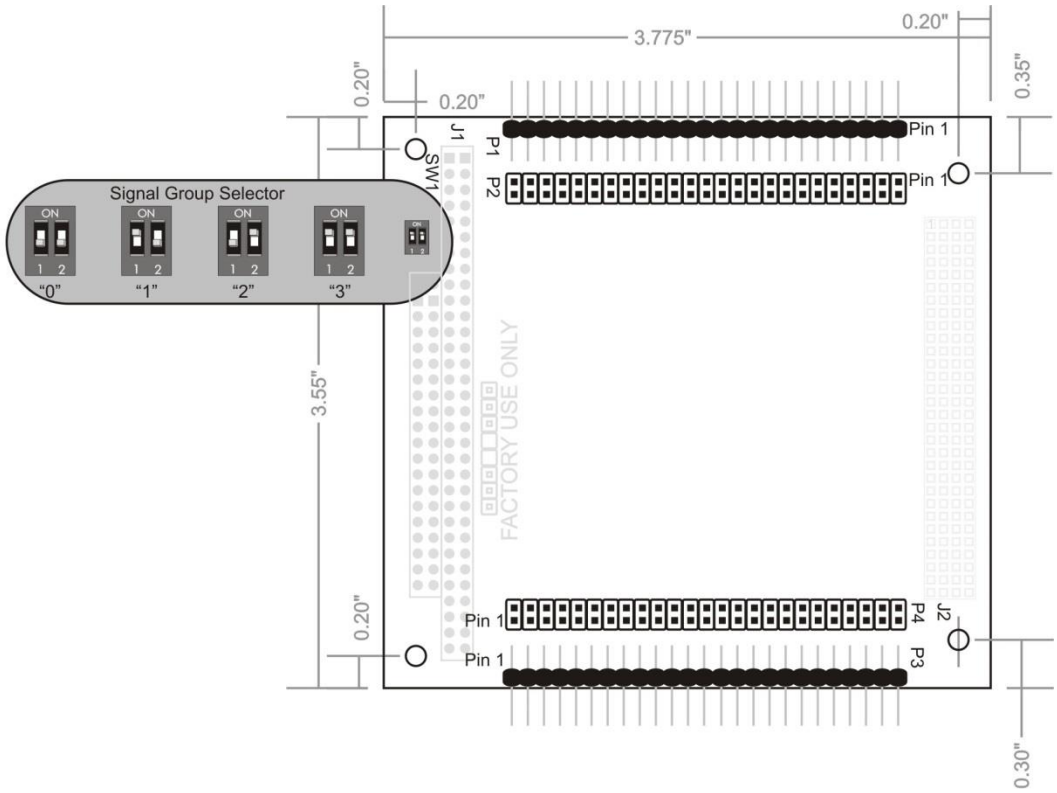


Figure 3-1: Option Selection Map

Only four boards are allowed in a PCI-Plus stack, each board must get a specific set of signals. These signals are selected with two slide switches, labeled SEL-1 and SEL-2, which form a binary value to control the mux (SEL-1 is the least significant bit and SEL-2 is the most significant bit). If the board is closest to the CPU, slide both switches to the right. This will select the signal with the longest trace on the CPU board (signal group 0). If this product is the farthest board from the CPU, slide both switches to the left. This will select the signal with the shortest trace on the CPU board (signal group 3). Place the SEL-1 switch to the left and SEL-2 to the right to select signal group 1, place the SEL-1 switch to the right and SEL-2 to the left to select signal group 2.

Chapter 4: Address Selection

The system BIOS or operating system will assign the address. This board occupies 32 bytes of I/O space.

PCI architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCI cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the PCIFind.EXE, or PCINT utility program provided. This utility will display a list of all of the cards detected on the PCI bus, the addresses assigned to each function on each of the boards, and the respective Interrupt Request (IRQ) (if any) allotted.

Alternatively, some operating systems (Windows 95/98/2000) can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind (DOS), PCINT (Windows95/98/NT), or the Device Manager utility from the System Applet of the control panel. The board is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

The PCI bus supports 64K of I/O space. Your board's addresses may be located anywhere in the 0400 to FFE0 hex range.

PCIFind uses the Vendor ID and Device ID to search for your board, then reads the base address and IRQ.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for the board is 494F. (ASCII for "IO")
The Device ID for the “-96” board is 0x0C69
The Device ID for the “-48” board is 0x0C62
The Device ID for the “-48S” board is 0x0E62

Chapter 5: Programming

Hex (h)	Standard 8255 Register Compatibility	
Offset	Write	Read
Base+0	Group 0 Port A	Group 0 Port A
Base+1	Group 0 Port B	Group 0 Port B
Base+2	Group 0 Port C	Group 0 Port C
Base+3	Group 0 Command	N/A
Base+4	Group 1 Port A	Group 1 Port A
Base+5	Group 1 Port B	Group 1 Port B
Base+6	Group 1 Port C	Group 1 Port C
Base+7	Group 1 Command	N/A
Base+8	Group 2 Port A	Group 2 Port A
Base+9	Group 2 Port B	Group 2 Port B
Base+A	Group 2 Port C	Group 2 Port C
Base+B	Group 2 Command	N/A
Base+C	Group 3 Port A	Group 3 Port A
Base+D	Group 3 Port B	Group 3 Port B
Base+E	Group 3 Port C	Group 3 Port C
Base+F	Group 3 Command	N/A
Model Specific Registers below this row		
Base+10	Group 0 & 1 memory update & IRQ clear	Group 0 & 1 COS status
Base+11	Group 2 & 3 memory update & IRQ clear	Group 2 & 3 COS status
Base+12	Group 0 & 1 COS enable / disable	Group 0 & 1 COS enable status
Base+13	Group 2 & 3 COS enable / disable	Group 2 & 3 COS enable status
Base+14 Through Base+1F	Reserved	Reserved

Table 5-1: -96 Card Base Address Registers

This page refers only to the "-96" card.

The Interrupt function uses a bit mask and Comparator to detect and generate an IRQ on selected I/O pins. Each time the IRQ is cleared the Comparator is updated.

Base Address +10h - Change of State Status LSB, Groups 1 and 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Group 1 Port C Bit 7	Group 1 Port C Bit 6	Group 1 Port C Bit 5	Group 1 Port C Bit 4	Group 0 Port C Bit 7	Group 0 Port C Bit 6	Group 0 Port C Bit 5	Group 0 Port C Bit 4

Base Address +11h - Change of State Status MSB, Groups 3 and 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Group 3 Port C Bit 7	Group 3 Port C Bit 6	Group 3 Port C Bit 5	Group 3 Port C Bit 4	Group 2 Port C Bit 7	Group 2 Port C Bit 6	Group 2 Port C Bit 5	Group 2 Port C Bit 4

When the IRQ output is triggered, read from Base +10h and 11h (bytes or word) to get the COS status. Each 1 bit has an I/O pin that changed. To clear the IRQ output pin and update the Comparator's memory Write all 0's to Base +10h and 11h (bytes or word).

Base Address +12h - Change of State Enable LSB, Groups 1 and 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Group 1 Port C Bit 7	Group 1 Port C Bit 6	Group 1 Port C Bit 5	Group 1 Port C Bit 4	Group 0 Port C Bit 7	Group 0 Port C Bit 6	Group 0 Port C Bit 5	Group 0 Port C Bit 4

Base Address +13h - Change of State Enable MSB, Groups 3 and 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Group 3 Port C Bit 7	Group 3 Port C Bit 6	Group 3 Port C Bit 5	Group 3 Port C Bit 4	Group 2 Port C Bit 7	Group 2 Port C Bit 6	Group 2 Port C Bit 5	Group 2 Port C Bit 4

Write a bit pattern (mask) to Base +12h and 13h (bytes or word).
Each 1 bit will enable IRQs (COS detection) on the corresponding I/O bit.
Write all 0's to disable IRQs (Power ON default state).

Hex (h)	Standard 8255 Register Compatibility	
Offset	**Write**	**Read**
Base+0	Group 0 Port A	Group 0 Port A
Base+1	Group 0 Port B	Group 0 Port B
Base+2	Group 0 Port C	Group 0 Port C
Base+3	Group 0 Command	N/A
Base+4	Group 1 Port A	Group 1 Port A
Base+5	Group 1 Port B	Group 1 Port B
Base+6	Group 1 Port C	Group 1 Port C
Base+7	Group 1 Command	N/A
Model Specific Registers below this row		
Base+8	Group 0 Port A COS/IRQ Clear	Group 0 Port A COS Status
Base+9	Group 0 Port B COS/IRQ Clear	Group 0 Port B COS Status
Base+A	Group 0 Port C COS/IRQ Clear	Group 0 Port C COS Status
Base+B	Group 1 Port A COS/IRQ Clear	Group 1 Port A COS Status
Base+C	Group 1 Port B COS/IRQ Clear	Group 1 Port B COS Status
Base+D	Group 1 Port C COS/IRQ Clear	Group 1 Port C COS Status
Base+E	COS IRQ Enable	COS IRQ Enable Status
Base+F	N/A	N/A

Table 5-2: -48S Card Base Address Registers

The following refers only to the "-48S" card.

The card's glue logic contains registers (six 8 bit) that hold a snapshot of the I/O pins. The snapshot is taken by writing FFh to each register's address. This must be done before the Change of State system is usable. These registers are compared in real-time (1uS sample rate) with the I/O pins. Any differences (Change of State) are written to the COS Status registers which can be polled or used to generate an interrupt.

The Interrupt function uses a bit mask and Comparator to detect and generate an IRQ on selected I/O pins. Each time the IRQ is cleared the Comparator is updated.

Base Address +8h thru Base Address +Dh - Change of State Status LSB, Groups 1 and 0

Base +8h	Group 0 Port A Bit 7	Group 0 Port A Bit 6	Group 0 Port A Bit 5	Group 0 Port A Bit 4	Group 0 Port A Bit 3	Group 0 Port A Bit 2	Group 0 Port A Bit 1	Group 0 Port A Bit 0
Base +9h	Group 0 Port B Bit 7	Group 0 Port B Bit 6	Group 0 Port B Bit 5	Group 0 Port B Bit 4	Group 0 Port B Bit 3	Group 0 Port B Bit 2	Group 0 Port B Bit 1	Group 0 Port B Bit 0
Base +A	Group 0 Port C Bit 7	Group 0 Port C Bit 6	Group 0 Port C Bit 5	Group 0 Port C Bit 4	Group 0 Port C Bit 3	Group 0 Port C Bit 2	Group 0 Port C Bit 1	Group 0 Port C Bit 0
Base +B	Group 1 Port A Bit 7	Group 1 Port A Bit 6	Group 1 Port A Bit 5	Group 1 Port A Bit 4	Group 1 Port A Bit 3	Group 1 Port A Bit 2	Group 1 Port A Bit 1	Group 1 Port A Bit 0
Base +C	Group 1 Port B Bit 7	Group 1 Port B Bit 6	Group 1 Port B Bit 5	Group 1 Port B Bit 4	Group 1 Port B Bit 3	Group 1 Port B Bit 2	Group 1 Port B Bit 1	Group 1 Port B Bit 0
Base +D	Group 1 Port C Bit 7	Group 1 Port C Bit 6	Group 1 Port C Bit 5	Group 1 Port C Bit 4	Group 1 Port C Bit 3	Group 1 Port C Bit 2	Group 1 Port C Bit 1	Group 1 Port C Bit 0

When a program detects that one or more lines have changed state, either through polling or interrupt, read each status register and deal with the info and then write the value back to that register. This will clear only the COS status bits that are known to have changed. Other bits may have changed while the program's ISR is active. Repeat the process until all status bits are zero, the interrupt signal will become in-active. Note that bytes, words, or double words can be read and written.

Base Address +Eh - Change of State Status MSB, Groups 1 and 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Group 1 Port C High	Group 1 Port C Low	Group 1 Port B	Group 1 Port A	Group 0 Port C High	Group 0 Port C Low	Group 0 Port B	Group 0 Port A

Each bit in the pattern written to Base+E will enable interrupts from a specific port.

The following refers only to the "-48" card.

Hex (h)	**Standard 8255 Register Compatibility**	
Offset	**Write**	**Read**
Base+0	Group 0 Port A	Group 0 Port A
Base+1	Group 0 Port B	Group 0 Port B
Base+2	Group 0 Port C	Group 0 Port C
Base+3	Group 0 Command	N/A
Base+4	Group 1 Port A	Group 1 Port A
Base+5	Group 1 Port B	Group 1 Port B
Base+6	Group 1 Port C	Group 1 Port C
Base+7	Group 1 Command	N/A

Table 5-3: -48 Card Base Address Registers

Developing Your Own Software

Four register locations are required per 24-bit group. Thus the 96 channel board uses a total of 16 registers for groups 0 through 3.

The board is designed to use each of these PPI's in mode 0 wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (CHi, CLo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

Each PPI contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Output buffers are automatically set by hardware logic according to the control register states. Control registers are located at base addresses +3h, +7h, +Bh, and +Fh. Bit assignments in each of these control registers are as follows:

Bit	Assignment	Function
D0	Port C Lo (C0-C3)	1 = Input, 0 = Output
D1	Port B	1 = Input, 0 = Output
D2	Backward Compatible	Must be 0
D3	Port C Hi (C4-C7)	1 = Input, 0 = Output
D4	Port A	1 = Input, 0 = Output
D5,D6	Backward Compatible	Must be 0
D7	Mode Set Flag	1 = Active

Table 5-4: Control Register Bit Assignments

Note:
Because all I/O pins are buffered, the 8255 individual bit control feature is not available. This board uses control registers to manage buffer direction.

The board emulates four Intel 8255 PPIs – in mode 0. The bit assignments and functionality of the control register has been kept to maintain backward compatibility with existing software. The emulated 8255 chips differ from the original in that when a port is configured to be outputs, the I/O pins follow their commanded state (the original 8255 default outputs were all high). A port that is programmed to be inputs may have a value written to it. A READ of the port will return the state of the I/O pins in that case. When that port is configured to be an output latch the value previously written to it will be driven on the I/O pins.

The board may, as a factory option, occupy two spaces in memory. One space is I/O mapped (standard). The other space is memory mapped and should be found below the 1 megabyte boundary (to facilitate DOS programs). The PCIFIND.EXE program will display the board's locations in memory.

Programming Example

The following programming example is provided as a guide to assist you in developing your working software. In this example, the board base address is 2D00 hex and I/O lines of Port 0 are to be setup as follows:

port A = Input
port B = Output
port C hi = Input
port C lo = Output

Configure bits of the Control Register as:

D7	1	Active Mode Set
D6	0	0
D5	0	0
D4	1	Port A = input
D3	1	Port C Hi = input
D2	0	0
D1	0	Port B = output
D0	0	Port C Lo = output

This corresponds to 98 hex. If the card base address is 2D00 hex, use the BASIC OUT command to write to the control register as follows:

```
10    BASEADDR=&H2D00
20    OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C, use the BASIC INPUT command:

```
30    X=INP(BASEADDR)'Read Port A
40    Y=INP(BASEADDR+2)/16'Read Port C Hi
```

To set outputs high ("1") at Port B and the lower nybble of Port C:

```
50    OUT BASEADDR+1,&HFF'Turn on all Port B bits
60    OUT BASEADDR+2,&HF'Turn on all bits of Port C Lo
```

Chapter 6: Connector Pin Assignments

Note that the board uses four 50-pin male headers, each with identical pinouts. The headers are designated P1 through P4 (refer to the Option Selection Map in Chapter 3 for the physical arrangement and orientation).

Assignment		Pin
Port C Hi (can be enabled for COS detection on the "-96")	PC7	1
	PC6	3
	PC5	5
	PC4	7
Port C Lo	PC3	9
	PC2	11
	PC1	13
	PC0	15
Port B	PB7	17
	PB6	19
	PB5	21
	PB4	23
	PB3	25
	PB2	27
	PB1	29
	PB0	31
Port A	PA7	33
	PA6	35
	PA5	37
	PA4	39
	PA3	41
	PA2	43
	PA1	45
	PA0	47
Fused +5 VDC		49

Table 6-1: Connector Pin Assignments

Notes:

1. All even numbered pins are board ground.
2. Connectors P1 through P4 correspond to I/O Groups 0 through 3.
3. P1 and P3 are right-angle headers with 0.100" spacing for IDC ribbon cabling.
4. P2 and P4 are vertical headers.
5. P1 and P3 are populated for P104-DIO-48 and 48S (Groups 0 and 2)

Chapter 7: Specification

Digital Inputs (TTL Compatible)

- Logic High: 2.0 to 5.0 VDC
- Logic Low: -0.5 to +0.8 VDC
- Input Load (High): 10uA
- Input Load (Low): -10Ua

Digital Outputs

- Logic High: 2.5 VDC min., source 32 mA
- Logic Low: 0.5 VDC max., sink 64 mA
- Power Output: +5 VDC from computer bus

Environmental

- Operating Temperature: 0°C to +70°C, Factory Option -40°C to +85°C
- Storage Temperature: -50°C to +120°C
- Humidity: 5 to 95% RH, non-condensing

Power Required

- 3.3V quiescent current for the '96, '48S, and '48 = 10mA
- 3.3V typical current for the '96 = 50mA
- 3.3V typical current for the '48S and '48 = 30mA
- 5V typical current with all outputs low for the '96 = 352mA
- 5V typical current with all outputs low for the '48s and '48 = 176mA
- 5V typical current with all outputs high (no load) for the '96, '48S, and '48 = < 50uA
- 5V typical current with all I/O set as inputs for the '96, '48S, and '48 = < 250uA

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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10623 Roselle Street, San Diego CA 92121
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