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10623 Roselle Street, San Diego, CA 92121 • (858) 550-9559 • FAX (858) 550-7322
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MODELS PCI-DIO-24D and PCI-DIO-24H

Digital I/O Cards

USER MANUAL

FILE: MPCI-DIO-24DH.G1r

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Chapter 1: Introduction

Features

- 24 Bits of Digital Input/Output.
- All 24 I/O Lines Buffered on the Card.
- I/O Buffers Can Be Tri-stated under Program Control.
- Four and Eight Bit Ports Independently Selectable for I/O.
- Pull-Ups on I/O Lines. Pull Down resistors may be installed at the factory (**per port 8 bit**)
- Resettable fused +5V Supply Available to the User.
- "H" version compatible with Industry Standard I/O Racks.
- Three optional 82c54 type (**9 16-bit converters**) counters.

Applications

- Automatic Test Systems.
- Laboratory Automation.
- Robotics.
- Machine Control.
- Security Systems, Energy Management.
- Relay Monitoring and Control.
- Parallel Data Transfer to PC.
- Sensing Switch Closures or TTL, DTL, CMOS Logic.
- Driving Indicator Lights or Recorders.

Description

The card comes in two basic models. The difference between the two models is that I/O connections to the D are via a standard 37-pin D-sub connector while I/O connections to the H are via a 50-pin connector. The cards are 4.8 inches long and may be installed in any 5V PCI-bus slot in IBM and compatible personal computers.

These cards provide 24 bits of parallel digital input/output on the PCI bus. These cards contain a type 8255-5 Programmable Peripheral Interface (PPI) chip. They can be programmed to accept inputs or to provide outputs on three 8-bit ports designated Ports A, B, and C. Port C can be further divided into two 4-bit nibbles. The direction of each port is independent of other ports.

Each I/O line is buffered by a type 74ABT245B tristate buffer transceiver capable of sourcing 32 mA or sinking 64mA. Pull-ups on the card assure that there are no erroneous outputs at power up until the card is initialized by system software. The buffers are configured automatically by hardware logic for input or output use according to direction assignment from a control register in the PPI. Further, if a jumper is properly placed on the card, the tristate buffers may be enabled/disabled under program control. (See the Option Selection section to follow.)

I/O wiring connections for the H card are via a 50-pin connector on the back plate of the card. Flat insulation-displacement ribbon cables can be used to connect these cards to termination panels and relay output cards. Also, the 50-pin connection provides compatibility with OPTO-22, Gordos, Potter & Brumfield and Western Reserve Controls module mounting racks. Fused +5 VDC power is available on the I/O connector at pin 49. The on-board fuse is rated at 0.5A at room temperature, and can be reset by cycling computer power, or by removing the load.

I/O wiring connections for the D card are via a 37-pin D-sub connector on the back plate of the card. A 37-pin D-sub solder cup mating connector, or flat insulation-displacement ribbon cable can be used to connect these cards to termination panels. The "D" version has a fused 5 volts available at connector pin 20. The on-board fuse is rated at 0.5A, and can be reset the same as the H version.

The card can generate an interrupt to the computer on bit 3 of Port C if the IRQD jumper is installed and the INTSEL0 jumper is installed in the INT position. When bit C3 goes high (edge triggering) an interrupt is requested. For the H model card, a rising edge signal on pin 22 on the 50-pin connector can be used to generate an interrupt if the INTSEL0 jumper is installed in the EXT position. Pin 20 on the H model card and Pin 2 on the D model card are used to disable interrupts when set low (grounded).

Optional Counter/Timers
These cards have options to include one, two, or three 82C54 counter(s) that each include three 16-bit counter/timers factory configured in an optimal module for use as event counters, frequency output, pulse width, and frequency measurement. See the Block Diagram which shows one 82C54 counter. If your card has one or more of these optional counters, an -S01, -S02, or -S03 is appended to the model number for one, two, or three counters respectively. For example, a 24-bit digital input/output card with a 50-pin connector and two 82C54 counters is model H-S02.

The card can also generate an interrupt to the computer on Out2 of the first 82C54 if the IRQT jumper is installed.

Note
If you have a model D-S03, then the fused +5V power output is not available.

Specifications

Digital Inputs (TTL Compatible)

- Logic High: 2.0 to 5.0 VDC
- Logic Low: -0.5 to +0.8 VDC
- Load: ±20 µA

Digital Outputs

- Logic High: 2.0 VDC min., source 32 ma
- Logic Low: 0.55 VDC max., sink 64 ma

Optional Counter/Timers

- Type: 82C54 programmable interval counters (up to three)
- Output drive: Source 2.5 mA, sink 24 mA
- Input Gate: TTL/CMOS compatible
- Clock: On-board, 1 MHz crystal-controlled oscillator
- Active Count Edge: Negative edge (falling edge)
- Min. Clock Pulse Width: 30 ns high, 40 ns low
- Timer Range: 16 bits (x3 per i8254)
- Power Output: Resettable 0.5A fused +5 VDC from computer bus

Power Required

- Basic Unit: +5 VDC at 170 mA typical if no current is drawn from the auxiliary fused +5 VDC output
- With One Counter: +5 VDC at 190 ma
- With Two Counters: +5 VDC at 210 ma
- With Three Counters: +5 VDC at 230 ma

Environmental

- Operating Temperature Range: 0 °C. to 60 °C
- Storage Temperature Range: -50 °C. to +120 °C
- Humidity: 0 to 90% RH, non-condensing
- Size: 4.8" Long (122 mm)

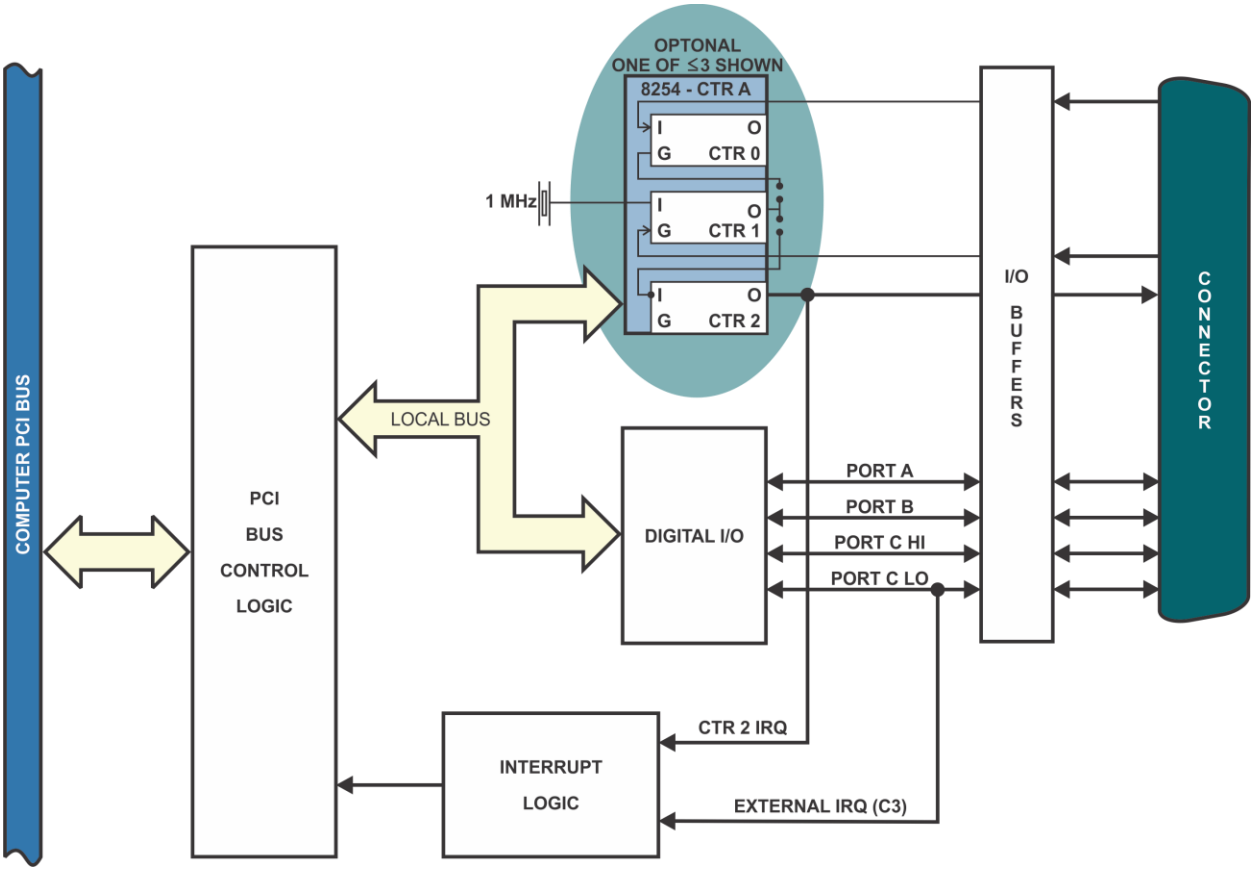


Figure 1-1: Card D or H Block Diagram

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the card for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this card is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system.

Configure Card Options via Jumper Selection
Before installing the card into your computer, carefully read Chapter 3: Option Selection of this manual, then configure the card according to your requirements. Our Windows based setup program can be used in conjunction with Chapter 3 to assist in configuring jumpers on the card, as well as provide additional descriptions for usage of the various card options.

CD Software Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS
1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS
1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX
1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Caution! * ESD A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.

Hardware Installation

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETUP.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the computer cover.
5. Carefully install the card in an available 5V or 3.3V PCI expansion slot (you may need to remove a backplate first).
6. Inspect for proper fit of the card and tighten screws. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
7. Install an I/O cable onto the card's bracket mounted connector.
8. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
9. Run PCIfind.exe to complete installing the card into the registry (for Windows only) and to determine the assigned resources.
10. Run one of the provided sample programs that was copied to the newly created card directory (from the CD) to test and validate your installation.

The base address assigned by BIOS or the operating system can change each time new hardware is installed into or removed from the computer. Please recheck PCIFind or Device Manager if the hardware configuration is changed. Software you write can automatically determine the base address of the card using a variety of methods depending on the operating system. In DOS, the PCI\SOURCE directory shows the BIOS calls used to determine the address and IRQ assigned to installed PCI devices. In Windows, the Windows sample programs demonstrate querying the registry entries (created by PCIFind and NTIOPCI.SYS during boot-up) to determine this same information.

Chapter 3: Option Selection

Refer to the setup programs on the CD provided with the card. Also, refer to the Block Diagram and the Option Selection Map when reading this section of the manual.

Buffer Mode Jumper

A means of enabling or disabling (tristating) the 74ABT245B input/output buffers under program control is provided at the jumper position labeled TST/BEN. When the jumper is in the BEN (Buffer Enable) position, the I/O buffers are always enabled. When the jumper is in the TST (Tristate) position, enabled/disabled state is controlled by a control register. See Chapter 6, Programming for a description.

Note
A jumper must be installed in EITHER the TST or the BEN position for the card to function.

Interrupt Mode Jumpers

Place the Interrupt Select 0 jumper in the INT position to select the Digital I/O interrupt (port C bit 3).
Place the Interrupt Select 0 jumper in the EXT position to select the External Input interrupt.

Install the IRQD jumper to enable the Digital I/O or External Input interrupts.
Install the IRQT jumper to enable the Timer generated interrupt.

The foregoing are the only manual setups necessary to use these cards. Input/Output selection is done via software by writing to a control register in the PPI as described in the Programming chapter of this manual.

Optionally, the card may have been modified at the factory to convert the pull up resistors to pull down resistors. The model number would then be similar to D S04 or H S04.

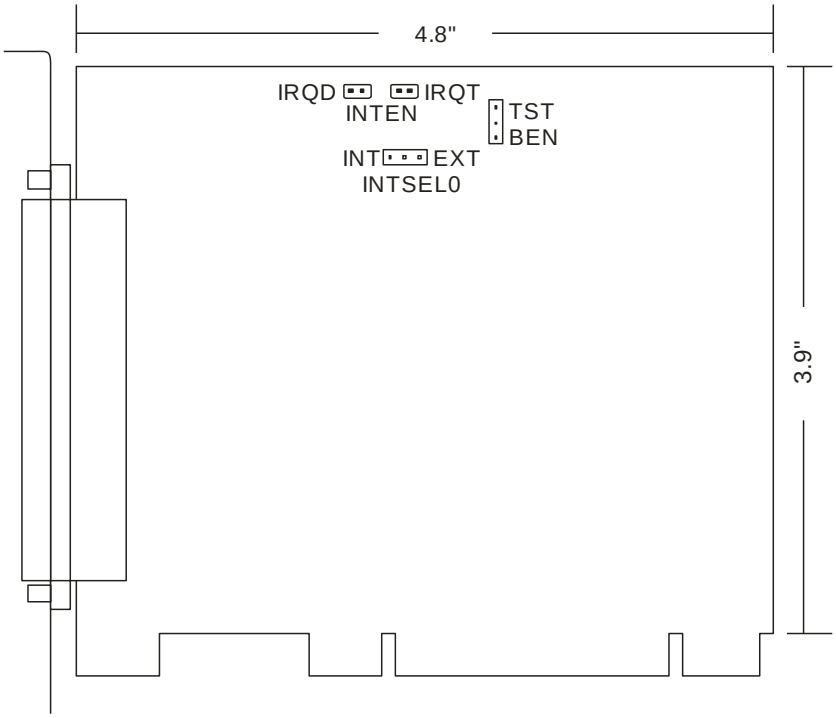


Figure 3-1: Option Selection Map version D

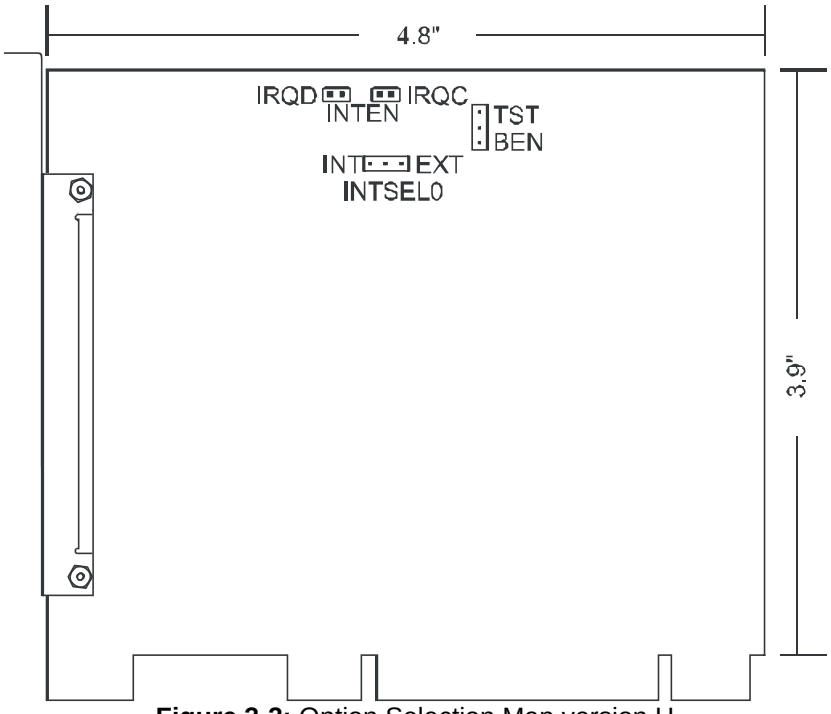


Figure 3-2: Option Selection Map version H

Chapter 4: Address Selection

These cards use one address space and occupy sixteen I/O locations. The S03 (which has 3 counters) version takes up 32 I/O locations.

PCI architecture is Plug-and-Play. This means that the BIOS or Operating System determines the resources assigned to PCI cards rather than the user selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the PCIFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI bus, the addresses assigned to each function on each of the cards, and the respective IRQs (if any) allotted.

Alternatively, some operating systems (Windows95/98/2000) can be queried to determine which resources were assigned. In these operating systems, you can use either PCINT or the Device Manager utility from the System Properties Applet of the control panel. These cards are installed in the Data Acquisition class of the Device Manager list. To display a list of the resources allocated, select the card, click "Properties", and then select the "Resources Tab".

PCIFind uses the Vendor ID and the Device ID to search for your card, then reads the base address and IRQ assigned. If you want to determine the base address and IRQ assigned, use the following information. The Vendor ID for these cards is 494F. The device ID's are:

D version: 0C51	H version: 0C50
D w/Counters: 0E52	H w/Counters: 0E51

The PCI bus supports 64K of address space, your card's addresses may be located anywhere in the 0000 to FFFF hex range.

Chapter 5: Software

There are sample programs provided with the card in C, Pascal, QuickBASIC, and several Windows languages. DOS samples are located in the DOS directory and Windows samples are located in the WIN32 directory. The following paragraphs describe the setup program and the 16- and 32-bit utility drivers.

SETUP.EXE

This program is supplied in the root or base directory as a tool for you to use in configuring jumpers on the card. It is menu-driven and provides pictures of the card on the computer monitor. You make simple keystrokes to select functions. The picture on the monitor then changes to show how the jumper should be placed to effect your choices.

The setup program is a stand-alone program that can be run at any time. It does not require that the card be plugged into the computer for any part of the setup. The program is self-explanatory with operation instructions and on-line help.

To run this program, at the DOS prompt, enter SETUP.EXE followed by Enter.

Chapter 6: Programming

These cards are I/O-mapped devices that are easily configured from any language and any language can easily perform digital I/O through the card's ports. This is especially true if the form of the data is byte or word wide. All references to the I/O ports would be in absolute port addressing.

Developing Your Application Software

If you wish to gain a better understanding of the programs on diskette, then the information in the following paragraphs will be of interest to you. Refer to the data sheets and 8255-5 specification in Appendix A.

A total of 16 register locations are used by these cards. With all counters (S03), the total becomes 32 register locations.

Address	Port Assignment	Operation
Base Address	PA Group 0	Read/Write
Base Address +1	PB Group 0	Read/Write
Base Address +2	PC Group 0	Read/Write
Base Address +3	Control byte	Write Only
Base Address +4	Unused	
Base Address +5	Unused	
Base Address +6	Unused	
Base Address +7	Unused	
Base Address +8	Unused	
Base Address +9	Unused	
Base Address +C	Enable/Disable Buffer	Write Only
Base Address +D	Disable Interrupts	Write Only
Base Address +E	Enable Interrupts	Write Only
Base Address +F	Clear Interrupt latch	Write Only
Base Address +10	Counter/Timer A0	Read/Write
Base Address +11	Counter/Timer A1	Read/Write
Base Address +12	Counter/Timer A2	Read/Write
Base Address +13	Counter/Timer A Control	Read/Write
Base Address +14	Counter/Timer B0	Read/Write
Base Address +15	Counter/Timer B1	Read/Write
Base Address +16	Counter/Timer B2	Read/Write
Base Address +17	Counter/Timer B Control	Read/Write
Base Address +18	Counter/Timer C0	Read/Write
Base Address +19	Counter/Timer C1	Read/Write
Base Address +1A	Counter/Timer C2	Read/Write
Base Address +1B	Counter/Timer C Control	Read/Write

Table 6-1: Address Assignment Table

These cards use an 8255-5 PPI to provide a total of 24 bits input/output capability. The card is designed to use the PPI in Mode 0 wherein:

a. There are two 8-bit groups (A and B) and two 4-bit groups (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

The PPI contains a Control Register. This write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. The PPI should be configured during initialization by writing to the Control Registers even if the ports are only going to be used as inputs. Output buffers are automatically set by hardware according to the Control Register states. Note that Control Register is located at base address +3 and bit assignments are as follows:

Bit	Assignment	Code
D0	Port C Lo (C0-C3)	1=Input, 0=Output
D1	Port B	1=Input, 0=Output
D2	Mode Select	1=Mode 1, 0=Mode 0
D3	Port C Hi (C4-C7)	1=Input, 0=Output
D4	Port A	1=Input, 0=Output
D5,D6	Mode Select	00=Mode 0, 01=Mode 1, 1X=Mode 2
D7	Mode Set Flag	1=Active

Table 6-2: Control Register Bit Assignment

Note

Mode 1 cannot be used by these cards without modification (Consult factory.). Thus, bits D2, D5, and D6 should always be set to "0". If your card has been modified for use in Mode 1, then there will be an Addenda sheet in the front of this manual. These cards cannot be used in PPI Mode 2 because of byte & nibble wide buffering .

Note

In Mode 0, do not use the control register byte for the individual bit control feature. The hardware uses the I/O bits to control buffer direction on this card. The control register should only be used for setting up input and output of the ports and enabling the buffer.

These cards provide a means to enable/disable the tristate I/O buffers under program control. If the TST/BEN jumper on the card is installed in the BEN position, the I/O buffers are permanently enabled. However, if that jumper is in the TST position, enable/disable of the buffers is software controlled via the control register as follows:

a. The card is initialized in the input mode by the computer reset command.
b. When bit D7 of the Control Register is set high, direction of the three groups of the associated PPI chip as well as the mode can be set. For example, a write to Base Address +3 with data bit D7 high programs port direction at 0 ports A, B, and C. If, for example, hex 80 is sent to Base Address +3, the Port 0 PPI will be configured in mode 0 with Groups A, B, and C as outputs.

At the same time, data bit D7 is also latched in a buffer controller for the associated PPI chip. A high state disables the buffers and, thus, all four buffers will be put in the tristate mode; i.e. disabled.

c. Now, if any of the ports are to be set as outputs, you may set the values to that port with the outputs still in the tristate condition. (If all ports are to be set as inputs, this step is not necessary.)

d. If data bit D7 is low when the control byte is written, ONLY the associated buffer controller is addressed. If, for example, a control byte of hex 80 has been sent as previously described, and the data to be output are correct, and it is now desired to open the three groups, then it is necessary to send a control byte of hex 00 to base address +3 to enable the Port 0 buffers. When you do this, the buffers will be enabled.

Note

All data bits except D7 must be the same for the two control bytes

Those buffers will now remain enabled until another control byte with data bit D7 high is sent to base address +3.

Programming Example (C)

The following program fragment in C language illustrates the foregoing:

```
const BASE_ADDRESS 0x300;
outportb(BASE_ADDRESS +3, 0x89);   /*This instruction sets the mode to Mode 0, ports A and
                                   B as output, and port C as input. Since bit D7 is high, the
                                   output buffers are set to tristate condition. See item b.
                                   above.*/
outportb(BASE_ADDRESS,0);
outportb(BASE_ADDRESS+1,0);        /*These instructions set the initial state of ports A and B
                                   to all zeroes. Port C is not set because it is configured as
                                   an input. See item c. above.*/
outportb(BASE_ADDRESS +3, 0x09);   /*Enable the tristate output buffers by using the same
                                   control byte used to configure the PPI, but now set bit
                                   D7 low. See item d. above.*/
```

Programming Example (Basic)

The following example in BASIC is provided as a guide to assist you in developing your working software. In this example, the card base address is 2D0 hex and the I/O lines of group 0 are to be setup as follows:

Port A	=	Input
Port B	=	Output
Port C Hi	=	Input
Port C Lo	=	Output

The first step is to configure the control register. Configure bits of the control register as:

D7	1	Active Mode Set
D6	0	Mode 0
D5	0	Mode 0
D4	1	Port A = input
D3	1	Port C Hi = input
D2	0	Mode 0
D1	0	Port B = output
D0	0	Port C Lo -= output

This corresponds to 98 hex. If the card address is 2D0 hex, use the BASIC OUT command to write to the control register as follows:

```
10      BASEADDR=&H2D0
20      OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C:

```
30      X=INP(BASEADDR)'Read Port A
40      Y=INP(BASEADDR+2)/16'Read Port C Hi
```

To set outputs high (1) at Port B and the lower nybble of Port C:

```
50      OUT BASEADDR+1,&HFF'Turn on all Port B bits
60      OUT BASEADDR+2,&HF'Turn on all bits of Port C lower nybble
```

Enabling/Disabling I/O Buffers

When using the tristate mode (Jumper in the TST position), the method to disable the I/O buffers involved writing a control word to the Control Register at Base Address +3. This control word was required to have bit D7 (the most significant bit) set. That meant that the PPI translated it as an "active mode set" and reset the output data latches to "zero" on all output ports and the output buffers were disabled. However, if the buffers are to be enabled at a later time, the output latches will be in a "zero" state. For example, if all the outputs were 1's, they will now be 0's and the output buffers will be disabled. This problem can be resolved as follows.

Two computer I/O bus addresses are available that permit you to enable or disable the I/O buffers at will, without programming the PPI mode. Buffers are enabled/disabled at Base Address + C. To enable the buffers and to set outputs to the desired state, you can write to Base + C with bit D7 low. If you wish to subsequently disable the buffers, you can write to Base + C with bit D7 high. In this way you can enable/disable the output buffers without programming the PPI mode.

Note

When writing a command byte to the card while the TST jumper is installed, the PPI output buffers are disabled. Thus, when you desire to to change the mode, you must first set the new mode and then enable the buffers. Enabling the buffers can be done at either Base Address +3 or Base Address +A.

Interrupts

The card has three sources of interrupts:

1. A Digital I/O signal on Pin 9 for the H version (50 pin), or Pin 7 for the D version (37 pin). The Digital I/O interrupt is Port C bit 3 and is enabled by installing jumpers IRQD and INT. Port C bit 3, if set for an output, can be toggled under program control to generate an interrupt.
2. An External TTL input signal on Pin 22 for the H version only. This interrupt is enabled by installing jumpers IRQD and EXT. The H version of the card also has an active-low input to disable interrupts on J1 pin 20.
3. An onboard Timer output signal from the first 82C54 output 2 (S01, S02, and S03 versions only). The Timer interrupt is enabled by installing jumpers IRQT and INT. This feature allows a “clock tick interrupt”.

All interrupts are triggered on the rising edge of the signal source.
All interrupts are enabled through software by writing any value to Base+E, and disabled through software by writing any value to Base+D.
All interrupts are cleared by writing any value to Base+F.

Refer to Chapter 3 for hardware enabling and disabling of interrupts. Refer to Table 6-1 for more on software control.

Chapter 7: 8254 Counter/Timer

These cards have the option of one, two, or three 82C54 counter(s) that each include three 16-bit counter/timers factory configured in an optimal module for use as event counters, frequency output, pulse width, and frequency measurement (See Block Diagram). Each counter can be programmed to any count as low as 1 or 2, and up to 65,535, depending on the mode chosen. For those interested in more detailed information, a full description can be found in the Intel (or equivalent manufacturer's) data sheet.

Operational Modes

The 8254 modes of operation are described in the following paragraphs to familiarize you with the versatility and power of this device. For those interested in more detailed information, a full description of the 8254 programmable interval timer can be found in the Intel (or equivalent manufacturers') data sheets. The following conventions apply for use in describing operation of the 8254 :

Clock:	A positive pulse into the counter's clock input
Trigger:	A rising edge input to the counter's gate input
Counter Loading:	Programming a binary count into the counter

Mode 0: Pulse on Terminal Count
After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing.

Mode 1: Retriggerable One-Shot
The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. This forms a retriggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator
This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low. This mode also works well as an alternative to mode 0 for event counting.

Mode 3: Square Wave Generator
This mode operates like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency synthesis are two possible applications for this mode. Note that in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the wave form.

Mode 4: Software Triggered Strobe
This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter.

Mode 5: Hardware Triggered Strobe
In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

Counter/Timer Registers

Base + 10 Write/Read: Counter#A0 When writing, this register is used to load a count value into the counter. The transfer is either a single or double byte transfer, depending on the control byte written to the counter control register at BASE ADDRESS +13. If a double byte transfer is used, then the least-significant byte of the 16 bit value is written first, followed by the most significant byte. When reading, the current count of the counter is read. The type of transfer is also set by the control byte.

Base + 11 Write/Read: Counter #A1 See description for Base + 10 Write/Read.

Base + 12 Write/Read: Counter #A2 See description for Base + 10 Write/Read.

Base + 13 Write: Counter Control Register The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows: These cards contain a type 8254 programmable counter/timer that allows you to implement such functions as a Real Time Clock, Event Counter, Digital One-Shot, Programmable Rate Generator, Binary Rate Multiplier, Complex Wave Generator and/or a Motor Controller. The 8254 consists of three, 16-bit, presettable, down counters. Each counter can be programmed to any count between 1 or 2 and 65,535 in binary format depending on the mode chosen.

Programming the 8254

The counters are programmed by writing a control byte into the counter control register. Refer to the previous register map for the base addresses of the counters and the counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows:

B7	B6	B5	B4	B3	B2	B1	B0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0-SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter #0
0	1	Program Counter #1
1	0	Program Counter #2
1	1	Read/Write Cmd.*

* See section on Reading and Loading the Counters.

RW0-RW1: These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0-M2: These bits set the operational mode of the selected counter.

Mode	M2	M1	M0
0	0	0	0
1	0	0	1
2	X	1	0
3	X	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (BCD = 0) or BCD (BCD = 1).

Reading and Loading the Counters

If you attempt to read the counters on the fly when there is a high input frequency, you will most likely get erroneous data. This is partly caused by carries rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it is possible that carries will be propagated from the low to the high byte during the read cycle.

To circumvent these problems, you can perform a counter-latch operation in advance of the read cycle. To do this, load the RW1 and RW2 bits with zeroes. This instantly latches the count of the selected counter (selected via the SC1 and SC0 bits) in a 16-bit hold register. (An alternative method of latching counter(s) that has an additional advantage of operating simultaneously on several counters is through a readback command to be discussed later.) A subsequent read operation on the selected counter returns the held value. Latching is the best way to read a counter on the fly without disturbing the counting process. You can only rely on directly read counter data if the counting process is suspended while reading by bringing the gate low.

For each counter you must specify in advance the type of read or write operation that you intend to perform. You have a choice of loading/reading (a) the high byte of the count, or (b) the low byte of the count, or (c) the low byte followed by the high byte. This last is most generally used and is selected for each counter by setting the RW1 and RW0 bits to ones. Subsequent read/load operations must be performed in pairs in this sequence or the sequencing flip-flop in the 8254 chip will get out of step. The readback command byte format is:

B7	B6	B5	B4	B3	B2	B1	B0
1	1	CNT	STA	C2	C1	C0	0

CNT: When 0, latches the counters selected by bits C0-C2.
STA: When 0, returns the status byte of counters selected by C0-C2.
C0, C1, C2: When high, select a particular counter for readback. C0 selects Counter 0, C1 selects Counter 1, and C2 selects Counter 2.

You can perform two types of operations with the readback command. When CNT=0, the counters selected by C2 through C0 are latched simultaneously. When STA=0, the counter status byte is read when the counter I/O location is accessed. The counter status byte provides information about the current output state of the selected counter and its configuration. The status byte returned if STA=0 is:

B7	B6	B5	B4	B3	B2	B1	B0
OUT	NC	RW1	RW2	M2	M1	M0	BCD

OUT: Current state of counter output pin.
NC: Null count. This indicates when the last count loaded into the counter register has been loaded into the actual counter. The exact time of load depends on the configuration selected. Until the count is loaded into the counter, it cannot be read.
RW1, RW0: Read/Write command.
M2, M1, M0: Counter mode.
BCD: BCD = 0 is binary mode, otherwise counter is in BCD mode.

If both STA and CNT bits in the readback command byte are set low and the RW1 and RW0 bits have both been previously set high in the counter control register (thus selecting two-byte reads), then reading a selected counter address location will yield:

1st Read: Status byte
2nd Read: Low byte of latched data
3rd Read: High byte of latched data

After any latching operation on a counter, the contents of its hold register must be read before any subsequent latches of that counter will have any effect. If a status latch command is issued before the hold register is read, then the first read will read the status, not the latched value.

8254 Driver

A simple driver is provided to perform basic counter/timer operations on this card. Source code for the driver and a sample program showing how to use the functions are located in the DOS\CSAMPLES directory. The following functions are provided:

Frequency Measure

The Frequency Measure function of the 8254 Counter Driver has the ability to measure an unknown frequency from 1KHz to 2MHz. This function requires as input the Base Address of the card. The unknown frequency is applied to the CLOCK IN pin of the card. The function will return the frequency as a long integer in Hz.

```
long frequency_measure(unsigned BaseAddress);
```

Event Counter

The Event Counter function has the ability to trace the number of events that have occurred. This function requires the Base Address and an additional parameter that identifies which features should be implemented on this call to the function. Each feature can be identified by its unique integer value. Multiple features can be run in a single call to the function by ORing the respective integer values together. Features will be executed in increasing integer order. The CLOCK IN pin of the card is the point of application for the incoming events. (Note: This function is limited by the input speed of the 8254 counter, and slow signals are preferred. Further only 65,535 events are possible without a RESET.) The function returns the number of events (based on priority) or 0 for those features that do not specify a return value.

Features:

```
INITIALIZE    = 1;    initialize the counter
START         = 2;    begin counting
SINCESTART    = 4;    return the number of events since the start
SINCELAST     = 8;    return the number of events since last check
STOP          = 16;   stop counting events
RESET         = 32;   reset number of events to 0
        unsigned event_counter(unsigned BaseAddress, int feature);
```

Generate Frequency

The Generate Frequency function will generate a square wave (0 to +5V) with the desired frequency. The Base Address of the card as well as the frequency are required as input to the function. The counter can generate a frequency with a range of 1Hz to 250KHz. The square wave can be read on the CLOCK OUT pin of the card.

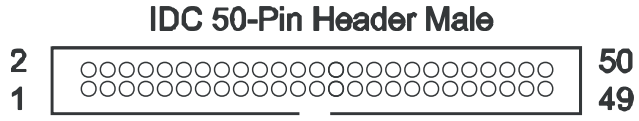
```
void generatefrequency(unsigned BaseAddress, unsigned long frequency);
```

Pulse Width

The Pulse Width function will measure the width of an applied event from its rise to its fall (effectively one half the period). The Base Address of the card is required as input to the function. The signal should be applied to the CLOCK IN pin of the card. Software latency will be affected by the operating system and will set a limit on the precision of the measurement.

```
unsigned pulse_width(unsigned BaseAddress);
```

Chapter 8: Connector Pin Assignments



The H card has a 50-pin connector provided on the back plate of these cards for I/O connections. The mating connector is an AMP type 1-746285-0 or equivalent. Connector pin assignments are listed below.

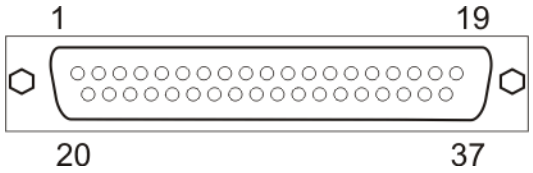
Assignment		Pin
Port C Hi	PC7	1
	PC6	3
	PC5	5
	PC4	7
Port C Lo	PC3	9
	PC2	11
	PC1	13
	PC0	15
Port B	PB7	17
	PB6	19
	PB5	21
	PB4	23
	PB3	25
	PB2	27
	PB1	29
	PB0	31
Port A	PA7	33
	PA6	35
	PA5	37
	PA4	39
	PA3	41
	PA2	43
	PA1	45
	PA0	47
Fused +5 VDC		49

Assignment	Pin
Counter A0 Freq In	2
Ctr A1 P.W.I. (Gate)	4
Counter A2 Freq Out	6
Counter B0 Freq in	8
Ctr B1 P.W.I. (Gate)	10
Counter B2 Freq Out	12
Counter C0 Freq In	14
Ctr C1 P.W.I. (Gate)	16
Ctr C2 Freq Out	18
Digital Interrupt Disable	20
External Interrupt Source	22
Even pins 24-50 are all Ground	24
	26
	28
	30
	32
	34
	36
	38
	40
	42
	44
	46
	48
	50

Table 8-1: 50-Pin Connector Pin Assignments

The D card has a 37-pin Male D-sub connector provided on the back plate of these cards for I/O connections.

If all three counters are present, pin 20 is counter C2's frequency output. Otherwise, pin 20 is fused +5V power.



Assignment	Pin	Assignment	Pin
		Ground	1
C2 Freq Out / Fused +5V	20	Digital Interrupt Disable	2
Ground	21	Port C 7 Hi	3
Port B 7	22	Port C 6 Hi	4
Port B 6	23	Port C 5 Hi	5
Port B 5	24	Port C 4 Hi	6
Port B 4	25	Port C 3 Lo	7
Port B 3	26	Port C 2 Lo	8
Port B 2	27	Port C 1 Lo	9
Port B 1	28	Port C 0 Lo	10
Port B 0	29	Counter A0 Freq In	11
Port A 7	30	Ctr A1 P.W.I. (Gate)	12
Port A 6	31	Counter A2 Freq Out	13
Port A 5	32	Counter B0 Freq in	14
Port A 4	33	Ctr B1 P.W.I. (Gate)	15
Port A 3	34	Counter B2 Freq Out	16
Port A 2	35	Counter C0 Freq In	17
Port A 1	36	Ctr C1 P.W.I. (Gate)	18
Port A 0	37	Ground	19

Table 8-2: 37-Pin Male D-Sub Connector Pin Assignments

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

ACCES I/O PRODUCTS, INC.
10623 Roselle Street, San Diego CA 92121
Tel. (858)550-9559 FAX (858)550-7322
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