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MODEL PCI-DIO-96C3

USER MANUAL

FILE: MPCI-DIO-96C3.A1j

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Chapter 1: Introduction

Features

- 96 Channels of Digital Input/Output.
- All I/O Lines are Buffered on the Card.
- Four and Eight Bit Ports are Independently Selectable for I/O on Each 24-Bit Group.
- Pull Down Resistors may be installed at the factory.
- Hysteresis on Inputs and Pull-Up Resistors on I/O Lines.
- Interrupt and Interrupt-Disable Capability.
- Tri-state I/O Ports Under Software Control.
- +5V, fused, ½A Supply at Room Temperature, per Each Group.
- Compatible with Industry Standard I/O Racks.
- Nine 16-bit 10MHz externally gated counters.

Applications

- Automatic Test Systems.
- Security Systems, Energy Management.
- Robotics.
- Relay Monitoring and Control.
- Parallel Data Transfer to PC.
- Sensing switch closures or TTL, DTL, CMOS Logic.
- Driving Indicator Lights or Recorders.

Each I/O line is buffered and capable of sourcing 32mA, or sinking 64mA. The board contains four 82c55 Programmable Peripheral Interface (PPI) chips. Each PPI supports two 8-bit ports (A, B) and two 4-bit ports (C_{hi}, C_{low}). Each port can be configured to function as either input or output. The I/O line buffers (type 74ABT245) are configured automatically by hardware logic for input or output according to the PPI 82c55 Control Register direction (as assigned by software).

The I/O buffers are pulled up through 10KΩ resistors to +5VDC. 680Ω pulldowns are available.

At power-on the I/O buffers are enabled, allowing transparent backwards compatibility. However, enable/disable of the buffers is also possible under software control.

One I/O line of each digital group and one counter of each counter group can be used to interface User Interrupts to the computer. Interrupts are enabled by jumper installation (IEN jumper).

I/O wiring connections are via 50-pin headers on the board. This provides compatibility with OPTO-22, Gordos, Potter & Brumfield, Western Reserve Controls, etc. module mounting racks. Every second conductor of the flat cables is grounded to minimize crosstalk between signals. If needed for external circuits, +5VDC power is available on each I/O connector at pin 49 through a 500mA resettable fuse.

The cards occupy 32 addresses within the PCI I/O space. The base address is assigned by the system. Refer to the Option Selection Section of this manual for a detailed description.

Specifications

Digital Input

- Logic High: 2.0 to 5.0 VDC.
- Logic Low: -0.5 to +0.8 VDC.
- Input Load (Hi): +20 uA.
- Input Load (Lo): -20 uA.

Digital Output

- Logic High: 2.5 VDC min., source 32 mA.
- Logic Low: 0.5 VDC max., sink 64 mA.
- Size: 11.8" long (300 mm).
- Power Req.: +5 VDC at 200 mA typical.
- Power Output: Resettable 0.5A fused +5 VDC from computer bus.

Counter/Timers

- Type: 82C54 programmable interval counters.
- Output Drive: Source 32mA, sink 64 mA.
- Gate/Clock Input: TTL/CMOS compatible. 10 MHz maximum clock rate.
- On-Board Gate/Clock Source: 1 MHz crystal-controlled oscillator, available by jumper.
- Active Count Edge: Negative edge (Falling edge).
- Minimum Clock Pulse Width: 30 ns high, 50 ns low.
- Timer Range: 16 bits each, 3 timers per IC.
- Power Output: Resettable 0.5A fused +5 VDC from computer bus.

Environmental

- Operating Temperature Range: 0 °C. to 60 °C.
- Storage Temperature Range: -50 °C. to +120 °C.
- Humidity: 0 to 90% RH, non-condensing.

Utility software provided on diskette with these cards is an illustrated setup program, SETUP.EXE. Interactive displays show locations and proper settings of jumpers to set up tristate control of the buffers and the interrupt enable function. Another utility program on the diskette, PCIFind.EXE, can be used to locate resources used by installed PCI-bus cards. Additionally, two sample programs and a utility driver for use with VisualBASIC for Windows are provided. See the Software section of this manual for a detailed description of the latter.

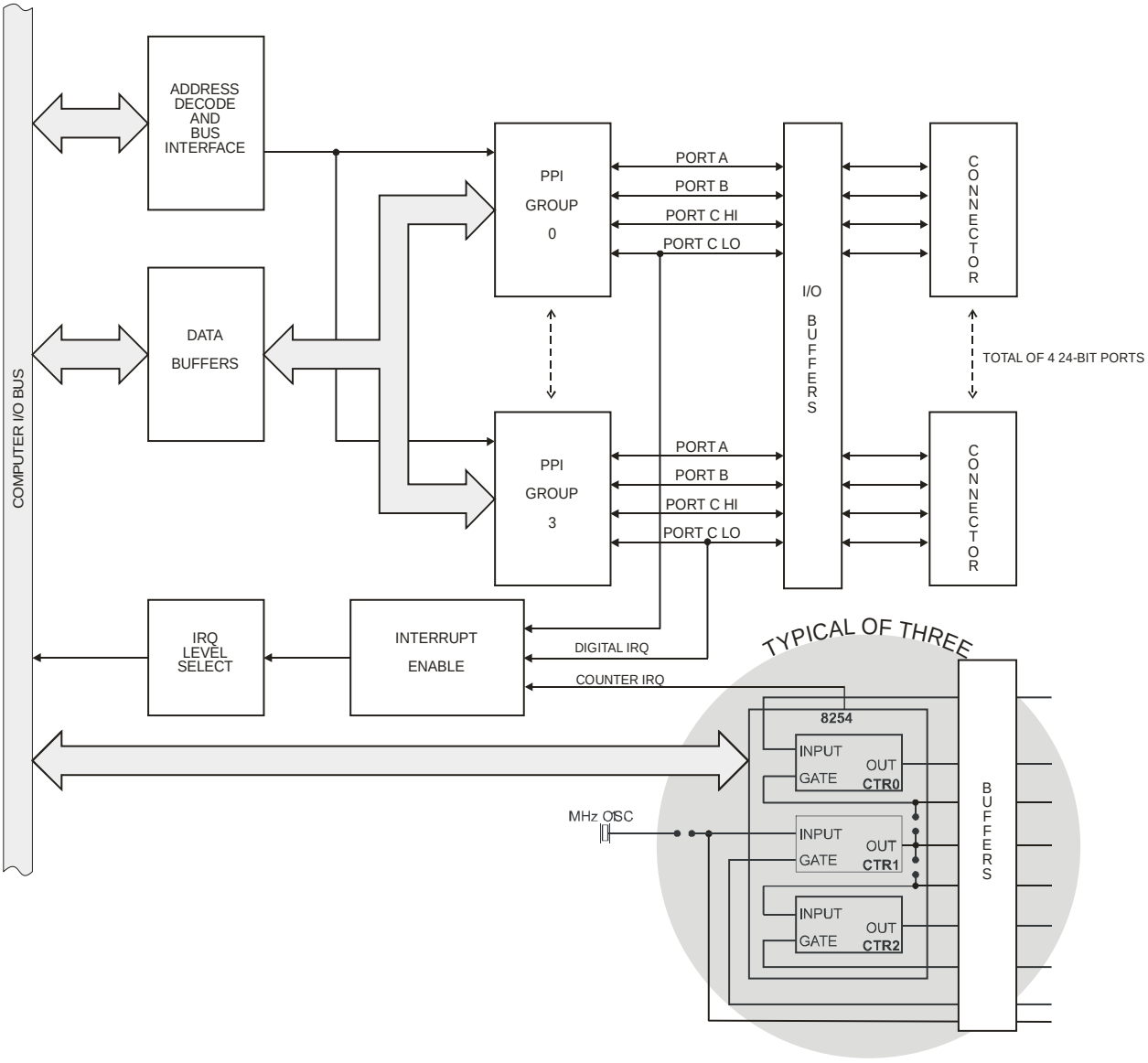


Figure 1-1: Block Diagram

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the card for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this card is on CD and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system.

Configure Card Options via Jumper Selection

Before installing the card into your computer, carefully read Chapter 3: Option Selection of this manual, then configure the card according to your requirements. Our Windows based setup program can be used in conjunction with Chapter 3 to assist in configuring jumpers on the card, as well as provide additional descriptions for usage of the various card options.

CD Software Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

DOS

1. Place the CD into your CD-ROM drive.
2. Type D : Enter to change the active drive to the CD-ROM drive.
3. Type I N S T A L L Enter to run the install program.
4. Follow the on-screen prompts to install the software for this board.

WINDOWS

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D : I N S T A L L, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

LINUX

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Caution! * ESD A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.

Hardware Installation

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETUP.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the computer cover.
5. Carefully install the card in an available 5V or 3.3V PCI expansion slot (you may need to remove a backplate first).
6. Inspect for proper fit of the card and tighten screws. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
7. Install an I/O cable onto the card's bracket mounted connector.
8. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
9. Run PCIfind.exe to complete installing the card into the registry (for Windows only) and to determine the assigned resources.
10. Run one of the provided sample programs that was copied to the newly created card directory (from the CD) to test and validate your installation.

The base address assigned by BIOS or the operating system can change each time new hardware is installed into or removed from the computer. Please recheck PCIFind or Device Manager if the hardware configuration is changed. Software you write can automatically determine the base address of the card using a variety of methods depending on the operating system. In DOS, the PCI\SOURCE directory shows the BIOS calls used to determine the address and IRQ assigned to installed PCI devices. In Windows, the Windows sample programs demonstrate querying the registry entries (created by PCIFind and NTIOPCI.SYS during boot-up) to determine this same information.

Chapter 3: Option Selection

Refer to the illustrated setup programs on the CD provided with the card when reading this section of the manual.

Interrupts from the digital I/O circuits are possible if the IEN jumper (one for each 24-bit port) is installed. Interrupts from the counter circuits are possible if the IEN jumper is installed; IEN4 enables interrupts from Counter A2, IEN5 from Counter B2, and IEN6 from Counter C2.

External interrupts are accepted on pin 9 (Bit C3) of each I/O connector. The interrupt signal should be a rising edge and is latched. The latch is cleared by a 'write' to Base Address +1F hex. An interrupt can also be generated by software by toggling bit 3 (low then high) of port C of any group.

Your program must enable/disable interrupts, interrupts are disabled at 'power up'. You enable interrupts globally by writing any value to Base Address +1F hex. Another 'write' to Base Address +1F hex will clear and enable all interrupts. Also, you can clear and disable interrupts by writing any value to Base Address +1E hex.

At power-on or reset, or when input mode is selected, the digital I/O buffers are not tristated. If the tristate feature is enabled by a write to Base + 1C with data bit 0 = HI, then a port I/O buffer is tristated when output mode is selected in the control byte. The port I/O buffer is automatically re-enabled when the port bit values are written. The tristate feature can be disabled by a write to Base + 1C with data bit 0 = LO.

The foregoing are the only manual setups necessary to use the card. Input/Output selection is done by writing to the PPI Control Registers as described in the Programming section of this manual.

The source of an IRQ can be determined by a read from Base + 1E or Base + 1F. The IRQ Status Register bits are as follows:

D0 = DIO Group 0, Port C Bit 3
D1 = DIO Group 1, Port C Bit 3
D2 = DIO Group 2, Port C Bit 3
D3 = DIO Group 3, Port C Bit 3
D4 = Counter Group A, Counter 2
D5 = Counter Group B, Counter 2
D6 = Counter Group C, Counter 2
D7 = IRQ enabled

Chapter 4: Address Selection

These cards use one address space, and occupy 32 register locations, 16 for the digital I/O and 8 for the timer/counters (8 are unused). These are defined in the Port Address Selection Table in the Programming section of this manual.

PCI architecture is inherently plug-and-play. This means that the BIOS or Operating System determines the resources assigned to PCI cards. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the PCIFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI bus, the addresses assigned to each function on each of the cards, and their respective IRQs.

Alternatively, some operating systems can be queried to determine which resources were assigned. In these operating systems, you can use either PCIFind or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

The PCI bus supports 64K of I/O address space, your card's addresses may be located anywhere in the 1000h to FFFFh hex range.

PCIFind uses the Vendor ID and Device ID to search for your card, then reads the base address and IRQ.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for the card is 494Fh. (ASCII for "IO")
The Device ID for the card is 2C58h.

Chapter 5: Software

Several programs are supplied to support these cards and to help you develop your application's software. These programs are on the CD or diskette that comes with your card and are briefly described in an earlier section of this manual. The following paragraphs contain additional information about the setup program.

SETUP.EXE

This program is supplied as a tool for you to use in configuring jumpers on the card. It is menu-driven and provides pictures of the card on the computer monitor. You make simple keystrokes to select the functions. In turn, the pictures then change to show how the jumpers should be placed to effect your choices.

The setup program is a stand-alone program that can be run at any time. It does not require the card to be plugged into the computer for any part of the setup. The program is self-explanatory with operation instructions and on-line help. (Of course, the card has to be installed to check the PCIFind utility.)

To run this program, at the DOS prompt, enter SETUP.EXE followed by the Enter key.

Chapter 6: Programming

The card uses thirty-two (32) registers in I/O space as listed in the following table.

Address	Function	Operation
Base Address	DIO Group 0 Port A	Read / Write
Base Address +1	DIO Group 0 Port B	Read / Write
Base Address +2	DIO Group 0 Port C	Read / Write
Base Address +3	DIO Group 0 Control	Write
Base Address +4	DIO Group 1 Port A	Read / Write
Base Address +5	DIO Group 1 Port B	Read / Write
Base Address +6	DIO Group 1 Port C	Read / Write
Base Address +7	DIO Group 1 Control	Write
Base Address +8	DIO Group 2 Port A	Read / Write
Base Address +9	DIO Group 2 Port B	Read / Write
Base Address +A	DIO Group 2 Port C	Read / Write
Base Address +B	DIO Group 2 Control	Write
Base Address +C	DIO Group 3 Port A	Read / Write
Base Address +D	DIO Group 3 Port B	Read / Write
Base Address +E	DIO Group 3 Port C	Read / Write
Base Address +F	DIO Group 3 Control	Write

Address	Function	Operation
Base Address +10	Counter A 0	Read / Write
Base Address +11	Counter A 1	Read / Write
Base Address +12	Counter A 2	Read / Write
Base Address +13	Counter A Control	Write
Base Address +14	Counter B 0	Read / Write
Base Address +15	Counter B 1	Read / Write
Base Address +16	Counter B 2	Read / Write
Base Address +17	Counter B Control	Write
Base Address +18	Counter C 0	Read / Write
Base Address +19	Counter C 1	Read / Write
Base Address +1A	Counter C 2	Read / Write
Base Address +1B	Counter C Control	Write
Base Address +1C	DIO Tristate Enable / Disable	Write
Base Address +1D	Reserved	N/A
Base Address +1E	Interrupt Clear and Disable Interrupt Status	Write Read
Base Address +1F	Interrupt Clear and Enable Interrupt Status	Write Read

Table 6-1: Address / Register Table

If you wish to gain a better understanding of the sample programs and source code, then the information in the following paragraphs will be of interest to you. Follow the 82c55 and 82c54 specifications located in the Chipspecs directory on the CD, to program the DIOs and Counters respectively.

The cards are designed to use each of these PPI's in mode 0 wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.

Each PPI contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each PPI should be configured during initialization by writing to the control registers even if the ports are going to be used as inputs. Output buffers are automatically set by hardware logic according to the control register states. Control registers are located at base addresses +3, +7, +B and +F. Bit assignments in each of these control registers are as follows:

Bit	Assignment	Function
D0	Port C Lo (C0-C3)	1 = Input, 0 = Output
D1	Port B	1 = Input, 0 = Output
D2	Mode Selection	1 = Mode 1, 0 = Mode 0
D3	Port C Hi (C4-C7)	1 = Input, 0 = Output
D4	Port A	1 = Input, 0 = Output
D5,D6	Mode Selection	01 = Mode 1, 00 = Mode 0
D7	Mode Set Flag & Tristate	1X = Mode 2 1 = Active & Tristate

Table 6-2: Control Register Bit Assignments

Note
PPI Mode 1 cannot be used with these cards without modification. Thus, bits D2, D5, and D6 should always be set to "0". If your card has been modified to operate in Mode 1, then there is an Addendum sheet in the front of this manual describing that modification. These cards cannot be modified to operate in PPI Mode 2.

Note
In Mode 0, do not use the control register byte for the individual bit control feature. The hardware uses the I/O bits to control buffer directions on this card. The control register should only be used for setting up input and output of the ports and enabling the buffer.

Programming Example

The following programming example is provided as a guide to assist you in developing your working software. In this example, the card base address is 2000 hex and I/O lines of Port 0 are to be setup as follows:

port A	=	Input
port B	=	Output
port C hi	=	Input
port C lo	=	Output

Configure bits of the Control Register as:

D7	1	Active Mode Set
D6	0	Mode 0
D5	0	Mode 0
D4	1	Port A = Input
D3	1	Port C Hi = Input
D2	0	Mode 0
D1	0	Port B = Output
D0	0	Port C Lo = Output

This corresponds to 98 hex. If the card base address is 2000 hex, use the BASIC OUT command to write to the control register as follows:

```
10  BASEADDR=&H2000
20  OUT BASEADDR+3,&H98
```

To read the inputs at Port A and the upper nybble of Port C, use the BASIC INPUT command:

```
30  X=INP(BASEADDR)'Read Port A
40  Y=INP(BASEADDR+2)/16'Read Port C Hi
```

To set outputs high ("1") at Port B and the lower nybble of Port C:

```
50  OUT BASEADDR+1,&HFF'Turn on all Port B bits
60  OUT BASEADDR+2,&HF'Turn on all bits of Port C Lo
```

Interrupt Examples

Example 1: Internal interrupt generated by software
The IEN interrupt option jumper for the group must be installed. Configure port C Low as an output and set bit C3 high. Enable interrupts globally by writing any value to Base Address+1Fh. Toggle bit C3 low for at least 1 µs then high. An interrupt service routine may clear and disable all interrupts from the board by writing any value to Base Address+1Eh.

Example 2: External interrupt
The IEN interrupt option jumper for the group must be installed. Configure port C Low as an input and enable interrupts globally by writing any value to Base Address+1Fh. The pulse at pin 9 (bit C3) must go low for at least 1 µs then high. An interrupt service routine may clear and disable all interrupts from the board by writing any value to Base Address+1Eh.

Example 3: Internal interrupt from Counter 2
The IEN interrupt option jumper for the group must be installed. Disable interrupts by writing any value to the register at base+1Eh. Program Counter 1 and Counter 2 to divide the 1MHz onboard clock down to a tick frequency.

Chapter 7: Connector Pin Assignments

For I/O connections, 50-pin headers are provided on the cards; one for each group of 24 I/O lines, and one for all three counter groups. Mating connectors are AMP type 1-746285-0 or equivalent.

Assignment	Pin		Assignment	Pin
Port C Hi Bit 7	1		All Even Numbered Pins are Ground	2
Port C Hi Bit 6	3			4
Port C Hi Bit 5	5			6
Port C Hi Bit 4	7			8
Port C Lo Bit 3*	9			10
Port C Lo Bit 2	11			12
Port C Lo Bit 1	13			14
Port C Lo Bit 0	15			16
Port B Bit 7	17			18
Port B Bit 6	19			20
Port B Bit 5	21			22
Port B Bit 4	23			24
Port B Bit 3	25			26
Port B Bit 2	27			28
Port B Bit 1	29			30
Port B Bit 0	31			32
Port A Bit 7	33			34
Port A Bit 6	35			36
Port A Bit 5	37			38
Port A Bit 4	39			40
Port A Bit 3	41			42
Port A Bit 2	43			44
Port A Bit 1	45			46
Port A Bit 0	47			48
Fused +5 VDC	49			50

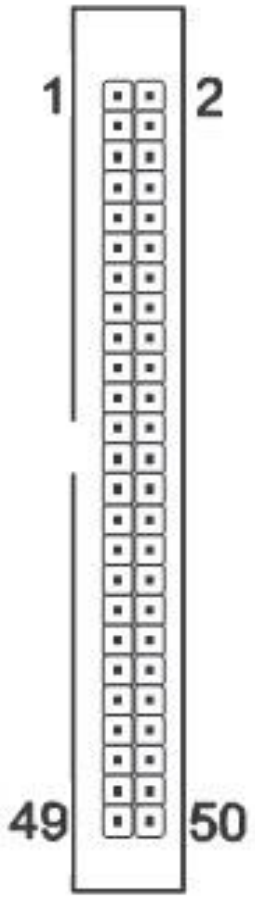


Table 7-1: Digital I/O Connector Pin Assignments
* This line is an I/O port and also a User Interrupt.

Pin	Signal		Pin	Signal
1	Counter A Clock 0		2	Ground
3	Counter A Gate 0		4	Ground
5	Counter A Out 0		6	Counter A Out 1
7	Ground		8	Counter A Gate 1
9	Ground		10	Counter A Clock 1
11	Ground		12	Counter A Clock 2
13	Ground		14	Counter A Gate 2
15	Ground		16	Counter A Out 2
17	Ground		18	Counter B Clock 0
19	Ground		20	Counter B Gate 0
21	Ground		22	Counter B Out 0
23	Counter B Out 1		24	Ground
25	Counter B Gate 1		26	Ground
27	Counter B Clock 1		28	Ground
29	Counter B Clock 2		30	Ground
31	Counter B Gate 2		32	Ground
33	Counter B Out 2		34	Fused +5 VDC
35	Counter C Out 0		36	Ground
37	Counter C Gate 0		48	Ground
39	Counter C Clock 0		40	Ground
41	Counter C Clock 1		42	Ground
43	Counter C Gate 1		44	Ground
45	Counter C Out 1		46	Counter C Out 2
47	Ground		48	Counter C Gate 2
49	Ground		50	Counter C Clock 2

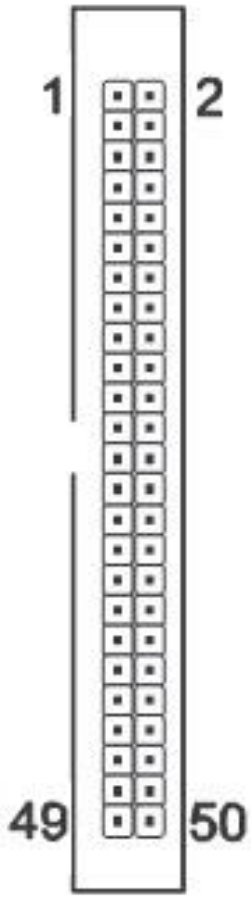


Table 7-2: Counter I/O Connector Pin Assignments

Chapter 8: Programmable Interval Timer

The card contains a type 8254 programmable counter/timer which allows you to implement such functions as a Real-Time Clock, Event Counter, Digital One-Shot, Programmable Rate Generator, Square-Wave Generator, Binary Rate Multiplier, Complex Wave Generator, and/or a Motor Controller. The 8254 is a flexible but powerful device that consists of three independent, 16-bit, presettable, down counters. Each counter can be programmed to any count as low as 1 or 2, and up to 65,535 in binary format, depending on the mode chosen.

On the card each counter group has three counters, designated Counter #0, Counter #1, and Counter #2. With none of the counter jumpers installed, each counter is un-dedicated, with the gate, output and clock connections fully accessible via the I/O connector. If a group's CLKx1 jumper is installed, Counter #1 receives clock inputs from a 1 MHz onboard oscillator. If a group's CLKx2 jumper is installed, the output of Counter #1 is used as the clock for Counter #2, thus Counters #1 and #2 are cascaded together to form a 32-bit counter. The output of counter #2 is also available at the I/O connector, pin 23. If the GATEx0 jumper is installed, the output of Counter #1 can be used as a gate input for Counter #0.

Operational Modes

The 8254 modes of operation are described in the following paragraphs to familiarize you with the versatility and power of this device. For those interested in more detailed information, a full description of the 8254 programmable interval timer can be found in the Intel (or equivalent manufacturers) data sheets. The following conventions apply for use in describing operation of the 8254:

Clock:	A positive pulse into the counter's clock input.
Trigger:	A rising edge input to the counter's gate input.
Counter Loading:	Programming of a binary count into the counter.

Mode 0: Pulse on Terminal Count
After the counter is loaded, the output is set low and will remain low until the counter decrements to zero. The output then goes high and remains high until a new count is loaded into the counter. A trigger enables the counter to start decrementing. This mode is commonly used for event counting with Counter #0.

Mode 1: Retriggerable One-shot
The output goes low on the clock pulse following a trigger to begin the one-shot pulse and goes high when the counter reaches zero. Additional triggers result in reloading the count and starting the cycle over. If a trigger occurs before the counter decrements to zero, a new count is loaded. Thus, this forms a re-triggerable one-shot. In mode 1, a low output pulse is provided with a period equal to the counter count-down time.

Mode 2: Rate Generator
This mode provides a divide-by-N capability where N is the count loaded into the counter. When triggered, the counter output goes low for one clock period after N counts, reloads the initial count, and the cycle starts over. This mode is periodic, the same sequence is repeated indefinitely until the gate input is brought low. This mode also works well as an alternative to mode 0 for event counting.

Mode 3: Square Wave Generator
This mode operates periodically like mode 2. The output is high for half of the count and low for the other half. If the count is even, then the output is a symmetrical square wave. If the count is odd, then the output is high for (N+1)/2 counts and low for (N-1)/2 counts. Periodic triggering or frequency synthesis are two possible applications for this mode. Note that in this mode, to achieve the square wave, the counter decrements by two for the total loaded count, then reloads and decrements by two for the second part of the wave form.

Mode 4: Software Triggered Strobe
This mode sets the output high and, when the count is loaded, the counter begins to count down. When the counter reaches zero, the output will go low for one input period. The counter must be reloaded to repeat the cycle. A low gate input will inhibit the counter.

Mode 5: Hardware Triggered Strobe
In this mode, the counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of the trigger.

Programming

On the card, the 8254 counters occupy addresses as described in Chapter 6.

The counters are programmed by writing a control byte into a counter control register. The control byte specifies the counter to be programmed, the counter mode, the type of read/write operation, and the modulus. The control byte format is as follows:

B7	B6	B5	B4	B3	B2	B1	B0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC0-SC1: These bits select the counter that the control byte is destined for.

SC1	SC0	Function
0	0	Program Counter 0
0	1	Program Counter 1
1	0	Program Counter 2
1	1	Read Back Command

RW0-RW1: These bits select the read/write mode of the selected counter.

RW1	RW0	Counter Read/Write Function
0	0	Counter Latch Command
0	1	Read/Write LS Byte
1	0	Read/Write MS Byte
1	1	Read/Write LS Byte, then MS Byte

M0-M2: These bits set the operational mode of the selected counter.

Mode	M2	M1	M0
0	0	0	0
1	0	0	1
2	X	1	0
3	X	1	1
4	1	0	0
5	1	0	1

BCD: Set the selected counter to count in binary (BCD bit = 0) or BCD (BCD bit = 1).

Reading and Loading the Counters

If you attempt to read an active counter, you will most likely get erroneous data. This is partly caused by carries rippling through the counter during the read operation. Also, the low and high bytes are read sequentially rather than simultaneously and, thus, it is possible that carries will be propagated from the low to the high byte during the read cycle. To circumvent these problems, you should perform a counter-

latch operation in advance of the read cycle. To do this, load the RW1 and RW2 bits with zeroes. This instantly latches the count of the selected counter(selected via the SC1 and SC0 bits) in a 16-bit hold register. A subsequent read operation on the selected counter returns the held value. Latching is the best way to read an active counter without disturbing the counting process. You can only rely on directly-read counter data if the counting process is suspended while reading, by bringing the gate low, or by halting the input pulses.

For each counter you must specify in advance the type of read or write operation that you intend to perform. You have a choice of loading/reading (a) the high byte of the count, or (b) the low byte of the count, or (c) the low byte followed by the high byte.

Programming Examples

Using Counter #0 as a Pulse Counter

Note that the counters are "down" counters so, when resetting them, it's better to load them with a full count value of 65,535 rather than zero.

```
outportb(BASEADDRESS + 7,0x30);      /* counter 0, mode 0 */
outportb(BASEADDRESS + 4,0xff);      /* counter 0 low load byte */
outportb(BASEADDRESS + 4,0xff);      /* counter 0 high load byte */
```

Reading Counter #0

```
outportb(BASEADDRESS + 7,0x00);      /* counter 0, latch command */
                                     /* read in both bytes of the latched value and combine into an integer */
value = inportb(BASEADDRESS + 4) + (inportb(BASEADDRESS + 4) * 256;
```

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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