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# MODEL
# PCIe-DIO-144
# Digital I/O Card

# USER MANUAL

FILE: PCIe-DIO-144.A1a

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# Chapter 1: Introduction

The PCIe-DIO-144 series are x1 lane PCI Express (PCIe) boards with 144 digital I/O lines designed for use in a variety of Digital I/O (DIO) applications. They use the high speed PCIe bus to transfer digital data to and from the board. The FPGA based DIO emulates 8255 compatible chips in mode 0, making it easy to program. This also allows for simple migration from older ACCES' PCI-based DIO boards. Lastly, the x1 lane PCIe connector is very flexible and can be inserted into any x1, x4, x8, x16, or x32 PCIe slot.

## Features

- 144 high-current DIO lines
- IRQ generation from DIO Bit C3 on each connector
- DIO lines buffered
- Five 50 pin male headers on side of card, one DB37F on mounting bracket
- Four and eight bit ports independently selectable for inputs or outputs
- Per port jumper selectable 10k ohm Pull-up/Pull-down resistors on DIO lines
- Global jumper selectable VCCIO (5V, 3.3V, 2.5V, 1.8V)
- VCCIO voltage available to the user via 0.5A resettable fuse
- Compatible with industry standard I/O racks like Grayhill, Opto 22, Western Reserve Controls, etc.

## Applications

- Automatic Test Systems
- Security Systems, Energy Management
- Robotics
- Relay Monitoring and Control
- Parallel Data Transfer to PC
- Sensing switch closures or TTL, DTL, CMOS Logic
- Driving Indicator Lights or Recorders

## Functional Description

## Buffers

Each I/O line is buffered and capable of sourcing or sinking 32mA when VCCIO is configured for 5V. The board contains FPGA circuitry that emulates type 8255 mode 0 Programmable Peripheral Interface (GROUP) to provide a computer interface to digital I/O lines. Each group supports two 8-bit ports (A, B) and two 4-bit ports (CHi, CLo). Each port can be configured to function as either input or output latches. The I/O line buffers are configured automatically by hardware logic for input or output according to the GROUP Control Register direction software assignment. All DIO lines can be tristated as well using the corresponding software command.

## Bias Resistors

Outputs of the I/O buffers are jumper configurable to be pulled up or down through 10kΩ resistor networks to VCCIO. There is a description in the Hardware Details chapter of this manual that describes how to configure these on your card.

## Interrupts

One digital I/O line of each group can be used to generate an interrupt with a rising edge at bit C3. Interrupts are enabled by software.

## Wiring

I/O wiring connections are via 50-pin headers on the board and a single DB37F connector on the card mounting bracket. The 50-pin headers provide compatibility with OPTO-22, Gordos, Potter & Brumfield, Western Reserve Controls, etc. module mounting racks. Every second conductor of the 50 pin header is grounded to minimize crosstalk between signals. If needed for external circuits, fused VCCIO power is available on each 50 pin I/O connector at pin 49.

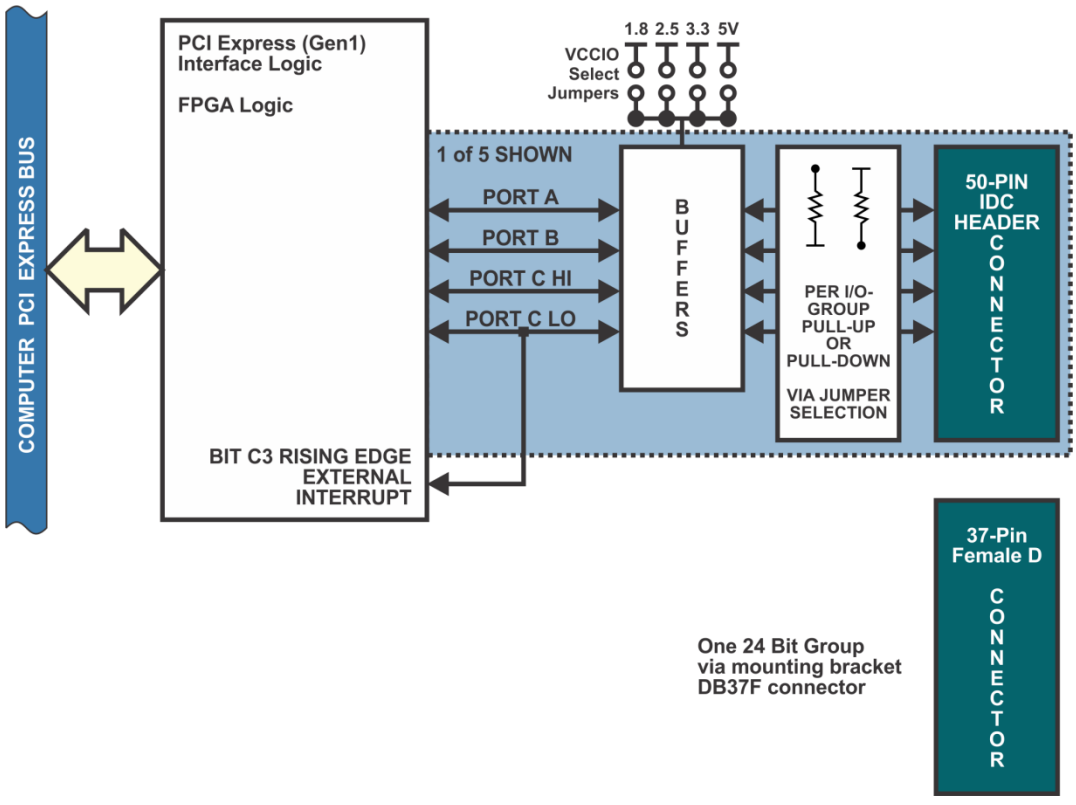



**Figure 1-1: Block Diagram**

## Ordering Guide

| | |
|---|---|
| PCIe-DIO-144 | 144 Channel Digital I/O Card |

## Model Options

| | |
|---|---|
| -T | Extended operating temperature (-40° to +85°C) |
| -RoHS | RoHS compliant version |

## Included with your board

The following components are included with your shipment. Please take time now to ensure that no items are damaged or missing.

PCIe-DIO-144 Board
Adjacent mounting bracket with strain relief bars for the 5 x 50 pin flat ribbon cables
Packing Slip

## Optional Accessories

| | |
|---|---|
| CAB50F-X | Ribbon cable assembly w/2-50 pin female connectors, X=length in feet |
| CAB50-6 | 6’ ribbon cable female 50 pin to 50 pin card edge connector |
| STB-50 | Screw terminal board for 50 pin headers on side of DIO card |
| STB-37 | Screw terminal board for DB37 connector on card mounting bracket |
| STB-120CH | 50-pin multi-header screw terminal board for 120 DIO lines |

# Chapter 2: Installation

## Software Installation

The software provided with this board is available by request on CD (see Optional Accessories in the ordering guide) for a fee, or downloaded via the product page for free and must be installed onto your hard disk prior to use.

## Installing from Downloaded Installer

Download the software package here (**http://accesio.com/files/packages/PCIe-DIO-144%20Install.exe**) or from the Downloads tab on the product page.

## Installing from CD

Perform the following steps as appropriate for your operating system. Substitute the appropriate drive letter for your drive where you see D: in the examples below.

## Windows

a. Place the CD into your CD-ROM drive.
b. The CD should automatically run the install program. If the install program does not run, click START | RUN and type D:INSTALL, click OK or press Enter.
c. Follow the on-screen prompts to install the software for this board.

## Linux

Please refer to linux.htm, and visit https://github.com/accesio for more.

***Caution! * ESD*** ***A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.***

## Hardware Installation

1. Make sure to set switches and jumpers from either the Hardware Details chapter of this manual or from the suggestions of SETTINGS.EXE.
2. Turn OFF computer power AND unplug AC power from the system.
3. Open the computer cover.
4. Lay the card on an ESD safe workstation mat and plug the 5 ribbon cables onto the headers on the side of the card. Lay the cables as they will be when installed in the PC.
5. Remove the 2 nuts holding the strain relief bars onto the adjacent mounting bracket and remove one of the strain relief bars, setting it aside along with the nuts.
6. Position the adjacent mounting bracket assembly under the cables, next to the card mounting bracket.
7. Install the strain relief bar removed in step 6 onto the adjacent mounting bracket screws and tighten the nuts without over-tightening.
8. Feed the ribbon cables secured by the adjacent mounting bracket out of the PC case through the open back plate *next to* the PCI Express slot you'll be plugging the card into and install the bracket screw.
9. Carefully plug the card into the PCI Express expansion slot while feeding the cable slack through the adjacent open back plate.
10. Inspect for proper fit of the card and tighten the bracket screw. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
11. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
12. Run one of the provided sample programs that was copied to the newly created card directory (from the CD or downloaded from the product page) to test and validate your installation.

# Chapter 3: Hardware Details

Refer to the illustrated setup program installed with the software package when reading this section of the manual. Also, refer to Figure 3-1, Option Selection Map.

External interrupts are accepted on pin 9 (Bit C3) of each 50 pin I/O connector when enabled by software. The interrupt signal should be a rising edge and is latched.

As pointed out in Chapter 1 of this manual, outputs of the I/O buffers may be either pulled-up to VCCIO or pulled down to ground. You can configure these resistors per port.

VCCIO signaling levels are globally configured via jumper selection. Refer to the specifications chapter for signal levels for each possible selection.

The foregoing are the only manual setups necessary to use these cards. Input/Output selection is done via software, by writing to the GROUP Control Registers as described in the Programming section of this manual.

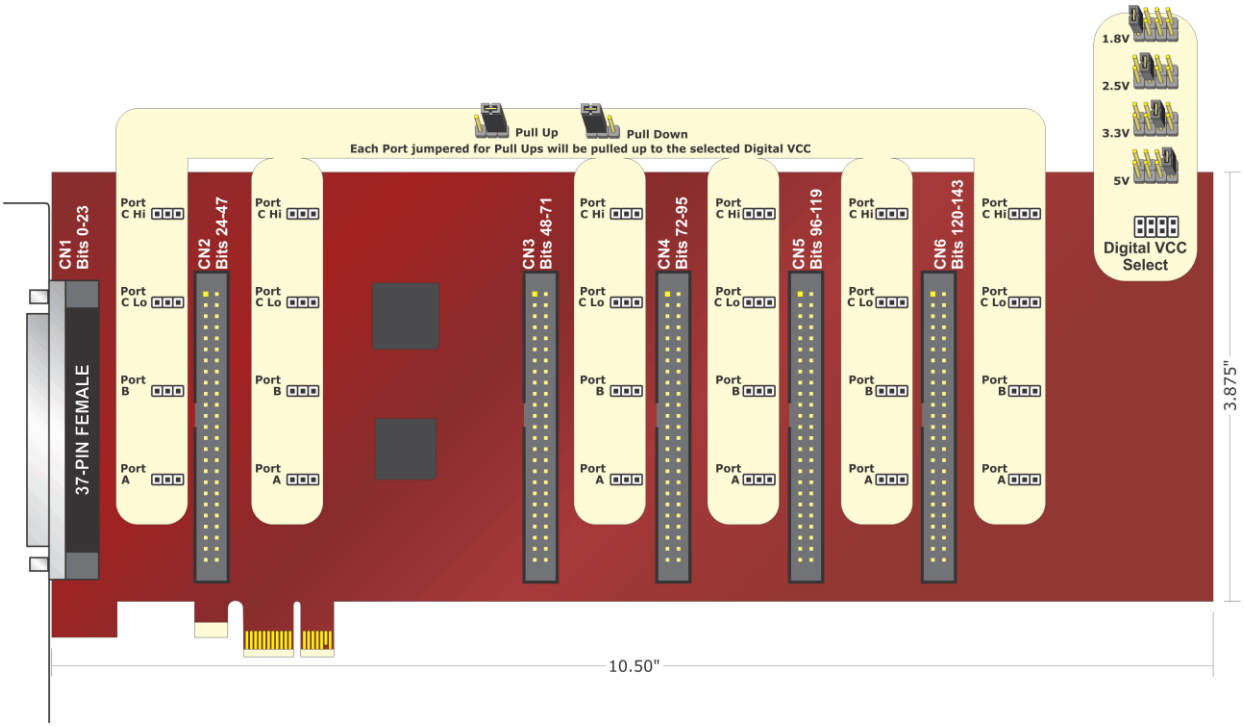



**Figure 3-1: Option Selection Map**

# Chapter 4: Address Selection

These cards use one address space, and occupy 64 register locations. These are defined in the Port Address Selection Table in the Programming section of this manual.

PCI Express architecture is inherently plug-and-play. This means that the BIOS or Operating System determines the resources assigned to PCI Express cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the AIOWDMFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI Express bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, some operating systems can be queried to determine which resources were assigned. In these operating systems, you can use either AIOWDMFind (Windows 7 or later) PCIFind or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for these cards is 494F. (ASCII for "IO")

The Device ID for the PCIe-DIO-144 is 0C40.

# Chapter 5: Programming

The 144 card is an I/O mapped device that can be easily configured from any language.

## Developing Your Own Software

Four register locations are required per 24-bit group. Thus, a total of 24 register locations are used by the PCIe-DIO-144 card for addressing groups 0 through 5.

| Address | Assignment | Operation |
|---|---|---|
| Base Address | PA Group 0 | Read/Write |
| Base Address +1 | PB Group 0 | Read/Write |
| Base Address +2 | PC Group 0 | Read/Write |
| Base Address +3 | Control Port 0 | Write Only |
| Base Address +4 | PA Group 1 | Read/Write |
| Base Address +5 | PB Group 1 | Read/Write |
| Base Address +6 | PC Group 1 | Read/Write |
| Base Address +7 | Control Port 1 | Write Only |
| Base Address +8 | PA Group 2 | Read/Write |
| Base Address +9 | PB Group 2 | Read/Write |
| Base Address +A | PC Group 2 | Read/Write |
| Base Address +B | Control Port 2 | Write Only |
| Base Address +C | PA Group 3 | Read/Write |
| Base Address +D | PB Group 3 | Read/Write |
| Base Address +E | PC Group 3 | Read/Write |
| Base Address +F | Control Port 3 | Write Only |
| Base Address +10 | PA Group 4 | Read/Write |
| Base Address +11 | PB Group 4 | Read/Write |
| Base Address +12 | PC Group 4 | Read/Write |
| Base Address +13 | Control Port 4 | Write Only |
| Base Address +14 | PA Group 5 | Read/Write |
| Base Address +15 | PB Group 5 | Read/Write |
| Base Address +16 | PC Group 5 | Read/Write |
| Base Address +17 | Control Port 5 | Write Only |
| Base Address +1C | DIO Buffer Enable | Read/Write |
| Base Address +1E | Clear/Disable Interrupts | Write Only |
| Base Address +1F | Clear/Enable Interrupts | Write Only |

**Table 6-1: Address Registry Table**

The cards are designed to emulate each GROUP wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.
e. The card is initialized in the input mode

Each GROUP contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each GROUP should be configured during initialization by writing to the control registers even if the ports are going to be used as inputs. Output buffers are automatically set by hardware logic according to the control register states. Control registers are located at base addresses +3, +7, +B, +F, +13, and +17. Bit assignments in each of these control registers are as follows:

| Bit | Assignment | Function |
|---|---|---|
| D0 | Port C Lo (C0-C3) | 1 = Input, 0 = Output |
| D1 | Port B | 1 = Input, 0 = Output |
| D2 | N/A | N/A |
| D3 | Port C Hi (C4-C7) | 1 = Input, 0 = Output |
| D4 | Port A | 1 = Input, 0 = Output |
| D5,D6 | N/A | N/A |
| D7 | Mode Set (see note 1) | Scratchpad |

**Table 6-2: Control Register Bit Assignments**

*Note 1: This bit is a read/write scratchpad. For maximum compatibility with the 8255, always set this bit (to 1).*

## Base Address +1C (read/write) DIO Buffer Enable / Disable (tri-state)

At power-up or reset, all DIO buffers on the card are enabled. To disable the DIO buffers, write a one to bit 0. To re-enable the DIO buffers, write a zero to bit 0. When buffers are disabled the pins are tri-stated and biased by the state of the pull up or down configuration jumpers. A read of bit 0 returns the enable / disable status.

## Base Address +1E/+1F (write only) Interrupt Clear & Disable/Enable

The interrupt is disabled at power-up or reset. A write to base +1F enables the interrupt whereas a write to base +1E disables it. A write to either of those address will also clear the interrupt.

# Chapter 6: Connector Pin Assignments

Five 50-pin headers are provided on the cards; one for each group of 24 I/O lines.



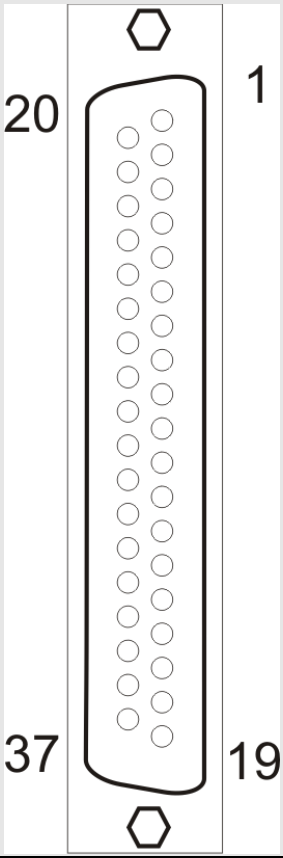

| Assignment | Pin | Assignment | Pin |
|---|---|---|---|
| Port C Hi PC7 | 1 | All Even numbered pins are Ground | 2 |
| Port C Hi PC6 | 3 | | 4 |
| Port C Hi PC5 | 5 | | 6 |
| Port C Hi PC4 | 7 | | 8 |
| Port C Lo PC3* | 9 | | 10 |
| Port C Lo PC2 | 11 | | 12 |
| Port C Lo PC1 | 13 | | 14 |
| Port C Lo PC0 | 15 | | 16 |
| Port B PB7 | 17 | | 18 |
| Port B PB6 | 19 | | 20 |
| Port B PB5 | 21 | | 22 |
| Port B PB4 | 23 | | 24 |
| Port B PB3 | 25 | | 26 |
| Port B PB2 | 27 | | 28 |
| Port B PB1 | 29 | | 30 |
| Port B PB0 | 31 | | 32 |
| Port A PA7 | 33 | | 34 |
| Port A PA6 | 35 | | 36 |
| Port A PA5 | 37 | | 38 |
| Port A PA4 | 39 | | 40 |
| Port A PA3 | 41 | | 42 |
| Port A PA2 | 43 | | 44 |
| Port A PA1 | 45 | | 46 |
| Port A PA0 | 47 | | 48 |
| Fused VCCIO | 49 | | 50 |

**Table 6-1: Connector Pin Assignments CN2 through CN6 50 pin headers**

* This line is an I/O port and also a User Interrupt.

One 37-pin female DB37 connector is provided on the card mounting bracket.

| Assignment | Pin |
|---|---|
| | |
| Fused VCCIO | 20 |
| Ground | 21 |
| PC7 | 22 |
| PC6 | 23 |
| PC5 | 24 |
| PC4 | 25 |
| PC3* | 26 |
| PC2 | 27 |
| PC1 | 28 |
| PC0 | 29 |
| PA7 | 30 |
| PA6 | 31 |
| PA5 | 32 |
| PA4 | 33 |
| PA3 | 34 |
| PA2 | 35 |
| PA1 | 36 |
| PA0 | 37 |




| Assignment | Pin |
|---|---|
| N/C No Connection | 1 |
| N/C | 2 |
| PB7 | 3 |
| PB6 | 4 |
| PB5 | 5 |
| PB4 | 6 |
| PB3 | 7 |
| PB2 | 8 |
| PB1 | 9 |
| PB0 | 10 |
| Ground | 11 |
| N/C | 12 |
| Ground | 13 |
| N/C | 14 |
| Ground | 15 |
| N/C | 16 |
| Ground | 17 |
| Fused VCCIO | 18 |
| Ground | 19 |

**Table 6-2: Connector Pin Assignments CN1 DB37F**

* This line is an I/O port and also a User Interrupt.

# Chapter 7: Specifications

## Digital I/O

| | |
|---|---|
| Lines | 144; (6 Groups) Ports A, B, CLo and CHi |
| Type | Emulates 8255 compatible chips in Mode 0 |
| Logic Level | VCCIO |
| Pull-up/down | 10k ohm, jumper selectable |

## VCCIO

| **Logic Levels** | **5V** | |
|---|---|---|
| Low Inputs | ≤ 1.5V | ≤ 2uA |
| High Inputs | ≥ 3.5V | ≤ 2uA |
| Low Outputs | ≤ 0.55V | 32mA |
| High Outputs | ≥ 3.8V | 32mA |
| | | |
| **Logic Levels** | **3.3V** | |
| Low Inputs | ≤ 0.8V | ≤ 2uA |
| High Inputs | ≥ 2.0V | ≤ 2uA |
| Low Outputs | ≤ 0.55V | 24mA |
| High Outputs | ≥ 2.4V | 24mA |
| | | |
| **Logic Levels** | **2.5V** | |
| Low Inputs | ≤ 0.7V | ≤ 2uA |
| High Inputs | ≥ 1.7V | ≤ 2uA |
| Low Outputs | ≤ 0.5V | 8mA |
| High Outputs | ≥ 1.9V | 8mA |
| | | |
| **Logic Levels** | **1.8V** | |
| Low Inputs | ≤ 0.63V | ≤ 2uA |
| High Inputs | ≥ 1.17V | ≤ 2uA |
| Low Outputs | ≤ 0.45V | 4mA |
| High Outputs | ≥ 1.2V | 4mA |

## Environmental

| | |
|---|---|
| Operating Temperature | 0° to 70°C<br>optional -40° to +85°C |
| Storage Temperature | -55° to +150°C |
| Humidity | 5% to 95% RH, w/o condensation |
| Card Dimensions | Length – 10.5" x height 3.875” (4.2" seated) |

## Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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