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10623 Roselle Street, San Diego, CA 92121 • (858) 550-9559 • FAX (858) 550-7322
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MODELS
PCIe-DIO-120,
PCIe-DIO-96,
and PCIe-DIO-72
Digital I/O Card

USER MANUAL

FILE: PCIe-DIO-120.B1

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Chapter 1: Introduction

The PCIe-DIO-120 series are x1 lane PCI Express (PCIe) boards with 120, 96, or 72 digital I/O lines designed for use in a variety of Digital I/O (DIO) applications. They use the high speed PCIe bus to transfer digital data to and from the board. The FPGA based DIO emulates 8255 compatible chips in mode 0, making it easy to program. This also allows for simple migration from older ACCES' PCI-based DIO boards. Lastly, the x1 lane PCIe connector is very flexible and can be inserted into any x1, x4, x8, x16, or x32 PCIe slot.

Features

- 72, 96 and 120 channels of digital input/output
- IRQ generation from Port C bit 3
- All I/O lines are buffered on the card
- Four and eight bit ports independently selectable for I/O on each 24-bit group
- Jumper configurable pull-up / pull-down 10kΩ resistors on I/O lines
- Fused VCCIO supply available to user on each 50 pin header
- I/O ports globally tri-stateable through software
- Compatible with industry standard I/O racks like Grayhill, Opto 22, Western Reserve Controls, etc.

Applications

- Automatic Test Systems
- Security Systems, Energy Management
- Robotics
- Relay Monitoring and Control
- Parallel Data Transfer to PC
- Sensing switch closures or TTL, DTL, CMOS Logic
- Driving Indicator Lights or Recorders

Functional Description

This manual applies to Models 120, 96, and 72. The same circuit board is used for all three models. The board is populated for 120 bits, 96 bits, and 72 bits respectively.

Buffers

Each I/O line is buffered and capable of sourcing or sinking 32mA when VCCIO is configured for 5V. The board contains FPGA circuitry that emulates type 8255 mode 0 Programmable Peripheral Interface (GROUP) to provide a computer interface to digital I/O lines. Each group supports two 8-bit ports (A, B) and two 4-bit ports (CHi, CLo). Each port can be configured to function as either input or output latches. The I/O line buffers are configured automatically by hardware logic for input or output according to the GROUP Control Register direction software assignment. All DIO lines can be tristated as well using the corresponding software command.

Bias Resistors

Outputs of the I/O buffers are jumper configurable to be pulled up or down through 10kΩ resistor networks to VCCIO. There is a description in the Option Selection section of this manual that describes how to configure these on your card.

Interrupts

One digital I/O line of each group can be used to generate an interrupt with a rising edge at bit C3. Interrupts are enabled by software.

Wiring

I/O wiring connections are via 50-pin headers on the board. This provides compatibility with OPTO-22, Gordos, Potter & Brumfield, Western Reserve Controls, etc. module mounting racks. Every second conductor of the flat cables is grounded to minimize crosstalk between signals. If needed for external circuits, VCCIO power is available on each I/O connector at pin 49.

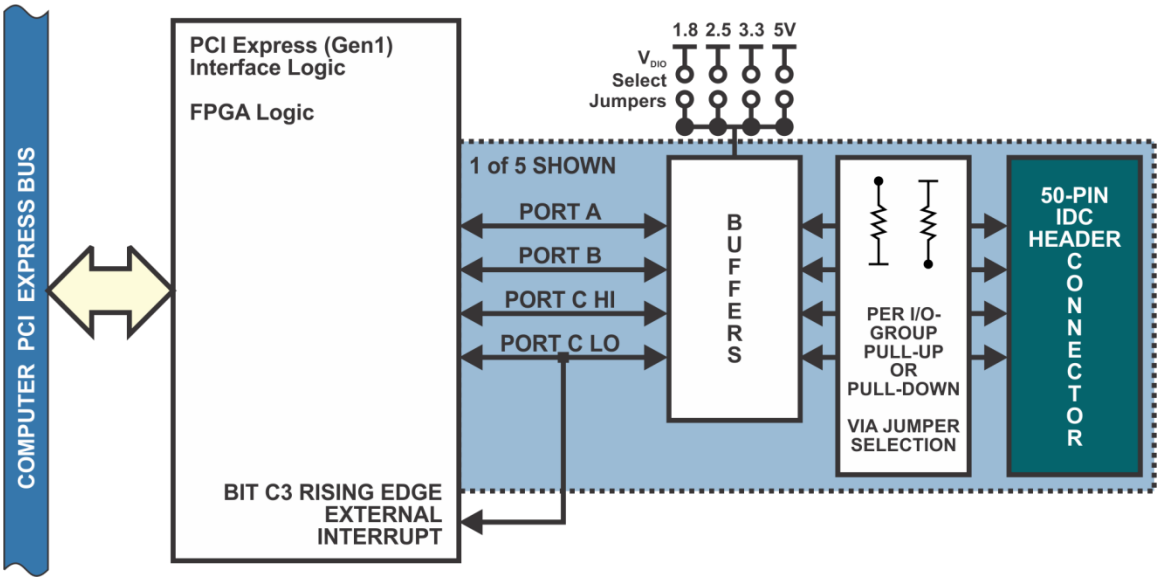


Figure 1-1: Block Diagram

Ordering Guide

PCIe-DIO-120	120 Channel Digital I/O Card
PCIe-DIO-96	96 Channel Digital I/O Card
PCIe-DIO-72	72 Channel Digital I/O Card

Model Options

-T	Extended operating temperature (-40° to +85°C)

Included with your board

The following components are included with your shipment. Please take time now to ensure that no items are damaged or missing.

DIO Board
Packing Slip

Optional Accessories

CAB50F-6	6’ ribbon cable with strain relieved 50 pin female connectors
STB-120CH	Large screw terminal board for PCIe-DIO-120 installed in T-Box
STB-96CH	Large screw terminal board for PCIe-DIO-96 installed in T-Box
STB-72CH	Large screw terminal board for PCIe-DIO-72 installed in T-Box
CAB50-6	6’ ribbon cable female 50 pin to 50 pin card edge connector

Chapter 2: Installation

A printed Quick-Start Guide (QSG) is packed with the card for your convenience. If you've already performed the steps from the QSG, you may find this chapter to be redundant and may skip forward to begin developing your application.

The software provided with this card is normally downloaded from the product page at accesio.com, or optionally on CD, and must be installed onto your hard disk prior to use. To do this, perform the following steps as appropriate for your operating system.

Configure Card Options via Jumper Selection

Before installing the card into your computer, carefully read Chapter 3: Option Selection of this manual, then configure the card according to your requirements. Our Windows based setup program can be used in conjunction with Chapter 3 to assist in configuring jumpers on the card, as well as provide additional descriptions for usage of the various card options.

CD Software Installation

The following instructions assume the CD-ROM drive is drive "D". Please substitute the appropriate drive letter for your system as necessary.

Windows

1. Place the CD into your CD-ROM drive.
2. The system should automatically run the install program. If the install program does not run promptly, click START | RUN and type D:\INSTALL, click OK or press Enter.
3. Follow the on-screen prompts to install the software for this board.

Linux

1. Please refer to linux.htm on the CD-ROM for information on installing under linux.

Caution! * ESD ***A single static discharge can damage your card and cause premature failure! Please follow all reasonable precautions to prevent a static discharge such as grounding yourself by touching any grounded surface prior to touching the card.***

Hardware Installation

1. Make sure to set switches and jumpers from either the Option Selection section of this manual or from the suggestions of SETTINGS.EXE.
2. Do not install card into the computer until the software has been fully installed.
3. Turn OFF computer power AND unplug AC power from the system.
4. Remove the computer cover.
5. Install I/O cables through the cutout in the mounting bracket, leaving one strain relief bar below the cables and setting the other bar aside along with the provided hex nuts. Plug all the cables onto their header connectors.
6. Install the second strain relief bar and tighten the hex nuts down firmly, but don't overtighten them.
7. Fish the ribbon cables through the open back plate next to the PCI Express slot you'll be plugging the card into, then carefully plug the card into the PCI Express expansion slot.
8. Inspect for proper fit of the card and tighten the bracket screw. Make sure that the card mounting bracket is properly screwed into place and that there is a positive chassis ground.
9. Replace the computer cover and turn ON the computer which should auto-detect the card (depending on the operating system) and automatically finish installing the drivers.
10. Run one of the provided sample programs that was copied to the newly created card directory (from the CD or downloaded from the product page) to test and validate your installation.

Chapter 3: Hardware Details

Refer to the illustrated setup program installed with the software package when reading this section of the manual. Also, refer to Figure 3-1, Option Selection Map.

External interrupts are accepted on pin 9 (Bit C3) of each I/O connector when enabled by software. The interrupt signal should be a rising edge and is latched.

As pointed out in Chapter 1 of this manual, outputs of the I/O buffers may be either pulled-up to VCCIO or pulled down to ground. You can configure these resistors per port.

VCCIO signaling levels are globally configured via jumper selection. Refer to the specifications chapter for signal levels for each possible selection.

The foregoing are the only manual setups necessary to use these cards. Input/Output selection is done via software, by writing to the GROUP Control Registers as described in the Programming section of this manual.

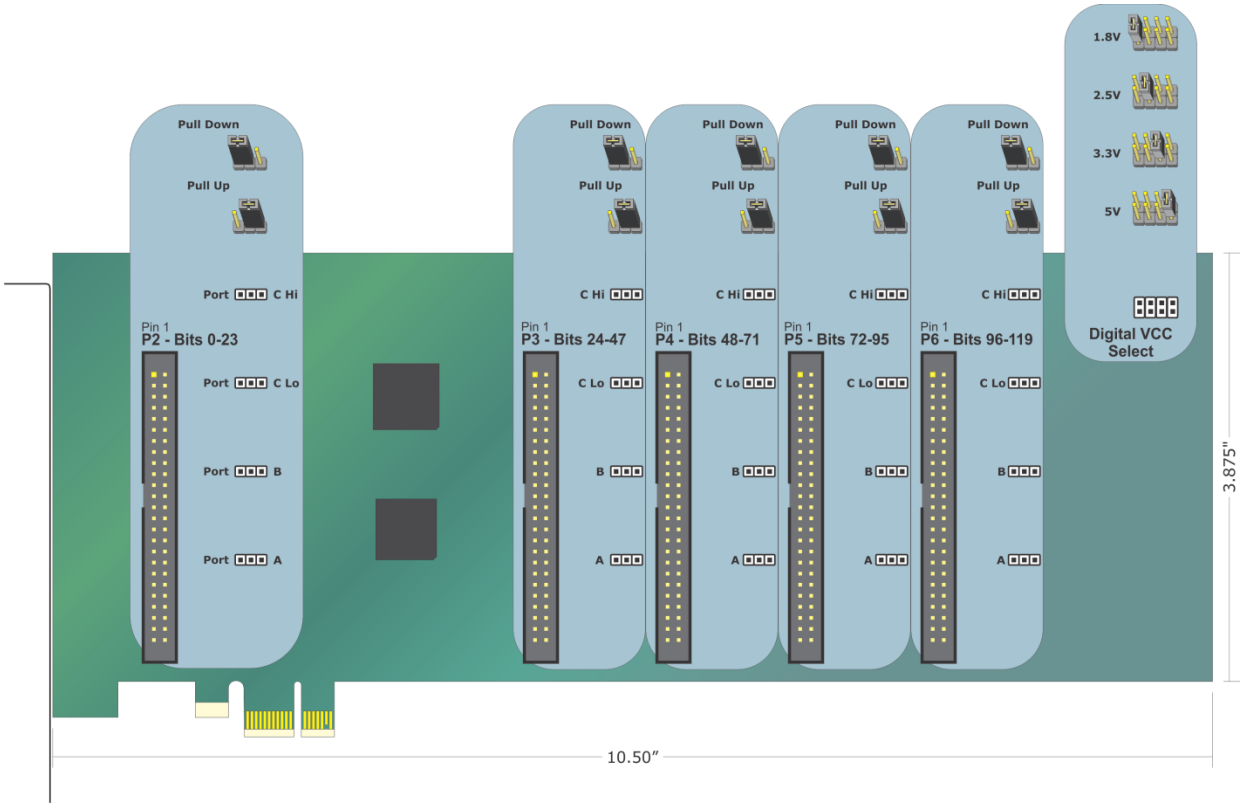


Figure 3-1: Option Selection Map

Chapter 4: Address Selection

These cards use one address space, and occupy 64 register locations. These are defined in the Port Address Selection Table in the Programming section of this manual.

PCI Express architecture is inherently plug-and-play. This means that the BIOS or Operating System determines the resources assigned to PCI Express cards rather than you selecting those resources with switches or jumpers. As a result, you cannot set or change the card's base address or IRQ level. You can only determine what the system has assigned.

To determine the base address that has been assigned, run the AIOWDMFind.EXE utility program provided. This utility will display a list of all of the cards detected on the PCI Express bus, the addresses assigned to each function on each of the cards, and the respective IRQs.

Alternatively, some operating systems can be queried to determine which resources were assigned. In these operating systems, you can use either AIOWDMFind (Windows 7 or later) PCIFind or the Device Manager utility from the System Properties Applet of the control panel. The card is installed in the Data Acquisition class of the Device Manager list. Selecting the card, clicking Properties, and then selecting the Resources Tab will display a list of the resources allocated to the card.

If you want to determine the base address and IRQ yourself, use the following information.

The Vendor ID for these cards is 494F. (ASCII for "IO")

The Device ID for the 72 is 0C6A.
The Device ID for the 96 is 0C71.
The Device ID for the 120 is 0C79.

Chapter 5: Programming

The 120/96/72 cards are I/O mapped devices that are easily configured from any language.

Developing Your Own Software

Four register locations are required per 24-bit group. Thus, a total of 20 register locations are used by the 120 for addressing groups 0 through 4. The 96 uses a total of 16 registers for groups 0 through 3, and the 72 uses 12 registers for groups 0 through 2.

Address	Assignment	Operation
Base Address	PA Group 0	Read/Write
Base Address +1	PB Group 0	Read/Write
Base Address +2	PC Group 0	Read/Write
Base Address +3	Control Port 0	Write Only
Base Address +4	PA Group 1	Read/Write
Base Address +5	PB Group 1	Read/Write
Base Address +6	PC Group 1	Read/Write
Base Address +7	Control Port 1	Write Only
Base Address +8	PA Group 2	Read/Write
Base Address +9	PB Group 2	Read/Write
Base Address +A	PC Group 2	Read/Write
Base Address +B	Control Port 2	Write Only
Base Address +C	PA Group 3	Read/Write
Base Address +D	PB Group 3	Read/Write
Base Address +E	PC Group 3	Read/Write
Base Address +F	Control Port 3	Write Only
Base Address +10	PA Group 4	Read/Write
Base Address +11	PB Group 4	Read/Write
Base Address +12	PC Group 4	Read/Write
Base Address +13	Control Port 4	Write Only
Base Address +1C	DIO Buffer Enable	Read/Write
Base Address +1E	Clear/Disable Interrupts	Write Only
Base Address +1F	Clear/Enable Interrupts	Write Only

Table 6-1: Address Registry Table

The cards are designed to emulate each GROUP wherein:

a. There are two 8-bit ports (A and B) and two 4-bit ports (C Hi and C Lo).
b. Any port can be configured as an input or an output.
c. Outputs are latched.
d. Inputs are not latched.
e. The card is initialized in the input mode

Each GROUP contains a control register. This Write-only, 8-bit register is used to set the mode and direction of the ports. At Power-Up or Reset, all I/O lines are set as inputs. Each GROUP should be configured during initialization by writing to the control registers even if the ports are going to be used as inputs. Output buffers are automatically set by hardware logic according to the control register states. Control registers are located at base addresses +3, +7, +B, +F, and +13. Bit assignments in each of these control registers are as follows:

Bit	Assignment	Function
D0	Port C Lo (C0-C3)	1 = Input, 0 = Output
D1	Port B	1 = Input, 0 = Output
D2	N/A	N/A
D3	Port C Hi (C4-C7)	1 = Input, 0 = Output
D4	Port A	1 = Input, 0 = Output
D5,D6	N/A	N/A
D7	Mode Set (see note 1)	Scratchpad

Table 6-2: Control Register Bit Assignments

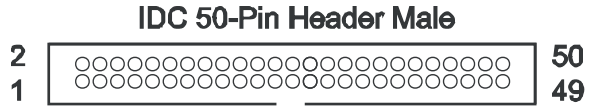
Note 1: This bit is a read/write scratchpad. For maximum compatibility with the 8255, always set this bit (to 1).

Base Address +1C (read/write) DIO Buffer Enable / Disable (tri-state)

At power-up or reset, all DIO buffers on the card are enabled. To disable the DIO buffers, write a one to bit 0. To re-enable the DIO buffers, write a zero to bit 0. When buffers are disabled the pins are tri-stated and biased by the state of the pull up or down configuration jumpers. A read of bit 0 returns the enable / disable status.

Chapter 6: Connector Pin Assignments

For I/O connections, 50-pin headers are provided on the cards; one for each group of 24 I/O lines. Mating connectors are TE Connectivity AMP 1-1658621-0 or equivalent.



Assignment	Pin		Assignment	Pin
Port C Hi PC7	1		All Even numbered pins are Ground	2
Port C Hi PC6	3			4
Port C Hi PC5	5			6
Port C Hi PC4	7			8
Port C Lo PC3*	9			10
Port C Lo PC2	11			12
Port C Lo PC1	13			14
Port C Lo PC0	15			16
Port B PB7	17			18
Port B PB6	19			20
Port B PB5	21			22
Port B PB4	23			24
Port B PB3	25			26
Port B PB2	27			28
Port B PB1	29			30
Port B PB0	31			32
Port A PA7	33			34
Port A PA6	35			36
Port A PA5	37			38
Port A PA4	39			40
Port A PA3	41			42
Port A PA2	43			44
Port A PA1	45			46
Port A PA0	47			48
Fused VCCIO	49			50

Table 6-1: Connector Pin Assignments

* This line is an I/O port and also a User Interrupt.

Chapter 7: Specifications

Digital I/O

Lines	120; (5 Groups) Ports A, B, CLo and CHi
Type	Emulates 8255 compatible chips in Mode 0
Logic Level	VCCIO
Pull-up/down	10k ohm, jumper selectable

VCCIO

Logic Levels	**5V**	
Low Inputs	≤ 1.5V	≤ 2uA
High Inputs	≥ 3.5V	≤ 2uA
Low Outputs	≤ 0.55V	32mA
High Outputs	≥ 3.8V	32mA
Logic Levels	**3.3V**	
Low Inputs	≤ 0.8V	≤ 2uA
High Inputs	≥ 2.0V	≤ 2uA
Low Outputs	≤ 0.55V	24mA
High Outputs	≥ 2.4V	24mA
Logic Levels	**2.5V**	
Low Inputs	≤ 0.7V	≤ 2uA
High Inputs	≥ 1.7V	≤ 2uA
Low Outputs	≤ 0.5V	8mA
High Outputs	≥ 1.9V	8mA
Logic Levels	**1.8V**	
Low Inputs	≤ 0.63V	≤ 2uA
High Inputs	≥ 1.17V	≤ 2uA
Low Outputs	≤ 0.45V	4mA
High Outputs	≥ 1.2V	4mA

Environmental

Operating Temperature	0° to 70°C optional -40° to +85°C
Storage Temperature	-55° to +150°C
Humidity	5% to 95% RH, w/o condensation
Card Dimensions	length – 10.5" Height - 4.2" seated

Customer Comments

If you experience any problems with this manual or just want to give us some feedback, please email us at: ***manuals@accesio.com.*** Please detail any errors you find and include your mailing address so that we can send you any manual updates.

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