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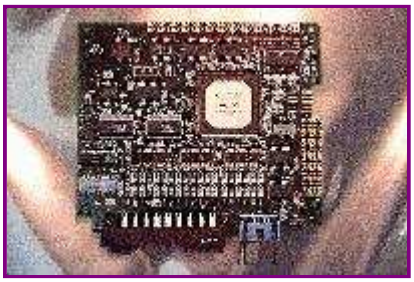
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Access DYNAMICS Incorporated

Product Data

DM-17 TTL/FPDP I/O Module



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Summary of Features

* 16 or 32 Bit TTL I/O
* Front Panel Data Port Compatible
* In-circuit Programmable Logic

Typical DM-17 applications:

* General Data Acquisition
* Data Source Simulation
* VSB to VSB data links

General Description

The DM-17 is an I/O Module for the DC-1 VSB I/O Controller. The heart of the DM-17 is an Altera EPM9480-15 complex programmable logic device (CPLD) which is connected to the DC-1 processor and

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FIFO data buffer interfaces and to TTL transceivers on the I/O connector. The exact functionality is set by the programming of the CPLD. Clock resources on the DM-17 include a socketed crystal oscillator, the DC-1 processor clock and the VMEbus SYSCLK (16MHz).

The DM-17 can be configured to be compatible with the Front Panel Data Port standard (VIAT 17-199X) for both input and output data transfers. An auxilliary connector is provided for general purpose control and external triggering.

The CPLD is an Altera EPM9480-15 device and is programmed on the DM-17 through a special JTAG test and programming connector. Once the CPLD is programmed the device retains its logic pattern when power is removed from the board.

Specifications

Data Signals -

32 TTL data lines organized as either 32 I/Olines or two sets of 16 data lines with independent direction controls

Programmable Logic -

CPLD - Altera EPM9480RC240-15

Processor Interface -

16 bit data bus, 8 bit address bus with module select line, processor interrupt, dual timers, module reset, module trigger

FIFO Interface -

32 bit data bus, four FIFO write strobes, four FIFO read strobes, full complement of FIFO status signals

I/O Connectors -

Main I/O, 80 pin, KEL 8831E-080-170L
Auxilliary I/O, 20 pin header, T&B Ansley 501-1007ES

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