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SDK60 User Guide

For Revision 3

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Preface

About this Guide

The Achronix Speedster Development Kit for the SPD60 (SDK60) delivers a practical platform for designers to evaluate Speedster performance and IP. This guide provides details on capabilities and use of the board. Both features available for customer use and those that are fixed (no explicit user control) are covered.

This guide consists of the following chapters:

Chapter 1 – "SDK60 Overview" provides an overview of the SDK 60.

Chapter 2 – "General Description" covers details of the SDK60.

Chapter 3 – "LEDs, Buttons, Switches and Jumpers" supplies details on the functions of the various LEDs, push buttons, switches, and jumpers on the SDK60.

Chapter 4 – "Interfaces" details the various high-speed interfaces of the on-board FPGA, accessible on the SGDK60.

Chapter 5 – "SDK60 Clocking" covers the clocking structure of the board and how the user can set the various clock sources.

Chapter 6 – "AVR Controller" describes the functionality of the on-board microcontroller.

Chapter 7 – "Targeting a Design to the SDK60" describes how a user can target an evaluation design to the SDK60.

This guide does not cover any of the Achronix extension cards currently in development. These extension cards will be covered later by separate user guides.

Reference Documents

Speedster FPGA Family Datasheet (DS001)

ACE User Guide (UG001)

ACE Installation and Licensing Guide (UG002)

ACE Quick Start Guide (UG003)

Bitporter User Guide (UG004)

SDK60 Quick Start Guide (UG005)

Conventions Used in this Guide

Item	Format	Examples
Command-line entries	Formatted with the Courier bold font face.	`$ Open top_level_name.log`
File Names	Formatted with the Courier font face.	`filename.ext`
GUI buttons, menus and radio buttons	Formatted with the Helvetica bold font face.	Click **OK** to continue. **File → Open**
Variables	Formatted with italic emphasis.	*design_dir*`/output.log`
Window and dialog box headings and sub-headings	Heading formatted in quotation marks.	Under "Output Files," select ...
Window and dialog box names	Initial caps.	From the Add Files dialog box, ...

Chapter 1 – SDK60 Overview

The Achronix Speedster Development Kit for the SPD60 (SDK60) delivers a practical platform for designers to evaluate Speedster performance and IP. The board allows designers to evaluate the high-performance Speedster features at speed, including logic, RAMs, multipliers, SerDes, programmable I/Os and Achronix' patented picoPIPE™ acceleration technology.

The SDK60 can also be used for interoperability and homologation testing, as well as SerDes performance evaluation for most of the 10G, 5G channels/lanes. In addition, the board is designed to allow the user to easily begin application development in advance of their own hardware development.

The board can operate stand-alone or as a PCI Express extender card, connecting via a PCIe cable, plus features a rich selection of on-board memories and data interfaces. The kit comes complete with development tools and a collection of standard reference designs.

Features

Off-Chip Memory

- DDR2 (128M × 72)
- DDR3 (128M × 8)
- RLDRAM (16M × 18)
- QDRII+ (4M × 18)

SerDes Interfaces

- Direct SerDes access (SMA connectors)
- x8 PCI Express socket connector
- x1 PCI Express socket connector
- 10 Gigabit Ethernet (XAUI module)
- Gigabit Ethernet (SGMII)
- Small Form-Factor Pluggable (SPF) optical transceiver modules
- Advanced Mezzanine Card (AMC) interface

Other High-Speed Data Interfaces

- Three 96-pin high-speed extension headers for daughter cards such as video (HDMI/DVI) and signal processing (ADC/DAC)

Extensions to Enable use of Off-the-Shelf Cards

- AMC connector
- PCI Mezzanine Card (PMC) connector

Other Headers (Extensions)

- Mictor 32-pin header, and three 6-pin headers

Control and Status

- DIP and pushbutton switches
- LEDs

Clocks

- On-board crystals and oscillators
- Connectors for external clock signals
- Clock Generators (to derive clocks from fundamental frequencies).
- Device Configuration Options
- IEEE 1149.1 JTAG
- SPI Flash
- CPU

Chapter 2 – General Description

The SDK60 board is a PCIe long form factor board (312 mm × 312 mm). In addition, the board supports various daughter cards via its extension connectors (PMC, AMC, High-Speed Extension). These interfaces enable the SDK60 to have additional communication and networking interfaces, as well as expansion for processor or storage cards -- allowing the SDK60 board to act as a complete system running embedded software.

Use Modes

Standalone

In standalone mode, power is supplied via an external power adapter (supplied). All the other functions are independently controlled on the board and by the FPGA.

In System

The SDK60 can be slaved to a host system via either its two PCI Express interfaces:

- A PCIe Gen2 x8 socket-connector interface (J84), providing an effective data bandwidth of 64 Gbps (5 GHz Tx, Rx = 10 GHz).

  Note: *10 GHz without 8B/10B encoding equals 8 Gbps data).*

- An alternative (secondary) PCIe x1 socket-connector interface (J83) is available on the opposite board edge.

The board can be connected to the host system using one of two PCIe extension cables:

- PCIEC-098-0500-EC-EC-P – PCIe x8 male to PCIe x8 male cable
- PCIEC-036-0500-EC-EC-P – PCIe x1 male to PCIe x1 male cable

Supplying Power

The board is powered by the included power supply via a 4-pin connector (J41), suppling +5V and +12V (**Figure 2-1**). Additional on-board power supplies (U21 to U36) regulate these rails to supply the board with 1.0V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V. An additional 4-pin power-supply connector (J42) is available for applications requiring additional power (for example, when additional peripherals are used).

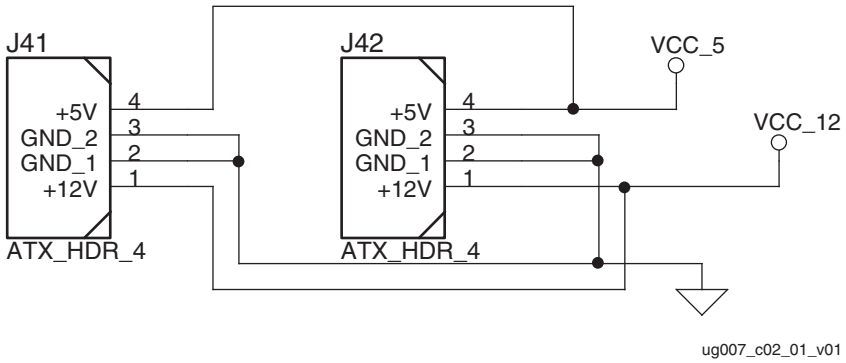


Figure 2-1: *Power Supply Connectors J41 and J42*

On-Board Memory

Four types of memory are available on board, but off chip.

- DDR2 (128M × 72) as a small-outline clocked DIMM (SOCDIMM) via a socket at U11
- DDR3 (128M × 8) SDRAM at location U10
- RLDRAM (16M × 18) at location U3
- QDRII+ (4M × 18) SRAM at location U2

Each of these blocks of memory are accessible by the FPGA (see **Chapter 4 – "Interfaces"** for details of the interface).

On-Board Controller

The SDK60 comes equipped with an on-board controller, the Atmel ATmega1280 AVR microcontroller. This microcontroller comes equipped with firmware that:

- Controls power sequencing of the board and any connected peripherals
- Measures the temperature captured via the on-chip temp diode of the SPD60.
- Measures core power consumed by the SPD60.

See **Chapter 6 – "AVR Controller"** for more details.

SDK60 Board

Figure 2-2 provides an annotated graphic of the SDK60 board with annotations for the key components referred to in this guide. These components are described in **Table 2-1**.

Table 2-1: *SDK60 Key Components*

Designator	Name	Description
DS11	Configuration done LED	Indicates the completion of a configuration cycle.
DS12	Configuration status LED	Indicates the start of a configuration cycle.
DS13	User LED	Controlled via SPD60
DS14	User LED	Controlled via SPD60

Table 2-1: *SDK60 Key Components (Continued)*

Designator	Name	Description
DS15	User LED	Controlled via SPD60
DS16	User LED	Controlled via SPD60
J12	AMC connector	Advanced Mezzanine Card interface
J41	Power supply connector	Main power connector
J49	JTAG connector	JTAG cable connector for Bitporter
J76	LCD connector	Connector for output to LCD display module.
J82	Fan power	Heatsink fan power supply.
J83	PCIe x1	Socket connector for PCIe x1 interface.
J84	PCIe x8	Socket connector for PCIe x8 interface
J86	RS232 Mode	Sets the mode for the RS-232 connection at P1
JN1	PMC connectors	PCI Mezzanine Card interface
JN2		
JN3		
P1	RS-232 DB-9 connector	RS-232 interface
S4	User pushbutton	Input to SPD60
S5	User pushbutton	Input to SPD60
S6	User pushbutton	Input to SPD60
S7	User pushbutton	Input to SPD60
U2	QDRII+ SRAM	P/N CY7C1563V18
U3	RLDRAM	P/N MT49H16M18
U10	DDR2 SDRAM	P/N MT41J128M8
U11	SOCDIMM socket	DDR2/QDR2 200-pin SODIMM socket

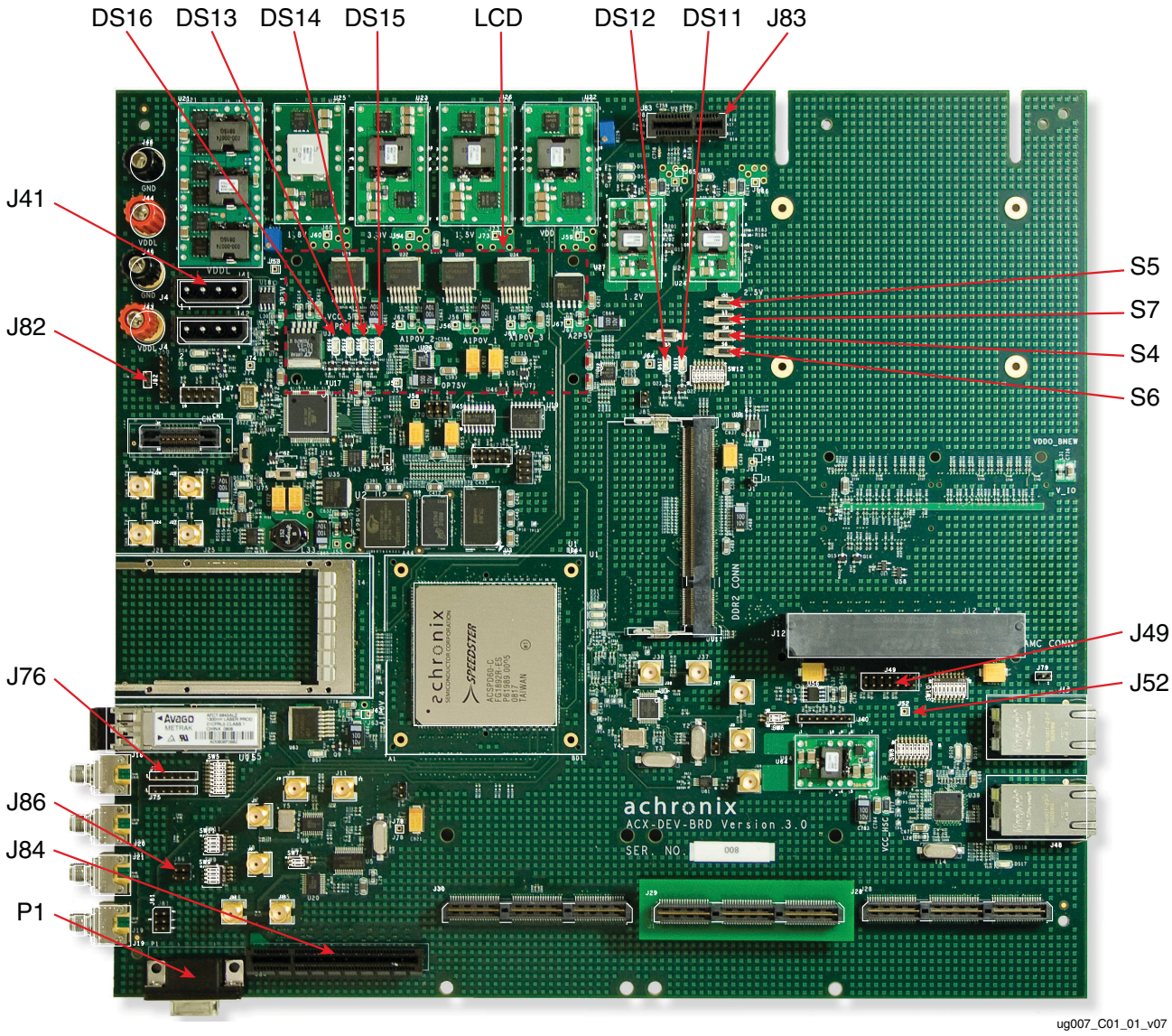


Figure 2-2: *SDK60 Development Board*

Setting Up the Board

Setting up the board in standalone mode is covered in *SDK60 Quick Start Guide* (UG005).

Configuring the Board

SDK60 supports three different configuration modes:

- Serial configuration mode with transition to JTAG.
- JTAG only mode.
- CPU mode with transition JTAG mode.

Refer to **"Configuring the Board"** in **Chapter 7 – Targeting a Design to the SDK60** for details.

Chapter 3 – LEDs, Buttons, Switches and Jumpers

The SDK60 comes equipped with a variety of LEDs, push buttons, and DIP switches. Some of these items are connected to the FPGA for design use, while others are involved in board configuration.

LEDs

User LEDs

Table 3-1 lists the LEDs that are controllable via the FPGA (schematic is shown in **Figure 3-1**).

Table 3-1: *User LEDs*

Designator	Purpose	Comments
DS13	User applications	Controlled via P_D33N_B1 (R34) of SPD60 (U1).
DS14	User applications	Controlled via P_D34N_B1 (T34) of SPD60 (U1).
DS15	User applications	Controlled via P_D35P_B1 (R35) of SPD60 (U1).
DS16	User applications	Controlled via P_D35N_B1 (T35) of SPD60 (U1).

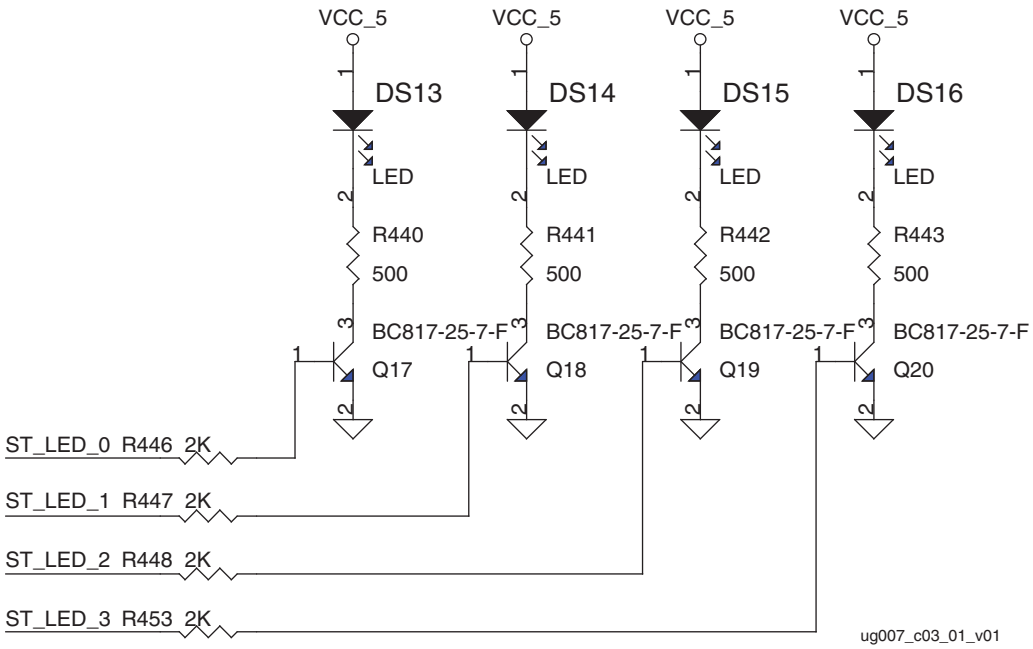


Figure 3-1: *User LED Connection Schematic*

Power and Status LEDs

Table 3-2 list the various power and status indicators on SDK60.

Table 3-2: *Power and Status LEDs*

Designator	Purpose	Comments
Power Indicators		
DS4	V_{DDL}	Indicates presence of V_{DDL} (?V).
DS5	V_{DD}	Indicates presence of V_{DD} (?V).
DS6	1.2V	Indicates presence of 1.2V supply.
DS7	1.5V	Indicates presence of 1.5V supply.
DS8	1.8V	Indicates presence of 1.8V supply.
DS9	2.5V	Indicates presence of 2.5V supply.
DS10	3.3V	Indicates presence of 3.3V supply.
Status Indicators		
DS1(1)	GIgabit Ethernet status (RGMII)	Tied to LED_0 of Marvel 88E1116 (U14).(2)
DS2(1)		Tied to LED_2 of Marvel 88E1116 (U14).(2)
DS3(1)		Tied to LED_1 of Marvel 88E1116 (U14).(2)
DS11	Configuration done	Indicates the completion of a configuration cycle. Tied to CONFIG_DONE (AW32) of SPD60 (11).
DS12	Configuration status	Indicates the start of a configuration cycle. Tied to CONFIG_STATUS (AU32) of SPD60 (11).
DS17(3)	GIgabit Ethernet status (SGMII)	Tied to STATUS0 of Marvel 88E1114 (U39).(4)
DS18(3)		Tied to STATUS1 of Marvel 88E1114 (U39).(4)
DS19(3)		Tied to LOS of Marvel 88E1114 (U39).(4)
DS20		Tied to INT of Marvel 88E1114 (U39).(4)
DS21	XAUI Status	X2 MSA link alarm status interrupt output. LED ON indicates that the status flag is triggered.

Notes:

1. See also **Figure 4-3**, page 19.
2. The function of these LEDs is programmable. Refer to the *Marvell 88E1116 Datasheet* for details.
3. See also **Figure 4-5**, page 21.
4. The function of these LEDs is programmable. Refer to the *Marvell 88E1114 Datasheet* for details

Push Buttons

User Push Buttons

Table 3-4 lists the user push buttons for SDK60 (schematic is shown in Figure 3-2).

Table 3-3: *SDK60 User Push Buttons*

Designator	Purpose	Comments
S4	User applications	Controls P_D35P_B3 (AK44) of SPD60 (U1)
S5	User applications	Controls P_D35N_B3 (AK43) of SPD60 (U1)
S6	User applications	Controls P_D34P_B3 (AK41) of SPD60 (U1)
S7	User applications	Controls P_D34N_B3 (AK42) of SPD60 (U1)

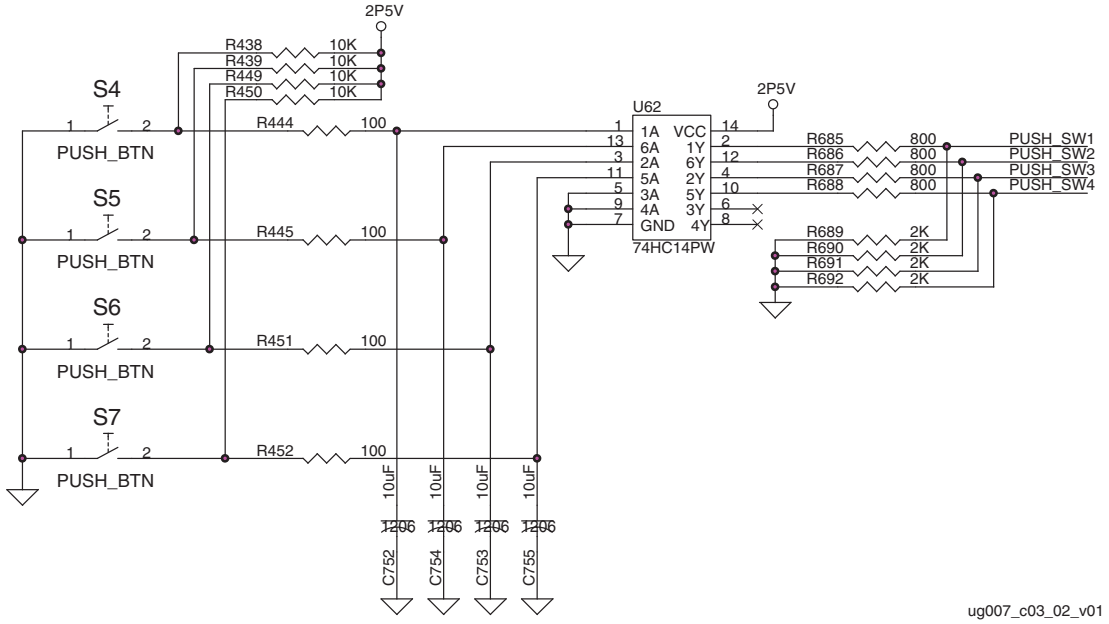


Figure 3-2: *Push Button Connection Schematic*

Resets

Table 3-4 lists the resets for SDK60.

Table 3-4: *SDK60 Reset Buttons*

Designator	Purpose	Comments
S2	AVR reset	Used to reset AVR processor. See Chapter 6 – "AVR Controller" for details.
S3	Configuration reset	Clears the configuration memory of the FPGA. Controls CONFIG_RSTN (AU29) of SPD60 (U1).

DIP Switches

User Switches

FPGA Switch 1 (SW5)

Eight position switch taking an FPGA input Low (on) or pulled High via a 10 kΩ resistor to 3.3V (off).

Table 3-5: *FPGA Switch (SW5)*

Position	Connection
1	Tied to P_D37N_BNW (F24) of SPD60 (U1).
2	Tied to P_D37P_BNW (E24) of SPD60 (U1).
3	Tied to P_D36N_BNW (F25) of SPD60 (U1).
4	Tied to P_D36P_BNW (G25) of SPD60 (U1).
5	Tied to P_D35N_BNW (G24) of SPD60 (U1).
6	Tied to P_D35P_BNW (H24) of SPD60 (U1).
7	Tied to P_D34N_BNW (J25) of SPD60 (U1).
8	Tied to P_D34P_BNW (J24) of SPD60 (U1).

Configuration Switches

Clock Select Switch (SW6)

See **"Clock Select Switch (SW6)"** in **Chapter 5 – SDK60 Clocking** for details.

Diff Clock Stop and Spread Spectrum Switch (SW7)

See **"Diff Clock Stop and Spread Spectrum Switch (SW7)"** in **Chapter 5 – SDK60 Clocking** for details.

Bypass and N-Divider Switch (SW8)

See **"Bypass and N-Divider Switch (SW8)"** in **Chapter 5 – SDK60 Clocking** for details.

Clock Frequency Select Switch (SW9)

See **"Clock Frequency Select Switch (SW9)"** in **Chapter 5 – SDK60 Clocking** for details.

M-Divider Switch (SW10)

See **"M-Divider Switch (SW10)"** in **Chapter 5 – SDK60 Clocking** for details.

Clock Source Selector Switch (SW11)

See **"Clock Source Selector Switch (SW11)"** in **Chapter 5 – SDK60 Clocking** for details.

FPGA Configuration (SW12)

Eight-position switch used to control the configuration settings of the FPGA. Used in conjunction with **"Configuration Mode (J70)."**

Note: *A switch setting of ON ties the signal to GND; and OFF allows the signal to be pulled High via 10 kΩ resistor to* V_{DDO_CFG}.

Table 3-6: *FPGA Configuration (SW12) Settings*

Position	Purpose	Comments
1	FPGA configuration mode select	Configuration mode selection inputs to define the FPGA configuration unit (FCU) mode of operation: • ON:ON:OFF – SPI x1 configuration mode (SDK60 default) • ON:OFF:ON – SPI x4 configuration mode • OFF:ON:ON – CPU configuration mode • ON:ON:ON – Unconfigured
2		
3		
4	Configuration SYS_CLK bypass	Pin statically enabling the bypass of the internal SYS_CLK (the default clock for the FCU). The default setting for the SDK60 is off (bypass enabled).
5	Configuration clock select	Pin controlling whether the FCU clock is sourced from the TCK input or the CPU_CLK input when CONFIG_SYSCLK_BYPASS is asserted active-High thus enabling the bypass of the internal SYS_CLK: • ON – CPU_CLK is selected (SDK60 default) • OFF – TCK is selected
6	Program enable	Pin enabling the programming of the eFuse for the AES encryption keys. • ON – disabled (default) • OFF – enabled
7	Reserved	Factory use.
8	–	Not used.

Jumpers

AVR Control (J51)

A jumper across J51 assert a power-on-reset signal for AVR microcontroller.

Configuration Mode (J70)

J70 is used to tell the AVR controller the configuration mode of the FPGA, as well as program the on-board EEPROM. Used in conjunction with **"FPGA Configuration (SW12)."**

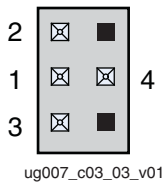


Figure 3-3: *Configuration Mode Jumper (J70)*

Table 3-7: *Configuration Mode (J70) Settings*

Jumper Settings	Programming Mode
None	JTAG mode
Across pins 1 and 2	EEPROM programming. Allows the EEPROM to programmed via **"FPGA SPI (J71)."**
Across pins 1 and 3	Serial mode
Across pins 1 and 4	CPU mode

PMC Enable (J79)

A jumper across J79 sets the value of the signal M66EN.

Table 3-8: *PMC Signal M66EN (J79) Settings*

Jumper Settings	Programming Mode
None	M66EN tied to GND.
Across pins 1 and 2	M66EN set High.

High-Speed Expansion Slot Voltage Select (J80)

A jumper across J80 sets the voltage (V_{CC_HSC}) of the high-speed expansion slot connectors (see **"High-Speed Expansion Connectors (J28, J29, and J30)"** in **Chapter 4 – Interfaces**). This voltage is suppled by U64.

The jumper configuration is identical to **Figure 3-3**.

Table 3-9: *High-Speed Expansion Slot Voltage Select (J80) Settings*

Jumper Settings	Programming Mode
None	0.8V (not recommended)
Across pins 1 and 2	1.2V
Across pins 1 and 3	2.5V
Across pins 1 and 4	3.3V

PCIe Data-Width Configuration (J81)

Table 3-10: *PCIe Data-Width Configuration*

Jumper Settings	Data Width
None	–
Across pins 1 and 2	×1 width selection
Across pins 1 and 3	×4 width selection
Across pins 1 and 4	×8 width selection

Heat Sink Fan Power Connector (J82)

Table 3-11: *Heat Sink Fan Power Connector (J82)*

Pin	Connection
1	12V
2	GND

RS-232 Mode Select (J86)

A jumper across J86 sets the operating mode of the RS-232 interface (see **"RS-232 Interface (P1),"** on page 47), and which type of cable must be used for connecting to the board.

Table 3-12: *RS-232 Mode Select (J86) Settings*

Jumper Settings	RS-232 Mode
Across pins 1 and 2	Sets SDK60 as DCE (standard cable)
Across pins 3 and 4	
Across pins 1 and 3	Sets SDK60 as DTE (null-modem cable)(1)
Across pins 2 and 4	

Notes:
1. Default setting of board when shipped.

Chapter 4 – Interfaces

Arrayed around the SPD60 are a number of interfaces (**Figure 4-1**), ranging from very-high speed (10 Gigabit Ethernet and OC48), expansion interfaces (PCIe, AMC and PMC), to standard speed interfaces using general-purpose I/Os. All of these interfaces take advantage of the wide range of resources available in the SPD60.

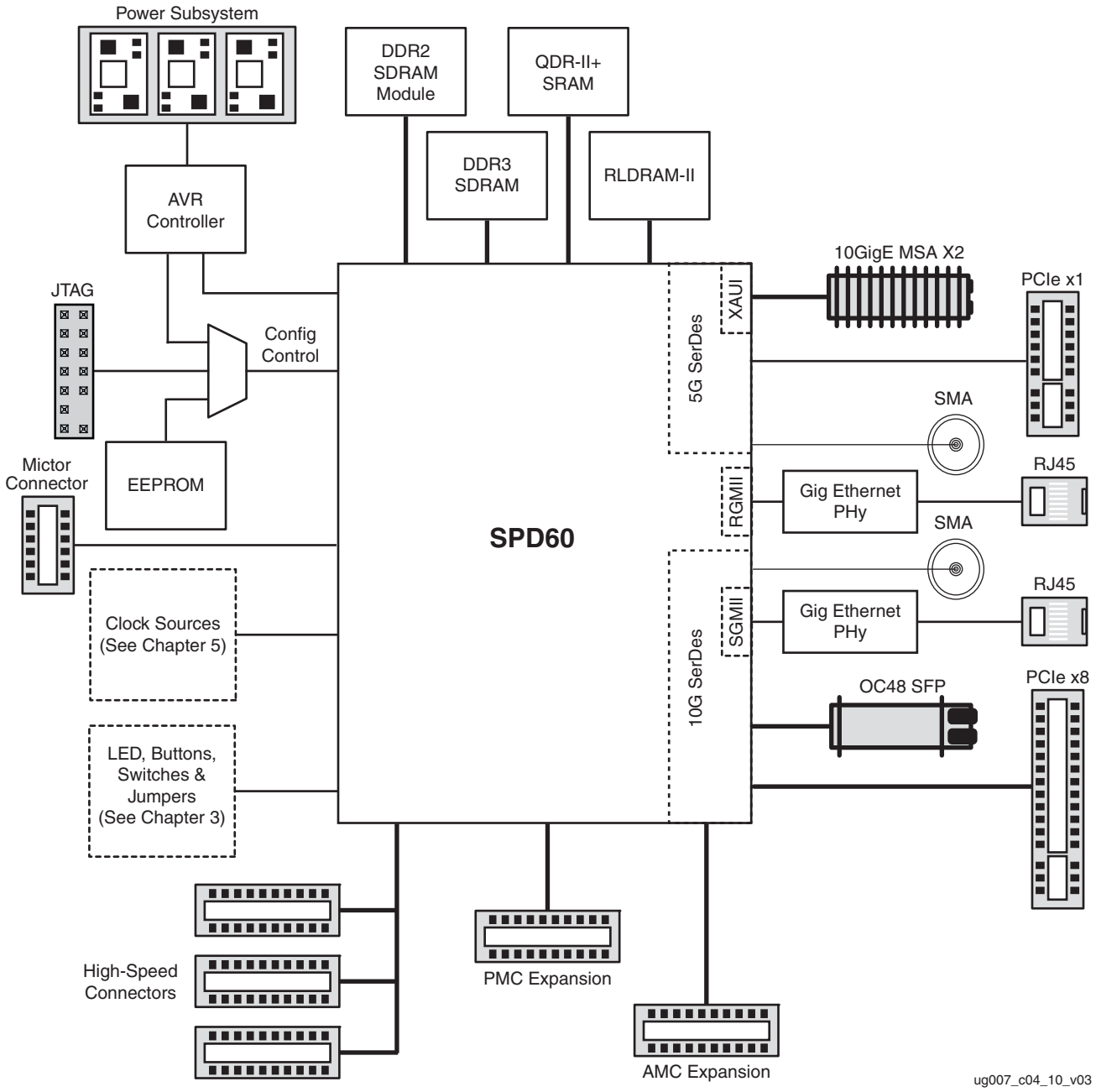


Figure 4-1: *SDK60 Interfaces for the SPD60*

Control Interfaces

PCIe x8 Socket Connector (J84)

PCIe x8 socket connector at J84 can serve as the primary interface to the host system. SDK60 can be tethered to the host system via a cable. This connector ties directly to the PCIe capable I/O of the FPGA.

Table 4-1: *PCIe x8 Connector (J84)*

Pin	Signal	Connection
A1	PRSNT1_N	Tied to J81 (pin 1).
A11	PERST_N	Tied to P_D0P_BSW (AP30) of SPD60 (U1).
B5	SMCLK	–
B6	SMDAT	–
x1		
A16	PER0P	Tied to P_6P5GD_LN3_RXP_I (BD6) of SPD60 (U1).
A17	PER0N	Tied to P_6P5GD_LN3_RXM_I (BD5) of SPD60 (U1).
B14	PET0P	Tied to P_6P5GD_LN3_TXP_O (BC6) of SPD60 (U1).
B15	PET0N	Tied to P_6P5GD_LN3_TXM_O (BC7) of SPD60 (U1).
B17	PRSNT2_N_X1	Tied to J81 (pin 2).
x4		
A21	PER1P	Tied to P_6P5GD_LN2_TXP_O (BC8) of SPD80 (U1)
A22	PER1N	Tied to P_6P5GD_LN2_TXM_O (BC9) of SPD80 (U1)
A25	PER2P	Tied to P_6P5GD_LN1_TXP_O (BC12) of SPD80 (U1)
A26	PER2N	Tied to P_6P5GD_LN1_TXM_O (BC13) of SPD80 (U1)
A29	PER3P	Tied to P_6P5GD_LN0_TXM_O (BC15) of SPD80 (U1)
A30	PER3N	Tied to P_6P5GD_LN0_TXP_O (BC14) of SPD80 (U1)
B19	PET1P	Tied to P_6P5GD_LN2_RXP_I (BD10) of SPD80 (U1)
B20	PET1N	Tied to P_6P5GD_LN2_RXM_I (BD9) of SPD80 (U1)
B23	PET2P	Tied to P_6P5GD_LN1_RXP_I (BD12) of SPD80 (U1)
B24	PET2N	Tied to P_6P5GD_LN1_RXM_I (BD11) of SPD80 (U1)
B27	PET3P	Tied to P_6P5GD_LN0_RXP_I (BD16) of SPD80 (U1)
B28	PET3N	Tied to P_6P5GD_LN0_RXM_I (BD15) of SPD80 (U1)
B31	PRSNT2_N_X4	Tied to J81 (pin 3).
x8		
A35	PER4P	Tied to P_6P5GC_LN3_TXP_O (BC18) of SPD80 (U1)
A36	PER4N	Tied to P_6P5GC_LN3_TXM_O (BC19) of SPD80 (U1)
A39	PER5P	Tied to P_6P5GC_LN2_TXP_O (BC20) of SPD80 (U1)
A40	PER5N	Tied to P_6P5GC_LN2_TXM_O (BC21) of SPD80 (U1)
A43	PER6P	Tied to P_6P5GC_LN1_TXP_O (BC24) of SPD80 (U1)
A44	PER6N	Tied to P_6P5GC_LN1_TXM_O (BC25) of SPD80 (U1)

Table 4-1: *PCIe x8 Connector (J84) (Continued)*

Pin	Signal	Connection
A47	PER7P	Tied to P_6P5GC_LN0_TXP_O (BC27) of SPD80 (U1)
A48	PER7N	Tied to P_6P5GC_LN0_TXM_O (BC26) of SPD80 (U1)
B33	PET4P	Tied to P_6P5GC_LN3_RXP_I (BD18) of SPD80 (U1)
B34	PET4N	Tied to P_6P5GC_LN3_RXM_I (BD19) of SPD80 (U1)
B37	PET5P	Tied to P_6P5GC_LN2_RXP_I (BD22) of SPD80 (U1)
B38	PET5N	Tied to P_6P5GC_LN2_RXM_I (BD21) of SPD80 (U1)
B41	PET6P	Tied to P_6P5GC_LN1_RXP_I (BD24) of SPD80 (U1)
B42	PET6N	Tied to P_6P5GC_LN1_RXM_I (BD23) of SPD80 (U1)
B45	PET7P	Tied to P_6P5GC_LN0_RXP_I (BD28) of SPD80 (U1)
B46	PET7N	Tied to P_6P5GC_LN0_RXM_I (BD27) of SPD80 (U1)
B48	PRSNT2_N_X8	Tied to J81 (pin 4).

PCIe x1 Socket-Connector Interface (J83)

PCIe x1 socket connector at J83 can serve as a secondary interface to the host system. SDK60 can be tethered to the host system via a cable. This connector ties directly to the PCIe capable I/O of the FPGA.

Table 4-2: *PCIe x1 Connector (J83)*

Pin	Signal	Connection
A11	PERST_N	Tied to P_D0N_BSW (AP29) of SPD60 (U1).
B5	SMCLK	Tied to P_D2P_BSW (AT31) of SPD60 (U1).
B6	SMDAT	Tied to P_D2N_BSW (AT30) of SPD60 (U1).
x1		
A16	PER0P	Tied to P_5GA_CH3_RX_P (A24) of SPD60 (U1).
A17	PER0N	Tied to P_5GA_CH3_RX_M (A23) of SPD60 (U1).
B14	PET0P	Tied to P_5GA_CH3_TX_P (B25) of SPD60 (U1).
B15	PET0N	Tied to P_5GA_CH3_TX_M (B24) of SPD60 (U1).

Communication and Networking Interfaces

10/100/1000 Ethernet A (J13)

The SDK60 provides a 10/100/1000Base-T Ethernet interface (**Figure 4-2**) via an RJ45 connector with integrated magnetics at J13 (Bel Fuse 0826-1X1T-23-F). The interface is provided by a Gigabit Ethernet PHY (Marvell 88E1116) driven by the SPD60 using a Reduced Gigabit Media Independent Interface (RGMII). This interface allows for a high-speed network connection to the FPGA over general-purpose I/O.

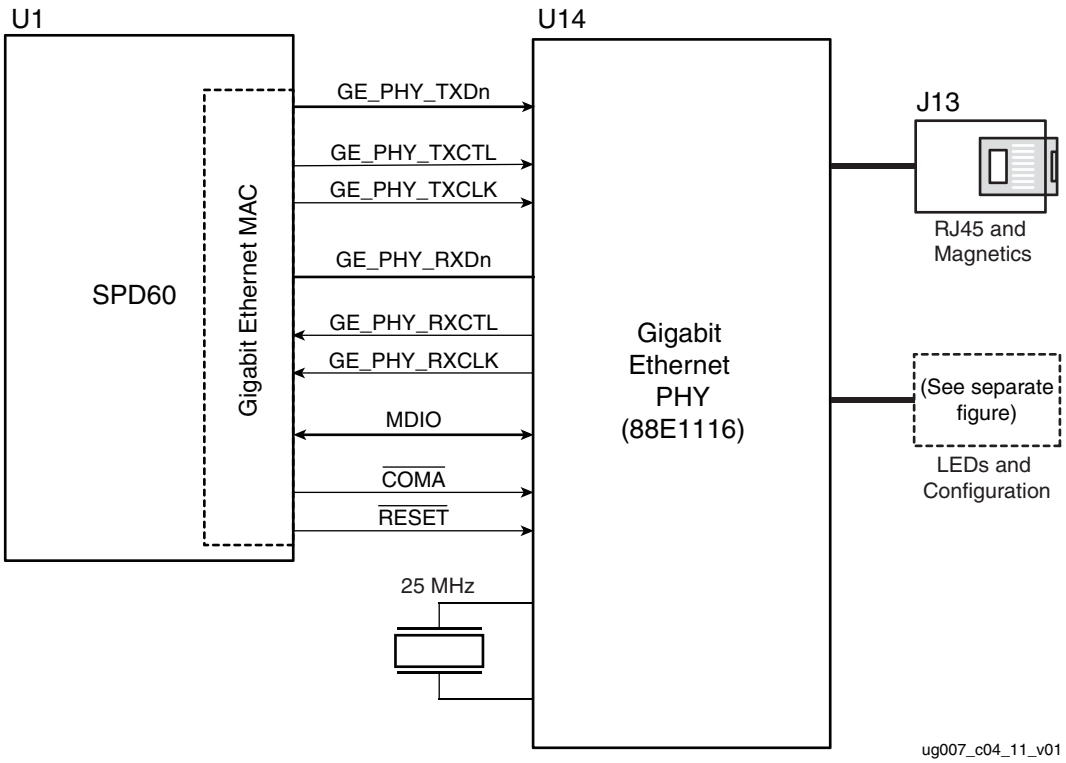


Figure 4-2: *10/100/1000 Ethernet A (J13)*

Table 4-3: *RGMII Interface to FPGA*

Signal	Connection
GE_PHY_TXD0	Tied to P_D6P_BSE (AP17) of SPD60 (U1).
GE_PHY_TXD1	Tied to P_D6N_BSE (AP18) of SPD60 (U1).
GE_PHY_RXD2	Tied to P_D5P_BSE (AR16) of SPD60 (U1).
GE_PHY_RXD3	Tied to P_D5N_BSE (AR17) of SPD60 (U1).
GE_PHY_TXCLK	Tied to P_D7P_BSE (AR19) of SPD60 (U1).
GE_PHY_TXD2	Tied to P_D7N_BSE (AR20) of SPD60 (U1).
GE_PHY_RSTN	Tied to P_D1P_BSE (AT14) of SPD60 (U1).
GE_PHY_MDC	Tied to P_D1N_BSE (AT15) of SPD60 (U1).
GE_PHY_RXD1	Tied to P_D4P_BSE (AT16) of SPD60 (U1).
GE_PHY_RXCLK	Tied to P_D4N_BSE (AT17) of SPD60 (U1).
GE_PHY_TXD3	Tied to P_D8P_BSE (AT18) of SPD60 (U1).

Table 4-3: *RGMII Interface to FPGA (Continued)*

Signal	Connection
GE_PHY_TXCTL	Tied to P_D8N_BSE (AT19) of SPD60 (U1).
GE_PHY_MDIO	Tied to P_D2P_BSE (AU15) of SPD60 (U1).
GE_PHY_COMA_N	Tied to P_D2N_BSE (AU16) of SPD60 (U1).
GE_PHY_RXCTL	Tied to P_D3P_BSE (AU17) of SPD60 (U1).
GE_PHY_RXD0	Tied to P_D3N_BSE (AU18) of SPD60 (U1).

PHY Power-Up (Reset) Configuration

During power-up or reset, a pin-saving feature of the Gigabit Ethernet PHY (U14) allows the four configuration pins to function as eight virtual configuration bits. During configuration/reset, each of the four configuration pins is mapped (**Figure 4-3**) to one of four levels: GND (00), LED_0 (01), LED_2 (10), and VDD (11). The configuration logic controls the the LED pins to determine the setting of each configuration bit. The pins LED_0, and LED_2 return to driving LEDs after power-up/reset completes.

Table 4-4 list the mapping of configuration bits. For example, a pin tied to LED_2 results in a mapping of BIT[1:0] to '10'.

Table 4-4: *Gigabit Ethernet PHY Configuration Mapping*

Configuration Mapping		
PIN	**BIT[1]**	**BIT[0]**
CONFIG_0	PHYADR[1]	PHYADR[0]
CONFIG_1	PHYADR[3]	PHYADR[2]
CONFIG_2	ENA_XC	PHYARD[4]
CONFIG_3	RGMII TX	RGMII RX

Notes:
1. PHYADDR[4:0] is set to 00000.
2. RGMII TX and RGMII RX are both se to '1'.

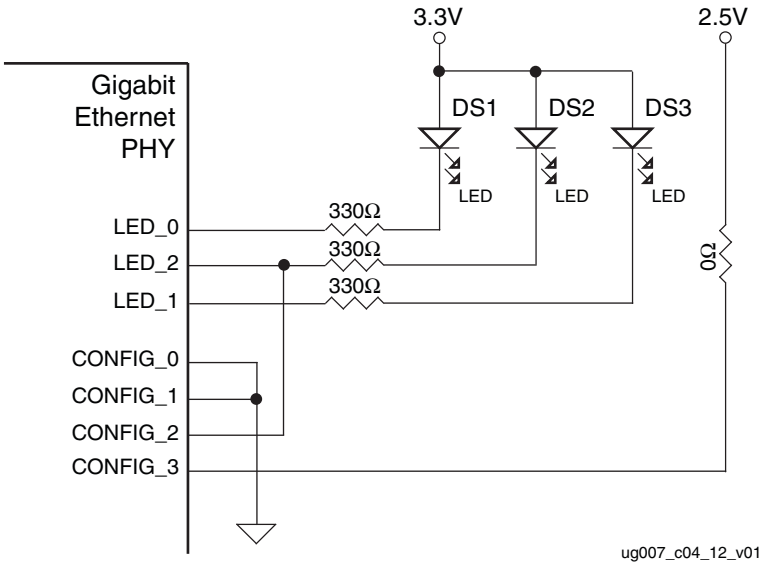


Figure 4-3: *LEDs and Configuration Pins*

10/100/1000 Ethernet B (J48)

The SDK60 provides a second 10/100/1000Base-T Ethernet interface (**Figure 4-3**) via an RJ45 connector with integrated magnetics at J48 (Bel Fuse 0826-1X1T-23-F). The interface is provided by a Gigabit Ethernet PHY (Marvell 88E1114) driven by the SPD60 using a Serial Gigabit Media Independent Interface (SGMII). This interface allows for a high-speed connection to the FPGA using one of the embedded 5G SerDes channels.

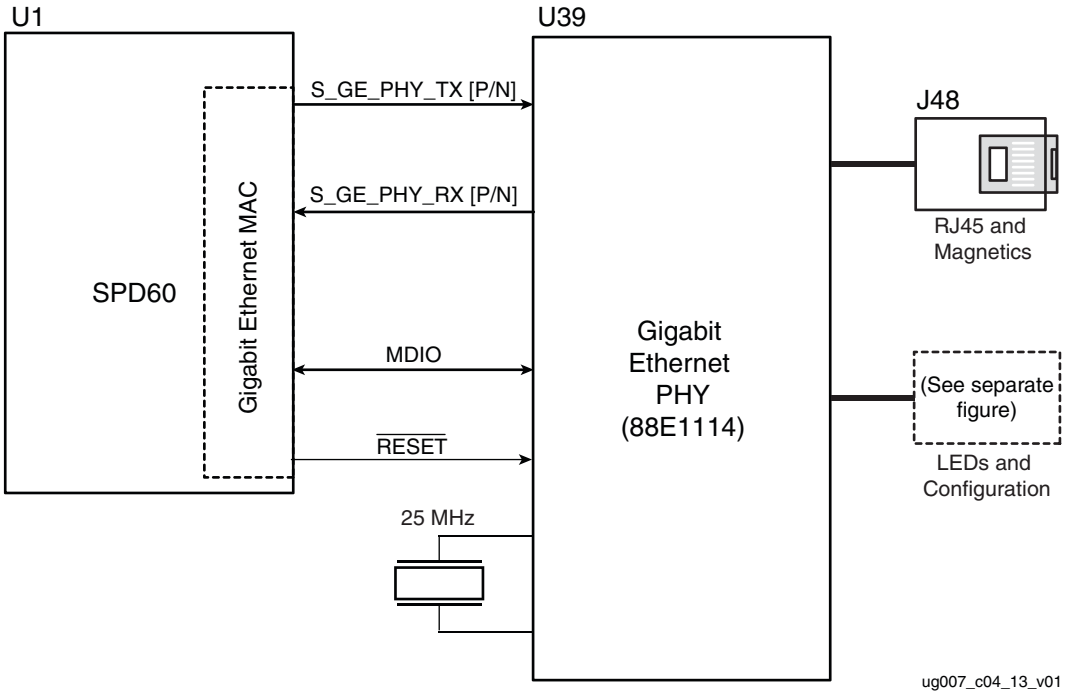


Figure 4-4: *10/100/1000 Ethernet A (J48)*

Table 4-5: *SGMII Interface to FPGA*

Signal	Connection
S_GE_PHY_TX_P	Tied to P_6P5GE_LN3_TXP_O (AR2) of SPD60 (U1).
S_GE_PHY_TX_N	Tied to P_6P5GE_LN3_TXM_O (AT2) of SPD60 (U1).
S_GE_PHY_RX_P	Tied to P_6P5GE_LN3_RXP_I (AR2) of SPD60 (U1).
S_GE_PHY_RX_N	Tied to P_6P5GE_LN3_RXM_I (AP1) of SPD60 (U1).
GE_PHY_MDIO	Tied to P_D2P_BSE (AU15) of SPD60 (U1).
GE_PHY_MDC	Tied to P_D1N_BSE (AT15) of SPD60 (U1).
GE_PHY_RSTN	Tied to P_D1P_BSE (AT14) of SPD60 (U1).

PHY Power-Up (Reset) Configuration

Similar to U14 during power-up or reset, a pin-saving feature of the Gigabit Ethernet PHY (U39) allows the five configuration pins to function as ten virtual configuration bits. During configuration/reset, each of the four configuration pins is mapped (**Figure 4-5**) to one of four levels: GND (00), STATUS0 (01), STATUS2 (10), and VDD (11). The configuration logic controls the LED pins to determine the setting of each configuration bit. The pins STATUS0, and STATUS2 return to driving LEDs after power-up/reset completes.

Table 4-6 list the mapping of configuration bits. For example, a pin tied to STATUS2 results in a mapping of BIT[1:0] to '10'.

Table 4-6: *Gigabit Ethernet PHY Configuration Mapping*

Configuration Mapping		
PIN	**BIT[1]**	**BIT[0]**
CONFIG0	PHYADR[1]	PHYADR[0]
CONFIG1	PHYADR[3]	PHYADR[2]
CONFIG2	SGMII_CLK	PHYARD[4
CONFIG3	SEL_TWSI	SEL_VTT
CONFIG4	EEPROM[1]	EEPROM[0]

Notes:
1. PHYADDR[4:0] is set to 00001.
2. SEL_TWSI is set to '0'.
3. SEL_VTT is set to '0'.
4. EEPROM[1:0] is set to '00'.

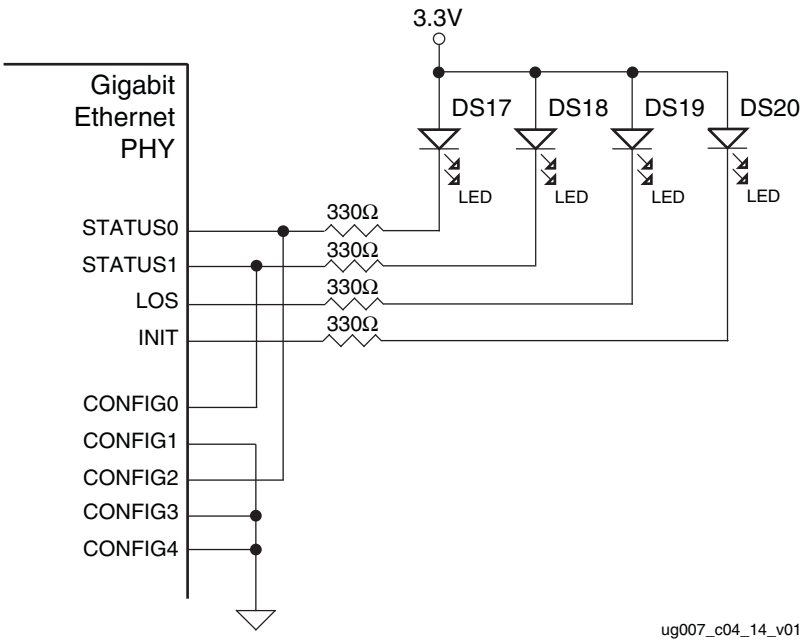


Figure 4-5: *LEDs and Configuration Pins*

10 Gigabit Ethernet (J14)

A 10 Gigabit Ethernet interface is available at the X2 MSA connector at J14. The interface is provided by a Gigabit Ethernet PHY driven by the SPD60 via a 10 Gigabit Attachment Unit Interface (XAUI). The interface uses one quad of the embedded 5G SerDes on the FPGA.

Note: *The front-end optics, electrical interface and cage assembly are according to the X2 MSA specification Revision 2.0.*

Table 4-7: *XAUI Interface to FPGA*

Signal	Connection
XAUI_TD_P	Tied to P_5GB_CH0_TX_P (B21) of SPD60 (U1).
XAUI_TD_N	Tied to P_5GB_CH0_TX_M (B20) of SPD60 (U1).
XAUI_RD_N	Tied to P_5GB_CH0_RX_M (A21) of SPD60 (U1).
XAUI_RD_P	Tied to P_5GB_CH0_RX_P (A22) of SPD60 (U1).
XAUI_TC_P	Tied to P_5GB_CH1_TX_P (B19) of SPD60 (U1).
XAUI_TC_N	Tied to P_5GB_CH1_TX_M (B18) of SPD60 (U1).
XAUI_RC_N	Tied to P_5GB_CH1_RX_M (A17) of SPD60 (U1).
XAUI_RC_P	Tied to P_5GB_CH1_RX_P (A18) of SPD60 (U1).
XAUI_TB_P	Tied to P_5GB_CH2_TX_P (B15) of SPD60 (U1).
XAUI_TB_N	Tied to P_5GB_CH2_TX_M (B14) of SPD60 (U1).
XAUI_RB_N	Tied to P_5GB_CH2_RX_M (A15) of SPD60 (U1).
XAUI_RB_P	Tied to P_5GB_CH2_RX_P (A16) of SPD60 (U1).
XAUI_TA_P	Tied to P_5GB_CH3_TX_P (B13) of SPD60 (U1).
XAUI_TA_N	Tied to P_5GB_CH3_TX_M (B12) of SPD60 (U1).
XAUI_RA_N	Tied to P_5GB_CH3_RX_M (A11) of SPD60 (U1).
XAUI_RA_P	Tied to P_5GB_CH3_RX_P (A12) of SPD60 (U1).

OC48 (U15)

An OC48 interface is available via an Small Form-Factor Pluggable (SFP) optical transceiver at U15. The SFP module interfaces with the FPGA via a single embedded 10.3G SerDes channel.

Note: *The front end optics, electrical interface and cage assembly are according to the SFP Transceiver MSA specification Revision 2.0.*

Table 4-8: *OC48 Interface to FPGA*

Signal	Connection
OC48_RX_P	Tied to P_6P5GE_LN2_RXP_I (AW1) of SPD60 (U1).
OC48_RX_N	Tied to P_6P5GE_LN2_RXM_I (AV1) of SPD60 (U1).
OC48_TX_P	Tied to P_6P5GE_LN2_TXP_O (AU2) of SPD60 (U1).
OC48_TX_N	Tied to P_6P5GE_LN2_TXM_O (AV2) of SPD60 (U1).
OC48_TDIS	Tied to P_D1P_BSW (AR29) of SPD60 (U1).
OC48_SD	Tied to P_D1N_BSW (AR28) of SPD60 (U1).

SMA Connector Interfaces

Direct 5G SerDes Connections

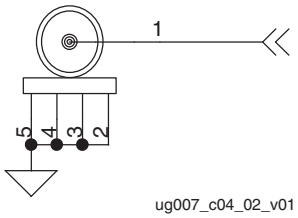


Figure 4-6: *5G SerDes SMA Connector*

Table 4-9: *Direct 5G SerDes SMA Connections*

Connector	Connection
J24	Tied to P_5GA_CH2_TX_M (B26) of SPD60 (U1).
J25	Tied to P_5GA_CH2_RX_P (B28) of SPD60 (U1).
J26	Tied to P_5GA_CH2_TX_P (B27) of SPD60 (U1).
J27	Tied to P_5GA_CH2_RX_M (A27) of SPD60 (U1).

Differential Clock Input (J3 and J4)

The SMA connectors J3 and J4 allow for an external differential clock input to U6.

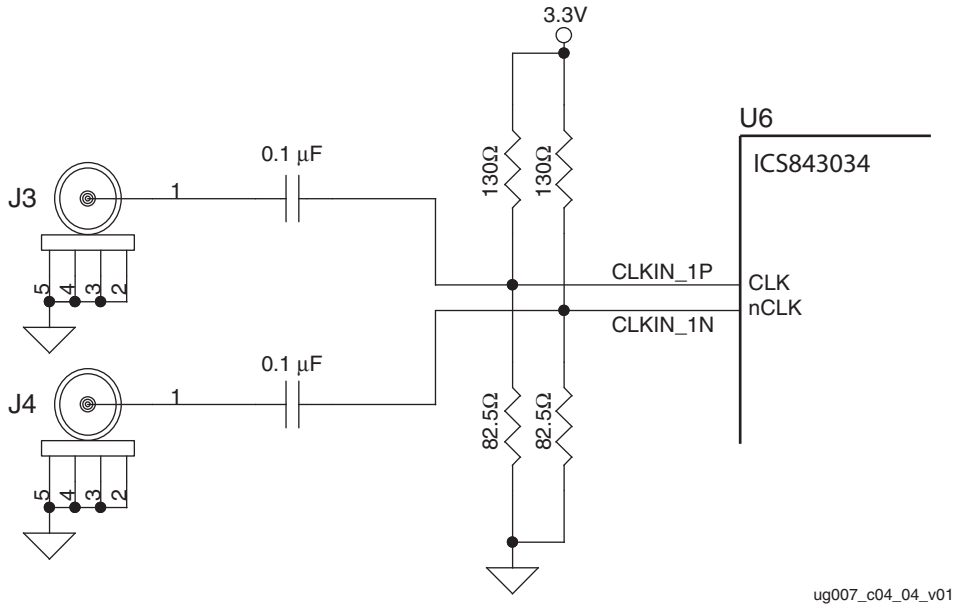


Figure 4-7: *Differential Clock Input (J3 and J4)*

Table 4-10: *Differential Clock Input (J3 and J4)*

Connector	Connection
J3	Tied to CLK (37)) of ICS843034 (U6).
J4	Tied to nCLK (38)) of ICS843034 (U6).

Differential Clock Input (J7 and J8)

The SMA connectors J7 and J8 allow for an external differential clock input to U9.

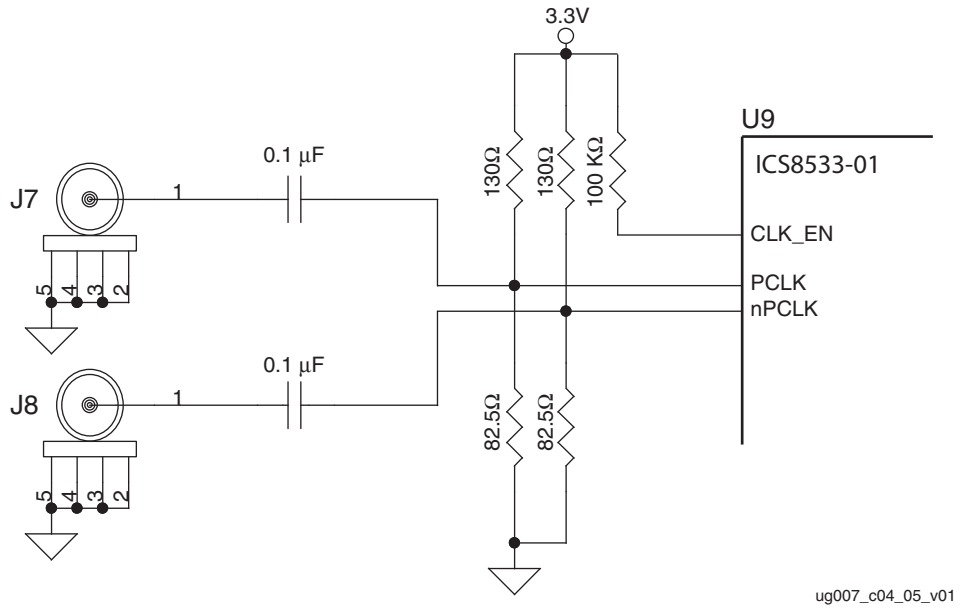


Figure 4-8: *Differential Clock Input (J7 and J8)*

Table 4-11: *Differential Clock Input (J7 and J8)*

Connector	Connection
J7	Tied to PCLK (37) of ICS8533-01(U9).
J8	Tied to nPCLK (38) of ICS8533-01 (U9).

Differential Clock Output (J9 and J11)

The SMA connectors J9 and J11 allow for an external differential clock output from U9.

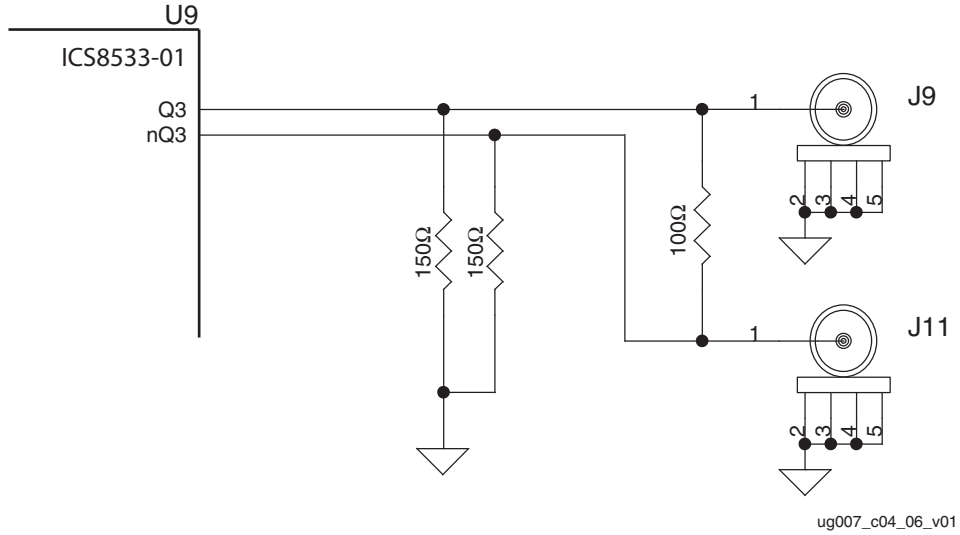


Figure 4-9: *Differential Clock Output (J7 and J8)*

Table 4-12: *Differential Clock Output (J9 and J11)*

Connector	Connection
J9	Tied to Q3 (12) of ICS8533-01(U9).
J11	Tied to nQ3 (11) of ICS8533-01 (U9).

Differential Clock Output (J35 and J36)

The SMA connectors J35 and J36 allow for an external differential clock output from U20. Connections are identical to **Figure 4-9**.

Table 4-13: *Differential Clock Output (J35 and J36)*

Connector	Connection
J35	Tied to Q3 (12) of ICS8533-01(U20).
J36	Tied to nQ3 (11) of ICS8533-01 (U20).

Differential Clock Output (J37 and J38)

The SMA connectors J37 and J38 allow for an external differential clock output from U6. Connections are identical to **Figure 4-9**.

Table 4-14: *Differential Clock Input (J37 and J38)*

Connector	Connection
J37	Tied to FOUTB0 (18) of ICS843034 (U6).
J38	Tied to nFOUTB0 (19) of ICS843034 (U6).

Debug and Trace Interface

Mictor Interface (CN1)

One 32-pin Mictor connector (CN1) is available for connecting a logic analyzer for signal monitoring and debug. The signals connect directly to general-purpose I/Os on the FPGA.

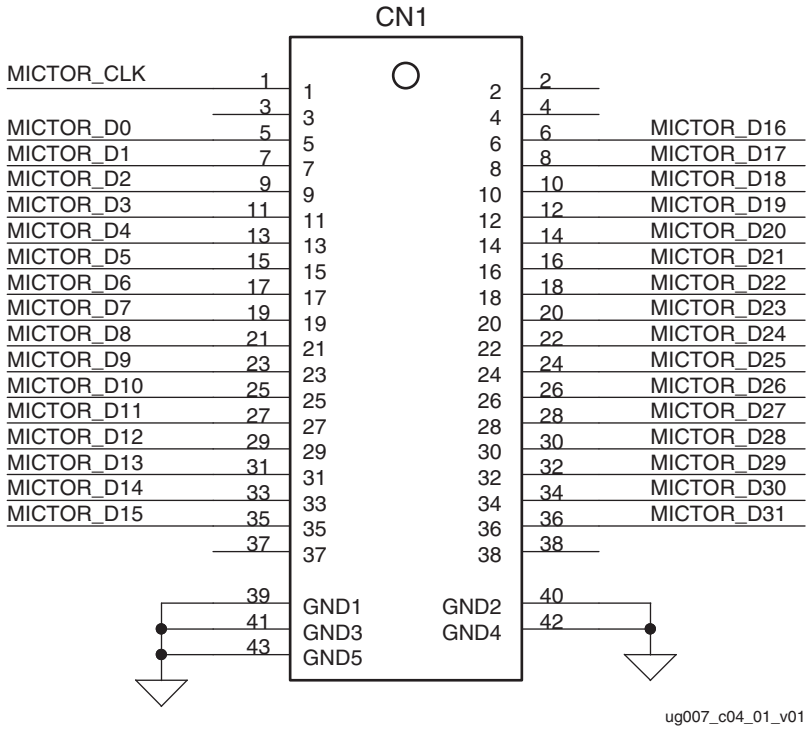


Figure 4-10: *Mictor Connector (CN1)*

Table 4-15: *Mictor Connector (CN1)*

Pin	Connection
1	Tied to P_D25N_BNW (J26) of SPD60 (U1).
5	Tied to P_D25P_BNW (J27) of SPD60 (U1).
6	Tied to P_D17P_BNW (H30) of SPD60 (U1).
7	Tied to P_D24N_BNW (K26) of SPD60 (U1).
8	Tied to P_D16N_BNW (G28) of SPD60 (U1).
9	Tied to P_D24P_BNW (K27) of SPD60 (U1).
10	Tied to P_D16P_BNW (G29) of SPD60 (U1).
11	Tied to P_D23N_BNW (L26) of SPD60 (U1).
12	Tied to P_D15N_BNW (F28) of SPD60 (U1).
13	Tied to P_D23P_BNW (L27) of SPD60 (U1).
14	Tied to P_D15P_BNW (F29) of SPD60 (U1).
15	Tied to P_D22N_BNW (M27) of SPD60 (U1).
16	Tied to P_D14N_BNW (E29) of SPD60 (U1).

Table 4-15: *Mictor Connector (CN1) (Continued)*

Pin	Connection
17	Tied to P_D22P_BNW (M28) of SPD60 (U1).
18	Tied to P_D14P_BNW (E30) of SPD60 (U1).
19	Tied to P_D21N_BNW (N26) of SPD60 (U1).
20	Tied to P_D13N_BNW (F30) of SPD60 (U1).
21	Tied to P_D21P_BNW (N27) of SPD60 (U1).
22	Tied to P_D13P_BNW (F31) of SPD60 (U1).
23	Tied to P_D20N_BNW (N28) of SPD60 (U1).
24	Tied to P_D12N_BNW (G30) of SPD60 (U1).
25	Tied to P_D20P_BNW (N29) of SPD60 (U1).
26	Tied to P_D12P_BNW (G31) of SPD60 (U1).
27	Tied to P_D19N_BNW (K28) of SPD60 (U1).
28	Tied to P_D11N_BNW (J30) of SPD60 (U1).
29	Tied to P_D19P_BNW (K29) of SPD60 (U1).
30	Tied to P_D11P_BNW (J31) of SPD60 (U1).
31	Tied to P_D18N_BNW (J28) of SPD60 (U1).
32	Tied to P_D10N_BNW (K30) of SPD60 (U1).
33	Tied to P_D18P_BNW (J29) of SPD60 (U1).
34	Tied to P_D10P_BNW (K31) of SPD60 (U1).
35	Tied to P_D17N_BNW (H29) of SPD60 (U1).
36	Tied to P_D9N_BNW (L29) of SPD60 (U1).

Memory Interfaces

DDR2/QDR2 200-Pin SODIMM Socket (U11)

A 200-pin SODIMM socket for DDR2 is available at U11 (the board ships with a 128M × 72 SOCDIMM). The socket can support up to 2GB of 577 MHz 72-bit DDR2. The socket at U11 connects directly to the FPGA general-purpose I/O configured as 1.8V SSTL. 32-bit 8MB QDR2 SRAM module can be used in the same socket; however the FPGA I/Os must be configured as HSTL.

Table 4-16: *SODIMM Socket (U11)*

Pin	Signal	Connection
110	A0	Tied to P_D36P_B3 (AJ41) of SPD60 (U1).
108	A1	Tied to P_D36N_B3 (AJ42) of SPD60 (U1).
107	A2	Tied to P_D37P_B3 (AJ44) of SPD60 (U1).
105	A3	Tied to P_D37N_B3 (AJ43) of SPD60 (U1).
104	A4	Tied to P_D39P_B3 (AG41) of SPD60 (U1).
103	A5	Tied to P_D39N_B3 (AG42) of SPD60 (U1).
102	A6	Tied to P_D40P_B3 (AG44) of SPD60 (U1).
99	A7	Tied to P_D40N_B3 (AG43) of SPD60 (U1).

Table 4-16: *SODIMM Socket (U11) (Continued)*

Pin	Signal	Connection
100	A8	Tied to P_D41P_B3 (AF44) of SPD60 (U1).
97	A9	Tied to P_D41N_B3 (AF43) of SPD60 (U1).
111	A10	Tied to P_D42P_B3 (AH34) of SPD60 (U1).
96	A11	Tied to P_D42N_B3 (AG34) of SPD60 (U1).
95	A12	Tied to P_D43P_B3 (AF34) of SPD60 (U1).
122	A13	Tied to P_D43N_B3 (AE34) of SPD60 (U1).
113	BA0	Tied to P_D45P_B3 (AF35) of SPD60 (U1).
112	BA1	Tied to P_D45N_B3 (AE35) of SPD60 (U1).
92	BA2	Tied to P_D46P_B3 (AD34) of SPD60 (U1).
126	CK0	Tied to P_D38P_B3 (AH44) of SPD60 (U1).
128	CK0#	Tied to P_D38N_B3 (AH43) of SPD60 (U1).
87	CKE0	Tied to P_D31P_B3 (AM44) of SPD60 (U1).
89	CKE1	Tied to P_D31N_B3 (AM43) of SPD60 (U1).
10	DM0	Tied to P_D5P_B3 (AT36) of SPD60 (U1).
26	DM1	Tied to P_D11P_B3 (AT40) of SPD60 (U1).
44	DM2	Tied to P_D17P_B3 (AK35) of SPD60 (U1).
60	DM3	Tied to P_D23P_B3 (AK38) of SPD60 (U1).
138	DM4	Tied to P_D42P_B2 (AD38) of SPD60 (U1).
154	DM5	Tied to P_D36P_B2 (AB40) of SPD60 (U1).
170	DM6	Tied to P_D30P_B2 (AC44) of SPD60 (U1).
186	DM7	Tied to P_D24P_B2 (W41) of SPD60 (U1).
76	DM8	Tied to P_D29P_B3 (AK40) of SPD60 (U1).
118	S0#	Tied to P_D30P_B3 (AN41) of SPD60 (U1).
121	S1#	Tied to P_D30N_B3 (AN42) of SPD60 (U1).
120	ODTO	Tied to P_D33P_B3 (AL41) of SPD60 (U1).
125	ODT1	Tied to P_D33N_B3 (AL42) of SPD60 (U1).
119	$\overline{\text{CAS}}$	Tied to P_D47P_B3 (AD35) of SPD60 (U1).
115	$\overline{\text{RAS}}$	Tied to P_D47N_B3 (AC35) of SPD60 (U1).
116	$\overline{\text{WE}}$	Tied to P_D46N_B3 (AC34) of SPD60 (U1).
42	RESET#	Tied to P_D44N_B3 (AG35) of SPD60 (U1).
3	DQ0	Tied to P_D0P_B3 (AV34) of SPD60 (U1).
7	DQ1	Tied to P_D0N_B3 (AU34) of SPD60 (U1).
15	DQ2	Tied to P_D1P_B3 (AV35) of SPD60 (U1).
17	DQ3	Tied to P_D1N_B3 (AU35) of SPD60 (U1).
4	DQ4	Tied to P_D3P_B3 (AV36) of SPD60 (U1).
6	DQ5	Tied to P_D3N_B3 (AU36) of SPD60 (U1).
14	DQ6	Tied to P_D4P_B3 (AT34) of SPD60 (U1).
16	DQ7	Tied to P_D4N_B3 (AR34) of SPD60 (U1).
21	DQ8	Tied to P_D6P_B3 (AV38) of SPD60 (U1).
23	DQ9	Tied to P_D6N_B3 (AU38) of SPD60 (U1).

Table 4-16: *SODIMM Socket (U11) (Continued)*

Pin	Signal	Connection
33	DQ10	Tied to P_D7P_B3 (AV39) of SPD60 (U1).
35	DQ11	Tied to P_D7N_B3 (AU39) of SPD60 (U1).
20	DQ12	Tied to P_D9P_B3 (AT38) of SPD60 (U1).
22	DQ13	Tied to P_D9N_B3 (AR38) of SPD60 (U1).
30	DQ14	Tied to P_D10P_B3 (AV40) of SPD60 (U1).
32	DQ15	Tied to P_D10N_B3 (AU40) of SPD60 (U1).
39	DQ16	Tied to P_D12P_B3 (AP34) of SPD60 (U1).
41	DQ17	Tied to P_D12N_B3 (AN34) of SPD60 (U1).
51	DQ18	Tied to P_D13P_B3 (AM34) of SPD60 (U1).
53	DQ19	Tied to P_D13N_B3 (AL34) of SPD60 (U1).
36	DQ20	Tied to P_D15P_B3 (AP35) of SPD60 (U1).
38	DQ21	Tied to P_D15N_B3 (AN35) of SPD60 (U1).
48	DQ22	Tied to P_D16P_B3 (AK34) of SPD60 (U1).
50	DQ23	Tied to P_D16N_B3 (AJ34) of SPD60 (U1).
57	DQ24	Tied to P_D18P_B3 (AP37) of SPD60 (U1).
59	DQ25	Tied to P_D18N_B3 (AN37) of SPD60 (U1).
69	DQ26	Tied to P_D19P_B3 (AM37) of SPD60 (U1).
71	DQ27	Tied to P_D19N_B3 (AL37) of SPD60 (U1).
54	DQ28	Tied to P_D21P_B3 (AP38) of SPD60 (U1).
56	DQ29	Tied to P_D21N_B3 (AN38) of SPD60 (U1).
64	DQ30	Tied to P_D22P_B3 (AK37) of SPD60 (U1).
66	DQ31	Tied to P_D22N_B3 (AJ37) of SPD60 (U1).
129	DQ32	Tied to P_D47P_B2 (AH37) of SPD60 (U1).
133	DQ33	Tied to P_D47N_B2 (AG37) of SPD60 (U1).
141	DQ34	Tied to P_D46P_B2 (AF37) of SPD60 (U1).
143	DQ35	Tied to P_D46N_B2 (AE37) of SPD60 (U1).
132	DQ36	Tied to P_D44P_B2 (AF38) of SPD60 (U1).
134	DQ37	Tied to P_D44N_B2 (AE38) of SPD60 (U1).
142	DQ38	Tied to P_D43P_B2 (AD37) of SPD60 (U1).
144	DQ39	Tied to P_D43N_B2 (AC37) of SPD60 (U1).
147	DQ40	Tied to P_D41P_B2 (AH40) of SPD60 (U1).
149	DQ41	Tied to P_D41N_B2 (AG40) of SPD60 (U1).
159	DQ42	Tied to P_D40P_B2 (AF39) of SPD60 (U1).
161	DQ43	Tied to P_D40N_B2 (AE39) of SPD60 (U1).
148	DQ44	Tied to P_D38P_B2 (AD40) of SPD60 (U1).
150	DQ45	Tied to P_D38N_B2 (AC40) of SPD60 (U1).
158	DQ46	Tied to P_D37P_B2 (AB39) of SPD60 (U1).
160	DQ47	Tied to P_D37N_B2 (AA39) of SPD60 (U1).
165	DQ48	Tied to P_D35P_B2 (AF41) of SPD60 (U1).
167	DQ49	Tied to P_D35N_B2 (AF42) of SPD60 (U1).

Table 4-16: *SODIMM Socket (U11) (Continued)*

Pin	Signal	Connection
177	DQ50	Tied to P_D34P_B2 (AE41) of SPD60 (U1).
179	DQ51	Tied to P_D34N_B2 (AE42) of SPD60 (U1).
164	DQ52	Tied to P_D32P_B2 (AD44) of SPD60 (U1).
166	DQ53	Tied to P_D32N_B2 (AD43) of SPD60 (U1).
174	DQ54	Tied to P_D31P_B2 (AC41) of SPD60 (U1).
176	DQ55	Tied to P_D31N_B2 (AC42) of SPD60 (U1).
183	DQ56	Tied to P_D29P_B2 (AB41) of SPD60 (U1).
185	DQ57	Tied to P_D29N_B2 (AB42) of SPD60 (U1).
193	DQ58	Tied to P_D28P_B2 (AB44) of SPD60 (U1).
197	DQ59	Tied to P_D28N_B2 (AB43) of SPD60 (U1).
180	DQ60	Tied to P_D26P_B2 (Y41) of SPD60 (U1).
182	DQ61	Tied to P_D26N_B2 (Y42) of SPD60 (U1).
188	DQ62	Tied to P_D25P_B2 (Y44) of SPD60 (U1).
192	DQ63	Tied to P_D25N_B2 (Y43) of SPD60 (U1).
9	DQS0#	Tied to P_D2N_B3 (AR35) of SPD60 (U1).
27	DQS1#	Tied to P_D8N_B3 (AR39) of SPD60 (U1).
45	DQS2#	Tied to P_D14N_B3 (AL35) of SPD60 (U1).
63	DQS3#	Tied to P_D20N_B3 (AL38) of SPD60 (U1).
135	DQS4#	Tied to P_D45N_B2 (AG38) of SPD60 (U1).
153	DQS5#	Tied to P_D39N_B2 (AE40) of SPD60 (U1).
171	DQS6#	Tied to P_D33N_B2 (AE43) of SPD60 (U1).
189	DQS7#	Tied to P_D27N_B2 (AA43) of SPD60 (U1).
81	DQS8#	Tied to P_D26N_B3 (AL40) of SPD60 (U1).
11	DQS0	Tied to P_D2P_B3 (AT35) of SPD60 (U1).
29	DQS1	Tied to P_D8P_B3 (AT39) of SPD60 (U1).
47	DQS2	Tied to P_D14N_B3 (AL35) of SPD60 (U1).
65	DQS3	Tied to P_D20N_B3 (AL38) of SPD60 (U1).
137	DQS4	Tied to P_D45P_B2 (AH38) of SPD60 (U1).
155	DQS5	Tied to P_D39P_B2 (AF40) of SPD60 (U1).
173	DQS6	Tied to P_D33P_B2 (AE44) of SPD60 (U1).
191	DQS7	Tied to P_D27P_B2 (AA44) of SPD60 (U1).
83	DQS8	Tied to P_D26P_B3 (AM40) of SPD60 (U1).
75	CB0	Tied to P_D24P_B3 (AP39) of SPD60 (U1).
77	CB1	Tied to P_D24N_B3 (AN39) of SPD60 (U1).
86	CB2	Tied to P_D25P_B3 (AM39) of SPD60 (U1).
88	CB3	Tied to P_D25N_B3 (AL39) of SPD60 (U1).
70	CB4	Tied to P_D27P_B3 (AP40) of SPD60 (U1).
72	CB5	Tied to P_D27N_B3 (AN40) of SPD60 (U1).
80	CB6	Tied to P_D28P_B3 (AK39) of SPD60 (U1).
82	CB7	Tied to P_D28N_B3 (AJ39) of SPD60 (U1).

DDR3 Memory (U10)

A 256MB of 1066MHz 64-bit, DDR3 SDRAM (MT41J128M8), organized as eight banks of 128Mb, is provided at U10. The memory is connected to the FPGA via general-purpose I/Os configured as 1.5V SSTL.

Note: *The DDR3 SDRAM interface is restricted to 48-pins (or one-half bank). As a result, higher address signals are not connected, preventing accessing all memory locations.*

Table 4-17: *DDR3 Memory (U10) Connections*

Pin	Signal	Connection
N3	A0	Tied to P_D36P_B1 (L37) of SPD60 (U1).
P7	A1	Tied to P_D36N_B1 (M37) of SPD60 (U1).
P3	A2	Tied to P_D37P_B1 (L38) of SPD60 (U1).
N2	A3	Tied to P_D37N_B1 (M38) of SPD60 (U1).
P8	A4	Tied to P_D39P_B1 (N37) of SPD60 (U1).
P2	A5	Tied to P_D39N_B1 (P37) of SPD60 (U1).
R8	A6	Tied to P_D40P_B1 (R37) of SPD60 (U1).
R2	A7	Tied to P_D40N_B1 (T37) of SPD60 (U1).
T8	A8	Tied to P_D41P_B1 (R38) of SPD60 (U1).
R3	A9	Tied to P_D41N_B1 (T38) of SPD60 (U1).
L7	A10	Tied to P_D42P_B1 (M42) of SPD60 (U1).
R7	A11	Tied to P_D42N_B1 (M41) of SPD60 (U1).
N7	A12	Tied to P_D43P_B1 (N43) of SPD60 (U1).
T3	A13	Tied to P_D43N_B1 (N44) of SPD60 (U1).
M2	BA0	Tied to P_D45P_B1 (P43) of SPD60 (U1).
N8	BA1	Tied to P_D45N_B1 (P44) of SPD60 (U1).
M3	BA2	Tied to P_D46P_B1 (R42) of SPD60 (U1).
J7	CK	Tied to P_D38P_B1 (N38) of SPD60 (U1).
K7	CK#	Tied to P_D38N_B1 (P38) of SPD60 (U1).
K9	CKE	Tied to P_D31P_B1 (L35) of SPD60 (U1).
L2	CS#	Tied to P_D30P_B1 (L34) of SPD60 (U1).
L3	WE#	Tied to P_D46N_B1 (R41) of SPD60 (U1).
K3	CAS#	Tied to P_D47P_B1 (R43) of SPD60 (U1).
J3	RAS#	Tied to P_D47N_B1 (R44) of SPD60 (U1).
E3	DQ0	Tied to P_D24P_B1 (F39) of SPD60 (U1).
F7	DQ1	Tied to P_D24N_B1 (G39) of SPD60 (U1).
F2	DQ2	Tied to P_D25P_B1 (H40) of SPD60 (U1).
F8	DQ3	Tied to P_D25N_B1 (J40) of SPD60 (U1).
H3	DQ4	Tied to P_D27P_B1 (K39) of SPD60 (U1).
H8	DQ5	Tied to P_D27N_B1 (L39) of SPD60 (U1).
G2	DQ6	Tied to P_D28P_B1 (K40) of SPD60 (U1).
H7	DQ7	Tied to P_D28N_B1 (L40) of SPD60 (U1).
F3	DQS	Tied to P_D26P_B1 (H39) of SPD60 (U1).
G3	DQS#	Tied to P_D26N_B1 (J39) of SPD60 (U1).
E7	DM	Tied to P_D29P_B1 (M40) of SPD60 (U1).
K1	ODT	Tied to P_D33P_B1 (N34) of SPD60 (U1).

QDR2 Memory (U2)

4Mb × 18 of 375MHz 32-bit, QDR2 SRAM (CY7C1176V18) is provided on-board at U2. The SRAM interfaces with the FPGA via general-purpose I/Os configured as 1.5V HSTL.

Note: *The QDR2 SRAM interface is restricted to 48-pins (or one-half bank). As a result, higher address signals are not connected, preventing accessing all memory locations.*

Table 4-18: *QDR2 Memory (U2) Connections*

Pin	Signal	Connection
R9	A0	Tied to P_D0P_B1 (E34) of SPD60 (U1).
A9	A1	Tied to P_D0N_B1 (F34) of SPD60 (U1).
R8	A2	Tied to P_D1P_B1 (E35) of SPD60 (U1).
P8	A3	Tied to P_D1N_B1 (F35) of SPD60 (U1).
B8	A4	Tied to P_D3P_B1 (G34) of SPD60 (U1).
R7	A5	Tied to P_D3N_B1 (H34) of SPD60 (U1).
P7	A6	Tied to P_D4P_B1 (J34) of SPD60 (U1).
N7	A7	Tied to P_D4N_B1 (K34) of SPD60 (U1).
C7	A8	Tied to P_D5P_B1 (J35) of SPD60 (U1).
N6	A9	Tied to P_D5N_B1 (K35) of SPD60 (U1).
R5	A10	Tied to P_D6P_B1 (E37) of SPD60 (U1).
P5	A11	Tied to P_D6N_B1 (F37) of SPD60 (U1).
N5	A12	Tied to P_D7P_B1 (E38) of SPD60 (U1).
C5	A13	Tied to P_D7N_B1 (F38) of SPD60 (U1).
R4	A14	Tied to P_D8P_B1 (G38) of SPD60 (U1).
P4	A15	Tied to P_D8N_B1 (H38) of SPD60 (U1).
B4	A16	Tied to P_D9P_B1 (G37) of SPD60 (U1).
R3	A17	Tied to P_D9N_B1 (H37) of SPD60 (U1).
A3	A18	Tied to P_D10P_B1 (J38) of SPD60 (U1).
A10	A19	Tied to P_D10N_B1 (K38) of SPD60 (U1).
P10	D0	Tied to P_D18P_B1 (J43) of SPD60 (U1).
M11	D1	Tied to P_D18N_B1 (J44) of SPD60 (U1).
J11	D2	Tied to P_D19P_B1 (K42) of SPD60 (U1).
E10	D3	Tied to P_D19N_B1 (K41) of SPD60 (U1).
C11	D4	Tied to P_D21P_B1 (L42) of SPD60 (U1).
D2	D5	Tied to P_D21N_B1 (L41) of SPD60 (U1).
G2	D6	Tied to P_D22P_B1 (L43) of SPD60 (U1).
L3	D7	Tied to P_D22N_B1 (L44) of SPD60 (U1).
N2	D8	Tied to P_D23P_B1 (M43) of SPD60 (U1).
P11	Q0	Tied to P_D12P_B1 (F42) of SPD60 (U1).
L11	Q1	Tied to P_D12N_B1 (F41) of SPD60 (U1).
J10	Q2	Tied to P_D13P_B1 (F40) of SPD60 (U1).
E11	Q3	Tied to P_D13N_B1 (G40) of SPD60 (U1).

Table 4-18: *QDR2 Memory (U2) Connections (Continued)*

Pin	Signal	Connection
B11	Q4	Tied to P_D15P_B1 (G43) of SPD60 (U1).
E3	Q5	Tied to P_D15N_B1 (G44) of SPD60 (U1).
G3	Q6	Tied to P_D16P_B1 (H42) of SPD60 (U1).
L2	Q7	Tied to P_D16N_B1 (H41) of SPD60 (U1).
P3	Q8	Tied to P_D17P_B1 (H43) of SPD60 (U1).
B6	K	Tied to P_D2P_B1 (G35) of SPD60 (U1).
A6	K#	Tied to P_D2N_B1 (H35) of SPD60 (U1).
A11	CQ	Tied to P_D14P_B1 (G42) of SPD60 (U1).
A1	CQ#	Tied to P_D14N_B1 (G41) of SPD60 (U1).
P6	QVLD	Tied to P_D17N_B1 (H44) of SPD60 (U1).
B7	BWS#	Tied to P_D23N_B1 (M44) of SPD60 (U1).
A8	RPS#	Tied to P_D11P_B1 (J37) of SPD60 (U1).
A4	WPS#	Tied to P_D11N_B1 (K37) of SPD60 (U1).

Expansion Bus Interfaces

Five expansion slots are available on the SDK60 evaluation board to enhance the functionality, and flexibility of the board. These expansion slots allow the embedded SPD60 to access not only off-the-shelf daughter cards, but also and customer-supplied cards.

The AMC expansion bus is SerDes-based, whereas the PMC and Hi-Speed Expansion buses use the SPD60's programmable I/Os (PCI at 66 MHz, and LVDS at 1 Gb/s).

AMC Connector (J12)

The ATCA Mezzanine Card (AMC) connector at J12 connects to the FPGA via two quads of embedded 5G SerDes.

Note: *There is an associated JTAG connector at J40 (see* **"AMC JTAG Connector (J40)"** *for details).*

Table 4-19: *AMC Connector (J12)*

Pin	Signal	Connection
11	TX0+	Tied to P_6P5GA_LN0_RXP_I (AP44) of SPD60 (U1).
12	TX0–	Tied to P_6P5GA_LN0_RXM_I (AR44) of SPD60 (U1).
14	RX0+	Tied to P_6P5GA_LN0_TXP_I (AT43) of SPD60 (U1).
15	RX0–	Tied to P_6P5GA_LN0_TXM_I (AR43) of SPD60 (U1).
20	TX1+	Tied to P_6P5GA_LN1_RXP_I (AV44) of SPD60 (U1).
21	TX1-	Tied to P_6P5GA_LN1_RXM_I (AW44) of SPD60 (U1).
23	RX1+	Tied to P_6P5GA_LN1_TXP_O (AV43) of SPD60 (U1).
24	RX1-	Tied to P_6P5GA_LN1_TXM_O (AU43) of SPD60 (U1).
29	TX2+	Tied to P_6P5GA_LN2_RXP_I (AY44) of SPD60 (U1).
30	TX2-	Tied to P_6P5GA_LN2_RXM_I (BA44) of SPD60 (U1).
32	RX2+	Tied to P_6P5GA_LN2_TXP_O (BB43) of SPD60 (U1).

Table 4-19: *AMC Connector (J12) (Continued)*

Pin	Signal	Connection
33	RX2-	Tied to P_6P5GA_LN2_TXM_O (BA43) of SPD60 (U1).
35	TX3+	Tied to P_6P5GA_LN3_RXP_I (BD42) of SPD60 (U1).
36	TX3-	Tied to P_6P5GA_LN3_RXM_I (BD41) of SPD60 (U1).
38	RX3+	Tied to P_6P5GA_LN3_TXP_O (BC42) of SPD60 (U1).
39	RX3-	Tied to P_6P5GA_LN3_TXM_O (BC43) of SPD60 (U1).
44	TX4+	Tied to P_6P5GB_LN0_RXP_I (BD40) of SPD60 (U1).
45	TX4-	Tied to P_6P5GB_LN0_RXM_I (BD39) of SPD60 (U1).
47	RX4+	Tied to P_6P5GB_LN0_TXP_O (BC38) of SPD60 (U1).
48	RX4-	Tied to P_6P5GB_LN0_TXM_O (BC39) of SPD60 (U1).
50	TX5+	Tied to P_6P5GB_LN1_RXP_I (BD36) of SPD60 (U1).
51	TX5-	Tied to P_6P5GB_LN1_RXM_I (BD35) of SPD60 (U1).
53	RX5+	Tied to P_6P5GB_LN1_TXP_O (BC36) of SPD60 (U1).
54	RX5-	Tied to P_6P5GB_LN1_TXM_O (BC37) of SPD60 (U1).
59	TX6+	Tied to P_6P5GB_LN2_RXP_I (BD34) of SPD60 (U1).
60	TX6-	Tied to P_6P5GB_LN2_RXM_I (BD33) of SPD60 (U1).
62	RX6+	Tied to P_6P5GB_LN2_TXP_O (BC32) of SPD60 (U1).
63	RX6-	Tied to P_6P5GB_LN2_TXM_O (BC33) of SPD60 (U1).
65	TX7+	Tied to P_6P5GB_LN3_RXP_I (BD30) of SPD60 (U1).
66	TX7-	Tied to P_6P5GB_LN3_RXM_I (BD29) of SPD60 (U1).
68	RX7+	Tied to P_6P5GB_LN3_TXP_O (BC30) of SPD60 (U1).
69	RX7-	Tied to P_6P5GB_LN3_TXM_O (BC31) of SPD60 (U1).

PMC Connector (JN1, JN2, and JN3)

The SDK60 comes equipped with a PMC (PCI Mezzanine Card) interface supporting 64-bit, 66 MHz PCI. The PMC connectors interface with the PCI-capable I/Os of the FPGA.

Table 4-20: *PMC Connector (JN1, JN2 and JN3)*

Pin	Signal	Connection
Connector JN1		
16	GNT_N	Tied to P_D1P_BNE (E12) of SPD60 (U1).
17	REQ_N	Tied to P_D1N_BNE (E13) of SPD60 (U1).
20	PCI_AD31	Tied to P_D2P_BNE (F12) of SPD60 (U1).
21	PCI_AD28	Tied to P_D2N_BNE (F13) of SPD60 (U1).
22	PCI_AD27	Tied to P_D3P_BNE (G12) of SPD60 (U1).
23	PCI_AD25	Tied to P_D3N_BNE (G13) of SPD60 (U1).
26	CBE_N3	Tied to P_D4P_BNE (H12) of SPD60 (U1).
27	PCI_AD22	Tied to P_D4N_BNE (H13) of SPD60 (U1).
28	PCI_AD21	Tied to P_D5P_BNE (J12) of SPD60 (U1).
29	PCI_AD19	Tied to P_D5N_BNE (J13) of SPD60 (U1).

Table 4-20: *PMC Connector (JN1, JN2 and JN3) (Continued)*

Pin	Signal	Connection
32	PCI_AD17	Tied to P_D6P_BNE (K12) of SPD60 (U1).
33	FRAME_N	Tied to P_D6N_BNE (K13) of SPD60 (U1).
36	IRDY_N	Tied to P_D7P_BNE (N14) of SPD60 (U1).
37	DEVSEL_N	Tied to P_D7N_BNE (N15) of SPD60 (U1).
40	LOCK_N	Tied to P_D8P_BNE (M14) of SPD60 (U1).
43	PAR	Tied to P_D9N_BNE (L16) of SPD60 (U1).
46	PCI_AD15	Tied to P_D3N_BNE (K14) of SPD60 (U1).
47	PCI_AD12	Tied to P_D10N_BNE (K15) of SPD60 (U1).
48	PCI_AD11	Tied to P_D11P_BNE (J14) of SPD60 (U1).
49	PCI_AD9	Tied to P_D11N_BNE (J15) of SPD60 (U1).
52	CBE_N0	Tied to P_D12P_BNE (G14) of SPD60 (U1).
53	PCI_AD6	Tied to P_D12N_BNE (G15) of SPD60 (U1).
54	PCI_AD5	Tied to P_D13P_BNE (F14) of SPD60 (U1).
55	PCI_AD4	Tied to P_D13N_BNE (F15) of SPD60 (U1).
58	PCI_AD3	Tied to P_D14P_BNE (E15) of SPD60 (U1).
59	PCI_AD2	Tied to P_D14N_BNE (E16) of SPD60 (U1).
60	PCI_AD1	Tied to P_D15P_BNE (F16) of SPD60 (U1).
61	PCI_AD0	Tied to P_D15N_BNE (F17) of SPD60 (U1).
64	REQ64_N	Tied to P_D16P_BNE (G16) of SPD60 (U1).
Connector JN2		
2	PMC_RSTN	Tied to P_D16N_BNE (G17) of SPD60 (U1).
13	PCI_RSTN	Tied to P_D16N_BNE (G17) of SPD60 (U1).
19	PCI_AD30	Tied to P_D17P_BNE (H15) of SPD60 (U1).
20	PCI_AD29	Tied to P_D17N_BNE (H16) of SPD60 (U1).
22	PCI_AD26	Tied to P_D18P_BNE (J16) of SPD60 (U1).
23	PCI_AD24	Tied to P_D18N_BNE (J17) of SPD60 (U1).
25	IDSEL	Tied to P_D19P_BNE (K16) of SPD60 (U1).
26	PCI_AD23	Tied to P_D19N_BNE (K17) of SPD60 (U1).
28	PCI_AD20	Tied to P_D20P_BNE (N16) of SPD60 (U1).
29	PCI_AD18	Tied to P_D20N_BNE (N17) of SPD60 (U1).
31	PCI_AD16	Tied to P_D21P_BNE (N18) of SPD60 (U1).
32	CBE_N2	Tied to P_D21N_BNE (N19) of SPD60 (U1).
35	TRDY_N	Tied to P_D22P_BNE (M17) of SPD60 (U1).
38	STOP_N	Tied to P_D22N_BNE (M18) of SPD60 (U1).
39	PERR_N	Tied to P_D23P_BNE (L18) of SPD60 (U1).
42	SERR_N	Tied to P_D23N_BNE (L19) of SPD60 (U1).
43	CBE_N1	Tied to P_D24P_BNE (K18) of SPD60 (U1).
45	PCI_AD14	Tied to P_D24N_BNE (K19) of SPD60 (U1).
46	PCI_AD13	Tied to P_D25P_BNE (J18) of SPD60 (U1).

Table 4-20: *PMC Connector (JN1, JN2 and JN3) (Continued)*

Pin	Signal	Connection
48	PCI_AD10	Tied to P_D25N_BNE (J19) of SPD60 (U1).
49	PCI_AD8	Tied to P_D26P_BNE (H18) of SPD60 (U1).
51	PCI_AD7	Tied to P_D26N_BNE (H19) of SPD60 (U1).
61	ACK64_N	Tied to P_D27P_BNE (G18) of SPD60 (U1).
Connector JN3		
4	CBE_N7	Tied to P_D27N_BNE (G19) of SPD60 (U1).
5	CBE_N6	Tied to P_D28P_BNE (F18) of SPD60 (U1).
6	CBE_N5	Tied to P_D28N_BNE (F19) of SPD60 (U1).
7	CBE_N4	Tied to P_D29P_BNE (E18) of SPD60 (U1).
10	PAR64	Tied to P_D29N_BNE (E19) of SPD60 (U1).
11	PCI_AD63	Tied to P_D30P_BNE (N20) of SPD60 (U1).
12	PCI_AD62	Tied to P_D30N_BNE (N21) of SPD60 (U1).
13	PCI_AD61	Tied to P_D31P_BNE (M19) of SPD60 (U1).
16	PCI_AD60	Tied to P_D31N_BNE (M20) of SPD60 (U1).
17	PCI_AD59	Tied to P_D32P_BNE (L21) of SPD60 (U1).
18	PCI_AD58	Tied to P_D32N_BNE (M21) of SPD60 (U1).
19	PCI_AD57	Tied to P_D33P_BNE (K20) of SPD60 (U1).
22	PCI_AD56	Tied to P_D33N_BNE (K21) of SPD60 (U1).
23	PCI_AD55	Tied to P_D34P_BNE (J20) of SPD60 (U1).
24	PCI_AD54	Tied to P_D34N_BNE (J21) of SPD60 (U1).
25	PCI_AD53	Tied to P_D3N_BNE (G21) of SPD60 (U1).
28	PCI_AD52	Tied to P_D35N_BNE (H21) of SPD60 (U1).
29	PCI_AD51	Tied to P_D36P_BNE (F20) of SPD60 (U1).
30	PCI_AD50	Tied to P_D36N_BNE (G20) of SPD60 (U1).
31	PCI_AD49	Tied to P_D37P_BNE (E21) of SPD60 (U1).
34	PCI_AD48	Tied to P_D37N_BNE (F21) of SPD60 (U1).
35	PCI_AD47	Tied to P_D38P_BNE (D21) of SPD60 (U1).
36	PCI_AD46	Tied to P_D38N_BNE (D22) of SPD60 (U1).
37	PCI_AD45	Tied to P_D39P_BNE (F22) of SPD60 (U1).
40	PCI_AD44	Tied to P_D3N_BNE (G22) of SPD60 (U1).
41	PCI_AD43	Tied to P_D40P_BNE (J22) of SPD60 (U1).
42	PCI_AD42	Tied to P_D40N_BNE (K22) of SPD60 (U1).
43	PCI_AD41	Tied to P_D41P_BNE (M22) of SPD60 (U1).
46	PCI_AD40	Tied to P_D41N_BNE (N22) of SPD60 (U1).
47	PCI_AD39	Tied to P_D41N_BNW (N23) of SPD60 (U1).
48	PCI_AD38	Tied to P_D41P_BNW (M23) of SPD60 (U1).
49	PCI_AD37	Tied to P_D40N_BNW (K23) of SPD60 (U1).
52	PCI_AD36	Tied to P_D40P_BNW (J23) of SPD60 (U1).
53	PCI_AD35	Tied to P_D39N_BNW (G23) of SPD60 (U1).

Table 4-20: *PMC Connector (JN1, JN2 and JN3) (Continued)*

Pin	Signal	Connection
54	PCI_AD34	Tied to P_D39P_BNW (F23) of SPD60 (U1).
55	PCI_AD33	Tied to P_D38N_BNW (D23) of SPD60 (U1).
58	PCI_AD32	Tied to P_D38P_BNW (D24) of SPD60 (U1).

High-Speed Expansion Connectors (J28, J29, and J30)

The SDK60 is equipped with three high-speed expansion slot connectors at J28, J289 and J30. These interfaces allow for interfacing custom cards, using a high-speed differential signaling (LVDS and LDT). Each of these expansion slots are connected to a single 96-pin bank of the FPGA. Each connector includes ground, a 5V supply, plus a selectable 1,2V, 2.5V or 3.3V supply (set via **"High-Speed Expansion Slot Voltage Select (J80)"**) in addition to the data pins.

Note: *The connector used is the Samtec QTE-040-02-F-D-A-GP. For best mechanical fit, daughter-card size is recommended to not exceed 2.25" x 5".*

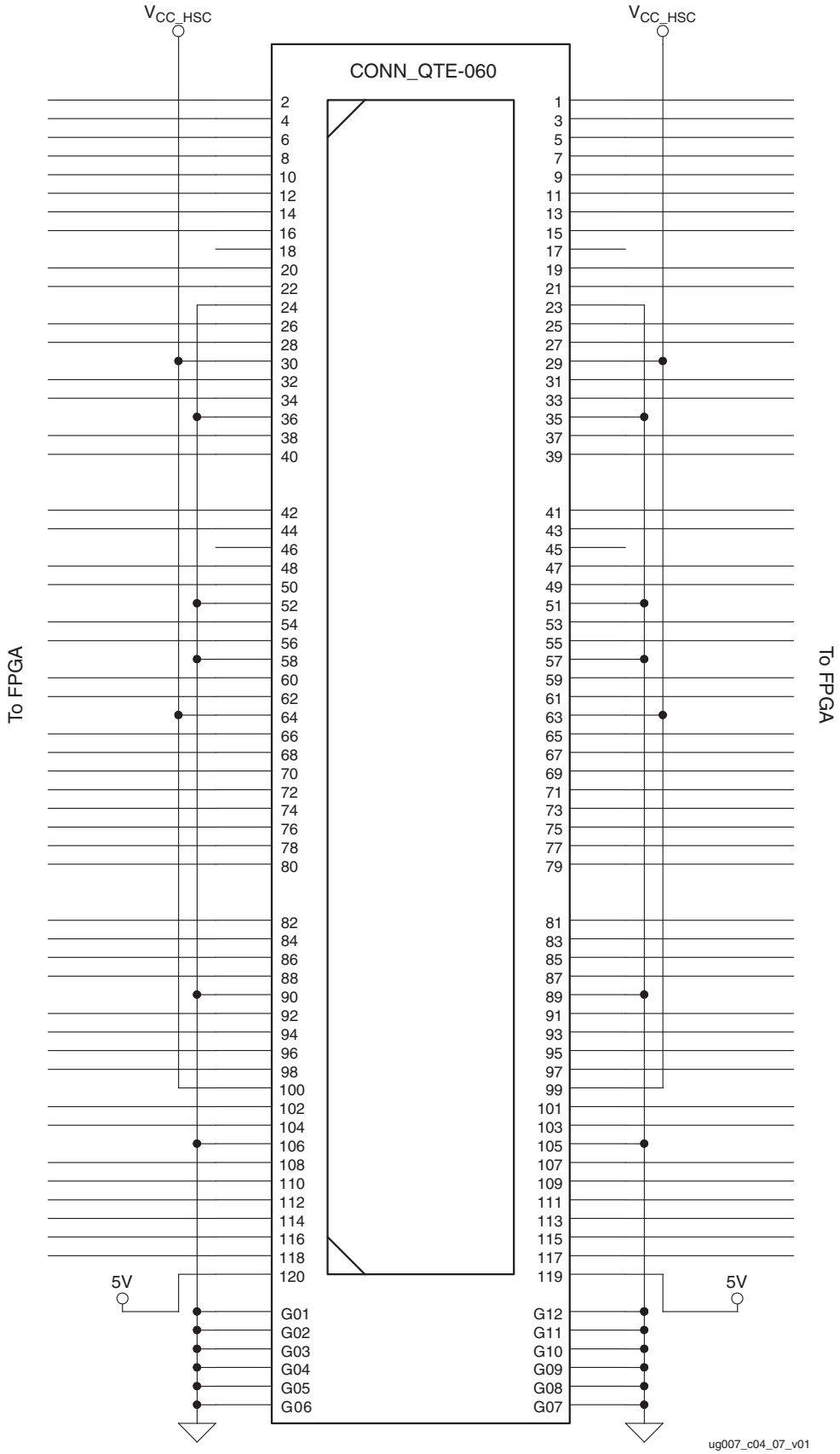


Figure 4-11: *High-Speed Expansion Slot Connector*

Table 4-21: *High-Speed Expansion Connectors (J28)*

Pin	Connection
1	Tied to P_D1P_CB4 (M32) of SPD60 (U1).(1)
2	Tied to P_D1P_B4 (AV10) of SPD60 (U1).
3	Tied to P_D1N_CB4 (M31) of SPD60 (U1).(1)
4	Tied to P_D1N_B4 (AU10) of SPD60 (U1).
5	Tied to P_D2P_B4 (AT10) of SPD60 (U1).
6	Tied to P_D3P_B4 (AV9) of SPD60 (U1).
7	Tied to P_D2N_B4 (AR10) of SPD60 (U1).
8	Tied to P_D3N_B4 (AU9) of SPD60 (U1).
9	Tied to P_D4P_B4 (AT11) of SPD60 (U1).
10	Tied to P_D5P_B4 (AT9) of SPD60 (U1).
11	Tied to P_D4N_B4 (AR11) of SPD60 (U1).
12	Tied to P_D5N_B4 (AR9) of SPD60 (U1).
13	Tied to P_D6P_B4 (AV7) of SPD60 (U1).
14	Tied to P_D7P_B4 (AV6) of SPD60 (U1).
15	Tied to P_D22N_B4 (AJ8) of SPD60 (U1).
16	Tied to P_D7N_B4 (AU6) of SPD60 (U1).
19	Tied to P_D8P_B4 (AT6) of SPD60 (U1).
20	Tied to P_D9P_B4 (AT7) of SPD60 (U1).
21	Tied to P_D8N_B4 (AR6) of SPD60 (U1).
22	Tied to P_D9N_B4 (AR7) of SPD60 (U1).
25	Tied to P_D10P_B4 (AV5) of SPD60 (U1).
26	Tied to P_D11P_B4 (AT5) of SPD60 (U1).
27	Tied to P_D10N_B4 (AU5) of SPD60 (U1).
28	Tied to P_D11N_B4 (AR5) of SPD60 (U1).
31	Tied to P_D12P_B4 (AP11) of SPD60 (U1).
32	Tied to P_D13P_B4 (AM11) of SPD60 (U1).
33	Tied to P_D12N_B4 (AN11) of SPD60 (U1).
34	Tied to P_D13N_B4 (AL11) of SPD60 (U1).
37	Tied to P_D14P_B4 (AM10) of SPD60 (U1).
38	Tied to P_D15P_B4 (AP10) of SPD60 (U1).
39	Tied to P_D14N_B4 (AL10) of SPD60 (U1).
40	Tied to P_D15N_B4 (AN10) of SPD60 (U1).
41	Tied to P_D16P_B4 (AK11) of SPD60 (U1).
42	Tied to P_D17P_B4 (AK10) of SPD60 (U1).
43	Tied to P_D16N_B4 (AJ11) of SPD60 (U1).
44	Tied to P_D17N_B4 (AJ10) of SPD60 (U1).
47	Tied to P_D18P_B4 (AP8) of SPD60 (U1).
48	Tied to P_D19P_B4 (AM8) of SPD60 (U1).

Table 4-21: *High-Speed Expansion Connectors (J28) (Continued)*

Pin	Connection
49	Tied to P_D18N_B4 (AN8) of SPD60 (U1).
50	Tied to P_D19N_B4 (AL8) of SPD60 (U1).
53	Tied to P_D20P_B4 (AM7) of SPD60 (U1).
54	Tied to P_D21P_B4 (AP7) of SPD60 (U1).
55	Tied to P_D20N_B4 (AL7) of SPD60 (U1).
56	Tied to P_D21N_B4 (AN7) of SPD60 (U1).
59	Tied to P_D22P_B4 (AK8) of SPD60 (U1).
60	Tied to P_D2P_CB4 (L33) of SPD60 (U1).(1)
61	Tied to P_D22N_B4 (AJ8) of SPD60 (U1).
62	Tied to P_D2N_CB4 (L32) of SPD60 (U1).(1)
65	Tied to P_D24P_B4 (AP6) of SPD60 (U1).
66	Tied to P_D25P_B4 (AM6) of SPD60 (U1).
67	Tied to P_D24N_B4 (AN6) of SPD60 (U1).
68	Tied to P_D25N_B4 (AL6) of SPD60 (U1).
69	Tied to P_D26P_B4 (AM5) of SPD60 (U1).
70	Tied to P_D27P_B4 (AP5) of SPD60 (U1).
71	Tied to P_D26N_B4 (AL5) of SPD60 (U1).
72	Tied to P_D27N_B4 (AN5) of SPD60 (U1).
73	Tied to P_D28P_B4 (AK6) of SPD60 (U1).
74	Tied to P_D29P_B4 (AK5) of SPD60 (U1).
75	Tied to P_D28N_B4 (AJ6) of SPD60 (U1).
76	Tied to P_D29N_B4 (AJ5) of SPD60 (U1).
77	Tied to P_D30P_B4 (AN4) of SPD60 (U1).
78	Tied to P_D31P_B4 (AM2) of SPD60 (U1).
79	Tied to P_D30N_B4 (AN3) of SPD60 (U1).
80	Tied to P_D31N_B4 (AM1) of SPD60 (U1).
81	Tied to P_D32P_B4 (AL2) of SPD60 (U1).
82	Tied to P_D33P_B4 (AL4) of SPD60 (U1).
83	Tied to P_D32N_B4 (AL1) of SPD60 (U1).
84	Tied to P_D33N_B4 (AL3) of SPD60 (U1).
85	Tied to P_D34P_B4 (AK4) of SPD60 (U1).
86	Tied to P_D35P_B4 (AK2) of SPD60 (U1).
87	Tied to P_D34N_B4 (AK3) of SPD60 (U1).
88	Tied to P_D35N_B4 (AK1) of SPD60 (U1).
91	Tied to P_D36P_B4 (AJ4) of SPD60 (U1).
92	Tied to P_D37P_B4 (AJ2) of SPD60 (U1).
93	Tied to P_D36N_B4 (AJ3) of SPD60 (U1).
94	Tied to P_D37N_B4 (AJ1) of SPD60 (U1).

Table 4-21: *High-Speed Expansion Connectors (J28) (Continued)*

Pin	Connection
95	Tied to P_D38P_B4 (AH2) of SPD60 (U1).
96	Tied to P_D39P_B4 (AG4) of SPD60 (U1).
97	Tied to P_D38N_B4 (AH1) of SPD60 (U1).
98	Tied to P_D39N_B4 (AG3) of SPD60 (U1).
101	Tied to P_D40P_B4 (AG2) of SPD60 (U1).
102	Tied to P_D41P_B4 (AF2) of SPD60 (U1).
103	Tied to P_D40N_B4 (AG1) of SPD60 (U1).
104	Tied to P_D41N_B4 (AF1) of SPD60 (U1).
107	Tied to P_D42P_B4 (AH11) of SPD60 (U1).
108	Tied to P_D42N_B4 (AG11) of SPD60 (U1).
109	Tied to P_D43P_B4 (AF11) of SPD60 (U1).
110	Tied to P_D43N_B4 (AE11) of SPD60 (U1).
111	Tied to P_D44P_B4 (AH10) of SPD60 (U1).
112	Tied to P_D44N_B4 (AG10) of SPD60 (U1).
113	Tied to P_D45P_B4 (AF10) of SPD60 (U1).
114	Tied to P_D45N_B4 (AE10) of SPD60 (U1).
115	Tied to P_D46P_B4 (AD11) of SPD60 (U1).
116	Tied to P_D46N_B4 (AC11) of SPD60 (U1).
117	Tied to P_D47P_B4 (AD10) of SPD60 (U1).
118	Tied to P_D47N_B4 (AC10) of SPD60 (U1).

Notes:
1. These pins have special termination. See **Figure 4-12**.

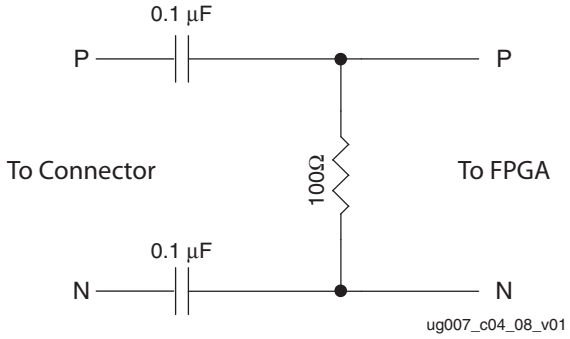


Figure 4-12: *Special Termination*

Table 4-22: *High-Speed Expansion Connectors (J29)*

Pin	Connection
1	Tied to P_D47P_B5 (AH48) of SPD60 (U1).
2	Tied to P_D46P_B5 (AF8) of SPD60 (U1).
3	Tied to P_D47N_B5 (AG8) of SPD60 (U1).
4	Tied to P_D46N_B5 (AE8) of SPD60 (U1).
5	Tied to P_D45P_B5 (AH7) of SPD60 (U1).
6	Tied to P_D44P_B5 (AF7) of SPD60 (U1).
7	Tied to P_D45N_B5 (AG7) of SPD60 (U1).
8	Tied to P_D44N_B5 (AE7) of SPD60 (U1).
9	Tied to P_D43P_B5 (AD8) of SPD60 (U1).
10	Tied to P_D42P_B5 (AD7) of SPD60 (U1).
11	Tied to P_D43N_B5 (AC8) of SPD60 (U1).
12	Tied to P_D42N_B5 (AC7) of SPD60 (U1).
13	Tied to P_D41P_B5 (AH5) of SPD60 (U1).
14	Tied to P_D40P_B5 (AF6) of SPD60 (U1).
15	Tied to P_D41N_B5 (AG5) of SPD60 (U1).
16	Tied to P_D40N_B5 (AE6) of SPD60 (U1).
19	Tied to P_D39P_B5 (AF5) of SPD60 (U1).
20	Tied to P_D38P_B5 (AD5) of SPD60 (U1).
21	Tied to P_D39N_B5 (AE5) of SPD60 (U1).
22	Tied to P_D38N_B5 (AC5) of SPD60 (U1).
25	Tied to P_D37P_B5 (AB6) of SPD60 (U1).
26	Tied to P_D36P_B5 (AB5) of SPD60 (U1).
27	Tied to P_D37N_B5 (AA6) of SPD60 (U1).
28	Tied to P_D36N_B5 (AA5) of SPD60 (U1).
31	Tied to P_D35P_B5 (AF4) of SPD60 (U1).
32	Tied to P_D34P_B5 (AE4) of SPD60 (U1).
33	Tied to P_D35N_B5 (AF3) of SPD60 (U1).
34	Tied to P_D34N_B5 (AE3) of SPD60 (U1).
37	Tied to P_D33P_B5 (AE2) of SPD60 (U1).
38	Tied to P_D32P_B5 (AD2) of SPD60 (U1).
39	Tied to P_D33N_B5 (AE1) of SPD60 (U1).
40	Tied to P_D32N_B5 (AD1) of SPD60 (U1).
41	Tied to P_D31P_B5 (AC4) of SPD60 (U1).
42	Tied to P_D30P_B5 (AC2) of SPD60 (U1).
43	Tied to P_D31N_B5 (AC3) of SPD60 (U1).
44	Tied to P_D30N_B5 (AC1) of SPD60 (U1).
47	Tied to P_D29P_B5 (AB4) of SPD60 (U1).
48	Tied to P_D28P_B5 (AB2) of SPD60 (U1).
49	Tied to P_D29N_B5 (AB3) of SPD60 (U1).

Table 4-22: *High-Speed Expansion Connectors (J29) (Continued)*

Pin	Connection
50	Tied to P_D28N_B5 (AB1) of SPD60 (U1).
53	Tied to P_D27P_B5 (AA2) of SPD60 (U1).
54	Tied to P_D26P_B5 (Y4) of SPD60 (U1).
55	Tied to P_D27N_B5 (AA1) of SPD60 (U1).
56	Tied to P_D26N_B (Y3) of SPD60 (U1).
59	Tied to P_D25P_B5 (Y2) of SPD60 (U1).
60	Tied to P_D24P_B5 (W4) of SPD60 (U1).
61	Tied to P_D25N_B5 (Y1) of SPD60 (U1).
62	Tied to P_D24N_B5 (W3) of SPD60 (U1).
65	Tied to P_D23N_B5 (W2) of SPD60 (U1).
66	Tied to P_D22N_B5 (V2) of SPD60 (U1).
67	Tied to P_D23P_B5 (W1) of SPD60 (U1).
68	Tied to P_D22P_B5 (V1) of SPD60 (U1).
69	Tied to P_D21N_B5 (V4) of SPD60 (U1).
70	Tied to P_D20N_B5 (U2) of SPD60 (U1).
71	Tied to P_D21P_B5 (V3) of SPD60 (U1).
72	Tied to P_D20P_B5 (U1) of SPD60 (U1).
73	Tied to P_D19N_B5 (T2) of SPD60 (U1).
74	Tied to P_D18N_B5 (T4) of SPD60 (U1).
75	Tied to P_D19P_B5 (T1) of SPD60 (U1).
76	Tied to P_D18P_B5 (T3) of SPD60 (U1).
77	Tied to P_D17N_B5 (AB7) of SPD60 (U1).
78	Tied to P_D16N_B5 (AB8) of SPD60 (U1).
79	Tied to P_D17P_B5 (AA7) of SPD60 (U1).
80	Tied to P_D16P_B5 (AA8) of SPD60 (U1).
81	Tied to P_D15N_B5 (Y7) of SPD60 (U1).
82	Tied to P_D14N_B5 (Y8) of SPD60 (U1).
83	Tied to P_D15P_B5 (W7) of SPD60 (U1).
84	Tied to P_D14P_B5 (W8) of SPD60 (U1).
85	Tied to P_D13N_B5 (V7) of SPD60 (U1).
86	Tied to P_D12N_B5 (V8) of SPD60 (U1).
87	Tied to P_D13P_B5 (U7) of SPD60 (U1).
88	Tied to P_D12P_B5 (U8) of SPD60 (U1).
91	Tied to P_D11N_B5 (AB10) of SPD60 (U1).
92	Tied to P_D10N_B5 (AB11) of SPD60 (U1).
93	Tied to P_D11P_B5 (AA10) of SPD60 (U1).
94	Tied to P_D10P_B5 (AA11) of SPD60 (U1).
95	Tied to P_D9N_B5 (Y11) of SPD60 (U1).
96	Tied to P_D8N_B5 (Y10) of SPD60 (U1).

Table 4-22: *High-Speed Expansion Connectors (J29) (Continued)*

Pin	Connection
97	Tied to P_D9P_B5 (W11) of SPD60 (U1).
98	Tied to P_D8P_B5 (W10) of SPD60 (U1).
101	Tied to P_D7N_B5 (V10) of SPD60 (U1).
102	Tied to P_D6N_B5 (V11) of SPD60 (U1).
103	Tied to P_D7P_B5 (U10) of SPD60 (U1).
104	Tied to P_D6P_B5 (U11) of SPD60 (U1).
107	Tied to P_D5N_B5 (Y5) of SPD60 (U1).
108	Tied to P_D5P_B5 (W5) of SPD60 (U1).
109	Tied to P_D4N_B5 (Y6) of SPD60 (U1).
110	Tied to P_D4P_B5 (W6) of SPD60 (U1).
111	Tied to P_D3N_B5 (U6) of SPD60 (U1).
112	Tied to P_D3P_B5 (T6) of SPD60 (U1).
113	Tied to P_D2N_B5 (V5) of SPD60 (U1).
114	Tied to P_D2P_B5 (U5) of SPD60 (U1).
115	Tied to P_D1N_B5 (T5) of SPD60 (U1).
116	Tied to P_D1P_B5 (R5) of SPD60 (U1).
117	Tied to P_D0N_B5 (R6) of SPD60 (U1).
118	Tied to P_D0P_B5 (P6) of SPD60 (U1).

Table 4-23: *High-Speed Expansion Connectors (J30)*

Pin	Connection
1	Tied to P_D47N_B6 (R2) of SPD60 (U1).
2	Tied to P_D46N_B6 (R4) of SPD60 (U1).
3	Tied to P_D47P_B6 (R1) of SPD60 (U1).
4	Tied to P_D46P_B6 (R3) of SPD60 (U1).
5	Tied to P_D45N_B6 (P2) of SPD60 (U1).
6	Tied to P_D44N_B6 (P4) of SPD60 (U1).
7	Tied to P_D45P_B6 (P1) of SPD60 (U1).
8	Tied to P_D44P_B6 (P3) of SPD60 (U1).
9	Tied to P_D43N_B6 (N2) of SPD60 (U1).
10	Tied to P_D42N_B6 (M4) of SPD60 (U1).
11	Tied to P_D43P_B6 (N1) of SPD60 (U1).
12	Tied to P_D42P_B6 (M3) of SPD60 (U1).
13	Tied to P_D41N_B6 (T7) of SPD60 (U1).
14	Tied to P_D40N_B6 (T8) of SPD60 (U1).
15	Tied to P_D41P_B6 (R7) of SPD60 (U1).
16	Tied to P_D40P_B6 (R8) of SPD60 (U1).
19	Tied to P_D39N_B6 (P8) of SPD60 (U1).
20	Tied to P_D38N_B (P7) of SPD60 (U1).

Table 4-23: *High-Speed Expansion Connectors (J30) (Continued)*

Pin	Connection
21	Tied to P_D39P_B6 (N8) of SPD60 (U1).
22	Tied to P_D38P_B6 (N7) of SPD60 (U1).
25	Tied to P_D37N_B6 (M7) of SPD60 (U1).
26	Tied to P_D36N_B6 (M8) of SPD60 (U1).
27	Tied to P_D37P_B6 (L7) of SPD60 (U1).
28	Tied to P_D36P_B6 (L8) of SPD60 (U1).
31	Tied to P_D35N_B6 (T10) of SPD60 (U1).
32	Tied to P_D34N_B6 (T11) of SPD60 (U1).
33	Tied to P_D35P_B6 (R10) of SPD60 (U1).
34	Tied to P_D34P_B6 (R11) of SPD60 (U1).
37	Tied to P_D33N_B6 (P11) of SPD60 (U1).
38	Tied to P_D32N_B6 (P10) of SPD60 (U1).
39	Tied to P_D33P_B6 (N11) of SPD60 (U1).
40	Tied to P_D32P_B6 (N10) of SPD60 (U1).
41	Tied to P_D31N_B6 (M10) of SPD60 (U1).
42	Tied to P_D30N_B6 (M11) of SPD60 (U1).
43	Tied to P_D31P_B6 (L10) of SPD60 (U1).
44	Tied to P_D30P_B6 (L11) of SPD60 (U1).
47	Tied to P_D29N_B6 (N5) of SPD60 (U1).
48	Tied to P_D28N_B6 (L5) of SPD60 (U1).
49	Tied to P_D29P_B6 (M5) of SPD60 (U1).
50	Tied to P_D28P_B6 (K5) of SPD60 (U1).
53	Tied to P_D27N_B6 (L6) of SPD60 (U1).
54	Tied to P_D26N_B6 (J6) of SPD60 (U1).
55	Tied to P_D27P_B6 (K6) of SPD60 (U1).
56	Tied to P_D26P_B6 (H6) of SPD60 (U1).
59	Tied to P_D25N_B6 (J5) of SPD60 (U1).
60	Tied to P_D24N_B6 (G6) of SPD60 (U1).
61	Tied to P_D25P_B6 (H5) of SPD60 (U1).
62	Tied to P_D24P_B6 (F6) of SPD60 (U1).
65	Tied to P_D23N_B6 (M2) of SPD60 (U1).
66	Tied to P_D22N_B6 (L2) of SPD60 (U1).
67	Tied to P_D23P_B6 (M1) of SPD60 (U1).
68	Tied to P_D22P_B6 (L1) of SPD60 (U1).
69	Tied to P_D21N_B6 (L4) of SPD60 (U1).
70	Tied to P_D20N_B6 (K2) of SPD60 (U1).
71	Tied to P_D21P_B6 (L3) of SPD60 (U1).
72	Tied to P_D20P_B6 (K1) of SPD60 (U1).
73	Tied to P_D19N_B6 (K4) of SPD60 (U1).

Table 4-23: *High-Speed Expansion Connectors (J30) (Continued)*

Pin	Connection
74	Tied to P_D18N_B6 (J2) of SPD60 (U1).
75	Tied to P_D19P_B6 (K3) of SPD60 (U1).
76	Tied to P_D18P_B6 (J1) of SPD60 (U1).
77	Tied to P_D17N_B6 (H2) of SPD60 (U1).
78	Tied to P_D16N_B6 (H4) of SPD60 (U1).
79	Tied to P_D17P_B6 (H1) of SPD60 (U1).
80	Tied to P_D16P_B6 (H3) of SPD60 (U1).
81	Tied to P_D15N_B6 (G2) of SPD60 (U1).
82	Tied to P_D14N_B6 (G4) of SPD60 (U1).
83	Tied to P_D15P_B6 (G1) of SPD60 (U1).
84	Tied to P_D14P_B6 (G3) of SPD60 (U1).
85	Tied to P_D13N_B6 (G5) of SPD60 (U1).
86	Tied to P_D12N_B6 (F4) of SPD60 (U1).
87	Tied to P_D13P_B6 (F5) of SPD60 (U1).
88	Tied to P_D12P_B6 (F3) of SPD60 (U1).
91	Tied to P_D11N_B6 (K8) of SPD60 (U1).
92	Tied to P_D10N_B6 (K7) of SPD60 (U1).
93	Tied to P_D11P_B6 (J8) of SPD60 (U1).
94	Tied to P_D10P_B6 (J7) of SPD60 (U1).
95	Tied to P_D0P_B5 (H8) of SPD60 (U1).
96	Tied to P_D8N_B6 (H7) of SPD60 (U1).
97	Tied to P_D9P_B6 (G8) of SPD60 (U1).
98	Tied to P_D8P_B6 (G7) of SPD60 (U1).
101	Tied to P_D7N_B6 (F7) of SPD60 (U1).
102	Tied to P_D6N_B6 (F8) of SPD60 (U1).
103	Tied to P_D7P_B6 (E7) of SPD60 (U1).
104	Tied to P_D6P_B6 (E8) of SPD60 (U1).
105	Tied to P_D5N_B6 (K10) of SPD60 (U1).
106	Tied to P_D4N_B6 (K11) of SPD60 (U1).
107	Tied to P_D5P_B6 (J10) of SPD60 (U1).
108	Tied to P_D4P_B6 (J11) of SPD60 (U1).
111	Tied to P_D3N_B6 (H11) of SPD60 (U1).
112	Tied to P_D2N_B6 (H10) of SPD60 (U1).
113	Tied to P_D3P_B6 (G11) of SPD60 (U1).
114	Tied to P_D2P_B6 (G10) of SPD60 (U1).
115	Tied to P_D1N_B6 (F10) of SPD60 (U1).
116	Tied to P_D0N_B6 (F11) of SPD60 (U1).
117	Tied to P_D1P_B (E10) of SPD60 (U1).
118	Tied to P_D0P_B6 (E11) of SPD60 (U1).

User Interfaces

The SDK60 has three headers used for general purpose interfaces to the FPGA. While these are often used for specific purposes by Achronix-supplied demos, they are available for customer use.

Utility (J75)

Table 4-24: *Utility Interface (J75)*

Pin	Connection
1	Tied to P_D33N_BNW (K24) of SPD60 (U1).
2	Tied to P_D33P_BNW (K25) of SPD60 (U1).
3	Tied to P_D32N_BNW (M24) of SPD60 (U1).
4	Tied to P_D32P_BNW (L25) of SPD60 (U1).
5	Tied to P_D31N_BNW (M25) of SPD60 (U1).
6	Tied to P_D31P_BNW (M26) of SPD60 (U1).

LCD (J76)

For some Achronix-supplied demos, J76 serves as the LCD interface.

Table 4-25: *LCD Interface (J76)*

Pin	Connection
1	Tied to P_D30N_BNW (N24) of SPD60 (U1).
2	Tied to P_D30P_BNW (N25) of SPD60 (U1).
3	Tied to P_D29N_BNW (E26) of SPD60 (U1).
4	Tied to P_D29P_BNW (E27) of SPD60 (U1).
5	Tied to P_D28N_BNW (F26) of SPD60 (U1).
6	Tied to P_D28P_BNW (F27) of SPD60 (U1).

RS-232 Interface (P1)

The DB-9 connector at P1 provides an RS-232 access to the FPGA. The mode of the interface is set via **"RS-232 Mode Select (J86),"** on page 13.

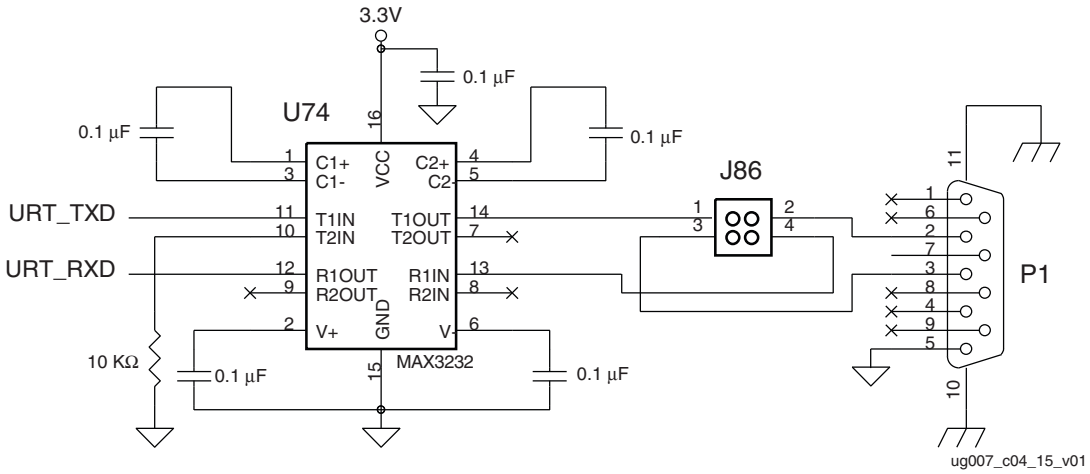


Figure 4-13: *RS-232 Interface (P1)*

Table 4-26: *RS-232 Interface (P1) Pinout*

Pin	Connection
1	–
2	Receive data (URT_RXD connects to P_D27N_BNW (G26) of SPD60)
3	Transmit data (URT_TXD connects to P_D27P_BNW (G27) of SPD60)
4	–
5	GND
6	–
7	–
8	–
9	–
10	Frame ground
11	Frame ground

Other Interfaces

AMC JTAG Connector (J40)

JTAG interface for AMC applications, independent of **"FPGA JTAG Connector (J49)."**

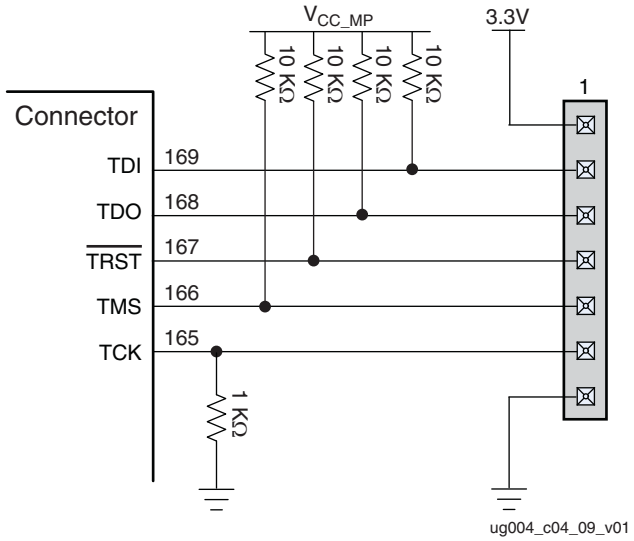


Figure 4-14: *AMC JTAG Connector (J40)*

Table 4-27: *AMC JTAG Connector (J40)*

Header Pin	Connector Pin	Signal
1	–	3.3V
2	165	TCK
3	166	TMS
4	167	$\overline{\text{TRST}}$
5	168	TDO
6	169	TDI
7	–	GND

AVR Controller SPI (J47)

J47 (a 5 x 2 header) is the SPI interface to the AVR controller.

Table 4-28: *AVR SPI Interface (J47)*

Pin	Signal
1	SCK
2	GND
3	PDO
4	VDD
5	RSTN

Table 4-28: *AVR SPI Interface (J47) (Continued)*

Pin	Signal
6	–
7	–
8	–
9	PDI
10	GND

FPGA JTAG Connector (J49)

J49 is the JTAG connector for programming the FPGA with the Bitporter. Refer to *ACE Programming Guide* (UG004) for details on programming the SPD60 with the Bitporter.

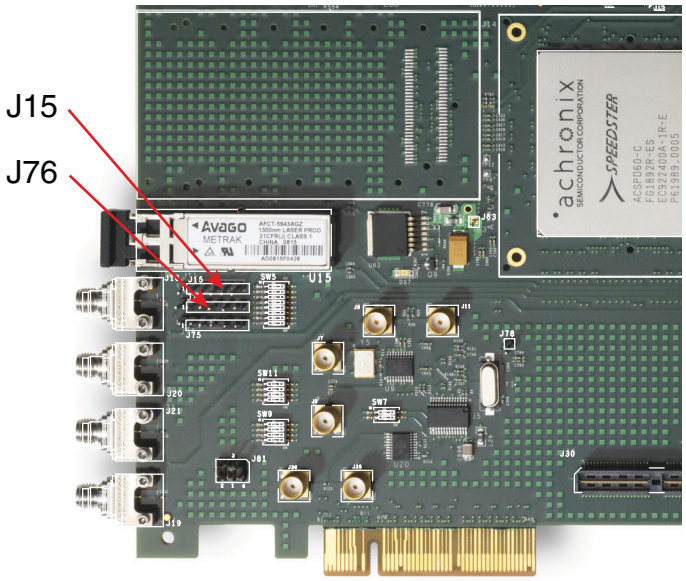


Figure 4-15: *FPGA JTAG Connector (J49)*

AVR Controller RS-232 (J50)

Table 4-29: *AVR Controller RS-232 (J50)*

Pin	Signal	Connection
1	–	–
2	–	–
3	TXD	Tied to TXD0/PE1(3) of AVR (U17)
4	RXD	Tied to RXD0/PCINT8/PE0 (2) of AVR (U17)
5	GND	–
6	3.3V	–

FPGA SPI (J71)

J71 (a 5 x 2 header) is used for programming the FPGA in the serial mode. For this mode pin 1 and 3 of the header J70 should be connected/shorted (see **"Configuration Mode (J70)"** in **Chapter 3 – LEDs, Buttons, Switches and Jumpers**).

Table 4-30: *FPGA SPI Interface (J71)*

Pin	Signal
1	E_SCK
2	GND
3	E_SDO
4	VDD
5	E_CS
6	–
7	–
8	–
9	E_SDI
10	GND

Chapter 5 – SDK60 Clocking

The SDK60 provides the user with a number of programmable clock sources for the various embedded PLLs, and 5G and 10G SerDes on the SPD60. The clock sources can come from either on-board oscillators or off-board differential source via SMA connectors. Generated clocks can also be driven off-board via SMA connectors.

On-Board Clock References

The SDK60 has four on-board oscillator sources (one 33 MHz and three 100 MHz) used to drive the PLL inputs of the FPGA and supply any IEEE P1386.1 PCI Mezzanine Card (PMC) add-in cards.

Table 5-1: *On-Board Clock References*

Source	Frequency	Purpose
Oscillator 1 (Y10)	33 MHz	Drives pin P_D0P_CB3 (N12) of SPD60 (U1). Also supplies PMC Connector 1 (JN1).
Oscillator 2 (Y11)	100 Mhz	Drives pin P_D0P_CB1 (AP33) of SPD60 (U1)
Oscillator 3 (Y12)		Drives pin P_D0P_CB2 (AP12) of SPD60 (U1)
Oscillator 4 (Y13)		Drives pin P_D0P_CB4 (N33) of SPD60 (U1)

SerDes Clock Sources

The SDK60 provides programmable clock sources for each of the five quad SerDes groups on the SPD60. These clock sources are generated via either a clock synthesizer device or a combination of frequency generators and clock multipliers. Inputs can come either from crystal oscillators or externally generated sources via SMA connectors. The output of these clock sources is controlled via a number of switches.

Clock Synthesizer Sources

A clock synthesizer at U6 generates the clock course for quad E of the 10G SerDes of SPD60. These clock sources are controlled via SW6, SW8, and SW10. For complete details on the operation of the clock synthesizer (ICS843034), see the IDT *Femtoclocks™ Multi-Rate 3.3V, 2.5V LVPECL Frequency Synthesizer Data Sheet.*

The output frequency of U6 (F_{OUT}) is set by varying the VCO divider M (position 8 of SW8 plus SW10) and the output divider N (positions 2–7 of SW8). The input clock source (F_{XTAL}) is set via SW6. The output frequency is:

$$F_{OUT} = \frac{F_{XTAL} \times M}{N}$$

Note: *The VCO's range is restricted to between 560 to 750 MHz.*

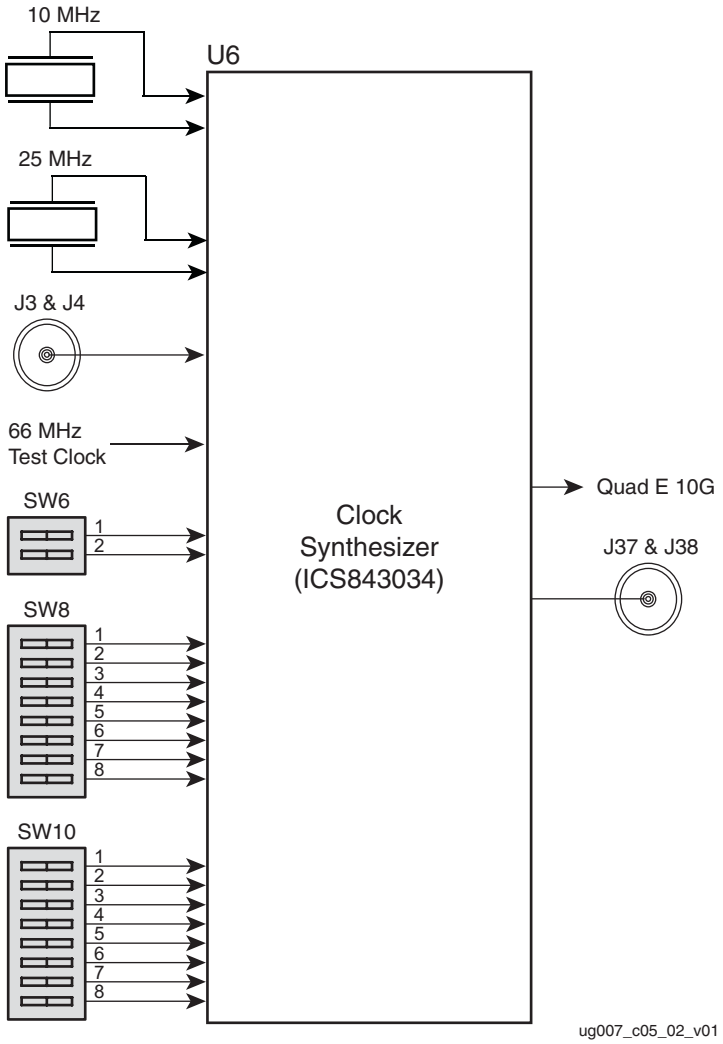


Figure 5-1: *Clock Synthesizer (U6)*

Clock Select Switch (SW6)

Table 5-2: *Clock Select (SW6) Settings*

Switch Setting		Clock Selected
Position 1	**Position 2**	
ON	ON	25 MHz crystal
ON	OFF	10 MHz Crystal
OFF	ON	Differential clock (SMA connectors J3 and J4)
OFF	OFF	66 MHz Test Clock

Notes:
1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.

Bypass and N-Divider Switch (SW8)

This switch is used for setting the PLL bypass and N-divider values.

Table 5-3: *Bypass and N-Divider Switch (SW8) Settings*

Position	Purpose	Comments
1	VCO_SEL	Determines whether synthesizer is in PLL or bypass mode: ON – bypass mode OFF – PLL mode
2	NA2	N-divider control for quad E of the 10G SerDes of SPD60 output. See **Table 5-4** for settings.
3	NA1	
4	NA0	
5	NB2	N-divider control for SMA (J37 and J38) output. See **Table 5-4** for settings
6	NB1	
7	NB0	
8	M8	M-divider input. See **Table 5-5** for M7:M0 settings.
Notes: 1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.		

Table 5-4: *N-Divider Settings*

Inputs			N Divider Value	Output Frequency (MHz)	
Nx2	Nx1	Nx0		Min	Max
ON	ON	ON	1	560	750
ON	ON	OFF	2	280	375
ON	OFF	ON	3	186.66	250
ON	OFF	OFF	4	140	187.5
OFF	ON	ON	5	112	150
OFF	ON	OFF	6	93.33	125
OFF	OFF	ON	8	70	93.75
OFF	OFF	OFF	16	35	46.875
Notes: 1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.					

M-Divider Switch (SW10)

SW10 (along with position 8 of SW8) set the M-divider values.

Table 5-5: *M-Divider Switch (SW10) Settings*

Position	Purpose	Comments
1	M7	M-divider control for quad E of the 10G SerDes of SPD60 output.
2	M6	
3	M5	
4	M4	
5	M3	
6	M2	
7	M1	
8	M0	

Notes:
1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.

Clock Frequency Generator Sources

Clock sources for the remaining quads of embedded SerDes on SPD60. These clock sources are controlled via SW7, SW9, and SW11.

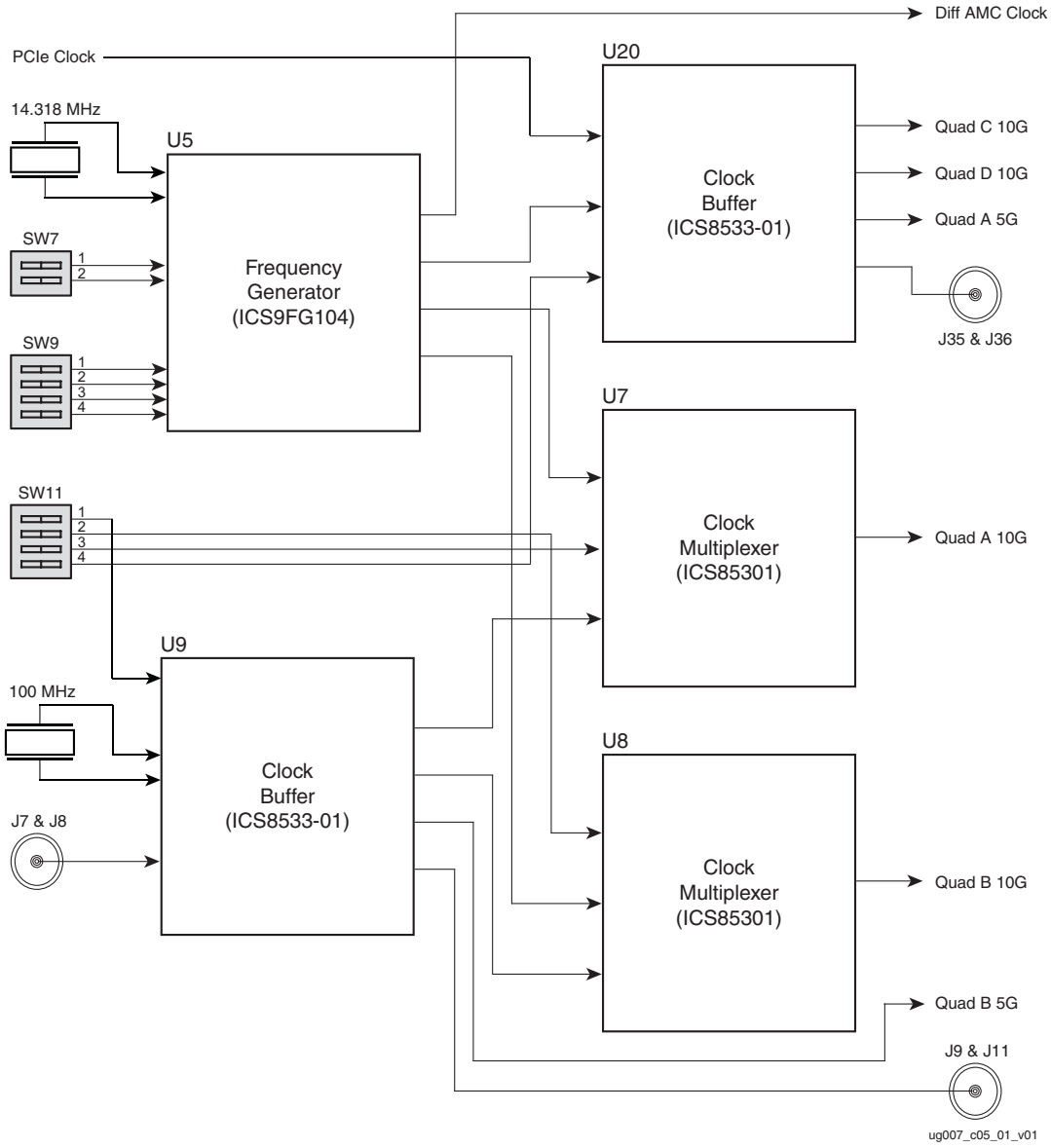


Figure 5-2: *Clock Frequency Generator*

Diff Clock Stop and Spread Spectrum Switch (SW7)

This switch is used for stopping the differential clock outputs from U5 and for enabling spread-spectrum clocking to reduce the EMI/EMC.

Table 5-6: *Diff Clock Stop and Spread Spectrum (SW7) Settings*

Position	Purpose	Comments
1	Differential clock	ON – disables the output clocks OFF – enables the output clocks
2	Spread spectrum	ON – disables spread-spectrum functionality OFF – enables spread-spectrum functionality
Notes: 1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.		

Clock Frequency Select Switch (SW9)

SW9 along with **"Clock Source Selector Switch (SW11)"** is used to select the clock sources to drive various quad SerDes groups, SMA connectors and the Advanced Mezzanine Card (AMC) connector (J12).

Table 5-7: *Clock Frequency Select (SW9) Settings*

Switch Setting				Selection
Position 1	**Position 2**	**Position 3**	**Position 4**	
OFF	–	–	–	14.318 MHz source
ON	–	–	–	25 MHz source
–	ON	ON	ON	100.00 Mhz output
–	ON	ON	OFF	125.00 Mhz output
–	ON	OFF	ON	133.33 Mhz output
–	ON	OFF	OFF	166.67 Mhz output
–	OFF	ON	ON	200.00 Mhz output
–	OFF	ON	OFF	166.67 Mhz output
–	OFF	OFF	ON	333.00 Mhz output
–	OFF	OFF	OFF	400.00 Mhz output
Notes: 1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.				

Clock Source Selector Switch (SW11)

Table 5-8: *Clock Source Selector Switch (SW11 Settings*

Position	Purpose	Comments
1	Clock source	ON – 100 MHz clock OFF – SMA conductor (J7 and J8)
2	10G Quad B clock source	ON – Clock source set by position 1 OFF – Clock source set by SW9
3	10G Quad A clock source	ON – Clock source set by position 1 OFF – Clock source set by SW9
4	5G Quad A, 10G Quad C, 10G Quad D, SMA connector (J35 and J36) clock source	ON – PCIe reference clock OFF – Clock source set by SW9
Notes: 1. A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.		

Clocking Examples

External Clock from SMA Connectors, Bypassing the Synthesizer

To select an external clock from SMA connectors J3 and J4 and bypass the frequency synthesizer U6:

- Set switch SW6, position 1–2 to OFF:ON to select the SMA input.
- Set switch SW8, position 1 to ON to bypass the PLL.

Setting 25 MHz Clock Source to Achieve 250 MHz Output

To select the 25 MHz crystal oscillator input to U6 and 250 MHz for both outputs (quad E of the 10G SerDes and SMA connectors J37 and J38):

- Set switch SW6, position 1–2 to ON:ON to select the 25 MHz crystal.
- Set switch SW8, position 1 to OFF to select PLL mode.
- Set switch SW8, positions 2–4 to ON:OFF:ON (for 10G SerDes output) and positions 5–7 to ON:OFF:ON (for SMA connectors J37 and J38) — N divider = 5.
- Set switch SW8, position 8 to ON; SW10, positions 1–8 to ON:ON:ON:OFF:OFF:OFF:OFF:ON — M divider = 30 ('000011110)

Note: *A switch setting of OFF results in a logic level '1' and ON in a logic level of '0' on the input.*

Setting Quad B 10G to 200 MHz

Setting clock frequency generator to provide the quad B of the embedded 10G SerDes with 200 MHz:

- Set switch SW7, position 1–2 to OFF:ON.
- Set switch SW9, positions 1–4 to OFF:OFF:ON:ON.
- Set switch SW11, position 2 to ON.

Chapter 6 – AVR Controller

The SDK60 comes equipped with an on-board controller, the Atmel ATmega1280 AVR microcontroller. This microcontroller comes equipped with firmware that:

- Assists in configuration of the FPGA.
- Controls power sequencing (during both power-up and power-down) of the board and any connected peripherals.
- Measures the temperature captured via the on-chip temp diode of the SPD60.
- Measures core power consumed by the SPD60.
- Provides warning and alarm messages when the FPGA temperature exceeds the warning and alarm thresholds.
- Powers down the supplies when the FPGA reaches the alarm temperature (for example, due to fan failure).

Note: *When two modules are included in the FPGA design, DCC module and LCD module, they pass temperature, power, and alarm information provided by the AVR controller to the LCD display when attached. All Achronix-supplied demo designs include these modules.*

While customers can access the features of the embedded firmware, it is not recommended that they attempt to modify the existing firmware or develop new firmware.

Peripheral Device Initialization/Communication

The AVR controller's general purpose I/O ports are used to configure different peripheral busses and attached cards supported by the SDK60, including the DDR2-SOCDIMM, PMC interface cards, and AMC interface peripherals.

Note: *Currently, only the start-up sequence for the DDR2-SOCDIMM has been verified.*

Temperature Sensing and Reporting

Each SPD60 FPGA contains a temperature-sensing diode located in the lower left corner of the die, near the configuration logic. The anode and cathode for the internal temperature sensing diode are connected to two dedicated pins (TEMP_DIODE_P and TEMP_DIODE_N).

The signals from the temperature-sensing diode are conditioned through a temperature sensing device. This conditioned signal is then fed to the AVR controller via a generic I/O port. On a periodic read of the temperature value from the sensing device, the AVR controller performs a temperature update operation (write) to the DCC module loaded in the FPGA for display to the LCD at J76 via LCD module in the FPGA.

Note: *These two modules are included in Achronix-supplied demo design, and are available for customer use.*

In addition to constantly monitoring the temperature, two alarm signals from the temperature sensing device (high and critical temperatures) are monitored by the AVR controller and passed to both the host and FPGA. If an over temperature condition is detected, the AVR controller will activate an FPGA power down sequence.

Power Measurement and Reporting

Core power consumed by SPD60 is sensed across a power resistor located in the V_{DDL} (1.0V) power supply (U21). A current sense conditioner converts the reading to an analog voltage, which is fed to one of the ADC converter of AVR controller. On a periodic read of the current value, the AVR controller performs a power update operation (write) to the DCC module loaded in the FPGA for display to the LCD at J76 via LCD module in the FPGA.

On a periodic read of the current, the AVR controller compares the value against a preset value and sends a high power alarm to the FPGA.

Power-Up Sequencing

Part of the AVR controller's code handles the proper power sequencing of the board and embedded FPGA, both during power-up and power-down. The coded sequencing and timing is set by the factory.

Chapter 7 – Targeting a Design to the SDK60

The SDK60 is intended not only as a demonstration platform, running designs created by Achronix for customer evaluation, but also as an evaluation and testing platform for customer designs. This section assumes that the board has been set-up per the *SDK60 Quick Start Guide* (UG005), and that the user is familiar with the ACE design process.

Board-Specific Design Issues

Although the SDK60 is very flexible, and showcases nearly every feature of the Speedster FPGA, it does place restrictions on designs targeted to the embedded FPGA. Any user-generated design targeting the SPD60 must take two issues into account:

- **The fixed pin-out of the FPGA**. Although many interfaces are made available, and there are a number user I/Os available, any design must respect the location and type of I/Os specified in the rest of this guide, or damage to the board and FPGA could result.
- **The available clock structure**. While the clocking structure of the SDK60 is both programmable and highly flexible, allowing the use of both on-board and off-board sources, any design targeting the FPGA is restricted to using the available clock structures (see **Chapter 5 – "SDK60 Clocking"**).

Other chapters in this guide provide a complete reference for each interface, clock, switch, jumper and LED accessible by the FPGA. To further assist customers in developing designs, the complete board schematics are available on the SDK60 CD. In addition, Achronix is developing a set of VHDL and Verilog port definitions, along with a set of I/O constraint files for customer use. Contact Achronix Technical Support for details.

Configuring the Board

SDK60 supports three different modes at for configuring the board:

- **Serial configuration mode with transition to JTAG mode**.
- **JTAG-only mode**.

Serial Configuration Mode with Transition to JTAG Mode

In this mode, the FPGA is configured from the on-board serial flash device. After configuration is complete, the FPGA can be placed in JTAG mode.

For this mode, the FPGA is programmed per **"Serial-Mode Configuration."** The Bitporter Pod is connected per *SDK60 Quick Start Guide* (UG005). Once the board is powered up and the FPGA configured, the JLOAD instruction is sent to the FPGA's TAP controller, placing the FPGA in JTAG configuration mode. New bitstreams can be download using the Bitporter Pod.

Note: *Sending the JLOAD command overrides the configuration mode set via* **"FPGA Configuration (SW12)."**

JTAG-Only Mode

In this mode, the FPGA is left unconfigured at power-up, and can be configured via JTAG.

For this mode, the FPGA is programmed per **"JTAG Configuration."**

Downloading a Design

Once a design is complete, and the appropriate bitstream is ready, the design can be downloaded to the board. This section covers how to configure the board only. Details of programming are covered in *ACE Programming Guide* (UG004).

Serial-Mode Configuration

Programming the On-Board EEPROM (U19)

[Details will be provided in the next release.]

Setting the Configuration Mode

1. Connect a jumper across pins 1 and 3 of the header **"Configuration Mode (J70)."**
2. Remove the SPI cable from the header **"FPGA SPI (J71)."**
3. Set **"FPGA Configuration (SW12)"** positions 1–3 to ON:ON:OFF for SPI x1 configuration mode
4. Power up the board. The FPGA configures from the EEPROM, lighting **"DS11"** when complete.

JTAG Configuration

1. Remove any jumpers from the header **"Configuration Mode (J70)."**
2. Set **"FPGA Configuration (SW12)"** positions 1–3 to ON:ON:ON to leave the FPGA unconfigured at power-up.
3. Connect the Bitporter Pod to **"FPGA JTAG Connector (J49)."** Power up the board.

FPGA configuration can now be accomplished per *ACE Programming Guide* (UG004) and *SDK60 Quick Start Guide* (UG005).

Revision History

The following table lists the revision history of this document.

Version	Revision
1.0	Initial release version.
1.1	Updated **"What is Included"** in **Chapter 1 – SDK60 Overview**.
1.2	• Removed **"What is Included"** in **Chapter 1 – SDK60 Overview.** • Updated **Table 2-1**, page 4. • Updated **Figure 2-2**, page 6. • Added **"RS-232 Mode Select (J86)"** in **Chapter 3 – LEDs, Buttons, Switches and Jumpers** and **"RS-232 Interface (P1),"** on page 47.
1.3	• Minor corrections made. • Updated **Table 2-1**, page 4. • Updated **Figure 2-2**, page 6 and **Figure 4-1**, page 15. • Removed **"SPD60 Reference Board Application"** in **Chapter 6 – AVR Controller**. • Removed CPU configuration support.

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