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M340

CompactFlash M-module

User Manual

Version 1.0

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1. INTRODUCTION

1.1. VALIDITY OF THE MANUAL

This document is of revision 1.0 and provides information on the use of the M340/R0.x

The M-module revision number is composed as Rx.y where x is the revision of the PCB and y is the revision of the FPGA firmware.

1.2. PURPOSE

This manual serves as instruction for the operation of the M340 CompactFlash M-module, the connection of CompactFlash cards and the integration on an M-module carrier. Furthermore it gives the user additional information for special applications and configurations of the product.
Detailed information concerning the individual assemblies (data sheets etc.) are not part of this manual. This manual also contains a description of the provided example software.

1.3. SCOPE

The scope of this manual is the usage of the M340 CompactFlash M-module and the APIS based example software written in ANSI-C.

1.4. DEFINITIONS, ACRONYMS AND ABBREVIATIONS

AcQ	AcQuisition Technology bv
APIS	AcQ Platform Interface Software
CF	CompactFlash
ESD	Electronic Static Discharge
FPGA	Field-Programmable Gate Array
M-module	Mezzanine I/O concept according to the M-module specification
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

1.5. NOTES CONCERNING THE NOMENCLATURE

Hex numbers are marked with a leading “0x”-sign: for example: 0x20 or 0xff.

File names are represented in italic: *filename.txt*.

Code examples are printed in `courier`.

Active-low signals are represented by a trailing asterisks (i.e. IACK*).

1.6. OVERVIEW

In chapter two a short description of the M340 hardware can be found. The next chapter covers the installation and setup of the M-module as well as the connection of the CompactFlash card. In chapter 4 the operation and usage of the M340 is described in detail. AcQ provides APIS based example software for the M340, the software is described in chapter 5. Finally this document contains an Annex containing a bibliography, component image, technical data and the document history.

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2. PRODUCT OVERVIEW

2.1. INTRODUCTION

The M340 CompactFlash M-module is used to add a CompactFlash card slot to any platform supporting the M-module standard. In combination with a appropriate carrier, VMEbus, PCI and CPCI bus systems are fully supported.

CompactFlash is a small form factor card standard that encompasses CompactFlash (CF) flash data storage cards, magnetic disk cards and I/O cards. The M340 supports all of these types CompactFlash cards.

One type I or type II CompactFlash (CF) or CF+ card interface slot with hot swap capabilities and low voltage support is available on the M340.

The CompactFlash card is located at the front of the M-module and as such can be inserted or removed without disassembling the system

2.2. TECHNICAL OVERVIEW

Below an overview of the functionality of the M340 is listed:

- CompactFlash (CF) and CompactFlash+ (CF+) compatible
- Type I and Type II card compatible
- MicroDrive compatible
- Low voltage support, 3.3V and 5V cards
- Hot socketing
- Card accessible through frontpanel
- Host Controller configurable for Memory mode or I/O mode
- Two individually configurable windows for accessing the CompactFlash card
- Host interrupts supported.
- A08/D16 M-module interface.
- Identification EEPROM.

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3. INSTALLATION AND SETUP

3.1. UNPACKING THE HARDWARE

The hardware is shipped in an ESD protective container. Before unpacking the hardware, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti static table covers.
- If handling the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

IMPORTANT: Never put the hardware on top of the conductive plastic bag in which the hardware is shipped. The external surface of this bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is static dissipative.)

Inspect the hardware to verify that no mechanical damage appears to have occurred. Please report any discrepancies or damage to your distributor or to AcQuisition Technology immediately and do not install the hardware.

3.2. CARD SLOT PIN-ASSIGNMENT

This section describes the pin-assignments of the CompactFlash or CF+ card connector. The connector consists of two rows of 25 male contacts each on 50 mil (1.27 mm) centers.

Pin Number	Signal Name	Pin Number	Signal Name
1	GND	26	CD1*
2	D03	27	D11
3	D04	28	D12
4	D05	29	D13
5	D06	30	D14
6	D07	31	D15
7	CE1*	32	CE2*
8	A10*	33	VS1
9	OE*	34	IORD*
10	a09	35	IOWR*
11	A08	36	WE*
12	A07	37	RDY/BSY

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Pin Number	Signal Name	Pin Number	Signal Name
13	VCC	38	VCC
14	A06	39	CSEL*
15	A05	40	VS2
16	A04	41	RESET
17	A03	42	WAIT*
18	A02	43	INPACK*
19	A01	44	REG*
20	A00	45	BVD2
21	D00	46	BVD1
22	D01	47	D08
23	D02	48	D09
24	WP	49	D10
25	CD2*	50	GND

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4. FUNCTIONAL DESCRIPTION

4.1. BLOCK DIAGRAM

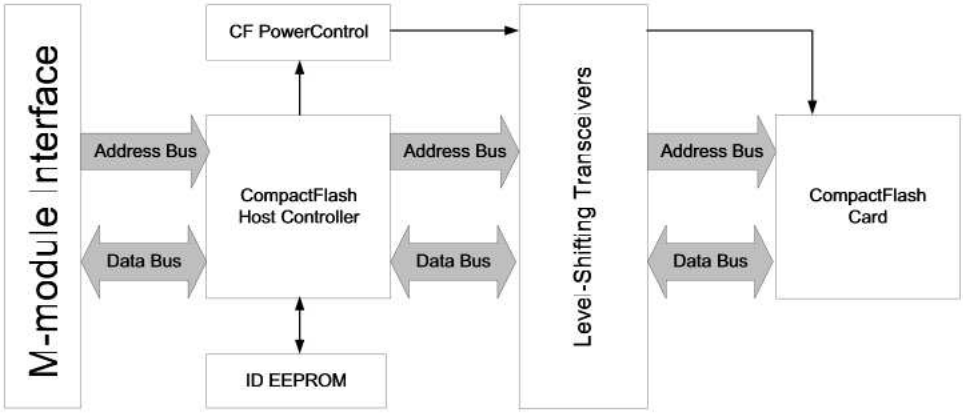


Figure 1 M340 Block Diagram

4.2. QUICK OVERVIEW

This section gives a quick overview of the address-map and on-card registers of the M340 CompactFlash M-module.

4.2.1. ADDRESS MAP OVERVIEW

The following table will give an overview of the address-map of the M340. The address-map as shown below gives an offset instead of an absolute address, since the absolute address is depending on the carrier on which the M340 is mounted.

Offset Range	Size	Width	Description
0x00-0x3F	0x40	16-bit	Window 0
0x40-0x7F	0x40	16-bit	Window 1
0x80-0xEF	0x70	16-bit	Reserved
0xF0-0xFF	0x10	8-bit Odd	Control Registers

4.2.2. CONTROL REGISTER OVERVIEW

The following table will give an overview of the on-card Control registers. Although the actual width of the M340 M-module bus is 16-bit wide, all registers are 8-bit wide and located at an odd byte address boundary (D7-D0).

Note: To avoid endianess problems it is best to access the on-card Control registers with 16-bit accesses at 16-bit address boundaries. This way the Control registers are located at the LSB of the 16-bit word.

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Mnemonic	Offset	Register bit description							
		MSB							LSB
		7	6	5	4	3	2	1	0
CFCTRLR	0xF3	RES	RES	RES	RES	RES	RES	RST	MIO
CFIER	0xF5	RES	RES	STCHIE	BCD2IE	BCD1IE	CDIE	WPIE	RDYIE
CFISR	0xF7	RES	RES	CDCHGACK	RES	STCHG	CD	RES	CIRQ
CFPWRLEDR	0xF9	RES	RES	VS2	VS1	LEDM	LEDE	V5E	V3E
CFWADRP0R	0xFB	RES	IOM	REG	A10	A9	A8	A7	A6
CFWADRP1R	0xFD	RES	IOM	REG	A10	A9	A8	A7	A6
EEPR	0xFF	RES	RES	RES	RES	RES	EEPCS	EEPCK	EEPDT

4.3. CompactFlash Controller

The CompactFlash card Host interface controller provides a bridge between the M-module bus and a CompactFlash card. On the M340, the controller is implemented in an FPGA using VHDL.
The interface controller has seven registers to control the various functions and configurations of the CompactFlash interface. Each register is described in the following sections.

Note: It is strongly advised to read the CF+ and CompactFlash Specification as mentioned in the Annex, to get an understanding of the CompactFlash interface and the meaning of their signals.

4.3.1. Control Register

This read/write register is used to control various control options like reset and card type of the CompactFlash interface.

CFCTRLR Offset: 0xF3

MSB							LSB
7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	RES	RST	MIO
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

RES[7:2] — Reserved

RST — Card Reset
This bit is used to control the CompactFlash card RESET signal. If this bit is set to '1', RESET to the CompactFlash card is asserted. If this bit is cleared to '0', RESET is deasserted.

MIO — Memory/IO
This bit is used to configure the CompactFlash interface for either Memory only cards ('0') or Memory/IO cards ('1'). Depending on this configuration several pins (interrupt and status pins) will change their function. See the description of the CFSTATUS register for details.

NOTE: This bit does not select between memory cycles or I/O cycles. Selection between memory or I/O cycles is done using the window address page registers (see CFWADRPxR register description).

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4.3.2. INTERRUPT CONTROL REGISTER

CompactFlash cards have two types of interrupts, Status Change Interrupts, which are generated by the Host Controller and Card Interrupts which are generated by the function on the card. Only I/O cards have Card Interrupts. Status Change Interrupts are handled differently for Memory and I/O cards.

For Memory-cards (MIO bit of the CFWCTRLR register is set to '0') :

- Battery Dead Detection
- Battery Low Warning
- Write Protect Change
- Change in Ready/Busy status
- Card Detect Change

The following register will describe the Interrupt Enable Register for Memory-cards

CFIER Offset: 0xF5
MSB LSB

7	6	5	4	3	2	1	0
RES	RES	STCHIE	BVD2IE	BVD1IE	CDIE	WPIE	RDYIE
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

RES[7:6] — Reserved

STCHGIE — Status Change Interrupt Enable
This bit act as a master interrupt enable. When this bit is set a status change of BVD2, BVD1, CD, WP or RDY will generate an interrupt request if the corresponding interrupt enable bits are set.

BVD2IE — Battery Voltage Detect 2 Interrupt Enable
When this bit is set, a status change of BVD2 will assert the STCHG (CFISR[5]) interrupt bit.

BVD1IE — Battery Voltage Detect 1 Interrupt Enable
When this bit is set, a status change of BVD1 will assert the STCHG (CFISR[5]) interrupt bit.

CDIE — Card Detect Interrupt Enable
When this bit is set, a status change of CD will assert the STCHG (CFISR[5]) interrupt bit.

WPIE — Write Protect Interrupt Enable
When this bit is set, a status change of WP will assert the STCHG (CFISR[5]) interrupt bit.

RDYIE — Ready Interrupt Enable
When this bit is set, a status change of RDY will assert the STCHG (CFISR[5]) interrupt bit.

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The following register will describe the Interrupt Status Register for Memory-cards

CFISR Offset: 0xF7
MSB LSB

7	6	5	4	3	2	1	0
RES	RES	STCHACK	BVD2	BVD1	CD	WP	RDY
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

RES[7:6] — Reserved

STCHACK — Status Change Interrupt and Interrupt Acknowledge
When this bit is set a status change of BVD2, BVD1, CD, WP or RDY has occurred if the corresponding interrupt enable bits are set. To determine the cause of the Status Change Interrupt, the CFISR[3:7] bits must be examined.

To negate the pending interrupt request, this bit must be cleared by writing a '1'.

BVD2 — Battery Voltage Detect 2
This bit reflexes the state of the BVD2 pin.

BVD1 — Battery Voltage Detect 1
This bit reflexes the state of the BVD1 pin.

CD — Card Detect
This bit reflexes the state of the CD pin, when set a card is inserted, when cleared a card is removed.

WP — Write Protect Interrupt
This bit reflexes the state of the WP pin, when set write protect is enabled, when cleared write protect is disabled.

RDY — Ready
This bit reflexes the state of the RDY pin, when set the card is ready, when cleared the card is busy.

For I/O Cards (MIO bit of the CFWCTRLR register is set to '1'):

- Card Detect Change
- Status Change Pin is asserted, the I/O card's configuration registers must be read to determine which of the status changes mentioned for Memory cards have occurred.
- Card Interrupt Request is asserted.

The following register will describe the Interrupt Enable Register for I/O Cards

CFIER Offset: 0xF5
MSB LSB

7	6	5	4	3	2	1	0
RES	RES	CDCHGIE	RES	STCHGIE	CDIE	RES	CIRQIE
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

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RES[7:6,4,1] — Reserved

CDCHGIE — Card Detect Change Interrupt Enable
This bit act as a master interrupt enable. When this bit is set a status change of CD will generate an interrupt request if the corresponding interrupt enable bit (CDIE) is set.

STCHGIE — Status Change Interrupt Enable
When this bit is set, a card status change interrupt will generate an interrupt request.

CDIE — Card Detect Interrupt Enable
When this bit is set, a status change of CD will assert the STCHG (CFISR[5]) interrupt bit.

CIRQIE — Card Interrupt Request Interrupt Enable
When this bit is set, a card interrupt request will generate an interrupt request.

The following register will describe the Interrupt Status Register for I/O Cards

CFISR Offset: 0xF7
MSB LSB

7	6	5	4	3	2	1	0
RES	RES	CDCHGACK	RES	STCHG	CD	RES	CIRQ
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

RES[7,6,4,1] — Reserved

CDCHGACK — Card Detect Change Interrupt and Interrupt Acknowledge
When this bit is set a status change of CD has occurred if the corresponding interrupt enable bit is set. To determine the cause of the Status Change Interrupt, the pin replacement register must be examined.

To negate the pending interrupt request, this bit must be cleared by writing a '1'.

STCHG — Status Change
This bit reflexes the state of the card Status Change pin, when set a status change event has occurred.

CD — Card Detect
This bit reflexes the state of the CD pin, when set a card is inserted, when cleared a card is removed.

CIRQ — Card Interrupt Request
This bit reflexes the state of the CompactFlash card IRQ pin, when set a card interrupt is asserted, when cleared a card interrupt is negated.

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4.3.3. POWER AND LED CONTROL REGISTER

CFPWRLEDR Offset: 0xF9

MSB							LSB
7	6	5	4	3	2	1	0
RES	RES	VS2	VS1	LEDM	LEDE	V5E	V3E
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

RES[7:6] — Reserved

VS[2:1] — Voltage sense Bits
Voltage sense signals, these signals must be used to determine which powersupply voltage must be applied to the CompactFlash cards.

VS2	VS1	Vcc at power up
0	0	Reserved
0	1	Reserved
1	0	3.3 Volt
1	1	5 Volt

LEDM — LED Mode
The bit controls the mode of the front LED when the LED is enabled (see CFPWRLEDR[2]), when set, the LED mode will be flashing with an interval of 0.5 seconds, when cleared the LED mode will be continuous.

LEDE — LED Enable
The bit turns the front LED on or off. When set the LED will be on (continuous or flashing, see LEDM), when cleared the LED will be off. If the CompactFlash card is removed, this bit will be automatically cleared and the LED will be turned off

V5E, V3E — Power Control Bits
These bits correspond with the power control lines of the MAX1602 PCMCIA/CardBus Power Controller from Maxim. It is used to control the power of the CompactFlash card according to the table below. If a CompactFlash card is removed, these bits are automatically cleared and the power will be turned off.

V5E	V3E	Vcc out
0	0	High-Z
0	1	3.3V
1	0	5V
1	1	Clamped to Ground

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4.3.4. WINDOW ADDRESS PAGE REGISTERS

The M340 CompactFlash interface has two separate windows which can be used to access the CompactFlash card. Each window is 0x40 bytes long and has its own window address page control register. Window0 is located at M-module Offset 0x00-0x3F and Window1 is located at M-module offset 0x40-0x7F.

CFWADRP0R Offset: 0xFB
CFWADRP1R 0xFD
MSB LSB

7	6	5	4	3	2	1	0
IOIS8	IOM	REG	A10	A9	A8	A7	A6
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

IOIS8 — I/O is 8 bit

This bit must be set for 8-bit I/O cards when this window is configured for I/O access cycles (IOM is '1')

Note: If this bit is set to '1' only 8-bit physical accesses are allowed, do not use 16-bit accesses.

IOM — I/O mode

This bit is used to control whether the window is configured to do memory access cycles (common or attribute) or I/O access cycles. If this bit is cleared ('0'), memory access cycles will be performed (using WE and OE signals). If this bit is set ('1'), I/O access cycles will be performed (using IORD and IOWR signals).

REG — REG*

This bit is used during memory cycles to distinguish between common memory and register (attribute) memory accesses. If this bit is set to '1', attribute memory is selected. If this bit is cleared ('0') common memory is selected.
This bit must also be active (set to '1') during I/O cycles (IOM is '1') when the I/O address is on the bus.

IOM	REG	Function
0	0	Common memory access
0	1	Attribute memory access
1	0	Illegal
1	1	I/O access

A[10:6] — Window Address Page Bits

These bits determine the value of the upper address lines of the CompactFlash card during a memory or I/O access. The value of lower address lines is determined by the offset within the window.

4.4. EEPROM REGISTER

The identification of an M-module is implemented using a serial EEPROM with a 64*16 word organization. The industry-standard component 93C46 is used in order to make the identification compatible throughout the complete range of available modules. Access to the identification EEPROM takes place through the following register:

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EEPR Offset: 0xFF
MSB LSB

7	6	5	4	3	2	1	0
RES	RES	RES	RES	RES	EEPCS	EEPCK	EEPDI/O
Reset:							
0	0	0	0	0	0	0	0
Read / Write							

EEPCS — Chip-Select
This bit corresponds to the chip select input of the EEPROM.

EEPCK — Clock
This bit corresponds to the clock input of the EEPROM.

EEPDI/O — Data input/output
This bit corresponds to the data input of the EEPROM when writing, and data output of the EEPROM when reading.

For information on controlling the EEPROM refer to the NM93C46 data sheets. A software example can be found in the file *ideeprom.c* that is part of the software distribution. For information on the memory organization refer to the M-module Specification.

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5. SOFTWARE

This chapter describes the example software which is available for the M340 CompactFlash M-module. The example software consists of a low level driver for ATA storage CompactFlash cards and an example application. A low level driver for serial input/output CompactFlash cards such as Bluetooth cards, GPS cards, Modem cards etc. and high level implementations of an MS-DOS compatible file system and a Bluetooth virtual serial port interface are available as separate packages.

The example software is distributed as ANSI-C source code and consists mainly of an M340 function library which provides functions for easy access to the M340 and a demo program which illustrates the usage of the software library.

The M340 library functions are APIS based, physical accesses and interrupt support are handled by APIS, AcQ Platform Interface Software. The next section contains general information on APIS, for detailed information please refer to the APIS Programmer's Manual.

5.1. APIS SUPPORT

AcQ produces and supports a large number of standard M-modules varying from networking and process I/O to motion control applications. Physically, the M-modules are supported by a large number of hardware platforms: VMEbus, PCI, CompactPCI as well as a wide variety of operating systems: OS-9, Windows NT, Linux etc.

APIS offers a way to program platform independent applications, example- and test software for controlling hardware. Application software written for APIS only needs re-compiling for a particular platform and is operational with little effort (provided that the application is operating system independent).

5.1.1. CONCEPT

Hardware accesses to registers and memory are handled by APIS. Some minor operating system dependent functions frequently used in hardware related software, such as interrupt handling and a delay function are also provided by APIS.

APIS platform support consists of an Application Programming Interface in the form of definition files coded in ANSI-C and platform dependent modules e.g. source files, libraries and/or drivers. In the most simple outline, a platform dependent APIS module consist of nothing more then macro definitions in which APIS calls are substituted by direct hardware accesses. But in most cases an APIS module will consist of a library with interface routines and in some implementations a device driver is needed for interaction with the operating system.

5.1.2. API

The Application Programming Interface for APIS is implemented in two ANSI-C coded definition files: *apis.h* which contains general definitions and *platform_apis.h* which contains platform specific definitions and references to the APIS function calls.

The application source file must include the APIS header file *apis.h*. Porting of the application to a platform, consists of re-compiling the source code with a defined pre-processor macro for selection of the used platform. The APIS header file contains generic APIS definitions and includes a platform specific header file according to the platform selection macro.

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APIS calls are translated to the platform specific calls in the APIS header file and the platform specific definition file *platform_apis.h* (*platform* is a name that identifies a hardware and operating system combination, e.g i4000os9).

The macro PLATFORM must be defined, either via a pre-processor definition provided at compile time or via a macro-definition in the application source.

5.1.3. Code Generation

APIS based example software is available in ANSI-C source code. Source code files must be compiled with pre-processor definition PLATFORM set to a valid value, conforming the target platform. Building of the example software for the M340 is platform dependent, for details refer to release notes of the APIS support package of the target platform and the APIS Programmer's Manual.

Example of APIS supported platforms are i4000os9, i2000dos, i3000win etc.

5.2. CompactFlash ATA driver

The M340 CompactFlash M-module comes with a generic low level ATA driver library for interfacing ATA storage cards (CompactFlash cards, Microdrive etc.). ATA compatible cards are sector based storage cards. The ATA library provides functions for initialization of the M340 and an inserted ATA card, functions for writing data to sectors on the card and for reading data from sectors of the card. Additionally a control function is provided for performing raw ATA commands, retrieving drive information and setting drive parameters.

The software is distributed as ANSI-C source code and is suitable for big endian as well as little endian systems. For implementation on little endian systems the preprocessor macro __LITTLE_ENDIAN__ must be defined, for the implementation on big endian systems __LITTLE_ENDIAN__ must NOT be defined, no further measures have to be taken.
The ATA driver can be configured for using M340 interrupts, to use interrupts the macro ATA_IRQ_BASED must be defined as 1, for polling the macro must not be defined as 1. If interrupts are used the macro's IVECTOR and ILEVEL can be used to specify the interrupt vector and interrupt level.

The following paragraphs contain a description of the non-ANSI-C types and structures required for interfacing the ATA library and an overview of the public functions of the library.

5.2.1. Type Definitions and Structures

The table below contains a list and description of all types and structures used in the M340 example software (standard ANSI-C types are not listed).

Name	Type	Description
UINT8	unsigned char	8-bit unsigned data
UINT16	unsigned short	16-bit unsigned signed data
UINT32	unsigned long	32-bit unsigned signed data
APIS_PATH	unsigned long	APIS physical path ID
APIS_HANDLE	void *	APIS handle

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Name	Type	Description

CFATA_CMDBLK	struct {
	UINT8 feature;
	UINT8 nblk;
	UINT8 cmd;
	UINT8 fnblk;
	UINT32 lba;
	UINT32 flba;
	UINT8 sts;
	UINT8 err;
	UINT8 xfrcat;
	void *buffer;
	}
		ATA command block
		Initial Feature Register
		Initial Number of Blocks
		Command
		Final Number of Blocks
		Initial Logical Block Number
		Final Logical Block Number
		Final Resulting Status
		Final Error Result
		Direction In, Out or No data
		Pointer to Host Data Buffer

ATA_DEV	APIS_HANDLE	ATA device handle

ATA_IOCTL_SF	struct {
	UINT8 feature;
	UINT8 config;
	}
		Set features command data format.

ATA_IOCTL_ID	struct {
	UINT32 sectorsPerCard;
	UINT32 cardSize;
	char serialnr[21];
	char firmwareRev[9];
	char modelNumber[41];
	}
		Identify data format
		Number of sectors per card
		Size of the card, in bytes
		Serial number (ASCII)
		Firmware revision (ASCII)
		Model number (ASCII)

ATA_IOCTL_SENSE	UINT8	Sense command data format
ATA_IOCTL_CMD	CFATA_CMDBLK	ATA command data format

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5.2.2. FUNCTION REFERENCE

m340_ata_open () — Initialize ATA device

Syntax: `int m340_ata_open(APIS_PATH path, ATA_DEV *dev)`

Description: This function will initialize the CompactFlash (CF) controller and the inserted CF ATA card. The CF controller will be initialized for memory cards, window 0 will be configured for accessing the card's common memory and window 1 will be configured for accessing the card registers resident in the attribute memory. The CF card's disk card mode will be set to Memory Mapped mode.
As a result the front LED of the M340 is turned on.

Arguments:
APIS_PATH path
APIS path of M340 module.
ATA_DEV *dev
Pointer to ATA device structure.

Returns: ATA_OKE or an appropriate error code.

m340_ata_close () — Close ATA device

Syntax: `int m340_ata_close(ATA_DEV *dev)`

Description: This function will turn off the power of the ATA slot and the front LED of the M340.

Arguments:
ATA_DEV *dev
Pointer to ATA device structure.

Returns: ATA_OKE or an appropriate error code.

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m340_ata_ioctl () — Perform I/O control operation on ATA device

Syntax: `int m340_ata_ioctl(ATA_DEV *dev, int request, void *data, int size)`

Description: This routine performs control and status functions on the ATA card. The following requests are currently supported:

ATAID - Identify drive
: This function is provided to retrieve drive information using the ATA command "Identify Drive". The data argument must be a pointer to the location where the information must be stored, the programmer must make sure enough storage capacity is available (sizeof (ATA_IOCTL_ID)), data will be stored according to the ATA_IOCTL_ID structure which can be found in m340_ata.h.

ATASENSE - Request Sense
: This function is provided to request extended error information for the previous command using the ATA command "Request Sense". The extended error information is returned as an 8-bit error code. For the definition of the extended error codes refer to the ATA specification.

ATASF - Set features
: This function will perform a "Set Features" command on the ATA device. The type of feature and the config data must be provided by the programmer as data according to the ATA_IOCTL_SF structure which can be found in m340_ata.h.

ATACMD - Perform a single raw ATA command
: This function provides a way to perform any ATA command on the ATA device. The command block, defined with ATA_IOCTL_CMD, must be provided. The programmer must make sure that the command block is fully initialized, the element "buffer" of the command structure requires special attention since this pointer must be initialized and enough storage must be available required by the ATA command. For details refer to the ATA specification.

Arguments:

ATA_DEV *dev
: Pointer to ATA device.

int request
: Operation request.

void *data
: Pointer to data block. The type of data depends on the request. Depending on the function request the data block is used for providing data to the device or for storing data, retrieved from the device.

int size
: Size of the storage referenced by the provided data pointer.

Returns: ATA_OKE or an appropriate error code.

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m340_ata_read () — Read from ATA device

Syntax: `int m340_ata_read(ATA_DEV *dev, void *data, UINT32 StartSect, UINT32 *NumSect)`

Description: This function performs a read operation on the ATA card. The caller must provide the sector number from where the data must be transferred from as well as the number of sectors to read. Data read, will be stored at the provided data pointer. The sector size is 512 Bytes conform the CompactFlash specification.

Arguments:

ATA_DEV *dev
: Pointer to ATA device structure.

void *data
: Pointer to Data Buffer.

UINT32 StartSector
: Source sector.

UINT32 *NumSect
: Number of Sectors to Transfer, after execution *NumSect contains the amount of sectors actually transferred.

Returns: ATA_OKE or an appropriate error code.

m340_ata_write () — Write to ATA device

Syntax: `int m340_ata_write(ATA_DEV *dev, void *data, UINT32 StartSect, UINT32 *NumSect)`

Description: This function performs a write operation on the ATA card. The data to be written must be provided by the caller as well as the destination sector and the number of sectors to write. The sector size is 512 Bytes conform the CompactFlash specification.

Arguments:

ATA_DEV *dev
: Pointer to ATA device structure.

void *data
: Pointer to Data Buffer.

UINT32 StartSector
: Destination sector.

UINT32 *NumSect
: Number of Sectors to Transfer, after execution *NumSect contains the amount of sectors actually transferred.

Returns: ATA_OKE or an appropriate error code.

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5.3. SOFTWARE DISTRIBUTION

This section gives an overview of the software distribution.

File	Description
PROJECT\M340\SOFTWARE\CFATA\EXAMPLE\m340_ata_demo.c	Example application
PROJECT\M340\SOFTWARE\CFATA\EXAMPLE\makefile.bor	Borland/Windows maker
PROJECT\M340\SOFTWARE\CFATA\EXAMPLE\makefile.os9	Microware/OS-9 Maker
PROJECT\M340\SOFTWARE\CFATA\EXAMPLE\makefile.lin	GNU/Linux Maker
PROJECT\M340\SOFTWARE\CFATA\LIB\m340_ata.c	M340 ATA library source code
PROJECT\M340\SOFTWARE\CFATA\LIB\m340_ata.h	Definitions for M340 ATA library
PROJECT\M340\SOFTWARE\DEFS\m340.h	M340 general definitions
PROJECT\MMOD ID\SOFTWARE\LIB\ideeprom.h	IDEEPROM definitions
PROJECT\MMOD ID\SOFTWARE\LIB\modideep.c	IDEEPROM interface library

M340 example software is API S based, therefore API S support for the target platform is required for code generation.

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The following figure is an example of the M340 software integrated in the APIS environment with as target platform the i4000/OS-9.

```
+---PROJECT                              AcQ s distribution
     +---APIS                            APIS basis distribution
     |    +---DOC                        APIS documentation
     |    +---SOFTWARE
     |         | readme.txt              Distribution overview
     |         +---COMMON
     |         |    +---DEFS
     |         |    |    apis.h          General definitions
     |         |    +---OS9TRAP
     |         |    |    +---CMDS
     |         |    |         apistrap   OS-9 trap handler
     |         +---I4000OS9              i4000/OS-9 support
     |         |    relnotes.txt         Release notes / version info
     |         |    apis_i4000os9.h      Platform specific definitions
     |         |    apis_i4000os9.c      Platform support library
     +---M340                            M385 distribution
     |    +---SOFTWARE
     |              +---DEFS
     |              |    m340.h          M340 Host Definitions
     |              +---CFATA
     |              |    +---LIB         M340 ATA Library
     |              |    |       m340_ata.c
     |              |    |       m340_ata.h
     |              |    +---EXAMPLE     M340 ATA example application
     |                        m340_ata_demo.c
     |                        makefile.*
     +---MMODID
          +---SOFTWARE
               +---LIB
                    modideep.c          M-module ID EEPROM library
                    ideeprom.h          M-module ID definitions
```

Code generation is platform dependent, for information on building the software please refer to the release notes of the target platform and the APIS Programmer's Manual.

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6. ANNEX

6.1. BIBLIOGRAPHY

Specification for M-module interface and physical dimensions
M-module specification manual, April 1996, MUMM.
Simon-Schöffel-Strasse 21, D-90427 Nürnberg, Germany.

CF+ and CompactFlash Specification Revision 1.4
CompactFlash Association.
P.O. Box 51537, Palo Alto, CA 94303, U.S.A
www.compactflash.org

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AcQuisition Technology
P.O. Box 627, 5340 AP Oss, The Netherlands.
Downloadable from www.acq.nl

6.2. COMPONENT IMAGE

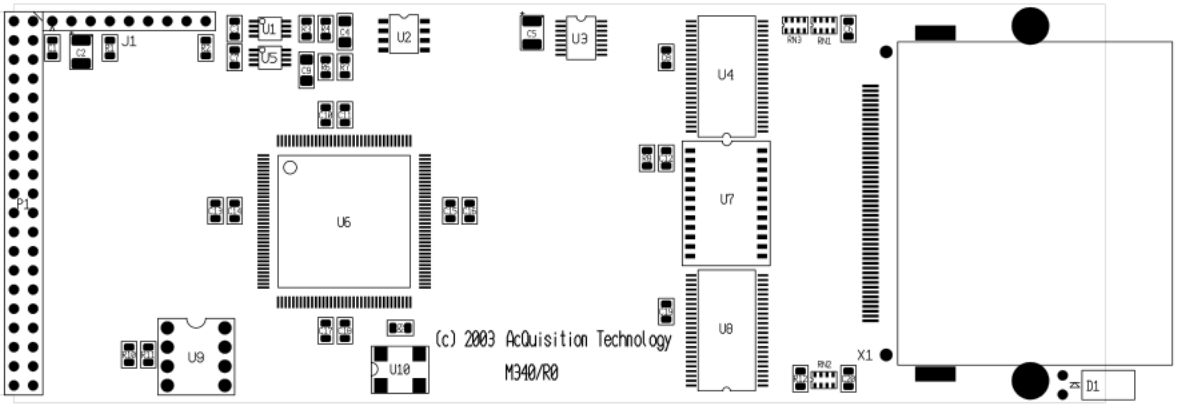


Figure 2 Component Image

6.3. TECHNICAL DATA

Slots on the base-board:
Requires one 16-bit M-module slot.

Connection:
To base-board via 40 pole M-module interface.
To CompactFlash card via a 50 pole CF/CF+ card slot pin-connector.

Power supply:
+5VDC +/-10%, typical 50 mA, without a CompactFlash card powered.

Temperature range:
Operating: 0..+60°C.
Storage:- 20..+70°C.

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Humidity:
Class F, non-condensing.

6.4. DOCUMENT HISTORY

- Version 1.0
  First release

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