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Find the *Acroamatics Telemetry Systems 501V VME* at our website: ***Click HERE***

Model 501V

32Mbps VME Bit Synchronizer

Tunable from 8bps to 32 Mbps (NRZ codes) and 16 Mbps (all others)

Processes all IRIG standard and randomized codes

Independent PCM encoders with both internal and external clock/data inputs

Viterbi, BERT, Ambiguity Resolution

Fast sync acquisition less than 32 bits, typical

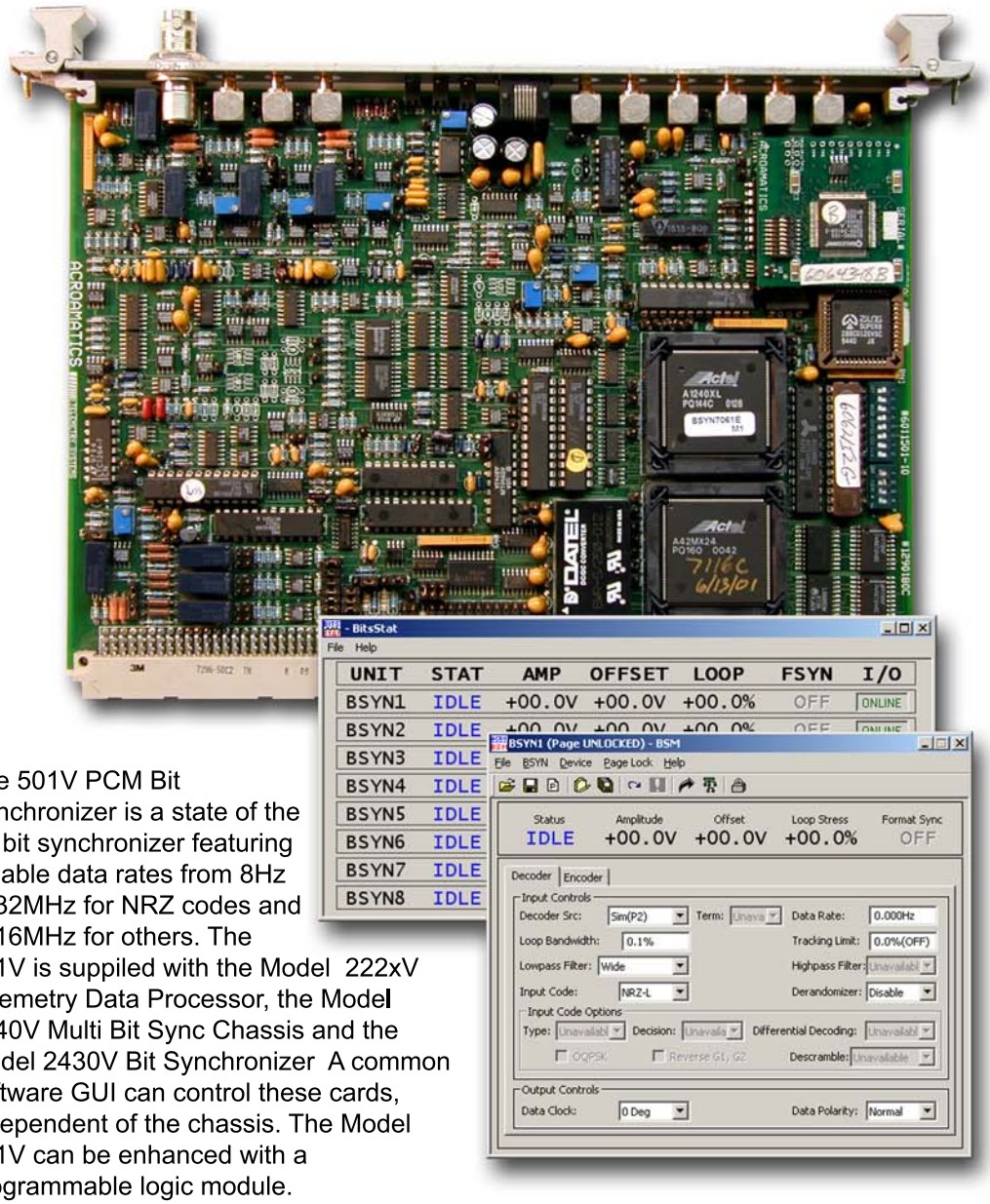
Excellent BER performance, 1dB or better

Direct decoding/encoding of TTL and RS422 clock/data sources

Frame Synchronizer with auto-polarity and automated data source selector

Full featured BERT with "live" data BER monitor

Field upgradeable options module for future expansion



The 501V PCM Bit Synchronizer is a state of the art bit synchronizer featuring tunable data rates from 8Hz to 32MHz for NRZ codes and to 16MHz for others. The 501V is suppiled with the Model 222xV Telemetry Data Processor, the Model 2440V Multi Bit Sync Chassis and the Model 2430V Bit Synchronizer A common software GUI can control these cards, independent of the chassis. The Model 501V can be enhanced with a programmable logic module.

Current options include Viterbi Decoding, a frame simulator/synchronizer and a built-in bit error rate test (BERT) generater/receiver. The logic module is reprogrammable and can be replaced in the field without any special tools, thus, minimizing down time when an upgrade becomes necessary. These unique capabilities allow you to respond quickly to evolving application requirements such as:

- Recovering data from newly defined or application specific coding schemes
- Creating canned formats for recovering data from concatenated or layered codes
- Monitoring data streams for frame synchronization to resolve ambiguities or polarity inversions typical with many modulation schemes

ACROAMATICS

TELEMETRY SYSTEMS

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Model 501V 32Mbps VME Bit Synchronizer

SIGNAL INPUTS

Source	Program select, 1 of 4 inputs
Isolation	Greater than 60dB at 32MHz
Impedance	Program selectable: Hi-Z/Lo-Z. Single Ended: 10kΩ/75Ω, Differential: 10kΩ/120Ω
Signal Level	Single Ended: 0.2 to 30V p-p, Differential: 0.2 to 25V p-p
DC Offset	20V max Single-Ended, Hi-Z
Baseline Variation	Tracks sinusoidal offsets to 100% p-p signal amplitude at 0.1% bit rate
PCM Codes	Program selectable: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RZ
Derandomizer	Program selectable: RNRZ 9/11/15/17/23, forward/reverse

SYNCHRONIZATION

Bit Rate Range	8bps-32Mbps NRZ , 8bps-16Mbps all others
Tuning Resolution	0.1% of bit rate
Capture Range	3 times the programmed loopwidth, typical
Tracking Range	±12% typical, with programmable limiter
Loop Bandwidth	0.1% to 3.2%, program selectable in 0.1% increments
Sync Threshold	0dB for NRZ-L and Biø-L codes
Sync Maintenance	(LW=0.1%) –2dB NRZ-L and Biø-L codes
Sync Acquisition	(LW=1.6%, SNR > 12dB) Typically less than 32 bit periods
Sync Retention	(LW=0.1%, SNR > 3dB) Retains sync through > 128 consecutive dropouts
Bit Error Rate	(LW=0.1%) to within 1dB of ideal bit error rate performance curves

DATA/CLOCK OUTPUTS

NRZ-L Data	Three TTL, one RS422/TTL
Data Clock	Two program selectable TTL: 0º, 90º, 180º, 270º
Quadrature Clocks	One each: 0º, 90º, 180º, 270º; RS422/TTL
2x Clock	One TTL, One RS422/TTL
Data Polarity	Program selectable: normal/inverted

SOFT BIT DECISION OUTPUT

Data/clock	Three bits Offset Binary plus 0º clock; TTL (open collector)
Sample Rate	Programmable to 32 megasamples per second

PCM ENCODER

Data Source	Program selectable: Recovered Data or External data/clock
Outputs	One bipolar, 4V p-p; Two TTL; One RS422/TTL
Randomizer	Program selectable: RNRZ 9/11/15/17/23
PCM Codes	Program selectable: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RZ

EXTERNAL DATA/CLOCK INPUT

Signal Type	Jumper selectable: RS422 or TTL
Impedance	120Ω RS422, 75Ω TTL
Data Code	Program selectable: NRZ-L/M/S, Biø-L/M/S, DBiø-M/S, DM-M/S, MDM-M/S, RZ
Data Clock	Program selectable: Normal/Inverted, 1x or 2x

CONVOLUTION ENCODER/DECODER (Optional)

Viterbi Decoder	Rate 1/2, k=7: includes differential decoding, V.35 descrambling, and G2 invert
Symbol Formats	Serial, parallel, and staggered parallel
Convolutional Encoder	Rate 1/2, k=7: includes differential encoder, V.35 scrambler, and G2 inverter
Symbol Formats	Serial, parallel, and staggered parallel

FORMAT GENERATORS/SYNCHRONIZER (Optional)

Format Generator	Programmable frame length, sync pattern and mask
Synchronizer Source	Recovered data, external data, or test generator
Synchronizer Strategy	Pattern match in "search", programmable error limits for "check" and "lock" states
Other Features	Bit slip enable, auto polarity enable, data source/ambiguity resolution

BIT ERROR RATE TESTER (Optional)

Transmitter Pattern	PRN sequence: 2^{11}-1, 2^{7}-1, 2^{9}-1, 2^{15}-1 (forward/reverse)
Pattern Clock Source	Selectable clock: External clock or programmable clock 1 bps to 40 mbps
Blanking	Program selectable: 32, 64, 128 bits
BER Sample Period	Program selectable: 103 to 109 bit periods, or continuous accumulate
Other Features	Automatic pattern synchronization, forced error ON/OFF, Tape Out attentuator

PHYSICAL

Format	Standard 6U VME single slot
Cooling Requirements	30 Linear FPM
Power Requirements	+5VDC @ 1.25A, +12VDC @ 800mA,-12VDC @500mA
Temperature	Operating 0 to +40°C, non-operating –40 to +86°C
Relative Humidity	Up to 90% non-condensing
Shock	Operating 6G, Non-operating 25G
Vibration	Operating .3G, 5 to 2000 Hz, Non-operating .8G, 5 to 500 Hz

Specifications subject to change without notice

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